June 2002

EXAR'S DUARTS COMPARED WITH TI'S TL16C752B

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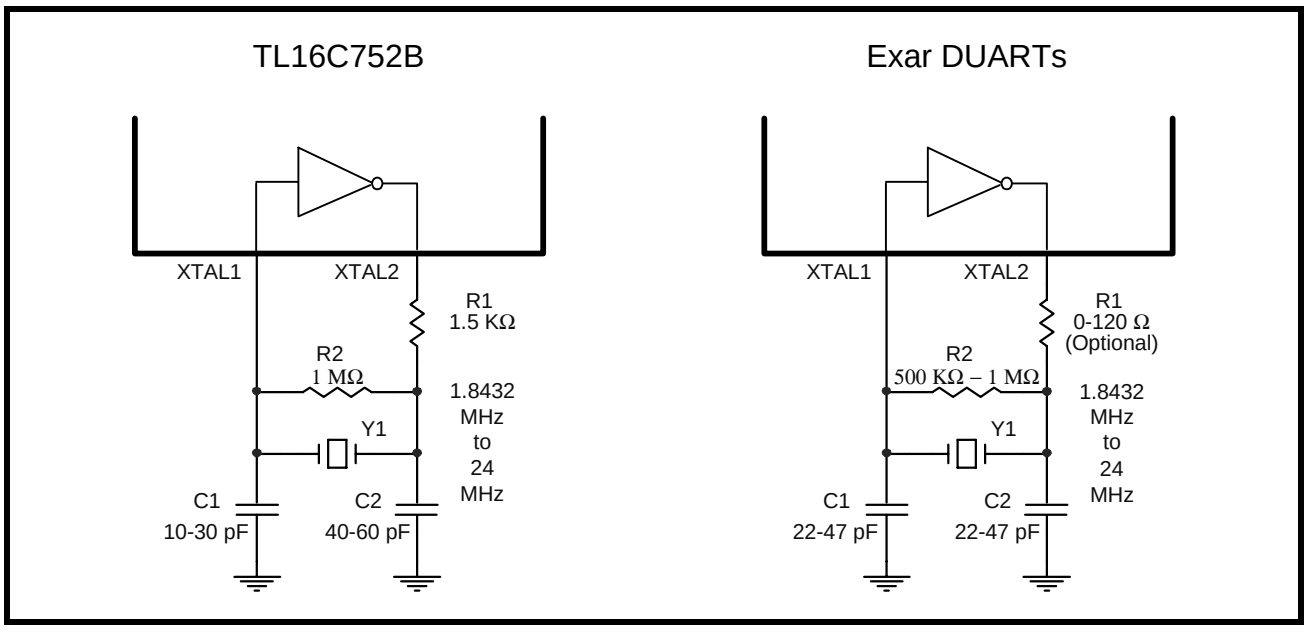
1.0 INTRODUCTION

This application note describes the major difference between Exar's DUARTs (ST16C2550, XR16L2750, XR16L2751 and XR16C2850) with TI's TL16C752B. These devices are very similar, with a few hardware, firmware-related and bus timing differences.

1.1 HARDWARE DIFFERENCES

- The ST16C2550, XR16L2750, XR16L2751, XR16C2850 and TL16C752B are all available in the 48-pin QFP package. Additionally, the ST16C2550, XR16L2750 and XR16C2850 are available in the 44-pin PLCC package and the ST16C2550 and XR16C2850 are available in the 40-pin PDIP package.
- In the QFP package, the ST16C2550, XR16L2750 and TL16C752B are pin-to-pin compatible. The XR16L2751 and XR16C2850 are not fully pin-to-pin compatible with the TL16C752B. The XR16L2751 has 4 pins that are inputs and the XR16C2850 has 3 pins that are inputs where they are "No Connects" on the TL16C752B. These extra input pins must be tied to VCC or GND. Please see datasheets for more details.
- Exar's 48-pin TQFP package is thinner (1.2 mm) than TI's 48-pin LQFP package (1.6 mm).
- The oscillator circuitry is similar and will operate in most cases, but there are some differences when using a crystal oscillator and when using an external clock. See Figure 1below for the differences in the oscillator circuitry for a crystal oscillator. When using an external clock input for frequencies greater than 24 MHz, Exar's DUARTs will require a 2K pull-up resistor on the XTAL2 pin.

FIGURE 1. CRYSTAL OSCILLATOR CIRCUITRY DIFFERENCES



1.2 Bus Timing Differences

- The TL16C752B requires that the -CS pin is asserted first before the -IOR or -IOW pin and the -IOR or -IOW pin must be de-asserted before the -CS pin is de-asserted. During a read, the Exar DUARTs can have either the -CS or the -IOR signal asserted first and have either signal be de-asserted first. The signals are wire-ORed in the Exar DUARTs, therefore the second signal asserted will initiate the read cycle and the first signal de-asserted terminates the read cycle. The same is true during a write for -CS and -IOW. The flexibility of the Exar DUARTs timing can be important in DSP, ARM, and MIPS designs.

1.3 Firmware Differences

1.3.1 Firmware Differences Between the ST16C2550 and TL16C752B

The internal registers in the ST16C2550 and TL16C752B are similar but with some exceptions:

Table 1: ST16C2550 and TL16C752B Register Set Differences

A2:A0	R/W	ST16C2550	TL16C752B
LCR Bit-7 = 0			
100	R/W	**Modem Control Register (MCR)** • Bit-6 = Not Used • Bit-2 = Reserved (OP1# during Internal Loopback)	**Modem Control Register (MCR)** • Bit-6 = TCR and TLR Register Enable • Bit-2 = FIFO Rdy Register Enable
LCR Bit-7 = 0, MCR Bit-6 = 1 (EFR Bit-4 = 1), MCR Bit-4 = 0, MCR Bit-2 = 0			
110	R/W	N/A	**Transmission Control Register (TCR)** • RX FIFO Trigger Level Halt and Resume Transmission Levels (4-60 in multiples of 4)
111	R/W	N/A	**Trigger Level Register (TLR)** • TX and RX Trigger Levels (4-60 in multiples of 4)
LCR Bit-7 = 0, MCR Bit-6 = 0 (EFR Bit-4 = 1), MCR Bit-4 = 0, MCR Bit-2 = 1			
111	R	N/A	**FIFO Ready Register (FIFO Rdy)** • Status Bits - TX FIFO level below TX Trigger Level for channels A and B • Status Bits - RX FIFO level above RX Trigger Level for channels A and B

R = Read-Only, W = Write-Only, R/W = Read/Write

1.3.1.1 Summary of Differences Between the ST16C2550 and TL16C752B

Some differences between the ST16C2550 and TL16C752B are summarized in the table below.

TABLE 2: DIFFERENCES BETWEEN EXAR'S ST16C2550 WITH TI'S TL16C752B

COMPARISON	ST16C2550	TL16C752B
Data Bus Standard	Intel	Intel
Device ID and Revision	N/A	N/A
Power Supply Operation	**3.3 and 5 V**	3.3 V only
3.3 V Operation with 5 V Tolerance	N/A	N/A
Max Operating Current	**1.3 mA @ 3.3 V** **3 mA @ 5 V**	20 mA @ 3.3 V
Max Frequency on XTAL1	30 MHz @ 3.3 V **64 MHz @ 5 V**	**48 MHz @ 3.3 V**
Data Sampling Rates	16X	16X
BRG Prescaler	1 or 4	1 or 4
Max Data Rate	1.875 Mbps @ 3.3 V **4 Mbps @ 5 V**	3 Mbps @ 3.3 V
Package	48-TQFP, 44-PLCC, 40-PDIP	48-LQFP
Operating Temperature Ranges	Commercial and Industrial	Commercial and Industrial
48-QFP package thickness	**1.2 mm**	1.6 mm
TX/RX FIFO Size	16	**64**
TX/RX Trigger Tables	1 Trigger Table	**2 Trigger Tables**
TX/RX FIFO Interrupt Trigger Levels	4 Selectable	**16 Selectable (TLR)** **4 Selectable (TLR = 0)**
TX/RX FIFO Counters	N/A	N/A
Single FIFO Ready Status Register	N/A	**FIFO Ready Status Register**
Hardware Flow Control	N/A	**Auto RTS/CTS Flow Control**
Software Flow Control	N/A	**Auto Xon/Xoff Flow Control**
Auto Hysteresis Level	N/A	**16 Selectable Levels** **Select Upper and Lower Hysteresis Levels irrespective of trigger level**
Infrared Mode	N/A	N/A
Sleep Mode	N/A	**Sleep Mode with Auto Wake-up**
Diagnostic Modes	Local loopback	Local Loopback
RS485 Mode	N/A	N/A
LSR bits 4-2 Interrupt Generation	Delayed	Delayed

1.3.2 Firmware Differences Between the XR16L2750 and TL16C752B

The internal registers in the XR16L2750 and TL16C752B are similar but with some exceptions:

TABLE 3: XR16L2750 AND TL16C752B REGISTER SET DIFFERENCES

A2:A0	R/W	XR16L2750	TL16C752B
LCR Bit-7 = 0			
100	R/W	**Modem Control Register (MCR)** • Bit-6 = Infrared Mode Enable • Bit-2 = Reserved (RI# during Internal Loop-back)	**Modem Control Register (MCR)** • Bit-6 = TCR and TLR Register Enable • Bit-2 = FIFO Rdy Register Enable
LCR Bit-7 = 0, MCR Bit-6 = 1 (EFR Bit-4 = 1), MCR Bit-4 = 0, MCR Bit-2 = 0			
110	R/W	N/A	**Transmission Control Register (TCR)** • RX FIFO Trigger Level Halt and Resume Transmission Levels (4-60 in multiples of 4)
111	R/W	N/A	**Trigger Level Register (TLR)** • TX and RX Trigger Levels (4-60 in multiples of 4)
LCR Bit-7 = 0, MCR Bit-6 = 0 (EFR Bit-4 = 1), MCR Bit-4 = 0, MCR Bit-2 = 1			
111	R	N/A	**FIFO Ready Register (FIFO Rdy)** • Status Bits - TX FIFO level below TX Trigger Level for channels A and B • Status Bits - RX FIFO level above RX Trigger Level for channels A and B
LCR Bit-7 = 0, FCTR Bit-6 = 1			
111	W	**Enhanced Mode Select Register (EMSR)** • 8X Sampling, LSR Interrupt Immediate, Auto RTS Hysteresis Select (MSB), RS485 Output Inversion, FLVL select - TX or RX FIFO	N/A
111	R	**FIFO Level Register (FLVL)** • Current Level of the TX or RX FIFO	N/A
LCR Bit-7 = 0, DLL = 0x00, DLM = 0x00			
000	R	**Device Revision (DREV)**	N/A
001	R	**Device ID (DVID)**	N/A
LCR = 0xBF			
000	R	**FIFO Data Count Register (FC)**	N/A
000	W	**Trigger Level Register (TRG)** • Programmable Trigger Levels 1-64 for TX and RX FIFO	N/A
001	R/W	**Feature Control Register (FCTR)** • RX/TX Programmable Trigger Level Select, Scratchpad Swap, Trigger Table Select, Auto RS485 Enable, RX Infrared Input Inversion, Auto RTS Hysteresis Select (LSB)	N/A

R = Read-Only, W = Write-Only, R/W = Read/Write

1.3.2.1 Summary of Differences Between the XR16L2750 and TL16C752B

Some differences between the XR16L2750 and TL16C752B are summarized in the table below.

TABLE 4: DIFFERENCES BETWEEN EXAR'S XR16L2750 WITH TI'S TL16C752B

COMPARISON	XR16L2750	TL16C752B
Data Bus Standard	Intel	Intel
Device ID and Revision	**Device ID and Revision**	N/A
Power Supply Operation	**2.5, 3.3 and 5 V**	3.3 V only
3.3 V Operation with 5 V Tolerance	**3.3 V Operation with 5 V Tolerance**	N/A
Max Operating Current	**2.7 mA @ 2.5 V** **2.7 mA @ 3.3 V** **4 mA @ 5 V**	20 mA @ 3.3 V
Max Frequency on XTAL1	**24 MHz @ 2.5 V** 33 MHz @ 3.3 V **50 MHz @ 5 V**	**48 MHz @ 3.3 V**
Data Sampling Rates	**16X or 8X**	16X
BRG Prescaler	1 or 4	1 or 4
Max Data Rate	**3 Mbps @ 2.5 V at 8X** **4 Mbps @ 3.3 V at 8X** **6.25 Mbps @ 5 V at 8X**	3 Mbps @ 3.3 V
Package	48-TQFP, 44-PLCC	48-LQFP
Operating Temperature Ranges	Commercial and Industrial	Commercial and Industrial
48-QFP package thickness	**1.2 mm**	1.6 mm
TX/RX FIFO Size	64	64
TX/RX Trigger Tables	**4 Trigger Tables**	2 Trigger Tables
TX/RX FIFO Interrupt Trigger Levels	**Programmable** (Table D) 4 Selectable (Tables A-C)	16 Selectable (TLR) 4 Selectable (TLR = 0)
TX/RX FIFO Counters	**TX/RX FIFO Counters**	N/A
Single FIFO Ready Status Register	N/A	**FIFO Ready Status Register**
Hardware Flow Control	Auto RTS/CTS Flow Control	Auto RTS/CTS Flow Control
Software Flow Control	Auto Xon/Xoff Flow Control	Auto Xon/Xoff Flow Control
Auto Hysteresis Level	16 Selectable Levels ±N from the trigger level	16 Selectable Levels Select Upper and Lower Hysteresis Levels irrespective of trigger level
Infrared Mode	**IrDA encoder/decoder (ver 1.0)**	N/A
Sleep Mode	Sleep Mode with Auto Wake-up	Sleep Mode with Auto Wake-up
Diagnostic Modes	Local loopback	Local Loopback
RS485 Mode	**Auto RS485 Mode**	N/A
LSR bits 4-2 Interrupt Generation	**Immediate or Delayed**	Delayed

1.3.3 Firmware Differences Between the XR16L2751 and TL16C752B

The internal registers in the XR16L2751 and TL16C752B are similar but with some exceptions:

TABLE 5: XR16L2751 AND TL16C752B REGISTER SET DIFFERENCES

A2:A0	R/W	XR16L2751	TL16C752B
LCR Bit-7 = 0			
100	R/W	**Modem Control Register (MCR)** • Bit-6 = Infrared Mode Enable • Bit-2 = Reserved (RI# during Internal Loop-back)	**Modem Control Register (MCR)** • Bit-6 = TCR and TLR Register Enable • Bit-2 = FIFO Rdy Register Enable
LCR Bit-7 = 0, MCR Bit-6 = 1 (EFR Bit-4 = 1), MCR Bit-4 = 0, MCR Bit-2 = 0			
110	R/W	N/A	**Transmission Control Register (TCR)** • RX FIFO Trigger Level Halt and Resume Transmission Levels (4-60 in multiples of 4)
111	R/W	N/A	**Trigger Level Register (TLR)** • TX and RX Trigger Levels (4-60 in multiples of 4)
LCR Bit-7 = 0, MCR Bit-6 = 0 (EFR Bit-4 = 1), MCR Bit-4 = 0, MCR Bit-2 = 1			
111	R	N/A	**FIFO Ready Register (FIFO Rdy)** • Status Bits - TX FIFO level below TX Trigger Level for channels A and B • Status Bits - RX FIFO level above RX Trigger Level for channels A and B
LCR Bit-7 = 0, FCTR Bit-6 = 1			
111	W	**Enhanced Mode Select Register (EMSR)** • 8X Sampling, LSR Interrupt Immediate, Auto RTS Hysteresis Select (MSB), RS485 Output Inversion, FLVL select - TX or RX FIFO	N/A
111	R	**FIFO Level Register (FLVL)** • Current Level of the TX or RX FIFO	N/A
LCR Bit-7 = 0, DLL = 0x00, DLM = 0x00			
000	R	**Device Revision (DREV)**	N/A
001	R	**Device ID (DVID)**	N/A
LCR = 0xBF			
000	R	**FIFO Data Count Register (FC)**	N/A
000	W	**Trigger Level Register (TRG)** • Programmable Trigger Levels 1-64 for TX and RX FIFO	N/A
001	R/W	**Feature Control Register (FCTR)** • RX/TX Programmable Trigger Level Select, Scratchpad Swap, Trigger Table Select, Auto RS485 Enable, RX Infrared Input Inversion, Auto RTS Hysteresis Select (LSB)	N/A

R = Read-Only, W = Write-Only, R/W = Read/Write

1.3.3.1 Summary of Differences Between the XR16L2751 and TL16C752B

Some differences between the XR16L2751 and TL16C752B are summarized in the table below.

TABLE 6: DIFFERENCES BETWEEN EXAR'S XR16L2751 WITH TI'S TL16C752B

COMPARISON	XR16L2751	TL16C752B
Data Bus Standard	**Intel and Motorola**	Intel
Device ID and Revision	**Device ID and Revision**	N/A
Power Supply Operation	**2.5, 3.3 and 5 V**	3.3 V only
3.3 V Operation with 5 V Tolerance	**3.3 V Operation with 5 V Tolerance**	N/A
Max Operating Current	**2.7 mA @ 2.5 V** **2.7 mA @ 3.3 V** **4 mA @ 5 V**	20 mA @ 3.3 V
Max Frequency on XTAL1	**24 MHz @ 2.5 V** 33 MHz @ 3.3 V **50 MHz @ 5 V**	**48 MHz @ 3.3 V**
Data Sampling Rates	**16X or 8X**	16X
BRG Prescaler	1 or 4	1 or 4
Max Data Rate	**3 Mbps @ 2.5 V at 8X** **4 Mbps @ 3.3 V at 8X** **6.25 Mbps @ 5 V at 8X**	3 Mbps @ 3.3 V
Package	48-TQFP, 44-PLCC	48-LQFP
Operating Temperature Ranges	Commercial and Industrial	Commercial and Industrial
48-QFP package thickness	**1.2 mm**	1.6 mm
TX/RX FIFO Size	64	64
TX/RX Trigger Tables	**4 Trigger Tables**	2 Trigger Tables
TX/RX FIFO Interrupt Trigger Levels	**Programmable** (Table D) 4 Selectable (Tables A-C)	16 Selectable (TLR) 4 Selectable (TLR = 0)
TX/RX FIFO Counters	**TX/RX FIFO Counters**	N/A
Single FIFO Ready Status Register	N/A	**FIFO Ready Status Register**
Hardware Flow Control	Auto RTS/CTS Flow Control	Auto RTS/CTS Flow Control
Software Flow Control	Auto Xon/Xoff Flow Control	Auto Xon/Xoff Flow Control
Auto Hysteresis Level	16 Selectable Levels ±N from the trigger level	16 Selectable Levels Select Upper and Lower Hysteresis Levels irrespective of trigger level
Infrared Mode	**IrDA encoder/decoder (ver 1.0)**	N/A
Sleep Mode	Sleep Mode with Auto Wake-up	Sleep Mode with Auto Wake-up
Powersave Mode	**Powersave Mode**	N/A
Diagnostic Modes	Local loopback	Local Loopback
RS485 Mode	**Auto RS485 Mode**	N/A
LSR bits 4-2 Interrupt Generation	**Immediate or Delayed**	Delayed

1.3.4 Firmware Differences Between the XR16C2850 and TL16C752B

The internal registers in the XR16c2750 and TL16C752B are similar but with some exceptions:

TABLE 7: XR16C2850 AND TL16C752B REGISTER SET DIFFERENCES

A2:A0	R/W	XR16C2850	TL16C752B
LCR Bit-7 = 0			
100	R/W	**Modem Control Register (MCR)** • Bit-6 = Infrared Mode Enable • Bit-2 = Reserved (RI# during Internal Loop-back)	**Modem Control Register (MCR)** • Bit-6 = TCR and TLR Register Enable • Bit-2 = FIFO Rdy Register Enable
LCR Bit-7 = 0, MCR Bit-6 = 1 (EFR Bit-4 = 1), MCR Bit-4 = 0, MCR Bit-2 = 0			
110	R/W	N/A	**Transmission Control Register (TCR)** • RX FIFO Trigger Level Halt and Resume Transmission Levels (4-60 in multiples of 4)
111	R/W	N/A	**Trigger Level Register (TLR)** • TX and RX Trigger Levels (4-60 in multiples of 4)
LCR Bit-7 = 0, MCR Bit-6 = 0 (EFR Bit-4 = 1), MCR Bit-4 = 0, MCR Bit-2 = 1			
111	R	N/A	**FIFO Ready Register (FIFO Rdy)** • Status Bits - TX FIFO level below TX Trigger Level for channels A and B • Status Bits - RX FIFO level above RX Trigger Level for channels A and B
LCR Bit-7 = 0, FCTR Bit-6 = 1			
111	W	**Enhanced Mode Select Register (EMSR)** • Auto RTS Hysteresis Select (MSB), FLVL select - TX or RX FIFO	N/A
111	R	**FIFO Level Register (FLVL)** • Current Level of the TX or RX FIFO	N/A
LCR Bit-7 = 0, DLL = 0x00, DLM = 0x00			
000	R	**Device Revision (DREV)**	N/A
001	R	**Device ID (DVID)**	N/A
LCR = 0xBF			
000	R	**FIFO Data Count Register (FC)**	N/A
000	W	**Trigger Level Register (TRG)** • Programmable Trigger Levels 1-64 for TX and RX FIFO	N/A
001	R/W	**Feature Control Register (FCTR)** • RX/TX Programmable Trigger Level Select, Scratchpad Swap, Trigger Table Select, Auto RS485 Enable, RX Infrared Input Inversion, Auto RTS Hysteresis Select (LSB)	N/A

R = Read-Only, W = Write-Only, R/W = Read/Write

1.3.4.1 Summary of Differences Between the XR16C2850 and TL16C752B

Some differences between the XR16C2850 and TL16C752B are summarized in the table below.

TABLE 8: DIFFERENCES BETWEEN EXAR'S XR16C2850 WITH TI'S TL16C752B

COMPARISON	XR16C2850	TL16C752B
Data Bus Standard	Intel	Intel
Device ID and Revision	**Device ID and Revision**	N/A
Power Supply Operation	**3.3 and 5 V**	3.3 V only
3.3 V Operation with 5 V Tolerance	**N/A**	N/A
Max Operating Current	**1.2 mA @ 3.3 V** **3 mA @ 5 V**	20 mA @ 3.3 V
Max Frequency on XTAL1	33 MHz @ 3.3 V **50 MHz @ 5 V**	**48 MHz @ 3.3 V**
Data Sampling Rates	**16X or 8X**	16X
BRG Prescaler	1 or 4	1 or 4
Max Data Rate	**4 Mbps @ 3.3 V at 8X** **6.25 Mbps @ 5 V at 8X**	3 Mbps @ 3.3 V
Package	48-TQFP, 44-PLCC, 40-PDIP	48-LQFP
Operating Temperature Ranges	Commercial and Industrial	Commercial and Industrial
48-QFP package thickness	**1.2 mm**	1.6 mm
TX/RX FIFO Size	128	64
TX/RX Trigger Tables	**4 Trigger Tables**	2 Trigger Tables
TX/RX FIFO Interrupt Trigger Levels	**Programmable** (Table D) 4 Selectable (Tables A-C)	16 Selectable (TLR) 4 Selectable (TLR = 0)
TX/RX FIFO Counters	**TX/RX FIFO Counters**	N/A
Single FIFO Ready Status Register	N/A	**FIFO Ready Status Register**
Hardware Flow Control	Auto RTS/CTS Flow Control	Auto RTS/CTS Flow Control
Software Flow Control	Auto Xon/Xoff Flow Control	Auto Xon/Xoff Flow Control
Auto Hysteresis Level	16 Selectable Levels ±N from the trigger level	16 Selectable Levels Select Upper and Lower Hysteresis Levels irrespective of trigger level
Infrared Mode	**IrDA encoder/decoder (ver 1.0)**	N/A
Sleep Mode	Sleep Mode with Auto Wake-up	Sleep Mode with Auto Wake-up
Diagnostic Modes	Local loopback	Local Loopback
RS485 Mode	**Auto RS485 Mode**	N/A
LSR bits 4-2 Interrupt Generation	Immediate	Delayed

1.4 REPLACING THE TL16C752B WITH THE ST16C2550, XR16L2750, XR16L2751 OR XR16C2850

You can directly replace TI's TL16C752B with Exar's ST16C2550 and XR16L2750 with minimal hardware changes if using the 48-QFP package. Also, you can replace the TL16C752B with the XR16L2751 or XR16C2850 if the extra input pins are tied to VCC or GND. The crystal oscillator circuitry should work in most cases, but it may be necessary to modify the oscillator circuitry as well. If replacing with the 44-PLCC or 40-PDIP packages, hardware changes will be required since the TL16C752B is not available in those packages.

Replacing the TL16C752B with the ST16C2550 is simple when the system is not using Automatic RTS/CTS Flow Control or Transmit Trigger Levels.

But, if the TL16C752B is replaced by the XR16L2750, XR16L2751 or XR16C2850, then the software will need to be updated to take advantage of the enhanced features of the Exar DUARTs that are not available in or different from the TL16C752B. For example, the Exar DUARTs have hysteresis levels while the TL16C752B has selectable halt and resume transmission levels. The hysteresis levels for the XR16L2750 take into effect when the FIFO fills up to the number of characters (hysteresis level selected) above and below the trigger level. The Halt and Resume Transmission Levels of the TL16C752B operate irrespective of the trigger level. It is up to the programmer to ensure that the upper level (Halt Transmission Level) is greater than the lower level (Resume Transmission Level). Differences like this example should be taken into consideration.

The TL16C752B is a 3.3 V device only, but can be replaced by any of the Exar DUARTs because they can all operate at 3.3 V as well as 5 V. The XR16L2750 and XR16L2751 can also operate at 2.5 V and can operate at 3.3 V with 5 V tolerance. At any voltage, the Exar DUARTs have a lower power consumption than the TL16C752B.

There should not be any timing problems replacing the TL16C752B with the Exar DUARTs because they are more flexible than the TL16C752B as described in the bus timing section.

1.5 TL16C752B KNOWN DEFICIENCIES

The TL16C752B has two known deficiencies and are directly stated in TI's datasheet, but TI does not have any plans to fix them.

On page 12 of the TL16C752B's datasheet dated "December 1999 - Revised August 2000," TI gives a note advising not to write to Baud Rate Divisors DLL and DLH (DLM) while in sleep mode. Exar DUARTs do not have any such problems.

On page 22 of the TL16C752B datasheet, they describe a "timing error condition" in non-FIFO mode where the LSR and IIR (ISR) reports a data byte as available to read from the RHR, but there is no valid data ready to be read from the RHR. The Exar DUARTs do not have this problem in FIFO or non-FIFO mode.

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