DALC208SC6Y

Automotive low capacitance diode array for ESD protection

Datasheet – production data

Features

- Protection of 4 lines
- Peak reverse voltage: V_{RRM} = 9 V per diode
- Very low capacitance per diode: C < 5 pF
- Very low leakage current: I_R < 1 µA

Benefits

- Cost effective solution compared with discrete solution
- High efficiency in ESD suppression
- No significant signal distortion thanks to very low capacitance
- High reliability offered by monolithic integration
- Lower PCB area consumption versus discrete solution
- AEC-Q101 qualified

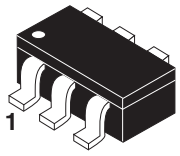
Complies with the following standards

- ISO10605 - C = 150 pF, R = 330 Ω:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- ISO10605 - C = 330 pF, R = 330 Ω
  - 8 kV (air discharge)
  - 8 kV (contact discharge)
- ISO7637-3:
  - Pulse 3a: V_s = -150V
  - Pulse 3b: V_s = +100V

Applications

Where ESD and EOS transient overvoltage protection in susceptible equipment is required, such as:

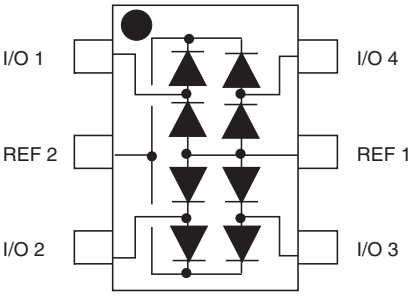
- Information and entertainment
- Signal communications
- Connectivity



SOT23-6L

- Comfort and convenience

Figure 1. Functional diagram (top view)



Description

The DALC208SC6Y diode array is designed to protect components which are connected to data and transmission lines from overvoltages caused by electrostatic discharge (ESD) or other transients. It is a rail-to-rail protection device also suited for overshoot and undershoot suppression on sensitive logic inputs.

The low capacitance of the DALC208SC6Y prevents significant signal distortion.

This is information on a product in full production. www.st.com

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP} (1)	Peak pulse voltage	ISO 10605 (C = 150 pF, R = 330 Ω) Air discharge Contact discharge ISO 10605 (C = 330 pF, R = 330 Ω) Air discharge Contact discharge	 15 8 8 8	kV
V_{RRM}	Peak reverse voltage per diode		9	V
ΔV_{REF}	Reference voltage gap between V_{REF2} and V_{REF1}		9	V
V_{In} max.	Maximum operating signal input voltage		V_{REF2}	V
V_{In} min.	Minimum operating signal input voltage		V_{REF1}	V
T_j	Operating junction temperature range		-40 to +150	°C
T_{stg}	Storage temperature range		-65 to +150	
T_L	Maximum junction temperature for soldering during 10 s		260	

1. For a surge greater than the maximum values the diode will fail in short-circuit.

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction to ambient (1)	500	°C/W

1. Device mounted on FR4 PCB with recommended footprint dimensions.

Figure 2. Electrical characteristics - definitions

Symbol		Parameter
V_F	=	Forward voltage drop
I_F	=	Forward current
I_{RM}	=	Leakage current @ V_{RM}
C_{line}	=	Line capacitance

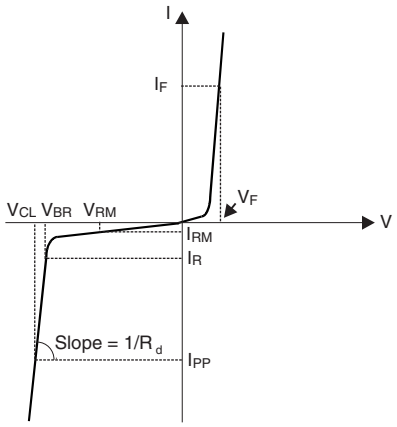


Table 3. Electrical characteristics - values (T_{amb} = 25 °C)

Symbol	Parameter	Conditions	Typ.	Max.	Unit
V_F	Forward voltage	I_F = 50 mA		1.2	V
I_R	Reverse leakage current per diode	V_R = 5 V		1	µA
C	Input capacitance between Line and GND	See *Figure 3.*	7	10	pF

Figure 3. Input capacitance measurement

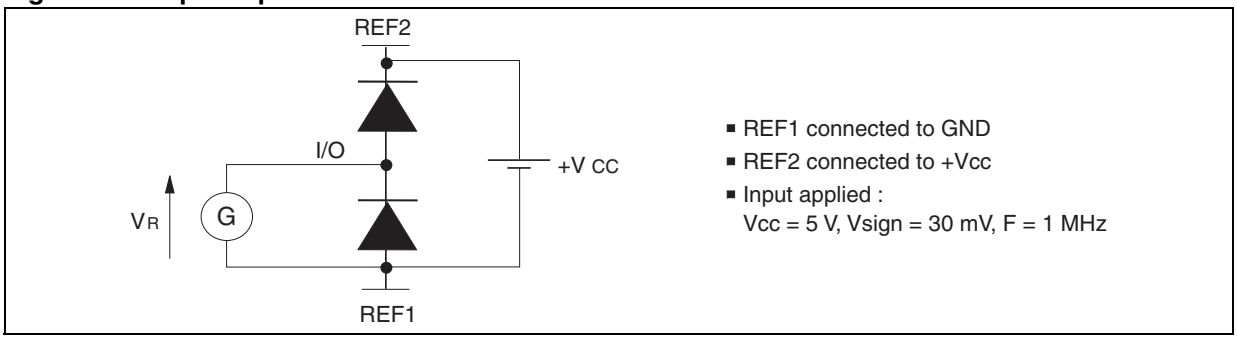


Figure 4. Reverse clamping voltage versus peak pulse current (T_j initial = 25 °C), typical values

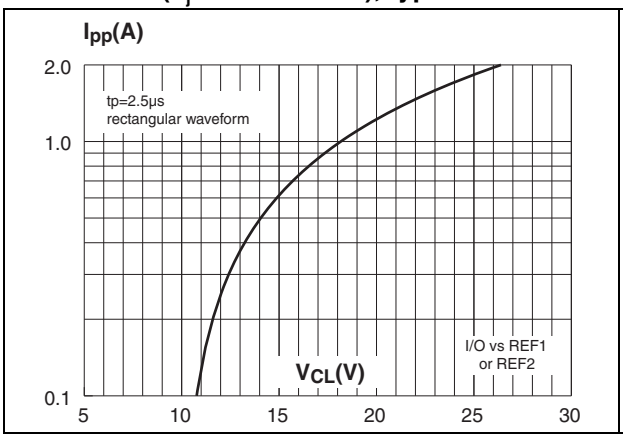


Figure 5. Variation of leakage current versus junction temperature (typical values)

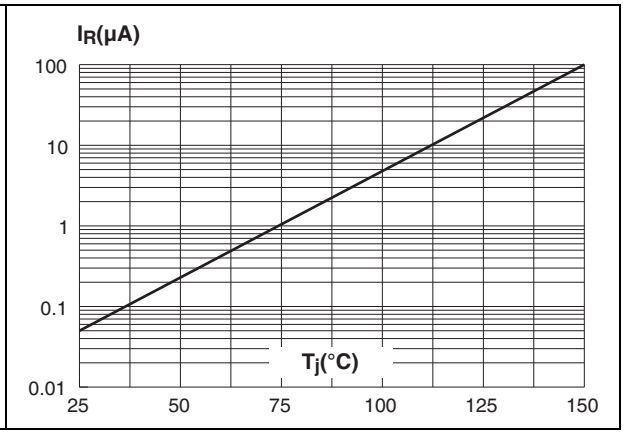
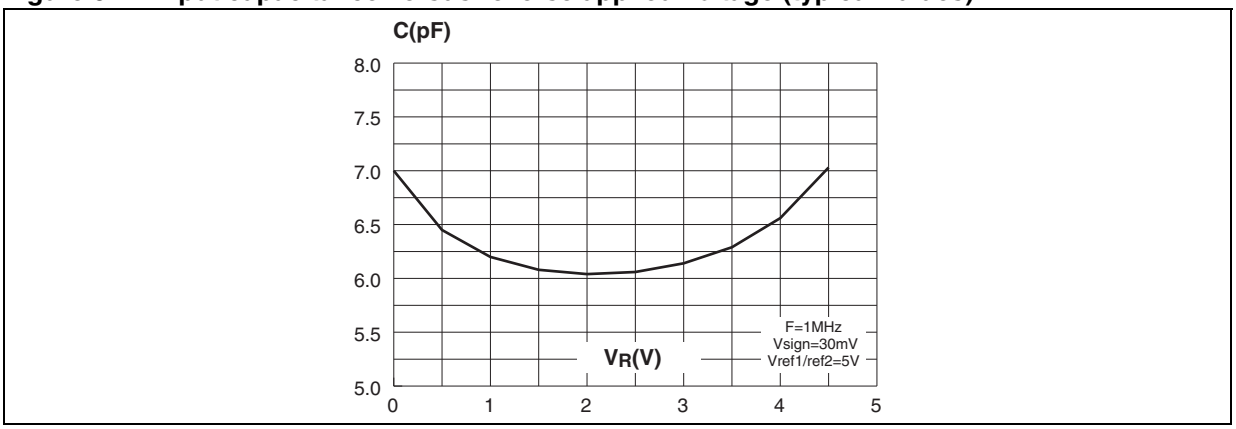


Figure 6. Input capacitance versus reverse applied voltage (typical values)



2 Technical information

2.1 Surge protection

The DALC208SC6Y is particularly optimized to perform surge protection based on the rail to rail topology.

The clamping voltage V_{CL} can be calculated as follow:

$V_{CL}+ = V_{REF2} + V_F$ for positive surges

$V_{CL}- = V_{REF1} - V_F$ for negative surges

with

$V_F = V_T + R_d.I_p$

(V_F forward drop voltage) / (V_T forward drop threshold voltage)

We assume that the value of the dynamic resistance of the clamping diode is typically $R_d = 0.7\ \Omega$ and $V_T = 1.2$ V.

For an IEC 61000-4-2 surge Level 4 (Contact Discharge: V_g=8 kV, $R_g = 330\ \Omega$), V_{REF2} = +5 V, V_{REF1} = 0 V, and if in first approximation, we assume that: $I_p = V_g / R_g$ ′ 24 A.

So, we find:

- $V_{CL}+$′ +23 V
- $V_{CL}-$′ -18 V

Note: The calculations do not take into account phenomena due to parasitic inductances.

2.2 Surge protection application example

If we consider that the connections from the pin REF_2 to V_{CC} and from REF_1 to GND are done by two tracks of 10 mm long and 0.5 mm large; we assume that the parasitic inductances of these tracks are about 6 nH. So when an IEC 61000-4-2 surge occurs, due to the rise time of this spike (t_r = 1 ns), the voltage V_{CL} has an extra value equal to Lw.dI/dt.

The dI/dt is calculated as: $dI/dt = I_p/t_r$ ′ 24 A/ns

The overvoltage due to the parasitic inductances is: Lw.dI/dt = 6 x 24 ′ 144V

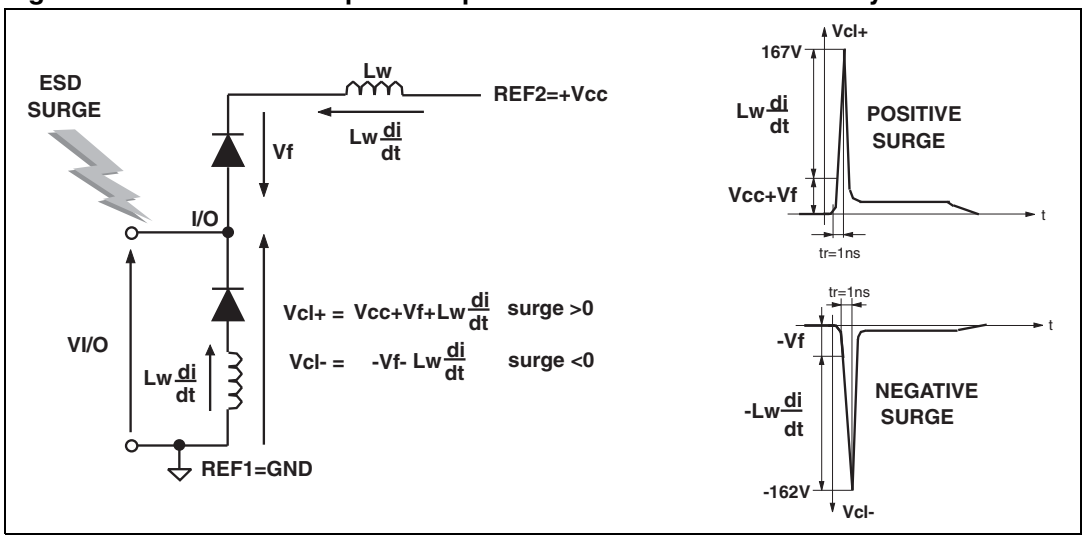
By taking into account the effect of these parasitic inductances due to unsuitable layout, the clamping voltage will be:

- $V_{CL}+ = +23 + 144$ ′ 167 V
- $V_{CL}- = -18 - 144$ ′ -162 V

We can reduce as much as possible these phenomena with simple layout optimization.

It's the reason why some recommendations have to be followed closely. See *Section 2.3: How to ensure good ESD protection*.

Figure 7. ESD behavior: parasitic phenomena due to unsuitable layout



2.3 How to ensure good ESD protection

While the DALC208SC6Y provides a high immunity to ESD surge, an efficient protection depends on the layout of the board. In the same way, with the rail to rail topology, the track from the V_{REF2} pin to the power supply $+V_{CC}$ and from the V_{REF1} pin to GND must be as short as possible to avoid over voltages due to parasitic phenomena. See *Figure 7*.

It's often harder to connect the power supply near to the DALC208SC6Y unlike the ground thanks to the ground plane that allows a short connection.

To ensure the same efficiency for positive surges when the connections can't be short enough, we recommend putting a capacitance of 100 nF close to the DALC208SC6Y, between V_{REF2} and ground, to prevent these kinds of overvoltage disturbances.
See *Figure 8*.

The addition of this capacitance will allow a better protection by providing a constant voltage during a surge.

Figure 9, *Figure 10*, and *Figure 11* show the improvement of the ESD protection according to the recommendations described above.

Figure 8. ESD behavior: optimized layout and add of a capacitance of 100 nF

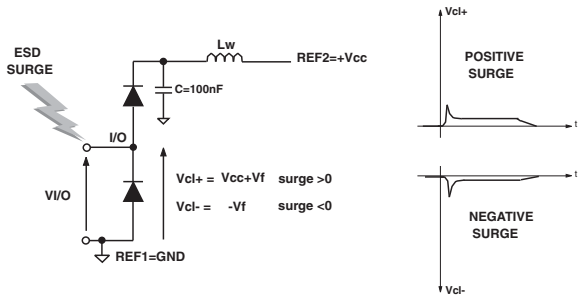


Figure 9. ESD behavior: measurement conditions (with coupling capacitance)

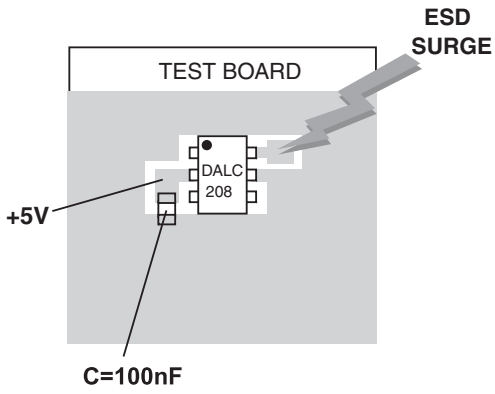


Figure 10. Remaining voltage after the DALC208SC6Y during positive ESD surge

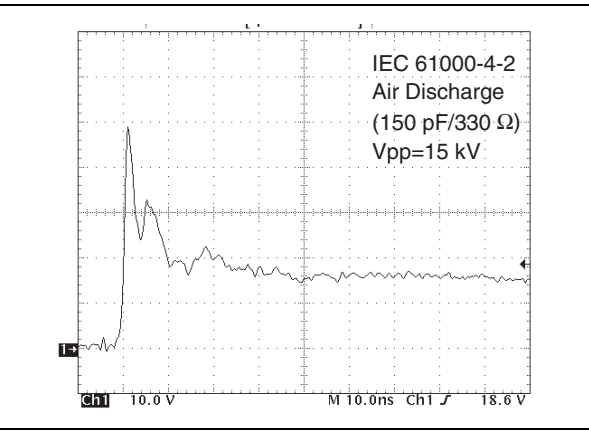
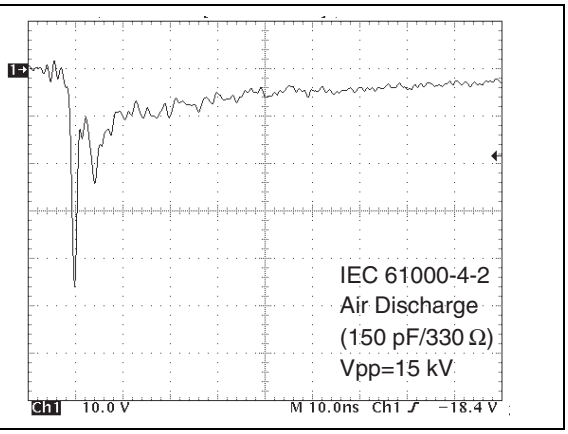


Figure 11. Remaining voltage after the DALC208SC6Y during negative ESD surge



Important

Put the protection device as close as possible to the disturbance source (generally the connector).

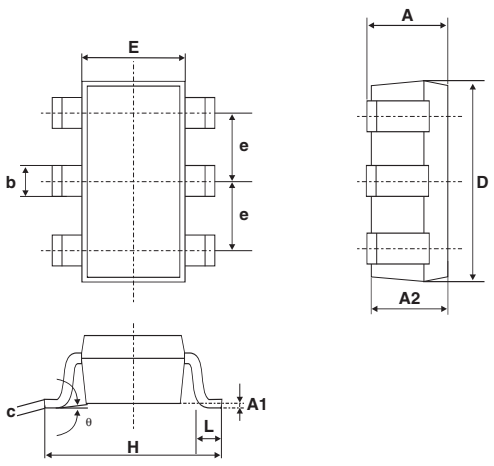
Note: The measurements have been done with the DALC208SC6Y in open circuit.

3 Package information

- Epoxy meets UL94, V0
- Lead-free package

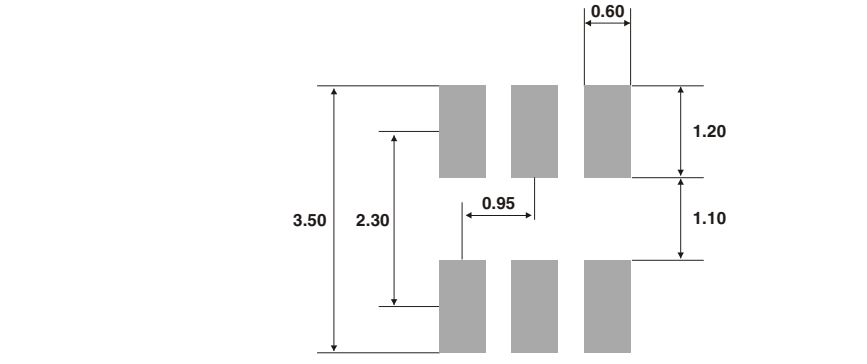
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 4. SOT23-6L dimensions



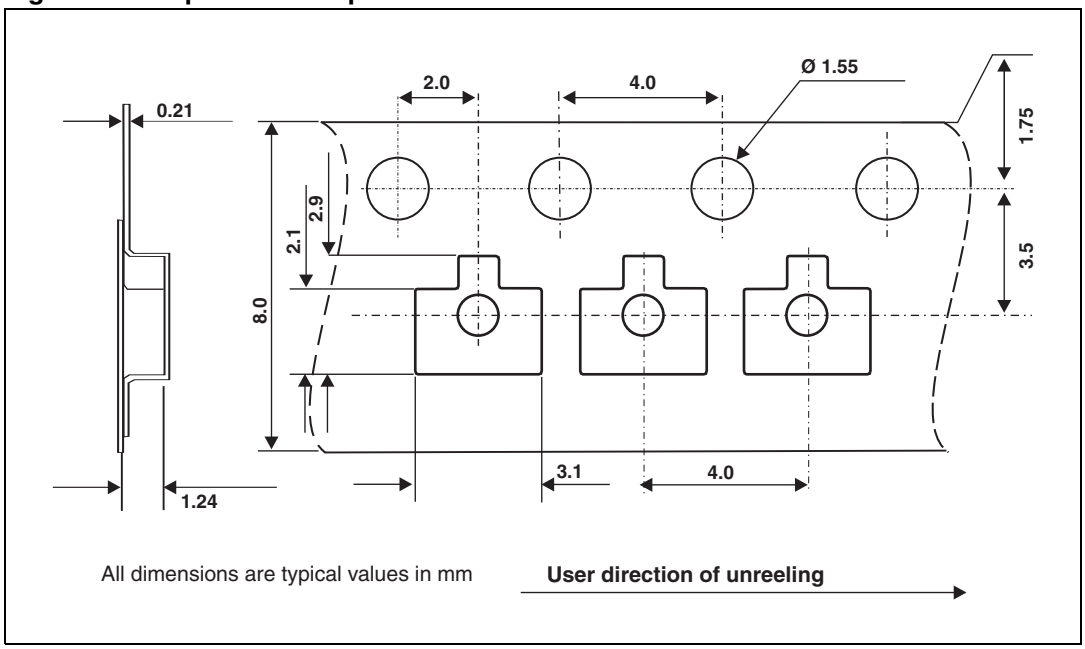
Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	0.035		0.057
A1	0		0.10	0		0.004
A2	0.90		1.30	0.035		0.051
b	0.35		0.50	0.014		0.020
c	0.09		0.20	0.004		0.008
D	2.80		3.05	0.11		0.118
E	1.50		1.75	0.059		0.069
e		0.95			0.037	
H	2.60		3.00	0.102		0.118
L	0.10		0.60	0.004		0.024
θ	0°		10°	0°		10°

Figure 12. Footprint (dimensions in mm)



Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 13. Tape and reel specification



4 Recommendation on PCB assembly

4.1 Solder paste

1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Offers a high tack force to resist component displacement during PCB movement.
4. Use solder paste with fine particles: powder particle size 20-45 µm.

4.2 Placement

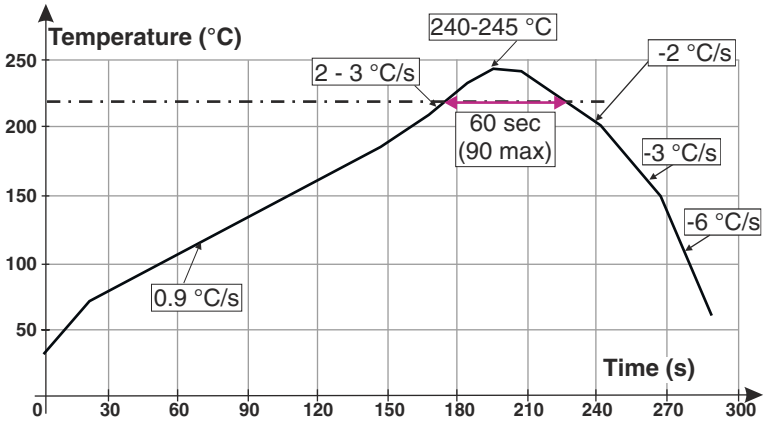
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.3 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.4 Reflow profile

Figure 14. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

5 Ordering information

Table 5. Ordering information

Order code	Marking	Package	Weight	Base qty	Packing mode
DALC208SC6Y	DALY	SOT23-6L	16.7 mg	3000	Tape and reel

For the latest information on available order codes see the product pages on www.st.com.

6 Revision history

Table 6. Document revision history

Date	Revision	Changes
07-Nov-2012	1	First issue.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2012 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com