



16-Bit, Single-Channel, $\pm 18\text{V}$ Output (Unbuffered), Ultra-Low Power, Serial Interface DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 16-Bit Resolution
- Output: $\pm 18\text{V}$ for $\pm 18\text{V}$ Reference Input
- $\pm 18\text{V}$ Supply Operation
- Very Low Power
- High Accuracy INL: 1LSB
- Low Noise: $10\text{nV}/\sqrt{\text{Hz}}$
- Fast Settling: $1\mu\text{s}$ to 1LSB
- Fast SPI™ Interface: Up To 50MHz
- 16-Pin TSSOP Package
- Selectable Reset to Zero or Midscale

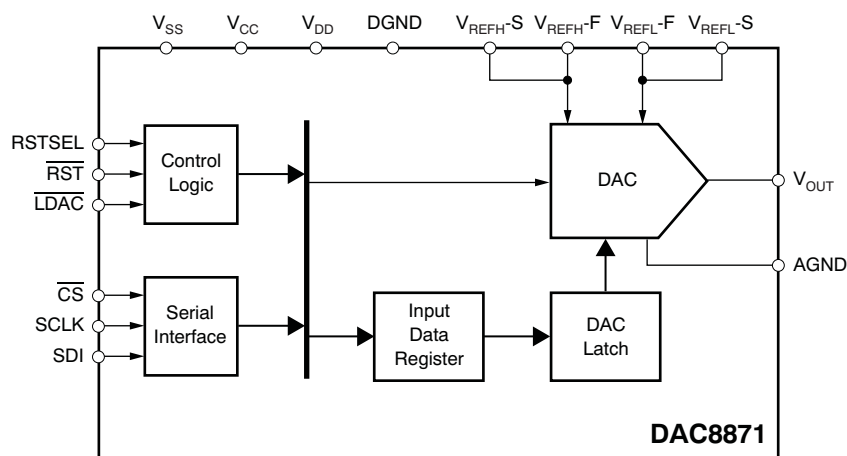
APPLICATIONS

- Portable Equipment
- Automatic Test Equipment
- Industrial Process Control
- Data Acquisition Systems
- Optical Networking

DESCRIPTION

The DAC8871 is a 16-bit, single-channel, serial input, voltage output digital-to-analog converter (DAC). The output range is determined by the reference voltage, V_{REFH} and V_{REFL} . By properly selecting the reference, the output can be unipolar or bipolar, and up to $\pm 18\text{V}$. The DAC8871 provides excellent linearity (1LSB INL), low noise, and fast settling ($1\mu\text{s}$ to 1LSB of full scale output) over the specified temperature range of -40°C to $+105^{\circ}\text{C}$. The output is unbuffered, which reduces the power consumption and the error introduced by the buffer. This device features a standard high-speed clock (up to 50MHz), and a 3V or 5V SPI serial interface to communicate with the DSP or microprocessors. For optimum performance, a set of Kelvin connections to external reference are provided.

The DAC8871 is available in a TSSOP-16 package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TI DSP is a trademark of Texas Instruments.

SPI, QSPI are trademarks of Motorola, Inc.

Microwire is a trademark of National Semiconductor.

All other trademarks are the property of their respective owners.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	PACKAGE- LEAD	PACKAGE DESIGNATOR
DAC8871B	±1	±1	–40°C to +105°C	8871	TSSOP-16	PW
DAC8871	±3	±1	–40°C to +105°C	8871	TSSOP-16	PW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range (unless otherwise noted).

	DAC8871	UNIT
V_{DD} to GND	–0.3 to +7	V
Digital input voltage to GND	–0.3 to ($V_{DD} + 0.3$)	V
AGND to DGND	–0.3 to +0.3	V
V_{CC} to V_{SS}	–0.3 to +39.6	V
V_{CC} to AGND	–0.3 to +19.8	V
V_{SS} to AGND	+0.3 to –19.8	V
V_{REFH} to V_{REFL}	–0.3 to +39.6	V
V_{REFH} to AGND	–0.3 to +19.8	V
V_{REFL} to AGND	–19.8 to +17.5	V
Operating temperature range	–40 to +105	°C
Storage temperature range	–65 to +150	°C
Maximum junction temperature (T_J max)	+150	°C
Power dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$	W
Thermal impedance, θ_{JA}	TSSOP-16	161.4
		C/W

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

All specifications at $T_A = T_{MIN}$ to T_{MAX} , $V_{CC} = +15V$, $V_{SS} = -15V$, $V_{REFH} = +10V$, $V_{REFL} = -10V$, and $V_{DD} = +5V$, unless otherwise noted; specifications subject to change without notice.

PARAMETER		CONDITIONS	DAC8871			UNIT	
			MIN	TYP	MAX		
STATIC PERFORMANCE							
Resolution			16			Bits	
Linearity error	DAC8871B	V _{REFH} = 10V, V _{REFL} = −5V	±0.75			±1	LSB
		V _{REFH} = 10V, V _{REFL} = −10V	±1			±1.5	LSB
	DAC8871		±1			±3	LSB
Differential linearity error			±0.25			±1	LSB
Gain error		T _A = +25°C	±0.5			2	LSB
Gain drift			±0.1				ppm/°C
Bipolar zero error		T _A = +25°C	±1			±4	LSB
Bipolar drift			±0.1				ppm/°C
Zero code error		T _A = +25°C	±0.5			±2	LSB
Zero code drift			±0.05				ppm/°C
OUTPUT CHARACTERISTICS							
Voltage output			V _{REFL}		V _{REFH}	V	
Output impedance			6.25			kΩ	
Settling time		To 1LSB of FS, C _L = 15 pF	1			μs	
Slew rate ⁽¹⁾		C _L = 15pF	40			V/μs	
Digital feedthrough ⁽²⁾			0.2			nV-s	
Output noise		T _A = +25°C	10			nV/√Hz	
Power supply rejection		Supplies vary ±10%				1	LSB
REFERENCE INPUT							
V _{REFH}	Ref high input voltage range		0		+18	V	
V _{REFL}	Ref low input voltage range		−18		V _{REFH} − 1.25	V	
	Ref high input current		1.3			mA	
	Ref low input current		−1.3			mA	
	Reference input impedance ⁽³⁾		7.5			kΩ	
	Reference input capacitance	Code = 0000h	75			pF	
		Code = FFFFh	120			pF	
DIGITAL INPUTS							
V _{IL}	Input low voltage	V _{DD} = +5V	DGND		0.8	V	
		V _{DD} = +3V	DGND		0.6	V	
V _{IH}	Input high voltage	V _{DD} = +5V	2.6		V _{DD}	V	
		V _{DD} = +3V	2.1		V _{DD}	V	
Input current			±1			μA	
Input capacitance			10			pF	

(1) Slew Rate is measured from 10% to 90% of transition when the output changes from 0 to full scale.

(2) Digital feedthrough is defined as the impulse injected into the analog output from the digital input. It is measured when the DAC output does not change; $\overline{CS}$ is held high, while SCLK and DIN signals are toggled. It is specified with a full-scale code change on the SDI bus (that is, from all 0s to all 1s and vice versa).

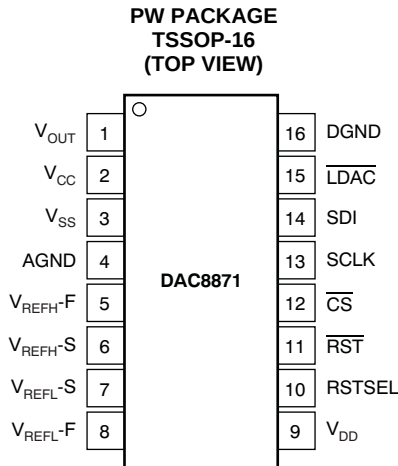
(3) Reference input resistance is code-dependent, with a minimum at 8555h

ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX} , $V_{CC} = +15V$, $V_{SS} = -15V$, $V_{REFH} = +10V$, $V_{REFL} = -10V$, and $V_{DD} = +5V$, unless otherwise noted; specifications subject to change without notice.

PARAMETER	CONDITIONS	DAC8871			UNIT
		MIN	TYP	MAX	
POWER SUPPLY					
V _{CC}		+13.5	+15	+19.8	V
V _{SS}		−19.8	−15	−13.5	V
V _{DD}		+2.7		+5.5	V
I _{CC}			0.01	2	μA
I _{SS}			−0.01	−2	μA
I _{DD}			3	10	μA
Power			15	30	μW
TEMPERATURE RANGE					
Specified performance		−40		+105	°C

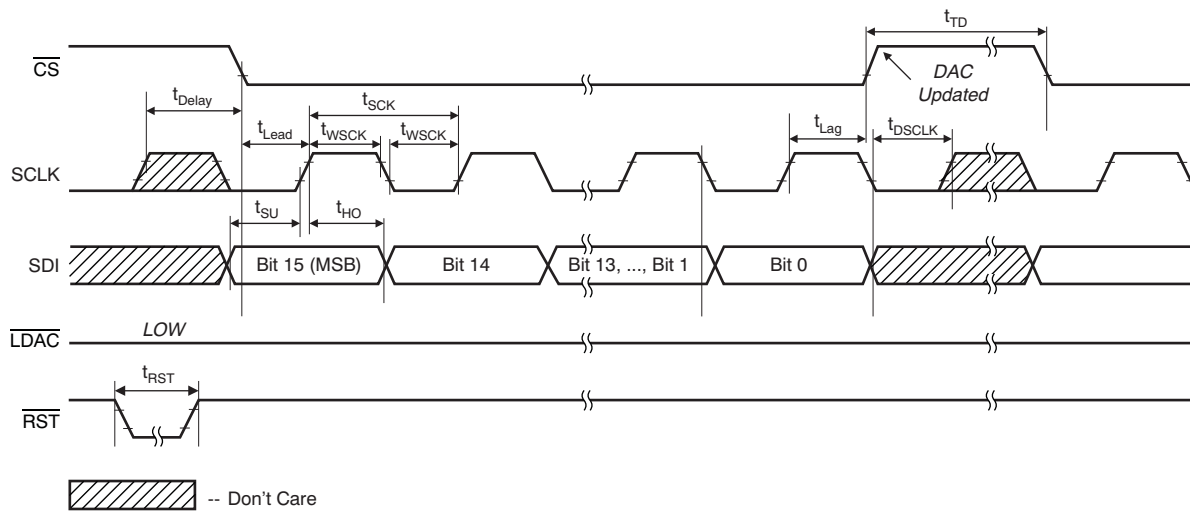
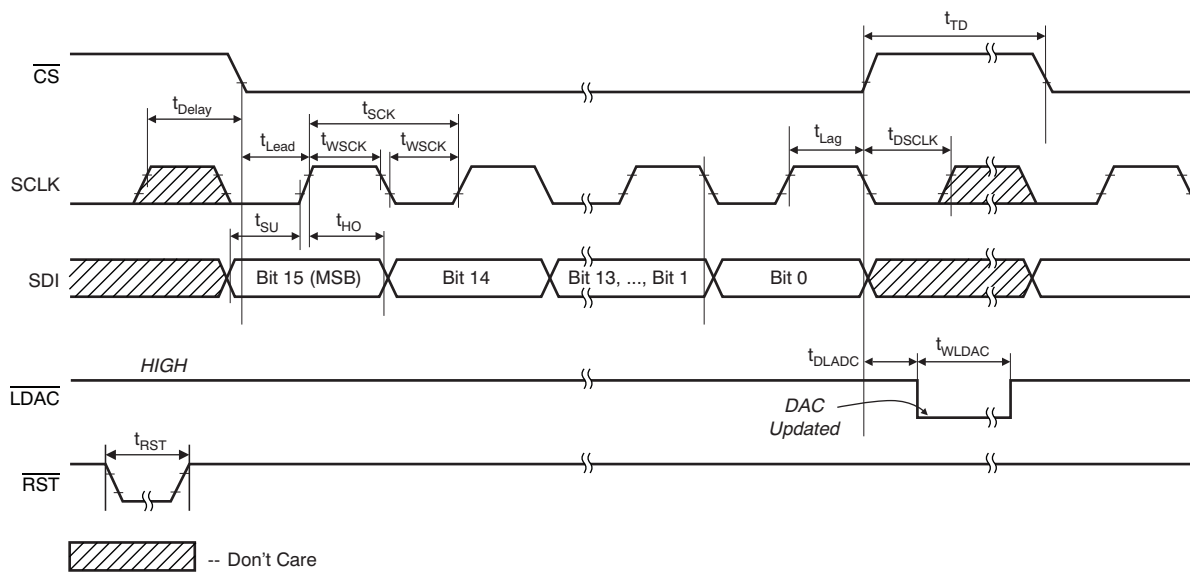
PIN CONFIGURATION (NOT TO SCALE)



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NO.	NAME	
1	V _{OUT}	Analog output of the DAC
2	V _{CC}	Positive analog power supply: +15V
3	V _{SS}	Negative analog power supply: –15V
4	AGND	Analog ground
5	V _{REFH-F}	V _{REFH} reference input (Force). Connect to external V _{REFH} .
6	V _{REFH-S}	V _{REFH} reference input (Sense). Connect to external V _{REFH} .
7	V _{REFL-S}	V _{REFL} reference input (Sense). Connect to external V _{REFL} .
8	V _{REFL-F}	V _{REFL} reference input (Force). Connect to external V _{REFL} .
9	V _{DD}	Digital power. +5V for 5V interface logic; +3V for 3V logic.
10	RSTSEL	Power-On-Reset select. Determines V _{OUT} after power-on reset. If tied to V _{DD} , the DAC latch is set to mid-scale after power-on, and V _{OUT} is (V _{REFH} – V _{REFL})/2. If tied to DGND, the DAC latch is cleared ('0'), and V _{OUT} is V _{REFL} .
11	RST	Reset (active low)
12	CS	Chip select input (active low). Data are not clocked into SDI unless CS is low.
13	SCLK	Serial clock input
14	SDI	Serial data input. Data are latched into input register on the rising edge of SCLK.
15	LDAC	Load DAC control input (active low). When LDAC is low, the DAC latch is simultaneously updated with the content of the input register.
16	DGND	Digital ground

TIMING DIAGRAMS

Figure 1. Case 1— $\overline{\text{LDAC}}$ Tied LowFigure 2. Case 2— $\overline{\text{LDAC}}$ Active

TIMING CHARACTERISTICS: $V_{DD} = +5V$ ⁽¹⁾ ⁽²⁾

At –40°C to +105°C, unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
t_{SCK}	SCLK period	20		ns
t_{WSCK}	SCLK high or low time	10		ns
t_{Delay}	Delay from SCLK high to $\overline{CS}$ low	10		ns
t_{Lead}	$\overline{CS}$ enable lead time	10		ns
t_{Lag}	$\overline{CS}$ enable lag time	10		ns
t_{DSCLK}	Delay from $\overline{CS}$ high to SCLK high	10		ns
t_{TD}	$\overline{CS}$ high between active period	30		ns
t_{SU}	Data setup time (input)	10		ns
t_{HO}	Data hold time (input)	0		ns
t_{WLDAC}	$\overline{LDAC}$ width	30		ns
t_{DLDAC}	Delay from $\overline{CS}$ high to $\overline{LDAC}$ low	30		ns
t_{RST}	Reset ($\overline{RST}$) low	10		ns
	V_{DD} high to $\overline{CS}$ low (power-up delay)	10		μs

(1) Assured by design. Not production tested.

(2) Sample tested during the initial release and after any redesign or process changes that may affect this parameter.

TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_{DD} = +5\text{V}$, $V_{CC} = +15\text{V}$, $V_{SS} = -15\text{V}$, $V_{REFH} = +10\text{V}$, and $V_{REFL} = -10\text{V}$, unless otherwise noted.

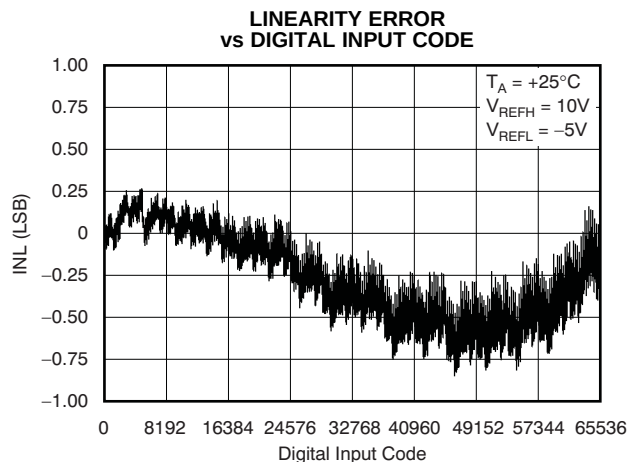


Figure 3.

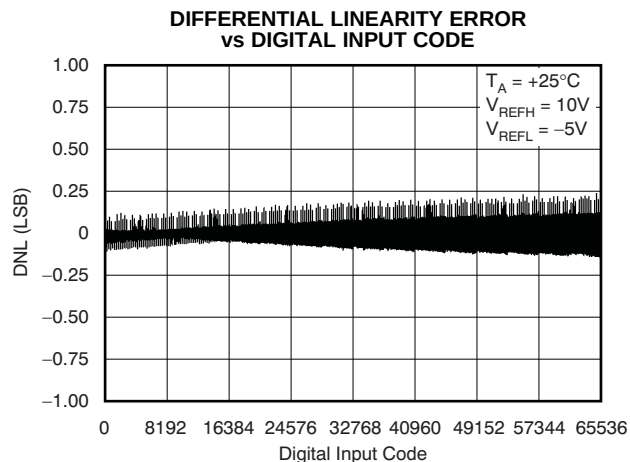


Figure 4.

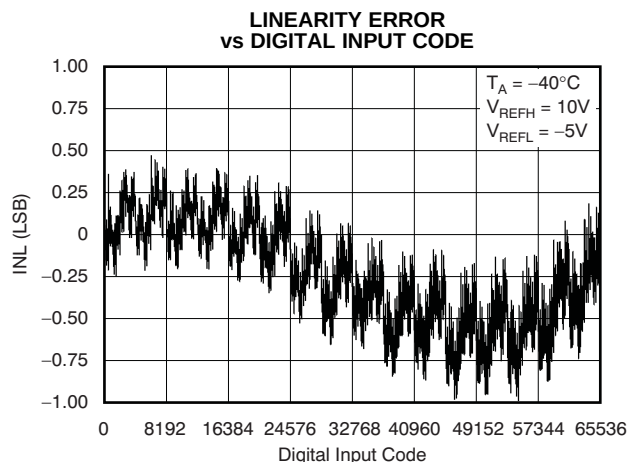


Figure 5.

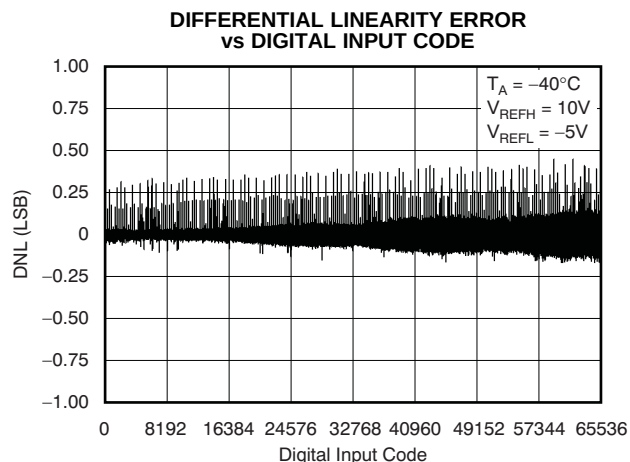


Figure 6.

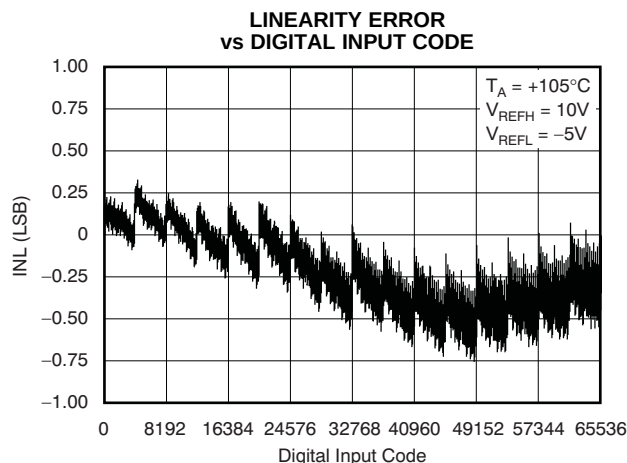


Figure 7.

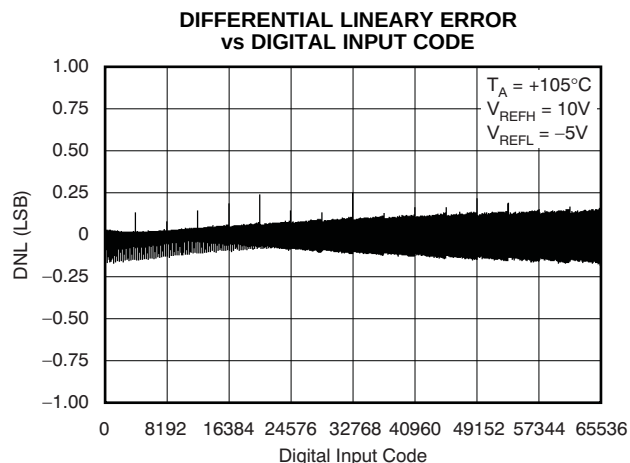


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_{DD} = +5\text{V}$, $V_{CC} = +15\text{V}$, $V_{SS} = -15\text{V}$, $V_{REFH} = +10\text{V}$, and $V_{REFL} = -10\text{V}$, unless otherwise noted.

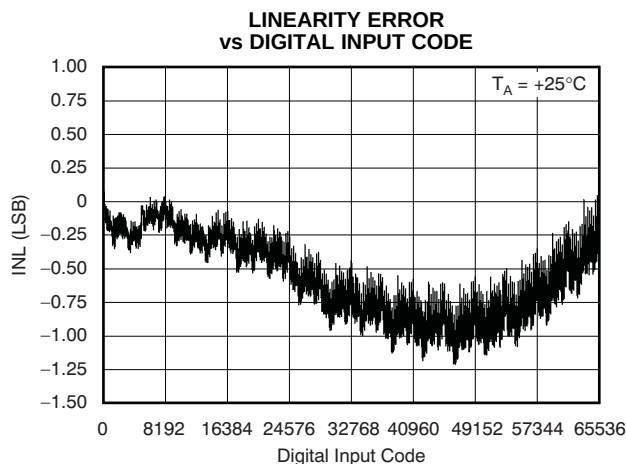


Figure 9.

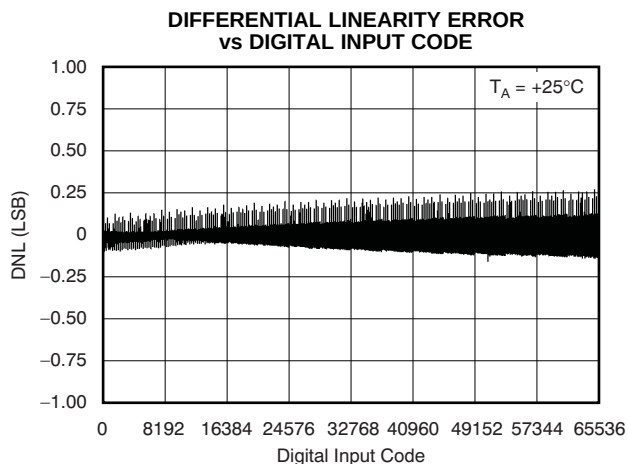


Figure 10.

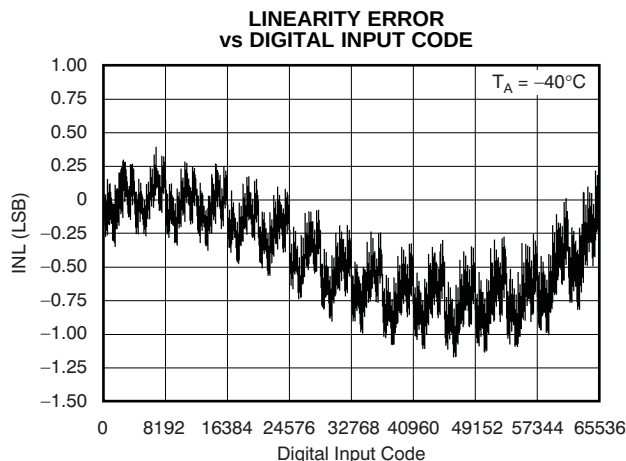


Figure 11.

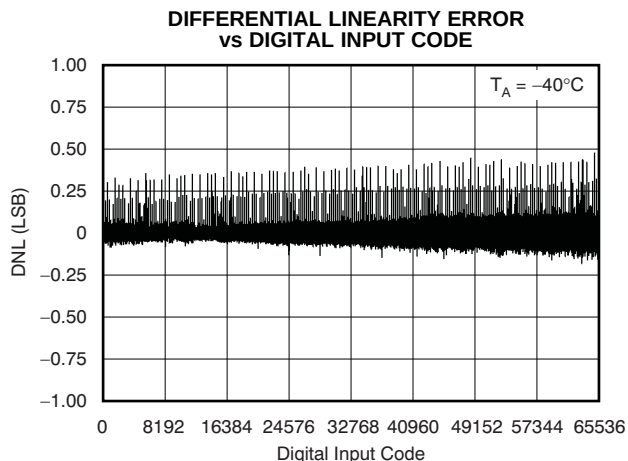


Figure 12.

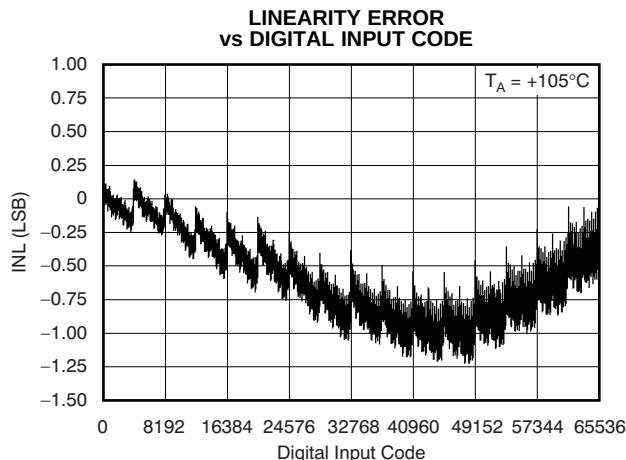


Figure 13.

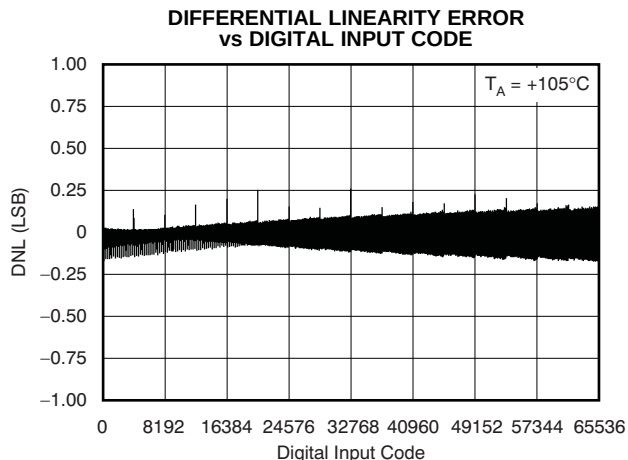


Figure 14.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_{DD} = +5\text{V}$, $V_{CC} = +15\text{V}$, $V_{SS} = -15\text{V}$, $V_{REFH} = +10\text{V}$, and $V_{REFL} = -10\text{V}$, unless otherwise noted.

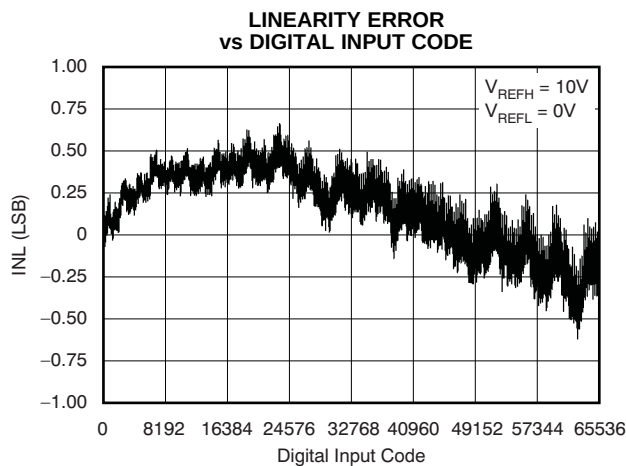


Figure 15.

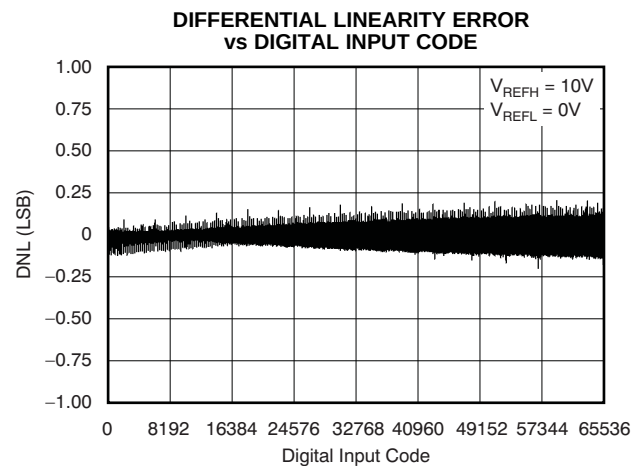


Figure 16.

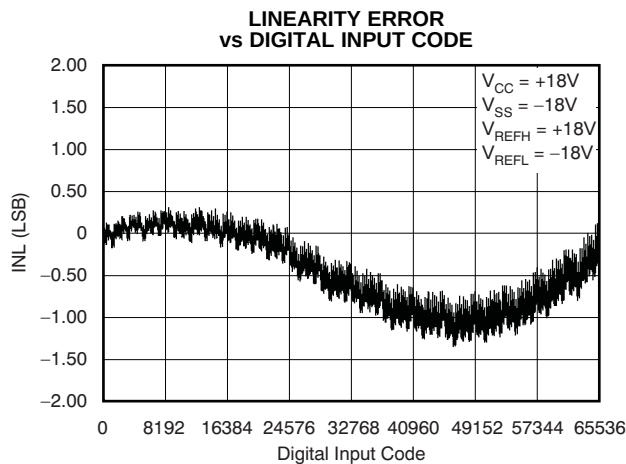


Figure 17.

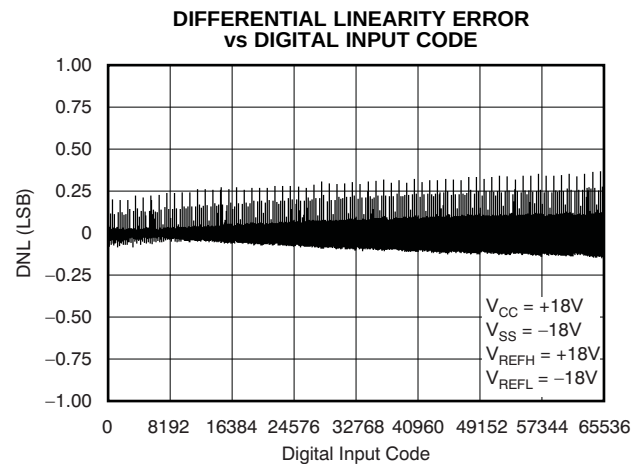


Figure 18.

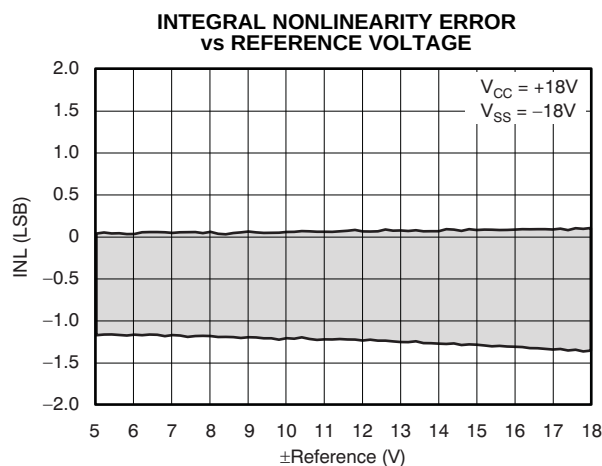


Figure 19.

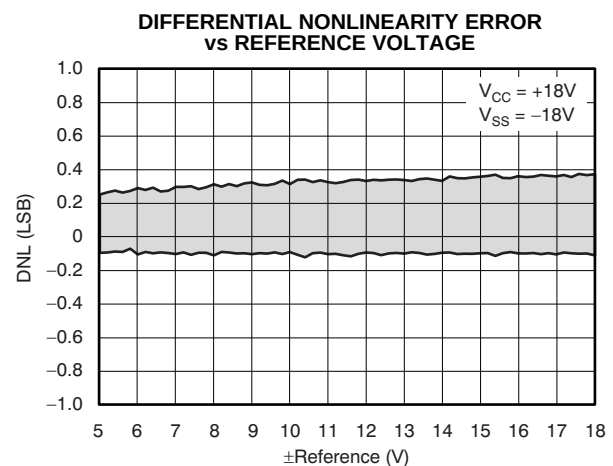


Figure 20.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_{DD} = +5\text{V}$, $V_{CC} = +15\text{V}$, $V_{SS} = -15\text{V}$, $V_{REFH} = +10\text{V}$, and $V_{REFL} = -10\text{V}$, unless otherwise noted.

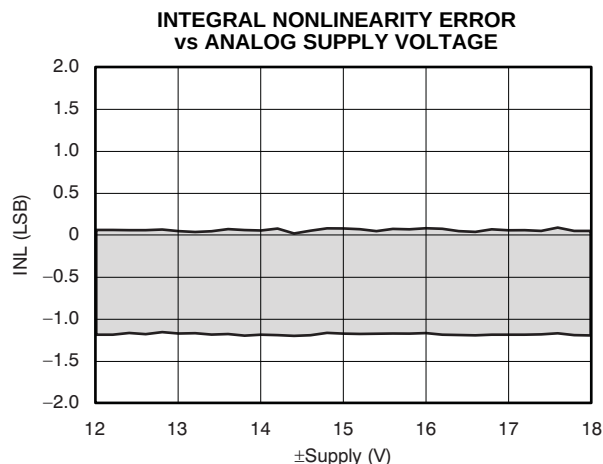


Figure 21.

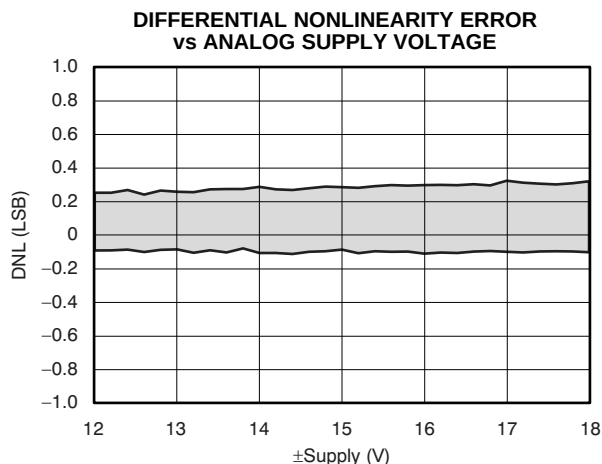


Figure 22.

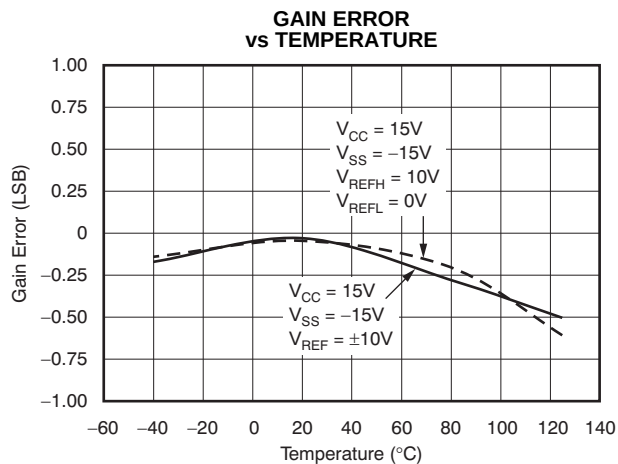


Figure 23.

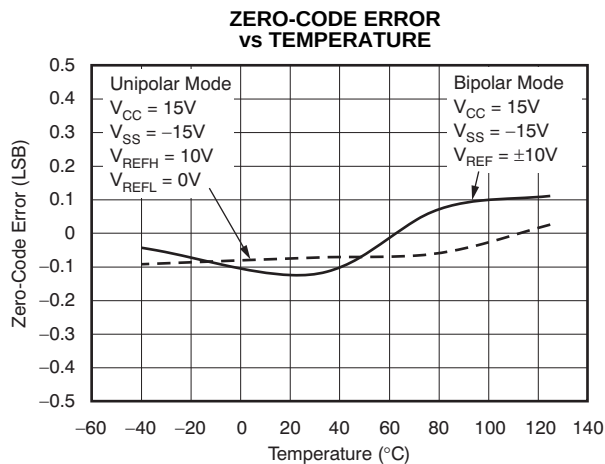


Figure 24.

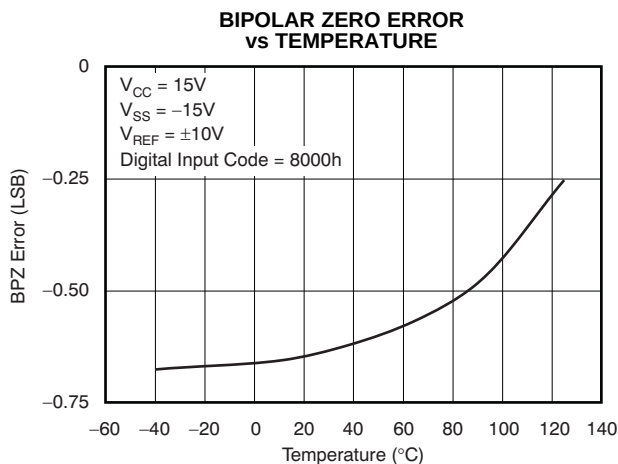


Figure 25.

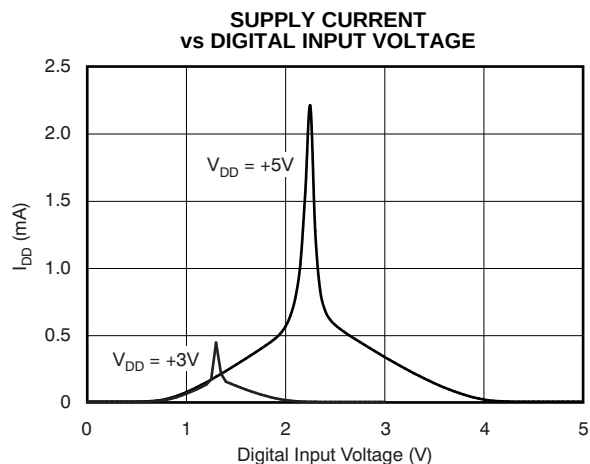


Figure 26.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_{DD} = +5\text{V}$, $V_{CC} = +15\text{V}$, $V_{SS} = -15\text{V}$, $V_{REFH} = +10\text{V}$, and $V_{REFL} = -10\text{V}$, unless otherwise noted.

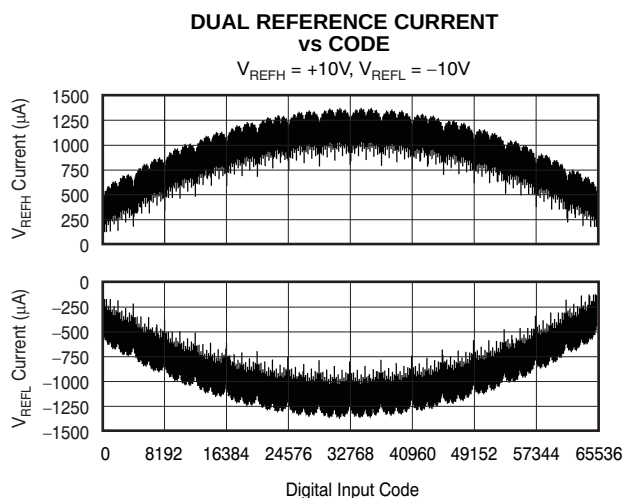


Figure 27.

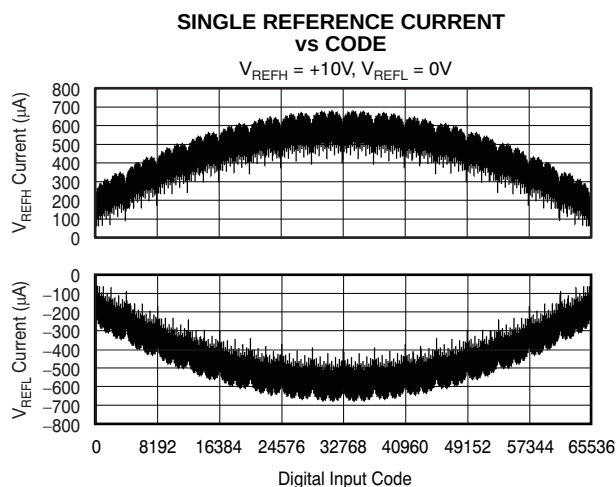


Figure 28.

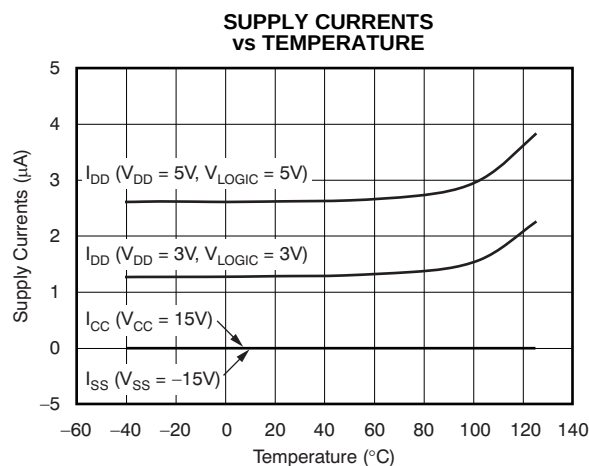


Figure 29.

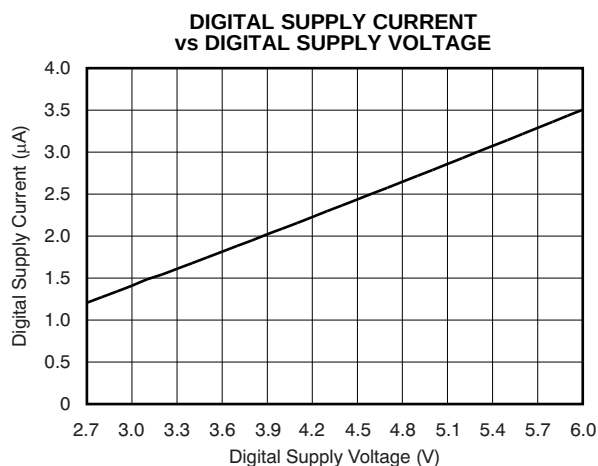


Figure 30.

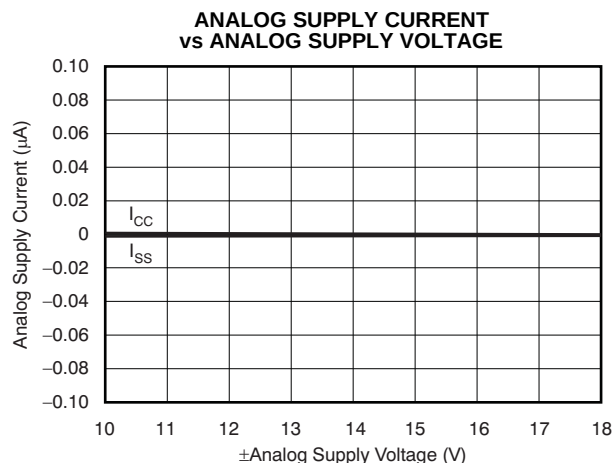


Figure 31.

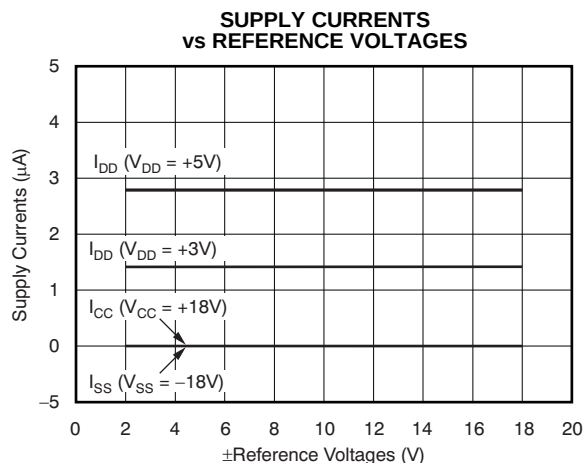


Figure 32.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_{DD} = +5\text{V}$, $V_{CC} = +15\text{V}$, $V_{SS} = -15\text{V}$, $V_{REFH} = +10\text{V}$, and $V_{REFL} = -10\text{V}$, unless otherwise noted.

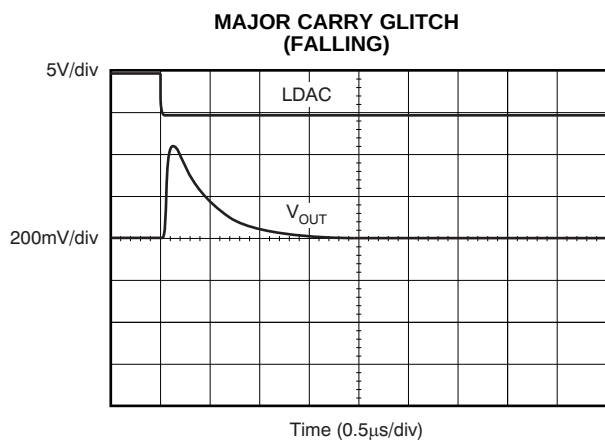


Figure 33.

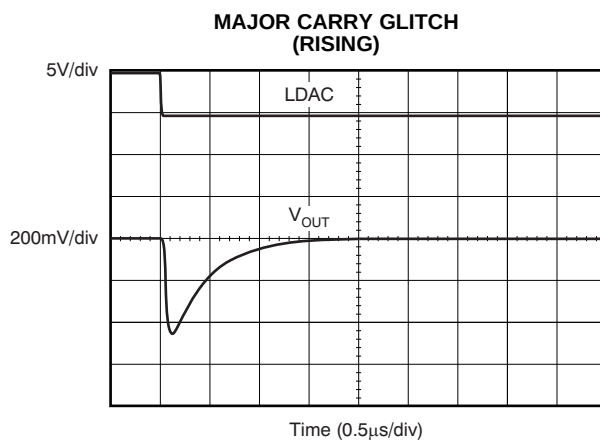


Figure 34.

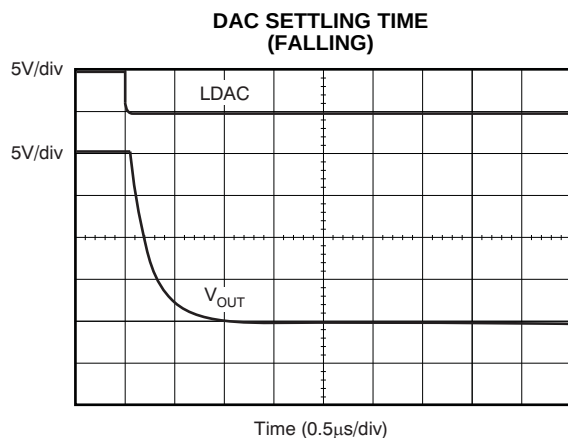


Figure 35.

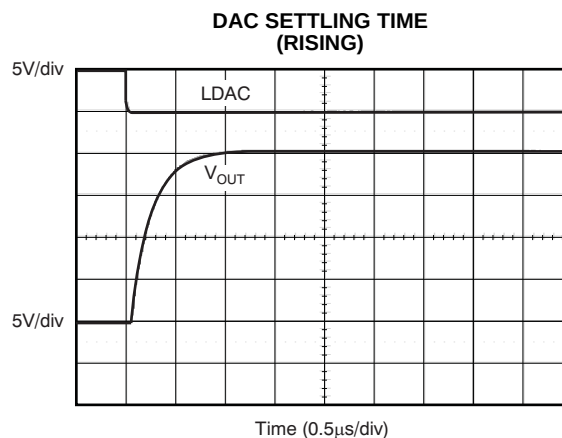


Figure 36.

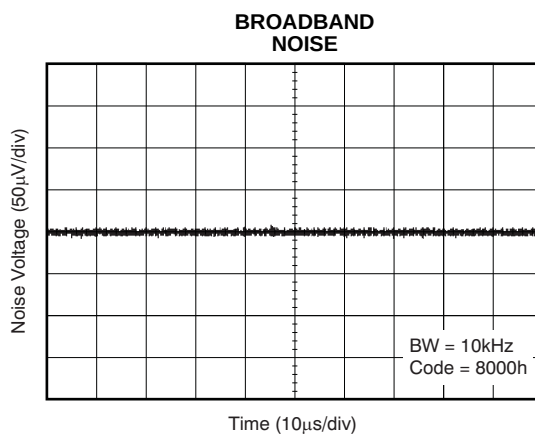


Figure 37.

THEORY OF OPERATION

GENERAL DESCRIPTION

The DAC8871 is a 16-bit, single-channel, serial-input, voltage-output DAC. It operates from a dual power supply ranging from $\pm 13.5\text{V}$ to $\pm 19.8\text{V}$, and typically consumes $10\mu\text{A}$. The output range is from V_{REFL} to V_{REFH} . Data are written to this device in a 16-bit word format, via an SPI serial interface. To ensure a known power-up state, the DAC8871 is designed with a power-on reset function. After power on, the state of the RSTSEL pin sets the value of the input register and DAC latch, which sets the output state of the V_{OUT} pin. Refer to the [Power-On Reset and Hardware Reset](#) section for more details.

Kelvin sense connections for the reference and analog ground are also included.

DIGITAL-TO-ANALOG SECTIONS

The DAC architecture consists of two matched DAC sections and is segmented. A simplified circuit diagram is shown in [Figure 38](#). The four MSBs of the 16-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of 15 matched resistors to either V_{REFH} or V_{REFL} . The remaining 12 bits of the data word drive switches S0 to S11 of a 12-bit voltage mode R-2R ladder network.

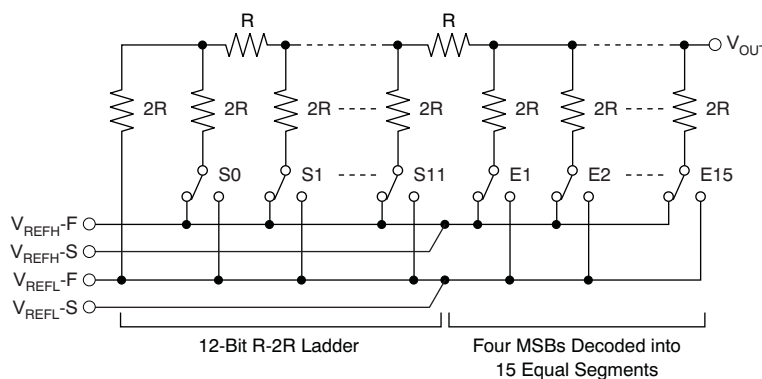


Figure 38. DAC Architecture

OUTPUT RANGE

The output of the DAC is:

$$V_{\text{OUT}} = \frac{V_{\text{REFH}} - V_{\text{REFL}}}{65536} \times \text{Code} + V_{\text{REFL}} \quad (1)$$

Where *Code* is the decimal data word loaded to the DAC latch.

For example, if V_{REFH} is $+10\text{V}$, and V_{REFL} is -10V , the range of V_{OUT} is from -10V (Code = 0000h) to $+10\text{V}$ (Code = FFFFh).

The range of V_{REFL} is from -18V to $(V_{\text{REFH}} - 1.25\text{V})$, and the range of V_{REFH} is 0V to $+18\text{V}$. The output from the DAC8871 can be unipolar (from 0V to $+18\text{V}$) or bipolar by setting the proper V_{REFL} and V_{REFH} values.

POWER-ON RESET AND HARDWARE RESET

The DAC8871 has a power-on reset function. When the RSTSEL pin is low (tied to DGND), and after power-on or a hardware reset signal is applied to the $\overline{\text{RST}}$ pin, the DAC latch is cleared ('0') and the V_{OUT} pin is set to negative full-scale. When RSTSEL is high, the DAC latch and V_{OUT} are set to mid-scale.

SERIAL INTERFACE

The DAC8871 digital interface is a standard 3-wire connection compatible with SPI, QSPI™, Microwire™ and TI DSP™ interfaces, which can operate at speeds up to 50 Mbits/second. The data transfer is framed by the chip select ($\overline{\text{CS}}$) signal. The DAC works as a bus slave. The bus master generates the synchronize clock (SCLK) and initiates the transmission. When $\overline{\text{CS}}$ is high, the DAC is not accessed, and SCLK and SDI are ignored. The bus master accesses the DAC by driving $\overline{\text{CS}}$ low. Immediately following the high-to-low transition of $\overline{\text{CS}}$, the serial input data on the SDI pin are shifted out from the bus master synchronously on the falling edge of SCLK and latched on the rising edge of SCLK into the input shift register, MSB first. The low-to-high transition of $\overline{\text{CS}}$ transfers the content of the input shift register to the input register.

All data registers are 16 bits. It takes 16 SCLK cycles to transfer one data word to the device. To complete a whole data word, $\overline{\text{CS}}$ must be taken high immediately after the 16th SCLK is clocked in. If more than 16 SCLK cycles are applied while $\overline{\text{CS}}$ is low, the last 16 bits are transferred into the input register on the rising edge of $\overline{\text{CS}}$. However, if $\overline{\text{CS}}$ is not kept low during the entire 16 SCLK cycles, the data are corrupted. In this case, reload the DAC latch with a new 16-bit word.

The DAC8871 has an $\overline{\text{LDAC}}$ pin that allows the DAC latch to be updated asynchronously by bringing $\overline{\text{LDAC}}$ low after $\overline{\text{CS}}$ goes high. In this case, $\overline{\text{LDAC}}$ must be kept high while $\overline{\text{CS}}$ is low. If $\overline{\text{LDAC}}$ is permanently tied low, the DAC latch will be updated immediately after the input register is loaded (caused by the low-to-high transition of $\overline{\text{CS}}$).

EXTERNAL AMPLIFIER SELECTION

The output of the DAC8871 is unbuffered. The output impedance is approximately 6.2k Ω . If the applications require an external buffer amplifier, the selected amplifier must have a low-offset voltage (1LSB = 305 μV for $\pm 10\text{V}$ output range), eliminating the need for output offset trims. Input bias current should also be low because the bias current multiplied by the DAC output impedance (approximately 6.25k Ω) adds to the zero-code error. Rail-to-rail input and output performance is required. For fast settling, the slew rate of the operational amplifier should not impede the settling time of the DAC. The output impedance of the DAC is constant and code-independent, but in order to minimize gain errors, the input impedance of the output amplifier should be as high as possible. The amplifier should also have a 3dB bandwidth of 1MHz or greater. The amplifier adds another time constant to the system, thus increasing the settling time of the output. A higher 3dB amplifier bandwidth results in a shorter effective settling time of the DAC and amplifier combination.

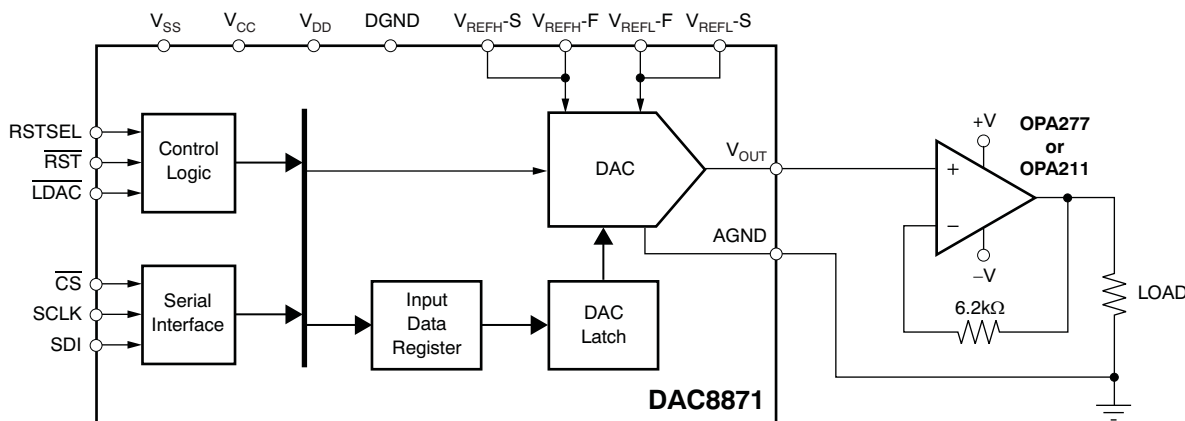


Figure 39. DAC8871 with External Amplifier

APPLICATION INFORMATION

REFERENCE INPUT

The DAC full-scale output voltage is determined by the reference voltage, as shown in the [Output Range](#) section.

Reference input V_{REFH} can be any voltage from 0V to +18V. Reference input V_{REFL} can be any voltage from –18V to ($V_{REFH} - 1.25V$). The current into the V_{REFH} input and out of V_{REFL} depends on the DAC output voltages. Refer to [Figure 27](#) and [Figure 28](#) for details. The reference input appears as a varying load to the reference. If the reference can sink or source the required current, a reference buffer is not required. The DAC8871 features a reference drive (force) and sense connection that minimizes the internal errors caused by the changing reference current and the circuit impedances. [Figure 40](#) shows a typical reference configuration.

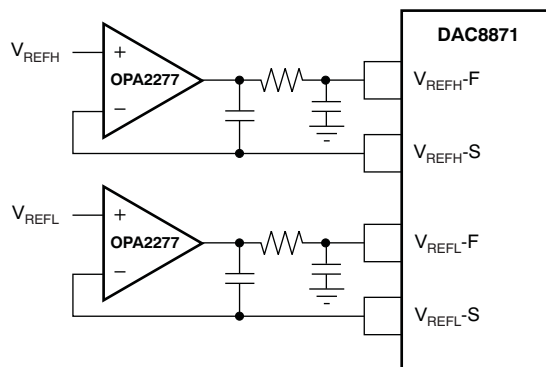


Figure 40. Buffered Reference Connection

POWER-SUPPLY BYPASSING

For accurate, high-resolution performance, bypassing the supply pins with a 10 μ F tantalum capacitor in parallel with a 0.1 μ F ceramic capacitor is recommended.

POWER-SUPPLY SEQUENCING

The analog supplies (V_{CC} and V_{SS}) must power up before the digital supply (V_{DD}). All three supplies must power up before the reference voltages (V_{REFH} and V_{REFL}) are applied. Additionally, because the DAC input shift register is not reset during a power-on reset (or a hardware reset through the $\overline{RST}$ pin), the $\overline{CS}$ pin must not be unintentionally asserted during power-up of the device. It is recommended that the $\overline{CS}$ pin be connected to V_{DD} through a pull-up resistor to avoid improper power-up.

Likewise, the state of the $\overline{LDAC}$ pin must not be accidentally changed during power-up. It is recommended that the $\overline{LDAC}$ pin be connected to V_{DD} through a pull-up resistor, unless it is permanently tied to ground.

To ensure that the ESD protection circuitry of this device is not activated, all other digital pins must be kept at ground potential until V_{DD} is applied.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC8871SBPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC8871	Samples
DAC8871SBPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC8871	Samples
DAC8871SBPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC8871	Samples
DAC8871SPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC8871	Samples
DAC8871SPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC8871	Samples
DAC8871SPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAC8871	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

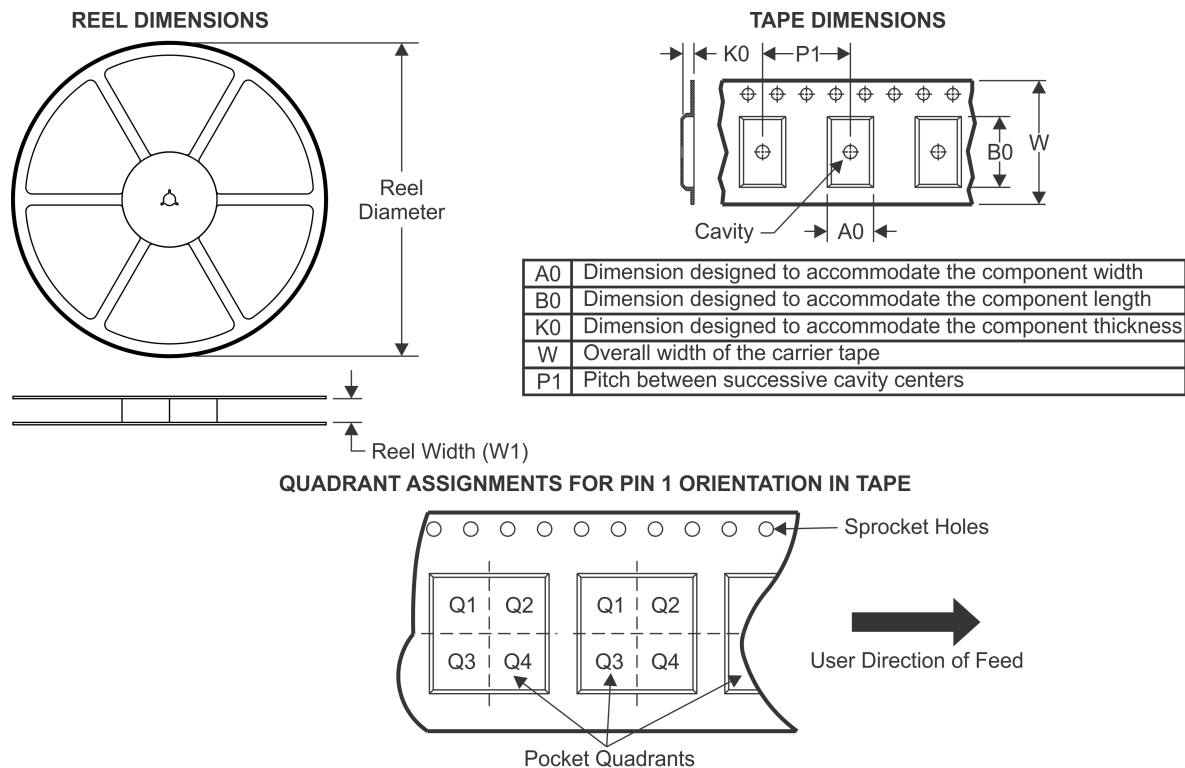
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

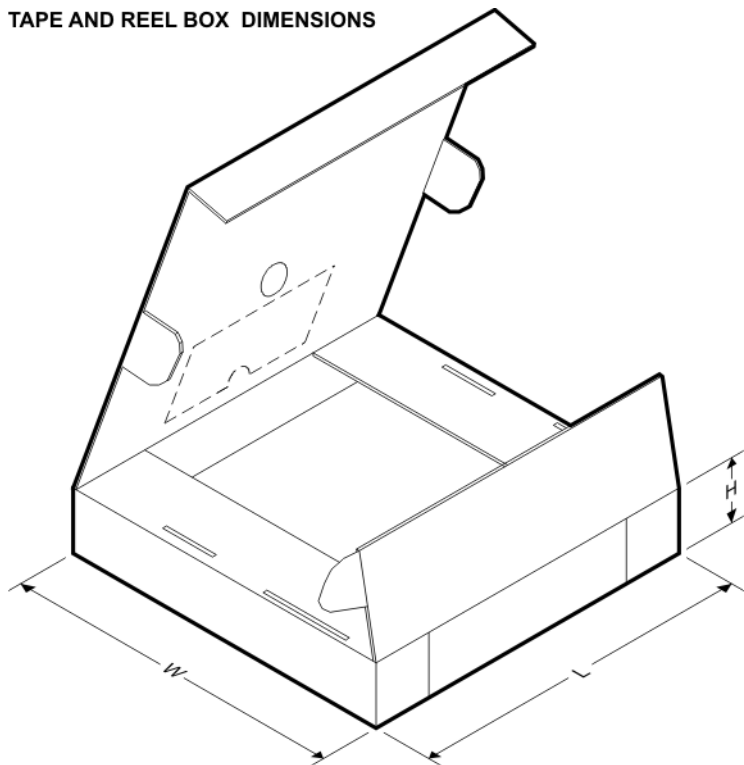
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

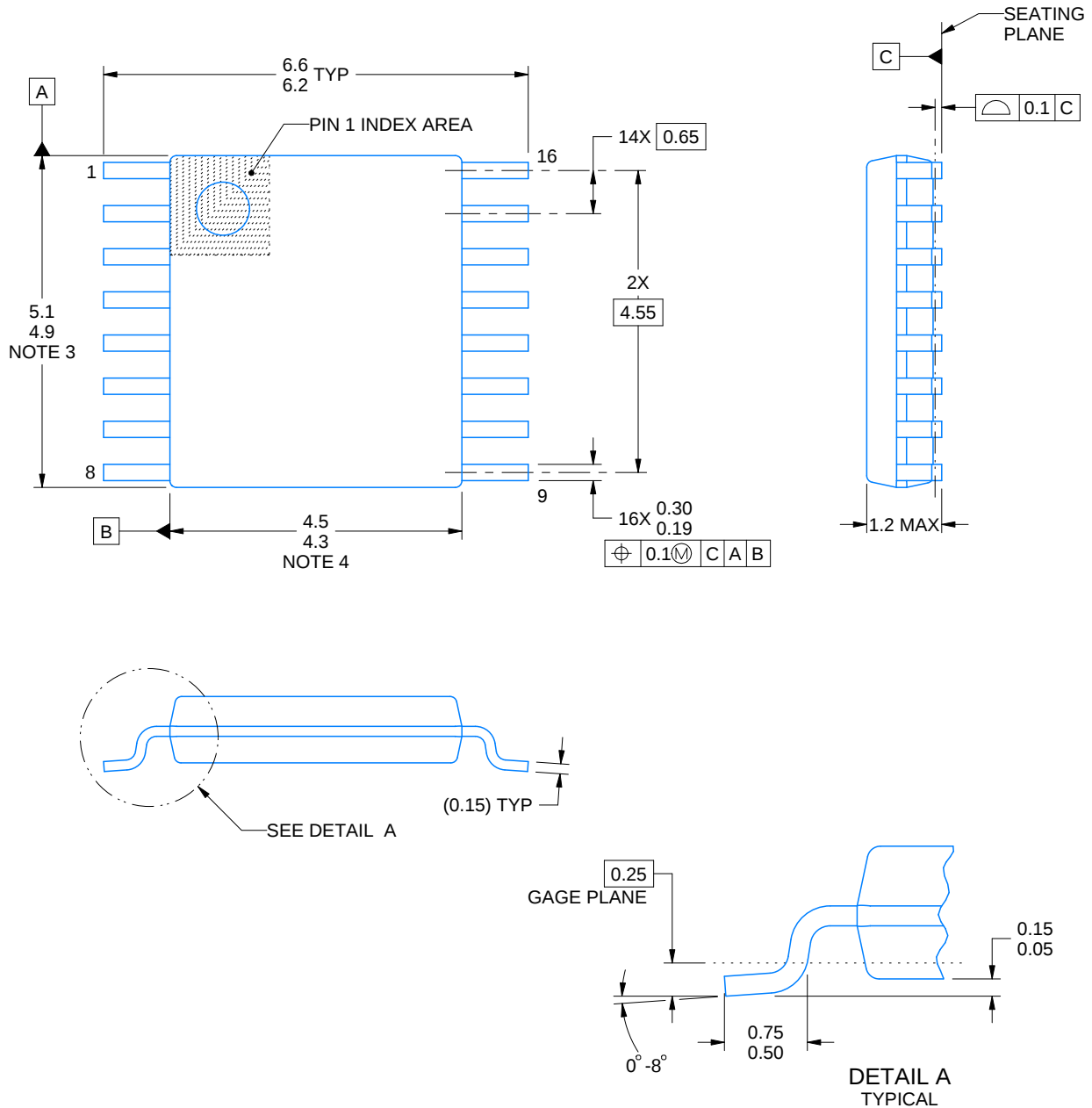
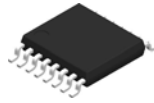
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8871SBPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DAC8871SPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8871SBPWR	TSSOP	PW	16	2000	350.0	350.0	43.0
DAC8871SPWR	TSSOP	PW	16	2000	350.0	350.0	43.0



4220204/A 02/2017

NOTES:

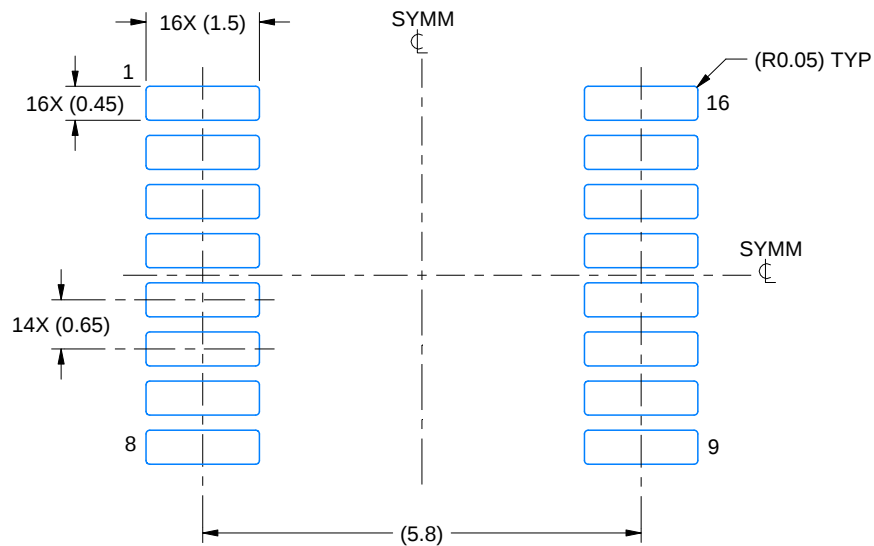
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

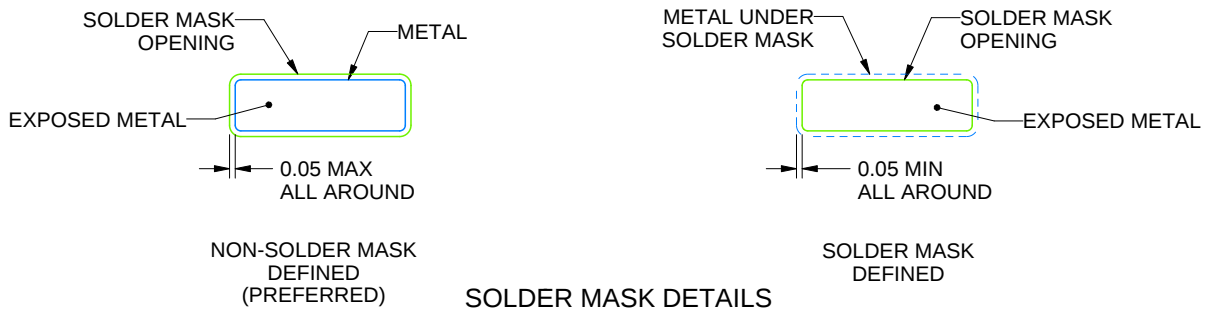
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

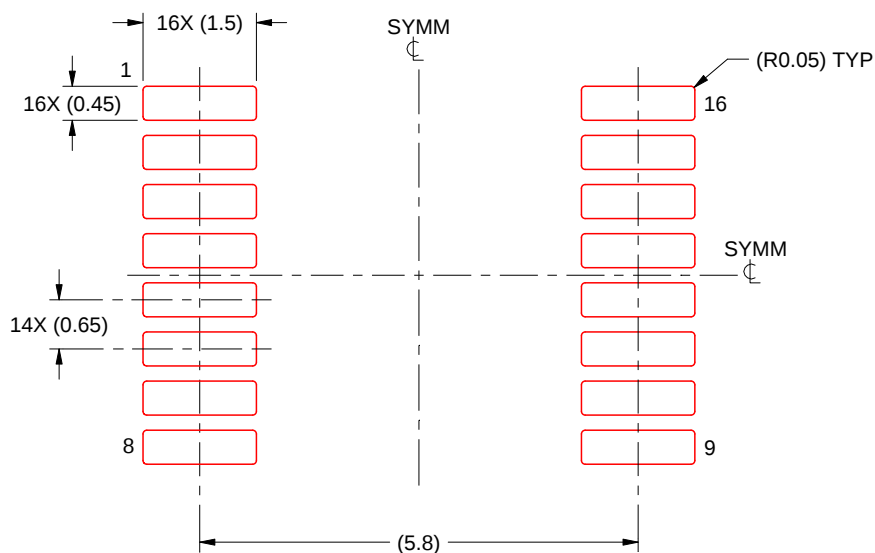
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated