16-Bit, Ultra-Low Power, Voltage-Output Digital-to-Analog Converters

FEATURES

- **Controlled Baseline**
  - **One Assembly**
  - **One Test Site**
  - **One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **16-Bit Resolution**
- **2.7-V to 5.5-V Single-Supply Operation**
- **Low Power: 15 µW for 3-V Power**
- **High Accuracy, INL: 1 LSB**
- **Low Glitch: 8 nV-s**
- **Low Noise: 10 nV/$\sqrt{\text{Hz}}$**
- **Fast Settling: 1 µs**
- **Fast SPI Interface Up to 50 MHz**
- **Reset to Zero-Code**
- **Schmitt-Trigger Inputs for Direct Optocoupler Interface**
- **Industry-Standard Pin Configuration**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

APPLICATIONS

- **Portable Equipment**
- **Automatic Test Equipment**
- **Industrial Process Control**
- **Data Acquisition Systems**
- **Optical Networking**

DESCRIPTION

The DAC8830 and DAC8831 are single, 16-bit, serial-input, voltage-output digital-to-analog converters (DACs) operating from a single 3-V to 5-V power supply. These converters provide excellent linearity, low glitch, low noise, and fast settling over the specified temperature range of –55°C to 125°C. The output is unbuffered, which reduces the power consumption and the error introduced by the buffer.

These parts feature a standard high-speed (clock up to 50 MHz), 3-V or 5-V SPI serial interface to communicate with the DSP or microprocessors.

The DAC8830 output is 0 V to V_{REF}. However, the DAC8831 provides bipolar mode output ($\pm V_{REF}$) when working with an external buffer. The DAC8830 and DAC8831 are both reset to zero-code after power up.

For optimum performance, a set of Kelvin connections to external reference and analog ground input are provided on the DAC8831.

The DAC8830 is available in an SO-8 package and the DAC8831 is available in an SO-14 package. Both have industry standard pinouts (see Table 3, the Cross Reference table in the *Application Information* section for details).

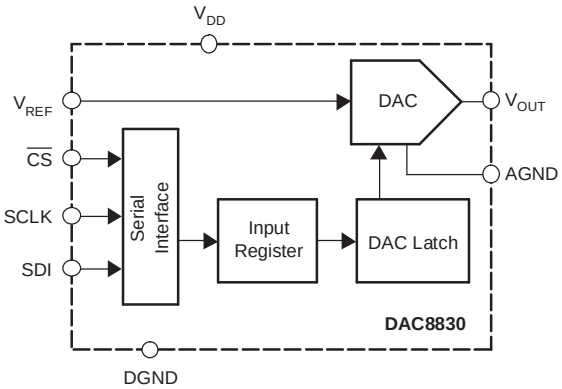
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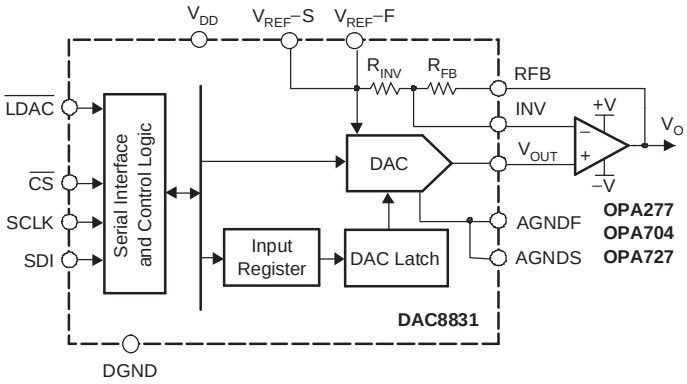
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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DAC8830
Functional Block Diagram



DAC8831
Functional Block Diagram



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	POWER-ON RESET VALUE	SPECIFICATION TEMPERATURE RANGE	PACKAGE MARKING	PACKAGE-LEAD	PACKAGE(2) DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8830MCD	±1	±1	Zero-Code	–55°C to 125°C	8830M	SO-8	D	DAC8830MCDREP	Tape and Reel, 2500
								DAC8830MCDEP	Tube, 75
DAC8831MCD	±1	±1	Zero-Code	–55°C to 125°C	8831M	SO-14	D	DAC8831MCDREP	Tape and Reel, 2500
								DAC8831MCDEP	Tube, 50

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the Texas Instruments website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
V_{DD} to AGND		–0.3 to 7	V
Digital input voltage to DGND		–0.3 to V_{DD} + 0.3	V
V_{OUT} to AGND		–0.3 to V_{DD} + 0.3	V
AGND, AGNDF, AGNDS to DGND		–0.3 to 0.3	V
Operating temperature range		–55 to 125	°C
Storage temperature range		–65 to 150	°C
Junction temperature range (T_J max)		150	°C
Power dissipation		(T_J max – T_A)/ θ_{JA}	W
Thermal impedance, θ_{JA}	SO-8	149.5	°C/W
	SO-14	104.5	°C/W
Lead temperature, soldering	Vapor phase (60 s)	215	°C
	Infrared (15 s)	220	°C

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

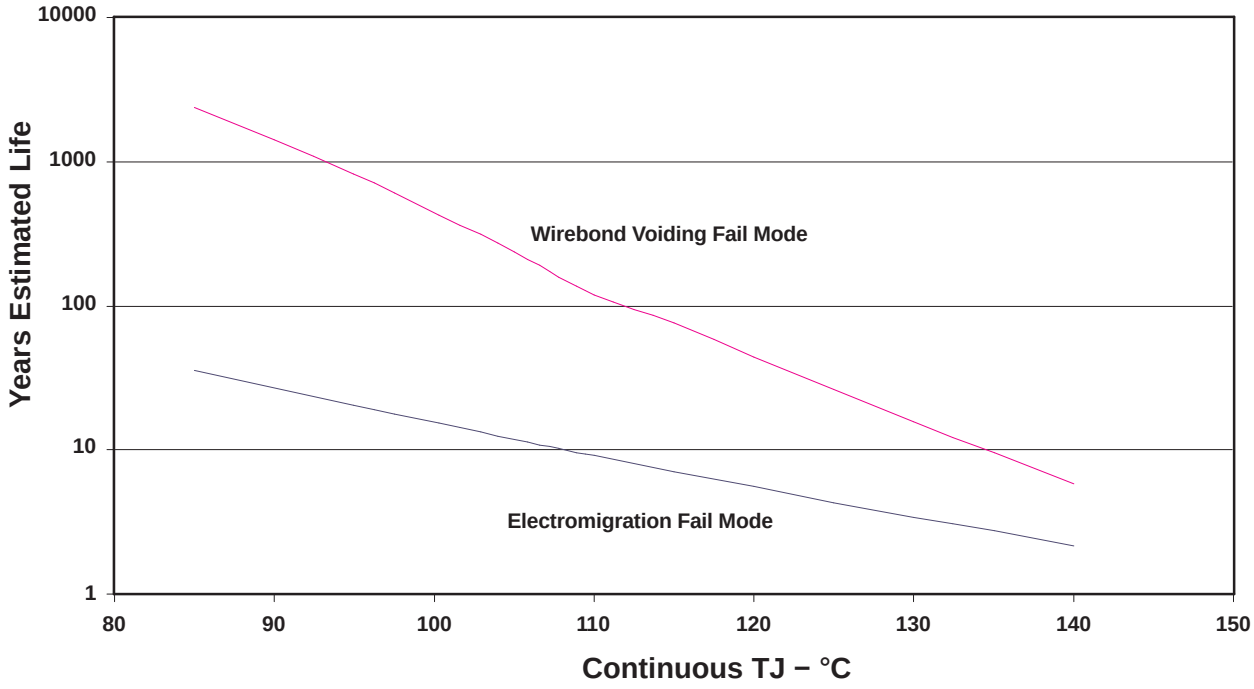


Figure 1. DAC8831MEP Operating Life Derating Chart

ELECTRICAL CHARACTERISTICS

All specifications at $T_A = T_{MIN}$ to T_{MAX}, V_{DD} = 3 V, or V_{DD} = 5 V, V_{REF} = 2.5 V (unless otherwise noted); specifications subject to change without notice.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
Resolution			16			bits
Linearity error		T_A = 25°C		±0.5	±1	LSB
		T_A = –40°C to 105°C (DAC8831 only)		±0.5	±1.5	
		T_A = –55°C to 125°C (DAC8831 only)			±4	
		T_A = –55°C to 125°C (DAC8830 only)		±0.5	±1.5	
Differential linearity error		All grades		±0.5	±1	LSB
Gain error		T_A = 25°C		±1	±5	LSB
		T_A = –55°C to 125°C			±7	
Gain drift				±0.1		ppm/°C
Zero code error		T_A = 25°C		±0.25	±1	LSB
		T_A = –40°C to 105°C (DAC8831 Only)			±2.5	
		T_A = –55°C to 125°C (DAC8831 Only)			±3	
		T_A = –55°C to 125°C (DAC8830 Only)			±2	
Zero code drift				±0.05		ppm/°C
OUTPUT CHARACTERISTICS						
Voltage output (1)		Unipolar operation	0		V_{REF}	V
	(DAC8831 only)	Bipolar operation	$–V_{REF}$		V_{REF}	V
Output Impedance				6.25		kΩ
Settling time		To 1/2 LSB of FS, C_L = 10 pF		1		µs
Slew rate (2)		C_L = 10 pF		25		V/µs
Digital-to-analog glitch		1 LSB change around major carry		8		nV-s
Digital feedthrough (3)				0.2		nV-s
Output noise	DAC8830	T_A = 25°C		10		nV/√Hz
	DAC8831			18		
Power supply rejection		V_{DD} varies ±10%			±1	LSB
Bipolar resistor matching	DAC8831 only	R_{FB} / R_{INV}		1		Ω/Ω
		Ratio error		±0.0015%	±0.01%	
Bipolar zero error	DAC8831 only	T_A = 25°C		±0.25	±5	LSB
		T_A = –55°C to 125°C			±7	
Bipolar zero drift	DAC8831 only			±0.2		ppm/°C

(1) TheDAC8830 output is unipolar (0 V to V_{REF}). TheDAC8831 output is bipolar (±V_{REF}) when it connects to an external buffer (see the *Bipolar Output Operation* section for details).
(2) Slew Rate is measure from 10% to 90% of transition when the output changes from 0 to full scale.
(3) Digital feedthrough is defined as the impulse injected into the analog output from the digital input. It is measured when the DAC output does not change, $\overline{CS}$ is held high, while SCLK and DIN signals are toggled.

ELECTRICAL CHARACTERISTICS (continued)

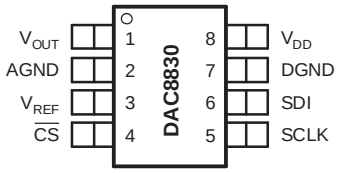
All specifications at $T_A = T_{MIN}$ to T_{MAX}, V_{DD} = 3 V, or V_{DD} = 5 V, V_{REF} = 2.5 V (unless otherwise noted); specifications subject to change without notice.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE INPUT						
	Reference input voltage range(4)		1.25		V_{DD}	V
	Reference input impedance(5)	Unipolar mode	9			kΩ
		Bipolar mode, DAC8831	7.5			
	Reference –3-dB bandwidth, BW	Code = FFFFh		1.3		MHz
	Reference feedthrough	Code = 0000h, V_{REF} = 1 V_{PP} at 100 kHz		1		mV
	Signal-to-noise ratio, SNR			92		dB
	Reference input capacitance	Code = 0000h		75		pF
		Code = FFFFh		120		
DIGITAL INPUTS						
V_{IL}	Input low voltage	V_{DD} = 2.7 V			0.6	V
		V_{DD} = 5 V			0.8	
V_{IH}	Input high voltage	V_{DD} = 2.7 V	2.1			V
		V_{DD} = 5 V	2.4			
	Input current				±1	µA
	Input capacitance				10	pF
	Hysteresis voltage			0.4		V
POWER SUPPLY						
V_{DD}			2.7		5.5	V
I_{DD}		V_{DD} = 3 V		5	20	µA
		V_{DD} = 5 V		5	20	
	Power	V_{DD} = 3 V		15	60	µW
		V_{DD} = 5 V		25	100	
TEMPERATURE RANGE						
	Specified performance		–55		125	°C

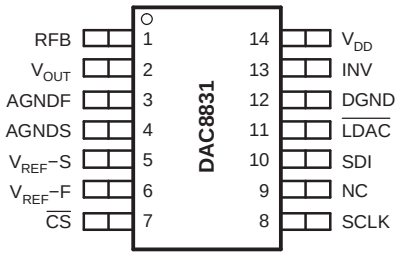
(4) Specified by design. V_{ref} production tested only at 2.5 V.
(5) Reference input resistance is code dependent, minimum at 8555h.

PIN CONFIGURATION (NOT TO SCALE)

DAC8830ID, DAC8830IBD, DAC8830ICD (SO-8) (TOP VIEW)



DAC8831ID, DAC8831IBD, DAC8831ICD (SO-14) (TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NO.	NAME	
DAC8830		
1	V_{OUT}	Analog output of DAC
2	AGND	Analog ground
3	V_{REF}	Voltage reference input
4	$\overline{CS}$	Chip select input (active low). Data is not clocked into SDI unless $\overline{CS}$ is low.
5	SCLK	Serial clock input
6	SDI	Serial data input. Data is latched into input register on the rising edge of SCLK.
7	DGND	Digital ground
8	VDD	Analog power supply, 3 V to 5 V
DAC8831		
1	RFB	Feedback resistor. Connect to the output of external operational amplifier in bipolar mode.
2	V_{OUT}	Analog output of DAC
3	AGNDF	Analog ground (Force)
4	AGNDS	Analog ground (Sense)
5	V_{REF}-S	Voltage reference input (Sense). Connect to external voltage reference.
6	V_{REF}-F	Voltage reference input (Force). Connect to external voltage reference.
7	$\overline{CS}$	Chip select input (active low). Data is not clocked into SDI unless $\overline{CS}$ is low.
8	SCLK	Serial clock input
9	NC	No internal connection
10	SDI	Serial data input. Data is latched into input register on the rising edge of SCLK.
11	$\overline{LDAC}$	Load DAC control input. Active low. When $\overline{LDAC}$ is Low, the DAC latch is simultaneously updated with the content of the input register.
12	DGND	Digital ground
13	INV	Junction point of internal scaling resistors. Connect to external operational amplifier's inverting input in bipolar mode.
14	VDD	Analog power supply, 3 V to 5 V

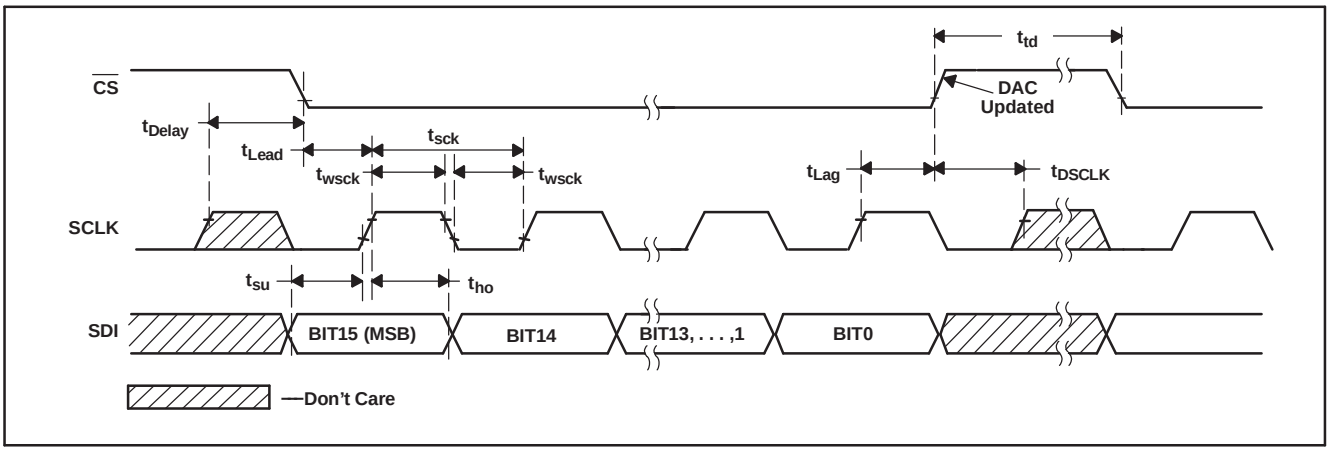


Figure 2. DAC8830 Timing Diagram

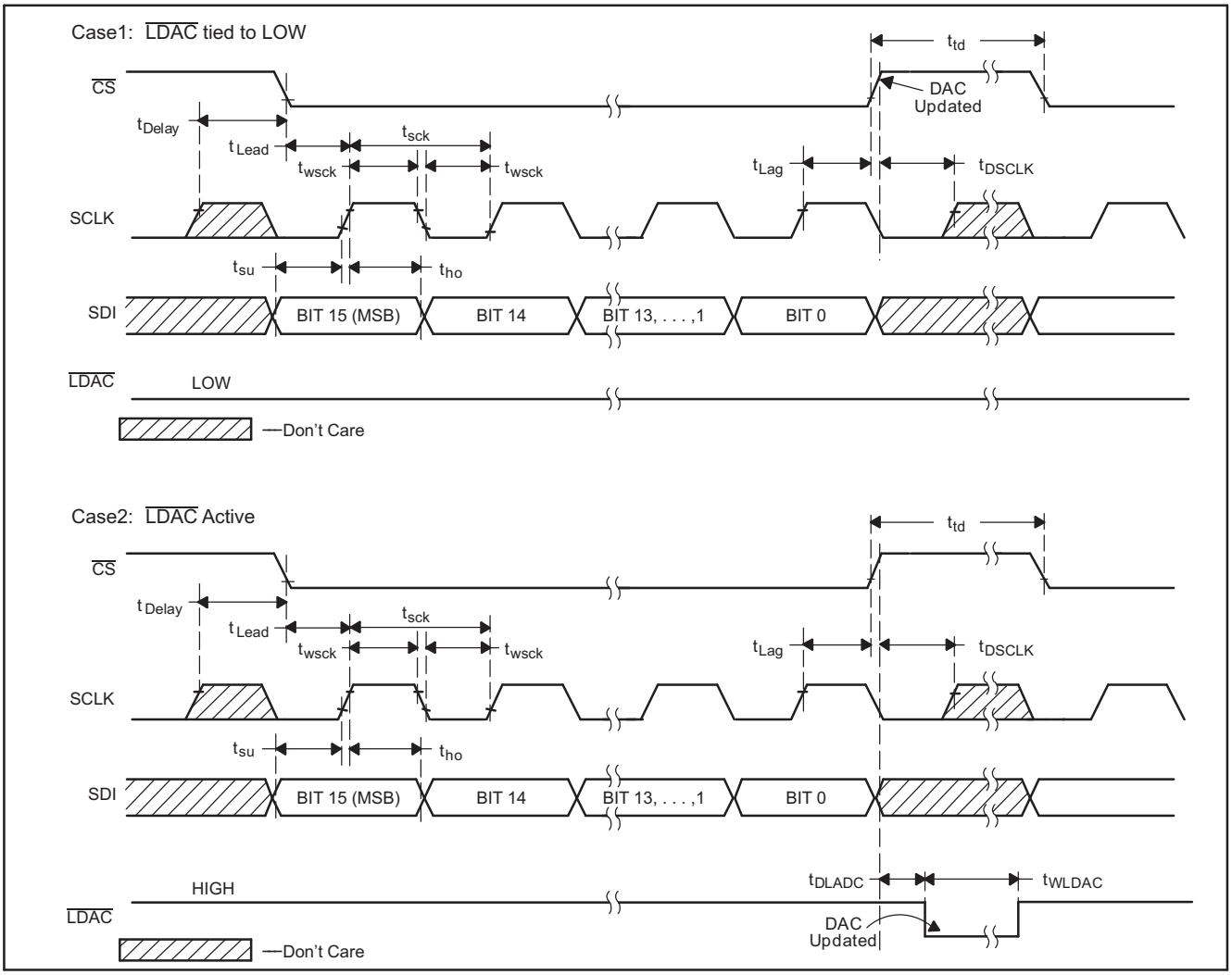


Figure 3. DAC8831 Timing Diagram

TIMING CHARACTERISTICS: V_{DD} = 5 V(1) (2)

At –55°C to 125°C (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
t_{sck}	SCLK period	20		ns
t_{wsck}	SCLK high or low time	10		ns
t_{Delay}	Delay from SCLK high to $\overline{CS}$ low	18		ns
t_{Lead}	$\overline{CS}$ enable lead time	12		ns
t_{Lag}	$\overline{CS}$ enable lag time	15		ns
t_{DSCLK}	Delay from $\overline{CS}$ high to SCLK high	15		ns
t_{td}	$\overline{CS}$ high between active period	30		ns
t_{su}	Data setup time (input)	10		ns
t_{ho}	Data hold time (input)	0		ns
t_{WLDAC}	$\overline{LDAC}$ width	30		ns
t_{DLDAC}	Delay from $\overline{CS}$ high to $\overline{LDAC}$ low	30		ns
	V_{DD} high to $\overline{CS}$ low (power-up delay)	10		µs

(1) Specified by design. Not production tested.
(2) Sample tested during the initial release and after any redesign or process changes that may affect this parameter.

TIMING CHARACTERISTICS: V_{DD} = 3 V(1) (2)

At –55°C to 125°C (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
t_{sck}	SCLK period	20		ns
t_{wsck}	SCLK high or low time	10		ns
t_{Delay}	Delay from SCLK high to $\overline{CS}$ low	18		ns
t_{Lead}	$\overline{CS}$ enable lead time	15		ns
t_{Lag}	$\overline{CS}$ enable lag time	15		ns
t_{DSCLK}	Delay from $\overline{CS}$ high to SCLK high	15		ns
t_{td}	$\overline{CS}$ high between active period	30		ns
t_{su}	Data setup time (input)	10		ns
t_{ho}	Data hold time (input)	0		ns
t_{WLDAC}	$\overline{LDAC}$ width	30		ns
t_{DLDAC}	Delay from $\overline{CS}$ high to $\overline{LDAC}$ low	30		ns
	V_{DD} high to $\overline{CS}$ low (power-up delay)	10		µs

(1) Specified by design. Not production tested.
(2) Sample tested during the initial release and after any redesign or process changes that may affect this parameter.

TYPICAL CHARACTERISTICS: V_{DD} = 5 V

At T_A = 25°C, V_{REF} = 2.5 V (unless otherwise noted)

LINEARITY ERROR vs DIGITAL INPUT CODE

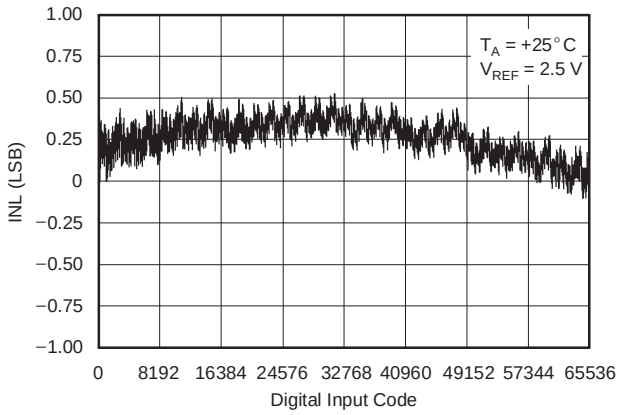


Figure 4.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

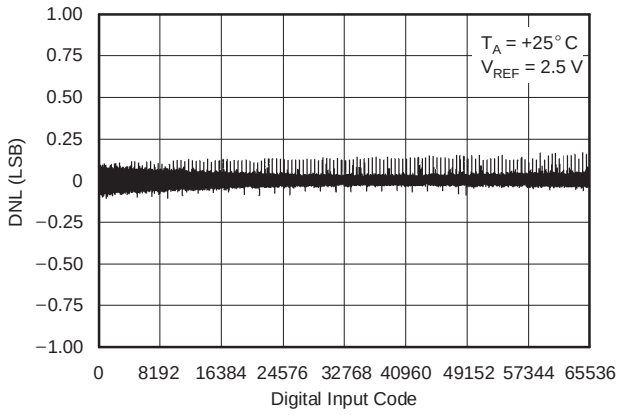


Figure 5.

LINEARITY ERROR vs DIGITAL INPUT CODE

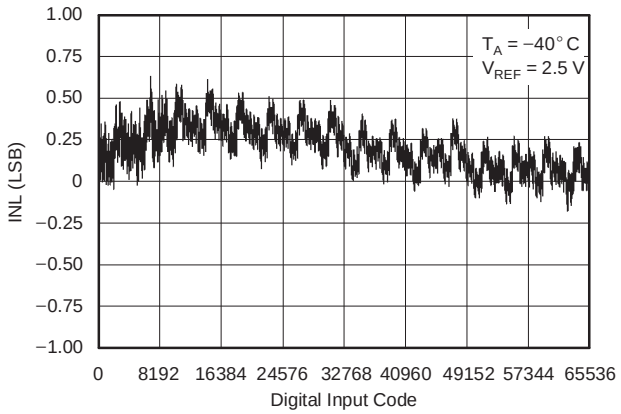


Figure 6.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

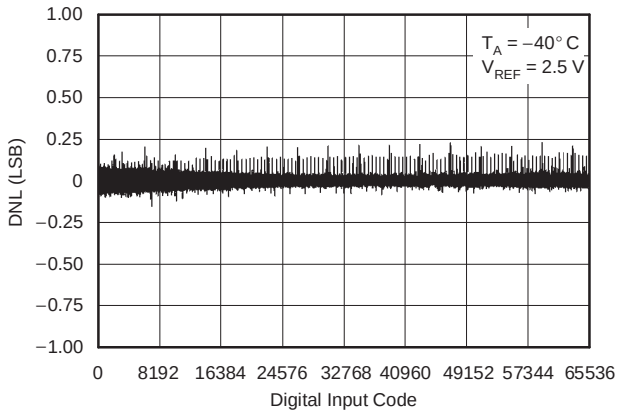


Figure 7.

LINEARITY ERROR vs DIGITAL INPUT CODE

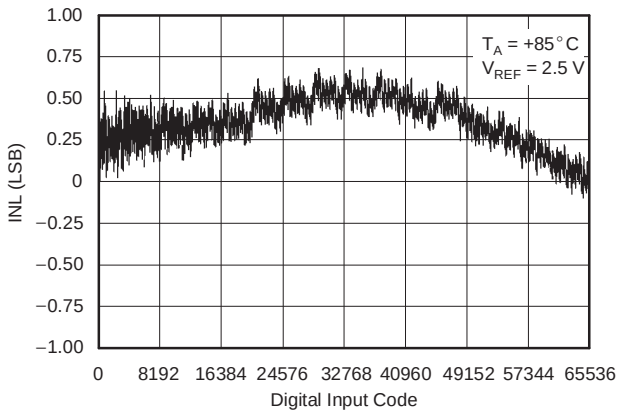


Figure 8.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

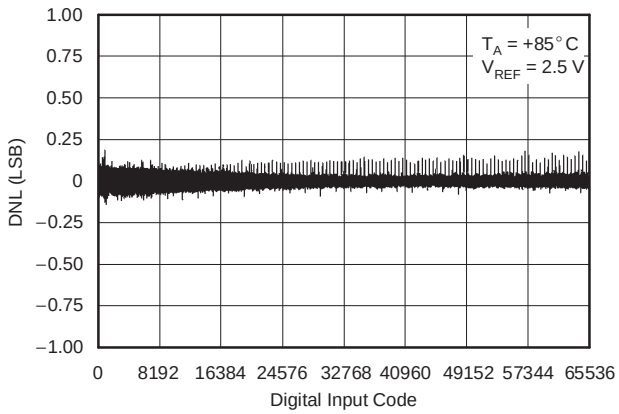


Figure 9.

TYPICAL CHARACTERISTICS: V_{DD} = 5 V (continued)

At T_A = 25°C, V_{REF} = 2.5 V (unless otherwise noted)

LINEARITY ERROR vs DIGITAL INPUT CODE

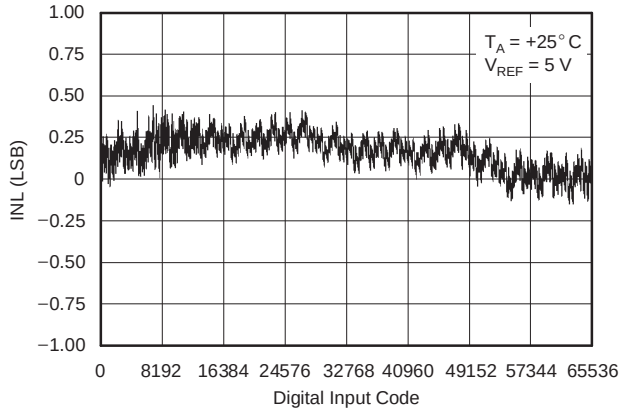


Figure 10.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

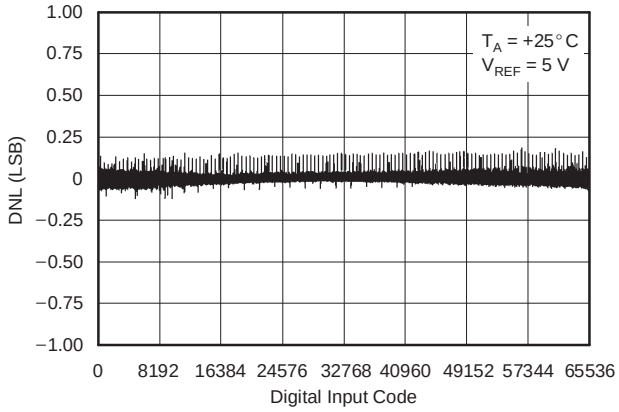


Figure 11.

LINEARITY ERROR vs REFERENCE VOLTAGE

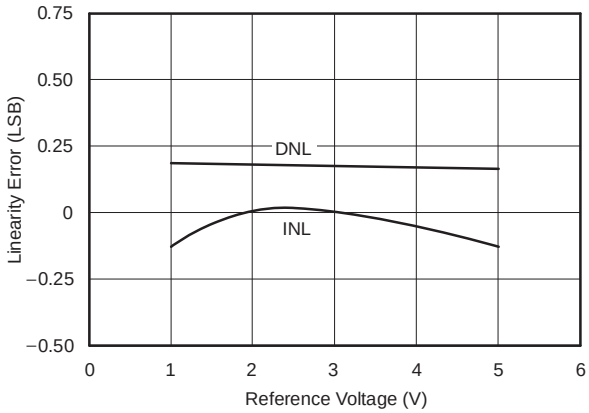


Figure 12.

LINEARITY ERROR vs SUPPLY VOLTAGE

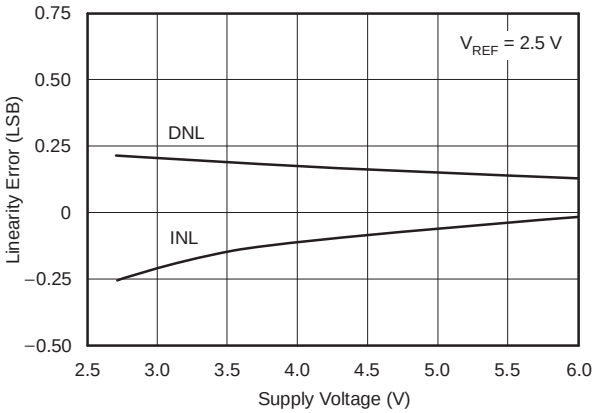


Figure 13.

GAIN ERROR vs TEMPERATURE

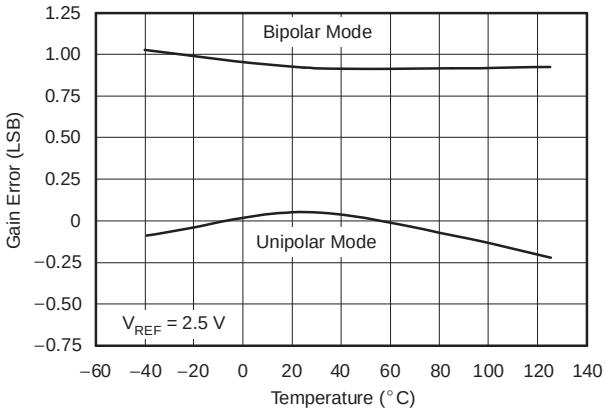


Figure 14.

ZERO-CODE ERROR vs TEMPERATURE

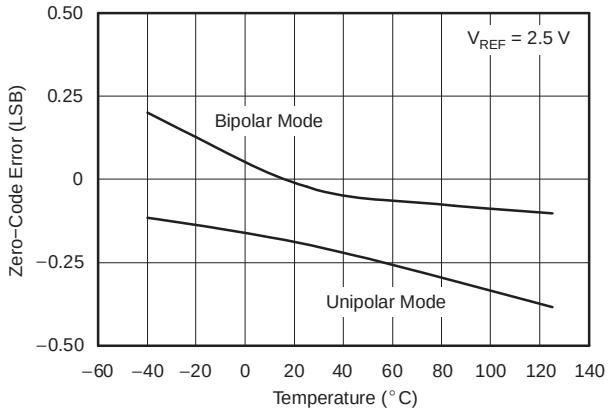


Figure 15.

TYPICAL CHARACTERISTICS: V_{DD} = 5 V (continued)

At T_A = 25°C, V_{REF} = 2.5 V (unless otherwise noted)

REFERENCE CURRENT vs CODE (UNIPOLAR MODE)

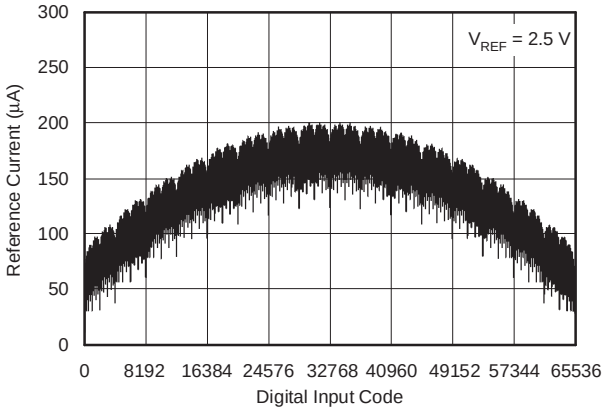


Figure 16.

REFERENCE CURRENT vs CODE (BIPOLAR MODE)

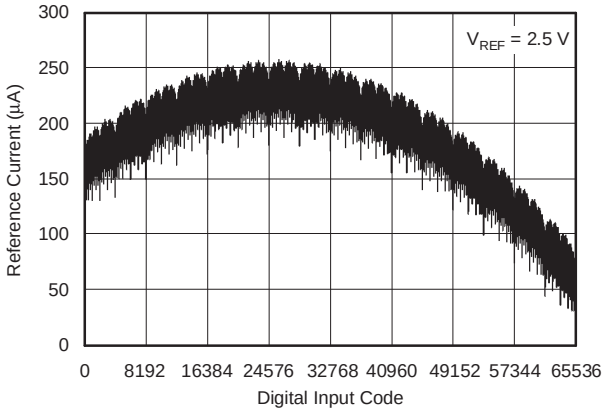


Figure 17.

SUPPLY CURRENT vs DIGITAL INPUT VOLTAGE

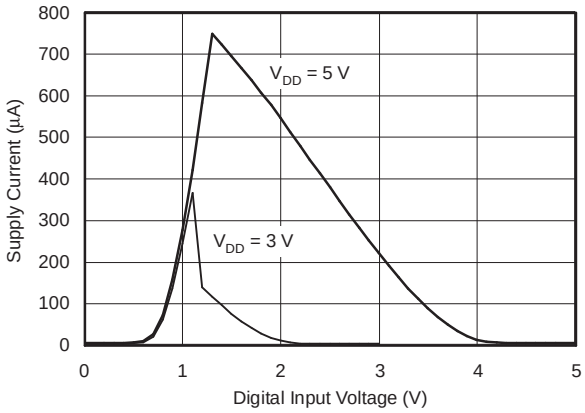


Figure 18.

SUPPLY CURRENT vs TEMPERATURE

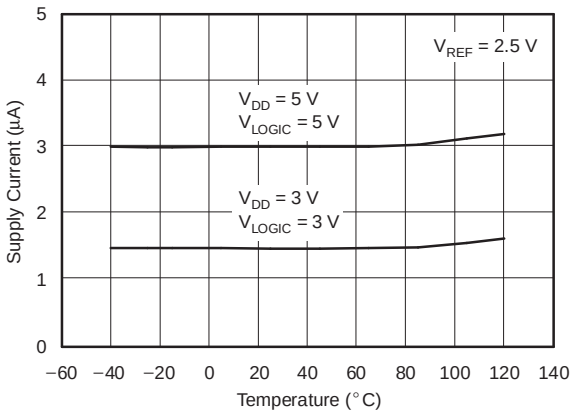


Figure 19.

SUPPLY CURRENT vs SUPPLY VOLTAGE

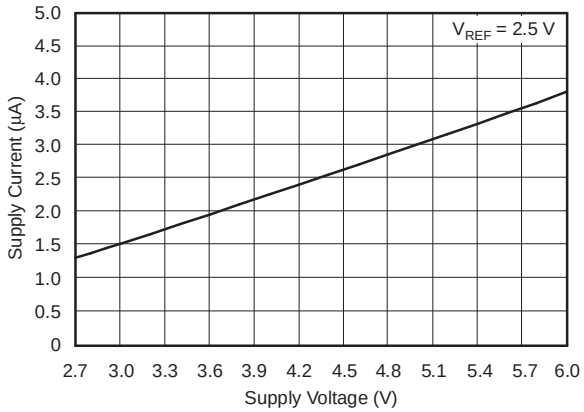


Figure 20.

SUPPLY CURRENT vs REFERENCE VOLTAGE

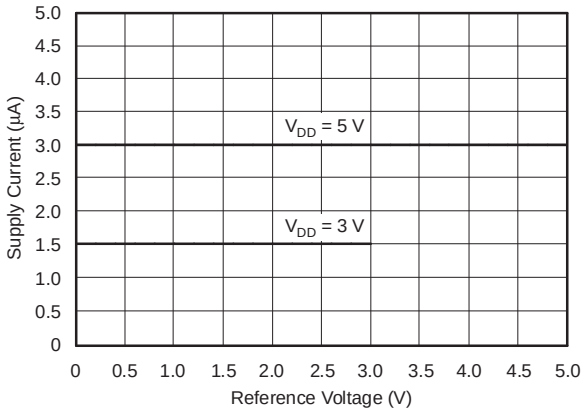


Figure 21.

TYPICAL CHARACTERISTICS: V_{DD} = 5 V (continued)

At T_A = 25°C, V_{REF} = 2.5 V (unless otherwise noted)

MAJOR-CARRY GLITCH (FALLING)

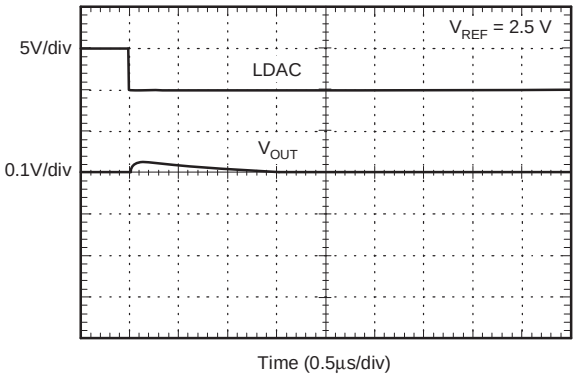


Figure 22.

MAJOR-CARRY GLITCH (RISING)

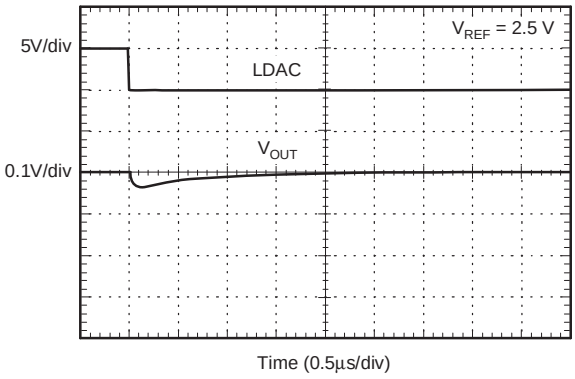


Figure 23.

DAC SETTLING TIME (FALLING)

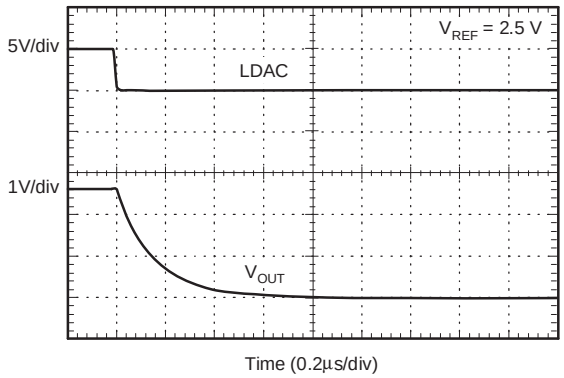


Figure 24.

DAC SETTLING TIME (RISING)

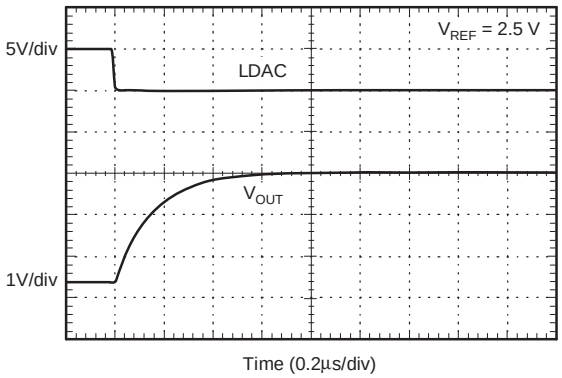


Figure 25.

DIGITAL FEEDTHROUGH

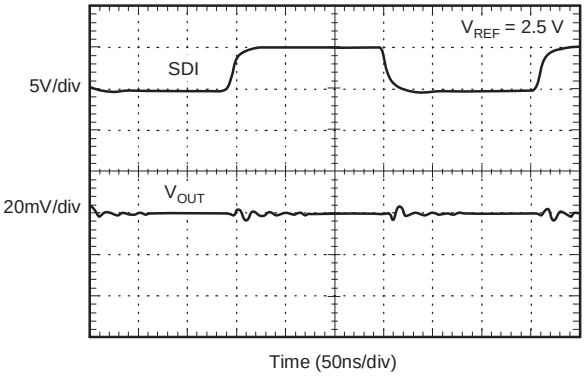


Figure 26.

TYPICAL CHARACTERISTICS: V_{DD} = 3 V

At T_A = 25°C, V_{REF} = 2.5 V (unless otherwise noted)

LINEARITY ERROR vs DIGITAL INPUT CODE

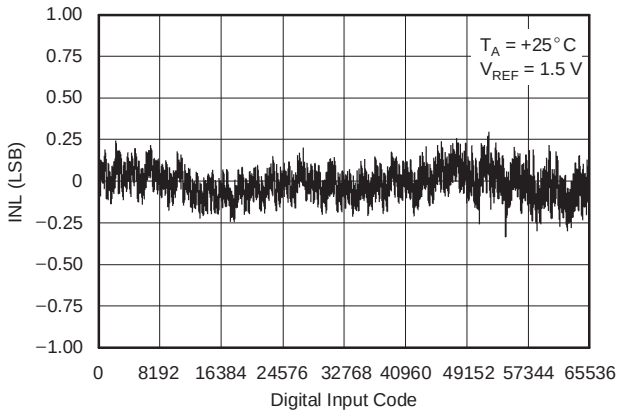


Figure 27.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

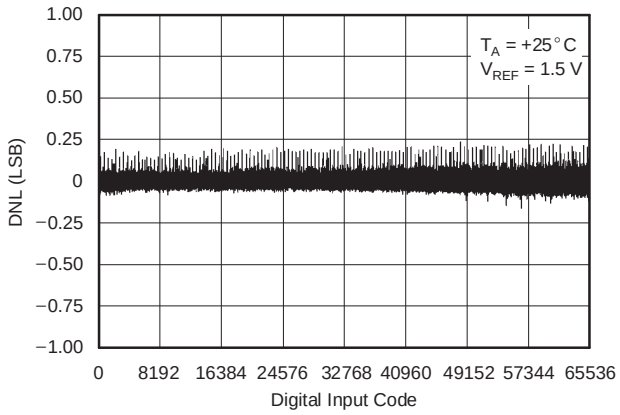


Figure 28.

LINEARITY ERROR vs DIGITAL INPUT CODE

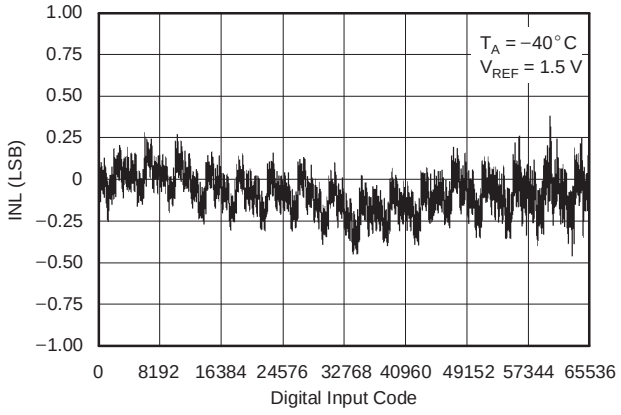


Figure 29.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

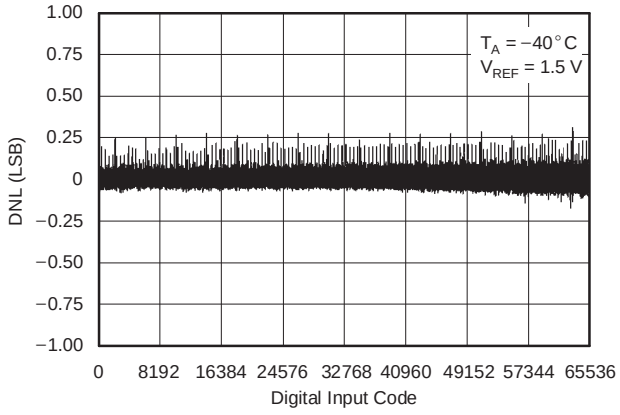


Figure 30.

LINEARITY ERROR vs DIGITAL INPUT CODE

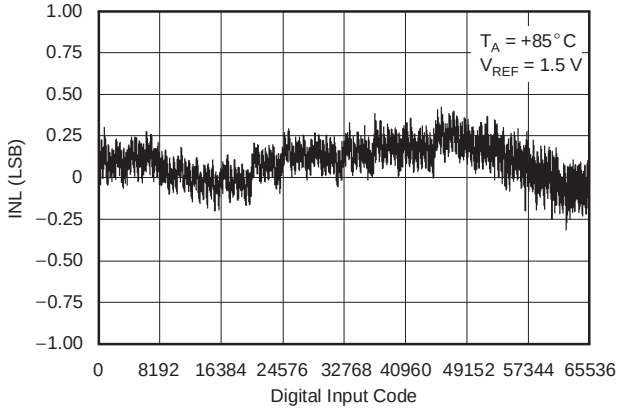


Figure 31.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

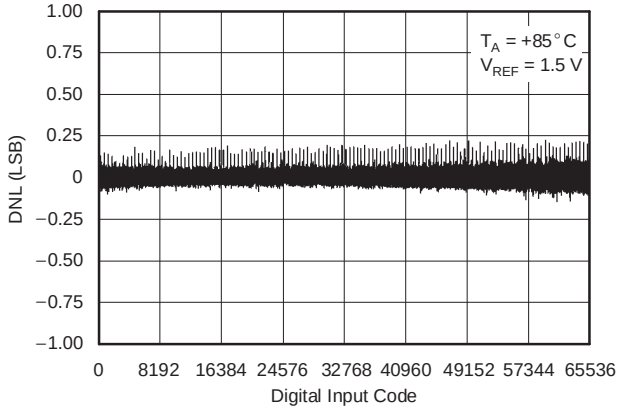


Figure 32.

TYPICAL CHARACTERISTICS: V_{DD} = 3 V (continued)

At T_A = 25°C, V_{REF} = 2.5 V (unless otherwise noted)

LINEARITY ERROR vs DIGITAL INPUT CODE

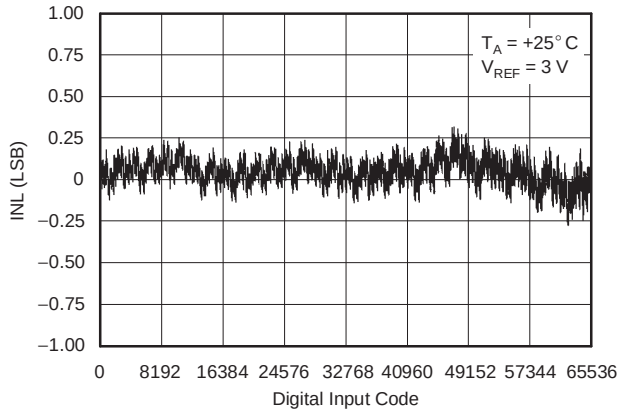


Figure 33.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

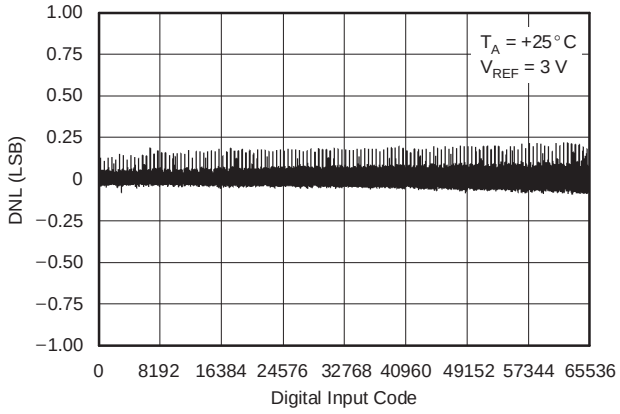


Figure 34.

LINEARITY ERROR vs REFERENCE VOLTAGE

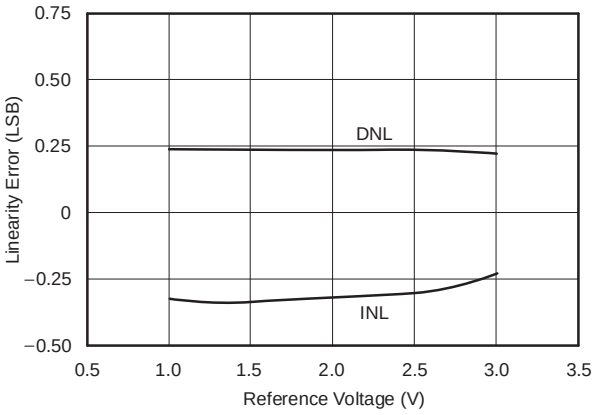


Figure 35.

GAIN ERROR vs TEMPERATURE

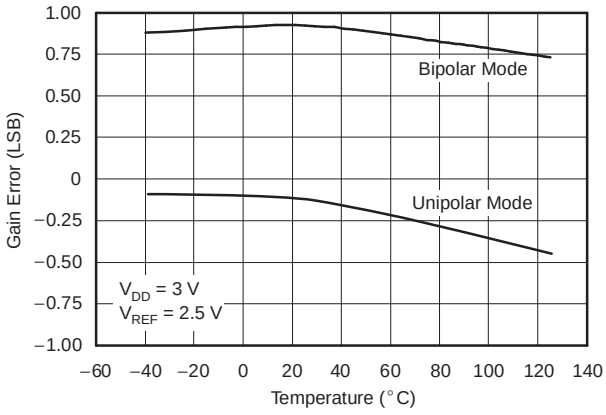


Figure 36.

ZERO-CODE ERROR vs TEMPERATURE

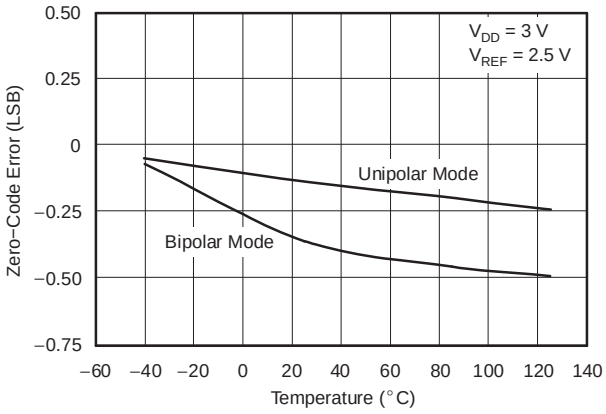


Figure 37.

REFERENCE CURRENT vs CODE (UNIPOLAR MODE)

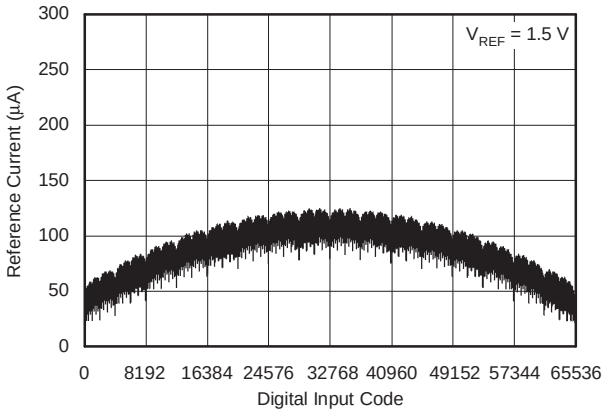


Figure 38.

TYPICAL CHARACTERISTICS: V_{DD} = 3 V (continued)

At T_A = 25°C, V_{REF} = 2.5 V (unless otherwise noted)

REFERENCE CURRENT vs CODE (BIPOLAR MODE)

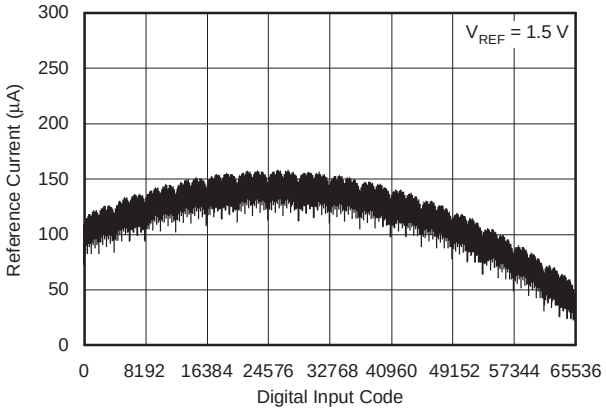


Figure 39.

DIGITAL FEEDTHROUGH

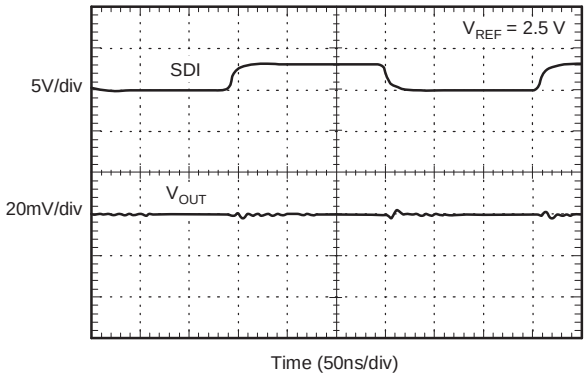


Figure 40.

MAJOR-CARRY GLITCH (FALLING)

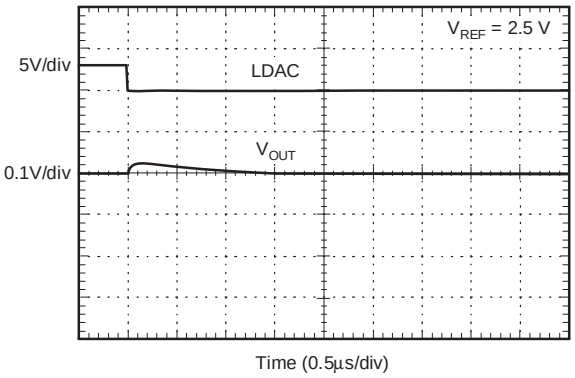


Figure 41.

MAJOR-CARRY GLITCH (RISING)

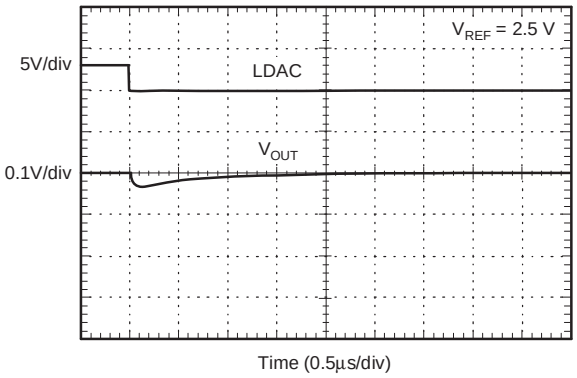


Figure 42.

DAC SETTLING TIME (FALLING)

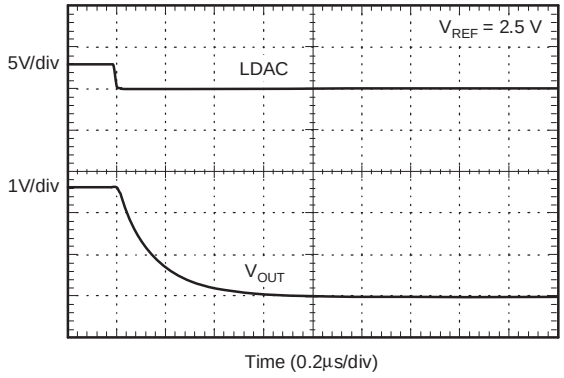


Figure 43.

DAC SETTLING TIME (RISING)

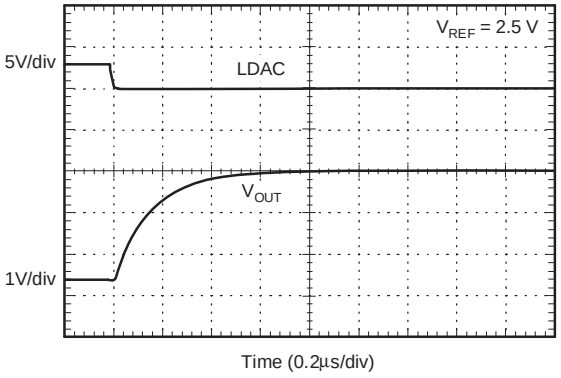


Figure 44.

THEORY OF OPERATION

General Description

The DAC8830 and DAC8831 are single, 16-bit, serial-input, voltage-output DACs. They operate from a single supply ranging from 2.7 V to 5 V, and typically consume 5 µA. Data is written to these devices in a 16-bit word format, via an SPI serial interface. To ensure a known power-up state, these parts were designed with a power-on reset function. The DAC8830 and DAC8831 are reset to zero code. In unipolar mode, the DAC8830 and DAC8831 are reset to 0V, and in bipolar mode, the DAC8831 is reset to $-V_{REF}$. Kelvin sense connections for the reference and analog ground are included on the DAC8831.

Digital-to-Analog Sections

The DAC architecture for both devices consists of two matched DAC sections and is segmented. A simplified circuit diagram is shown in Figure 45. The four MSBs of the 16-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of 15 matched resistors to either AGND or V_{REF}. The remaining 12 bits of the data word drive switches S0 to S11 of a 12-bit voltage mode R-2R ladder network.

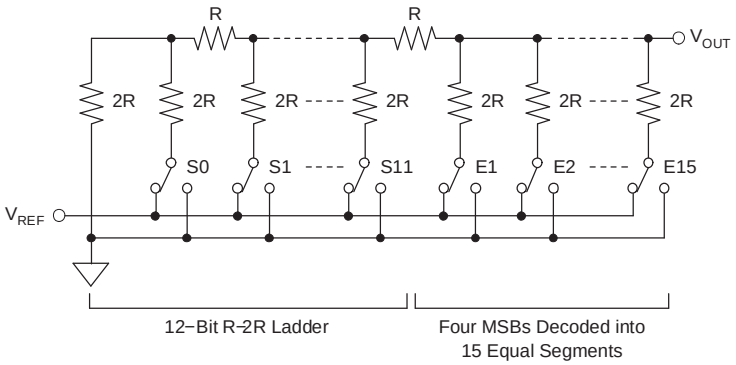


Figure 45. DAC Architecture

Output Range

The output of the DAC is

$$V_{OUT} = (V_{REF} \times Code/65536)$$

Where:

Code = Decimal data word loaded to the DAC latch

THEORY OF OPERATION (continued)

Power-on Reset

Both devices have a power-on reset function to ensure the output is at a known state upon power up. In the DAC8830 and DAC8831, on power up, the DAC latch and input registers contain all 0s until new data is loaded from the input serial shift register. Therefore, after power up, the output from pin V_{OUT} of the DAC8830 is 0 V. The output from pin V_{OUT} of the DAC8831 is 0 V in unipolar mode and $-V_{REF}$ in bipolar mode.

However, the serial register of the DAC8830 and DAC8831 is not cleared on power up, so its contents are undefined. When loading data initially to the device, 16 bits or more should be loaded to prevent erroneous data appearing on the output. If more than 16 bits are loaded, the last 16 are kept; if less than 16 are loaded, bits will remain from the previous word. If the device must be interfaced with data shorter than 16 bits, the data should be padded with 0s at the LSBs.

Serial Interface

The digital interface is standard 3-wire connection compatible with SPI, QSPI, Microwire, and Texas Instruments DSP interfaces, which can operate at speeds up to 50 Mbps. The data transfer is framed by $\overline{CS}$, the chip select signal. The DAC works as a bus slave. The bus master generates the synchronize clock, SCLK, and initiates the transmission. When $\overline{CS}$ is high, the DAC is not accessed, and the clock SCLK and serial input data SDI are ignored. The bus master accesses the DAC by driving pin $\overline{CS}$ low. Immediately following the high-to-low transition of $\overline{CS}$, the serial input data on pin SDI is shifted out from the bus master synchronously on the falling edge of SCLK, and latched on the rising edge of SCLK into the input shift register, MSB first. The low-to-high transition of $\overline{CS}$ transfers the contents of the input shift register to the input register. All data registers are 16 bit. It takes 16 clocks of SCLK to transfer one data word to the parts. To complete a whole data word, $\overline{CS}$ must go high immediately after 16 SCLKs are clocked in. If more than 16 SCLKs are applied during the low state of $\overline{CS}$, the last 16 bits are transferred to the input register on the rising edge of $\overline{CS}$. However, if $\overline{CS}$ is not kept low during the entire 16 SCLK cycles, data is corrupted. In this case, reload the DAC latch with a new 16-bit word.

In the DAC8830, the contents of the input register are transferred into the DAC latch immediately when the input register is loaded, and the DAC output is updated at the same time.

The DAC8831 has an $\overline{LDAC}$ pin allowing the DAC latch to be updated asynchronously by bringing $\overline{LDAC}$ low after $\overline{CS}$ goes high. In this case, $\overline{LDAC}$ must be maintained high while $\overline{CS}$ is low. If $\overline{LDAC}$ is tied permanently low, the DAC latch is updated immediately after the input register is loaded (caused by the low-to-high transition of $\overline{CS}$).

APPLICATION INFORMATION

Unipolar Output Operation

These DACs are capable of driving unbuffered loads of 60 kΩ. Unbuffered operation results in low supply current (typically 5 µA) and a low offset error. The DAC8830 provides a unipolar output swing ranging from 0 V to V_{REF}. The DAC8831 can be configured to output both unipolar and bipolar voltages. Figure 46 and Figure 47 show a typical unipolar output voltage circuit for each device, respectively. The code table for this mode of operation is shown in Table 1.

Table 1. Unipolar Code

DAC Latch Contents		Analog Output
MSB	LSB	
1111 1111 1111 1111		$V_{REF} \times (65{,}535/65{,}536)$
1000 0000 0000 0000		$V_{REF} \times (32{,}768/65{,}536) = V_{REF}$
0000 0000 0000 0001		$V_{REF} \times (1/65{,}536)$
0000 0000 0000 0000		0 V

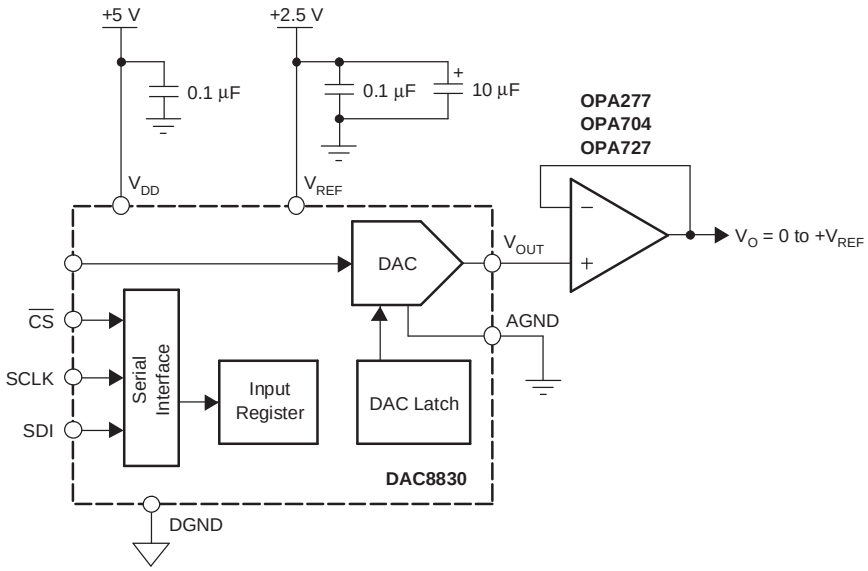


Figure 46. Unipolar Output Mode of DAC8830

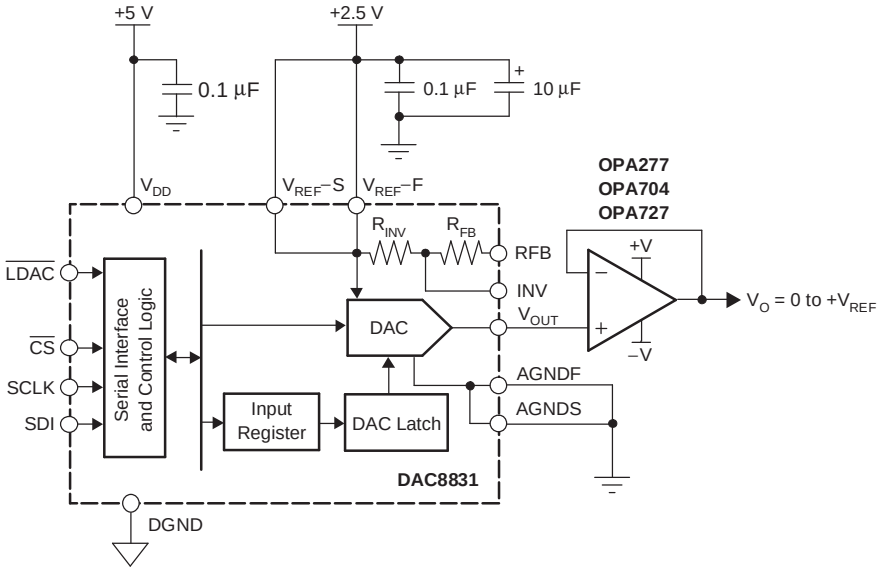


Figure 47. Unipolar Output Mode of DAC8831

Assuming a perfect reference, the worst-case output voltage may be calculated from the following equation:

Unipolar Mode Worst-Case Output

$$V_{OUT_UNI} = \frac{D}{2^{16}} \times \left(V_{REF} + V_{GE}\right) + V_{ZSE} + INL$$

Where:

V_{OUT_UNI} = Unipolar mode worst-case output
D = Code loaded to DAC
V_{REF} = Reference voltage applied to part
V_{GE} = Gain error in volts
V_{ZSE} = Zero scale error in volts
INL = Integral nonlinearity in volts

Bipolar Output Operation

With the aid of an external operational amplifier, the DAC8831 may be configured to provide a bipolar voltage output. A typical circuit of such an operation is shown in Figure 48. The matched bipolar offset resistors R_{FB} and R_{INV} are connected to an external operational amplifier to achieve this bipolar output swing; typically, $R_{FB} = R_{INV} = 28\ k\Omega$.

Table 2 shows the transfer function for this output operating mode. The DAC8831 also provides a set of Kelvin connections to the analog ground and external reference inputs.

Table 2. Bipolar Code

DAC Latch Contents MSB LSB	Analog Output
1111 1111 1111 1111	$V_{REF} \times (32{,}767/32{,}768)$
1000 0000 0000 0000	$V_{REF} \times (1/32{,}768)$
0111 1111 1111 1111	0 V
0000 0000 0000 0001	$-V_{REF} \times (1/32{,}768)$
0000 0000 0000 0000	$-V_{REF} \times (32{,}767/32{,}768) = -V_{REF}$

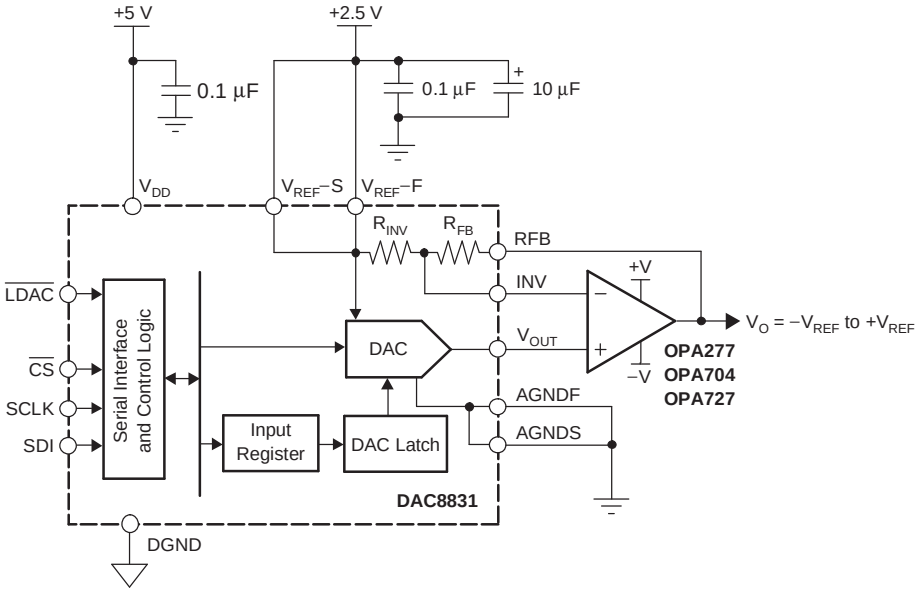


Figure 48. Bipolar Output Mode of DAC8831

Assuming a perfect reference, the worst-case output voltage may be calculated from the following equation:

Bipolar Mode Worst-Case Output

$$V_{OUT_BIP} = \frac{\left[\left(V_{OUT_UNI} + V_{OS}\right)(2 + RD) - V_{REF}(1 + RD)\right]}{1 + \left(\frac{2 + RD}{A}\right)}$$

Where:

V_{OS} = External operational amplifier input offset voltage
RD = R_{FB} and R_{IN} resistor matching error
A = Operational amplifier open-loop gain

Output Amplifier Selection

For bipolar mode, a precision amplifier should be used, supplied from a dual power supply. This provides the $\pm V_{REF}$ output.

In a single-supply application, selection of a suitable operational amplifier may be more difficult because the output swing of the amplifier does not usually include the negative rail; in this case, AGND. This output swing can result in some degradation of the specified performance unless the application does not use codes near 0.

The selected operational amplifier needs to have low-offset voltage (the DAC LSB is 38 μV with a 2.5-V reference), eliminating the need for output offset trims. Input bias current should also be low because the bias current multiplied by the DAC output impedance (approximately 6.25 kΩ) adds to the zero-code error.

Rail-to-rail input and output performance is required. For fast settling, the slew rate of the operational amplifier should not impede the settling time of the DAC. Output impedance of the DAC is constant and code-independent, but in order to minimize gain errors the input impedance of the output amplifier should be as high as possible. The amplifier should also have a 3 dB bandwidth of 1 MHz or greater. The amplifier adds another time constant to the system, thus increasing the settling time of the output. A higher 3-dB amplifier bandwidth results in a shorter effective settling time of the combined DAC and amplifier.

Reference and Ground

Since the input impedance is code-dependent, the reference pin should be driven from a low impedance source. The DAC8830 and DAC8831 operate with a voltage reference ranging from 1.25 V to V_{DD}. References below 1.25 V result in reduced accuracy.

The DAC full-scale output voltage is determined by the reference. Table 1 and Table 2 outline the analog output voltage for particular digital codes.

For optimum performance, Kelvin sense connections are provided on the DAC8831. If the application does not require separate force and sense lines, they should be tied together close to the package to minimize voltage drops between the package leads and the internal die.

Power Supply and Reference Bypassing

For accurate high-resolution performance, it is recommended that the reference and supply pins be bypassed with a 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor.

CROSS REFERENCE

The DAC8830 and DAC8831 have an industry-standard pinout configuration (see Table 3).

Table 3. Cross Reference

MODEL	INL (LSB)	DNL (LSB)	POWER-ON RESET TO	TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION	CROSS REFERENCE
DAC8830ICD	±1	±1	Zero-Code	–40°C to 85°C	8-Lead Small Outline IC	SO-8	AD5541CR, MAX541AESA
DAC8830IBD	±2	±1	Zero-Code	–40°C to 85°C	8-Lead Small Outline IC	SO-8	AD5541BR, MAX541BESA
DAC8830ID	±4	±1	Zero-Code	–40°C to 85°C	8-Lead Small Outline IC	SO-8	AD5541AR, MAX541CESA
DAC8830MCD	±1	±1	Zero-Code	–55°C to 125°C	8-Lead Small Outline IC	SO-8	N/A
N/A	±1	±1	Zero-Code	–40°C to 85°C	8-Lead Plastic DIP	PDIP-8	MAX541AEPA
N/A	±2	±1	Zero-Code	–40°C to 85°C	8-Lead Plastic DIP	PDIP-8	MAX541BEPA
N/A	±4	±1	Zero-Code	–40°C to 85°C	8-Lead Plastic DIP	PDIP-8	MAX541CEPA
N/A	±1	±1	Zero-Code	0°C to 70°C	8-Lead Small Outline IC	SO-8	AD5541LR
N/A	±2	±1.5	Zero-Code	0°C to 70°C	8-Lead Small Outline IC	SO-8	AD5541JR
N/A	±1	±1	Zero-Code	0°C to 70°C	8-Lead Plastic DIP	PDIP-8	MAX541AEPA
N/A	±2	±1	Zero-Code	0°C to 70°C	8-Lead Plastic DIP	PDIP-8	MAX541BEPA
N/A	±4	±1	Zero-Code	0°C to 70°C	8-Lead Plastic DIP	PDIP-8	MAX541CEPA
DAC8831ICD	±1	±1	Zero-Code	–40°C to 85°C	14-Lead Small Outline IC	SO-14	AD5542CR, MAX542AESD
DAC8831IBD	±2	±1	Zero-Code	–40°C to 85°C	14-Lead Small Outline IC	SO-14	AD5542BR, MAX542BESD
DAC8831ID	±4	±1	Zero-Code	–40°C to 85°C	14-Lead Small Outline IC	SO-14	AD5542AR, MAX542CESD
DAC8831MCD	±1	±1	Zero-Code	–55°C to 125°C	14-Lead Small Outline IC	SO-14	N/A
N/A	±1	±1	Zero-Code	–40°C to 85°C	14-Lead Plastic DIP	PDIP-14	MAX542ACPD
N/A	±2	±1	Zero-Code	–40°C to 85°C	14-Lead Plastic DIP	PDIP-14	MAX542BCPD
N/A	±4	±1	Zero-Code	–40°C to 85°C	14-Lead Plastic DIP	PDIP-14	MAX542CCPD
N/A	±4	±1	Zero-Code	–55°C to 125°C	14-Lead Ceramic SB	SB-14	MAX542CMJD
N/A	±1	±1	Zero-Code	0°C to 70°C	14-Lead Small Outline IC	SO-14	AD5542LR
N/A	±2	±1.5	Zero-Code	0°C to 70°C	14-Lead Small Outline IC	SO-14	AD5542JR
N/A	±1	±1	Zero-Code	0°C to 70°C	14-Lead Small Outline IC	SO-14	MAX542AEPD
N/A	±2	±1	Zero-Code	0°C to 70°C	14-Lead Small Outline IC	SO-14	MAX542BEPD
N/A	±4	±1	Zero-Code	0°C to 70°C	14-Lead Small Outline IC	SO-14	MAX542CEPD

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DAC8830MCDEP	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC8830MCDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC8831MCDEP	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC8831MCDREP	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
V62/06671-01XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
V62/06671-02XE	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
V62/06671-03YE	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
V62/06671-04YE	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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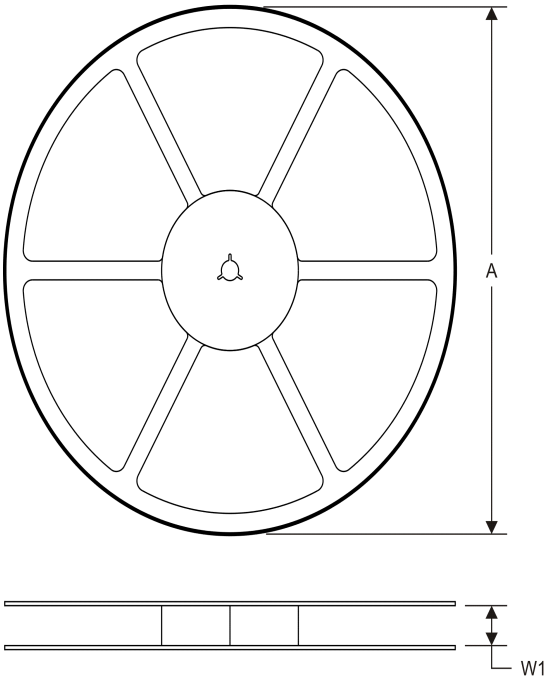
OTHER QUALIFIED VERSIONS OF DAC8830-EP, DAC8831-EP :
- Catalog: DAC8830, DAC8831

NOTE: Qualified Version Definitions:

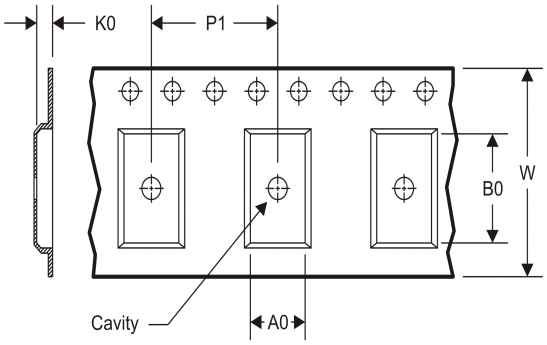
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



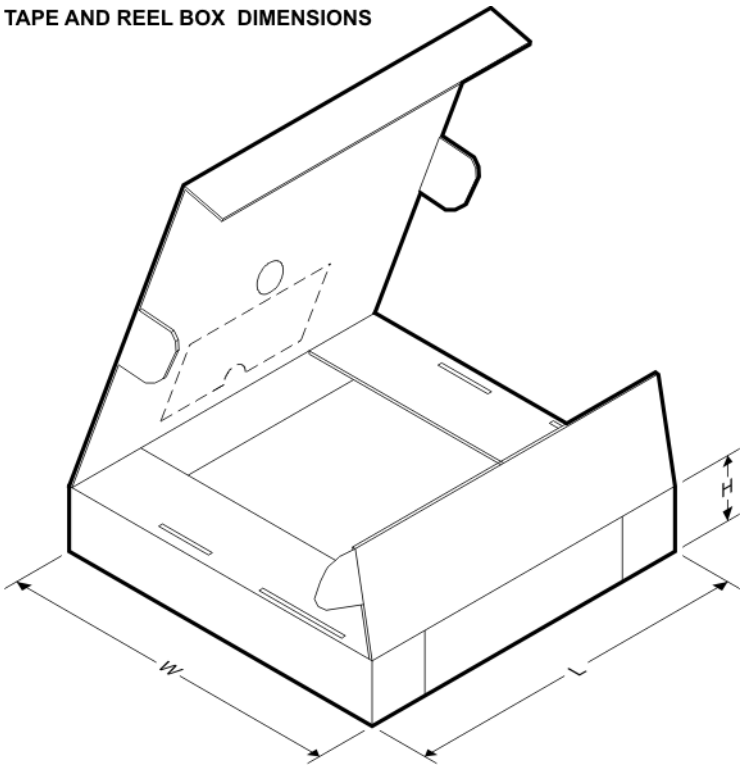
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8830MCDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
DAC8831MCDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

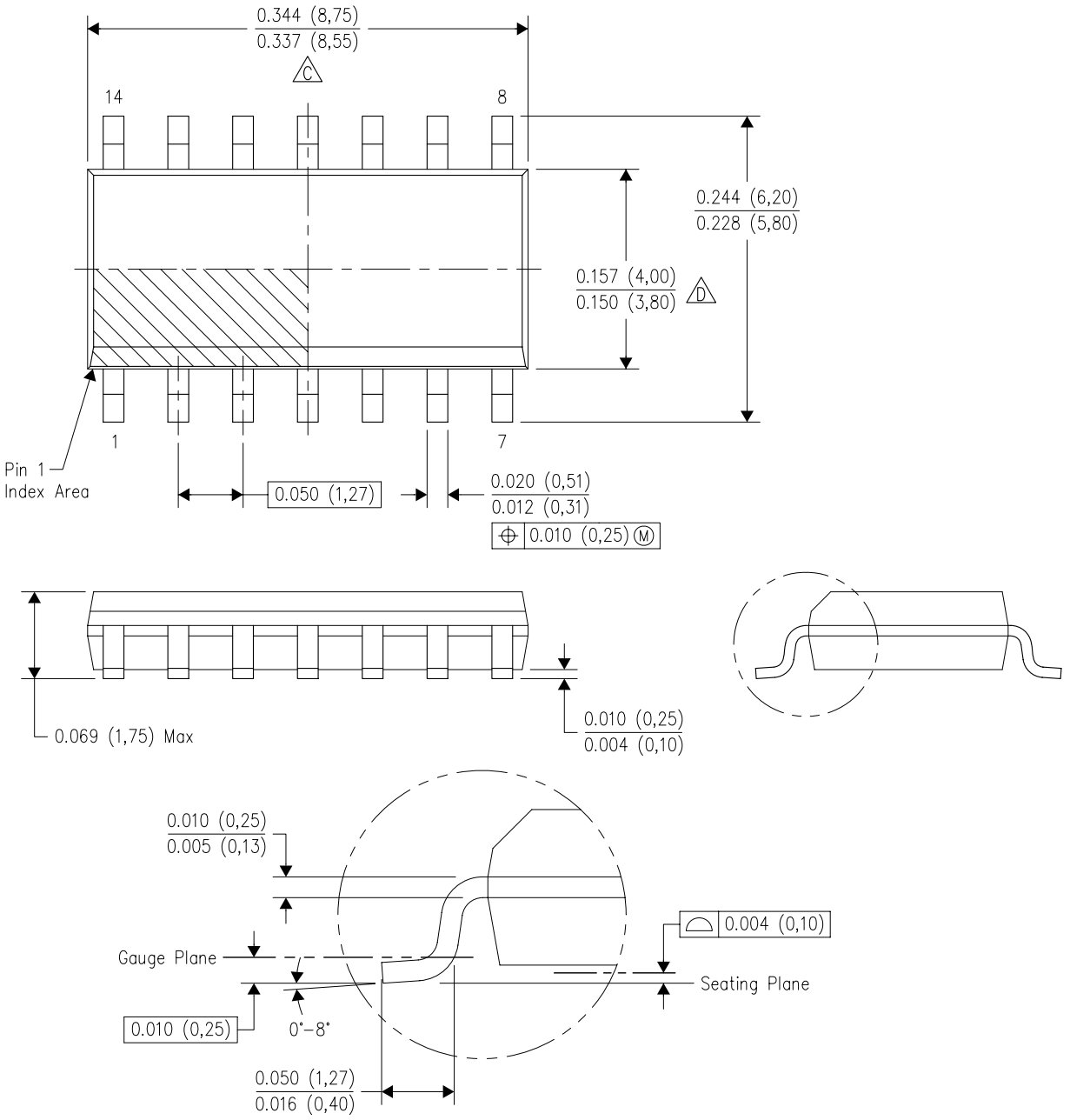
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8830MCDREP	SOIC	D	8	2500	367.0	367.0	35.0
DAC8831MCDREP	SOIC	D	14	2500	367.0	367.0	38.0

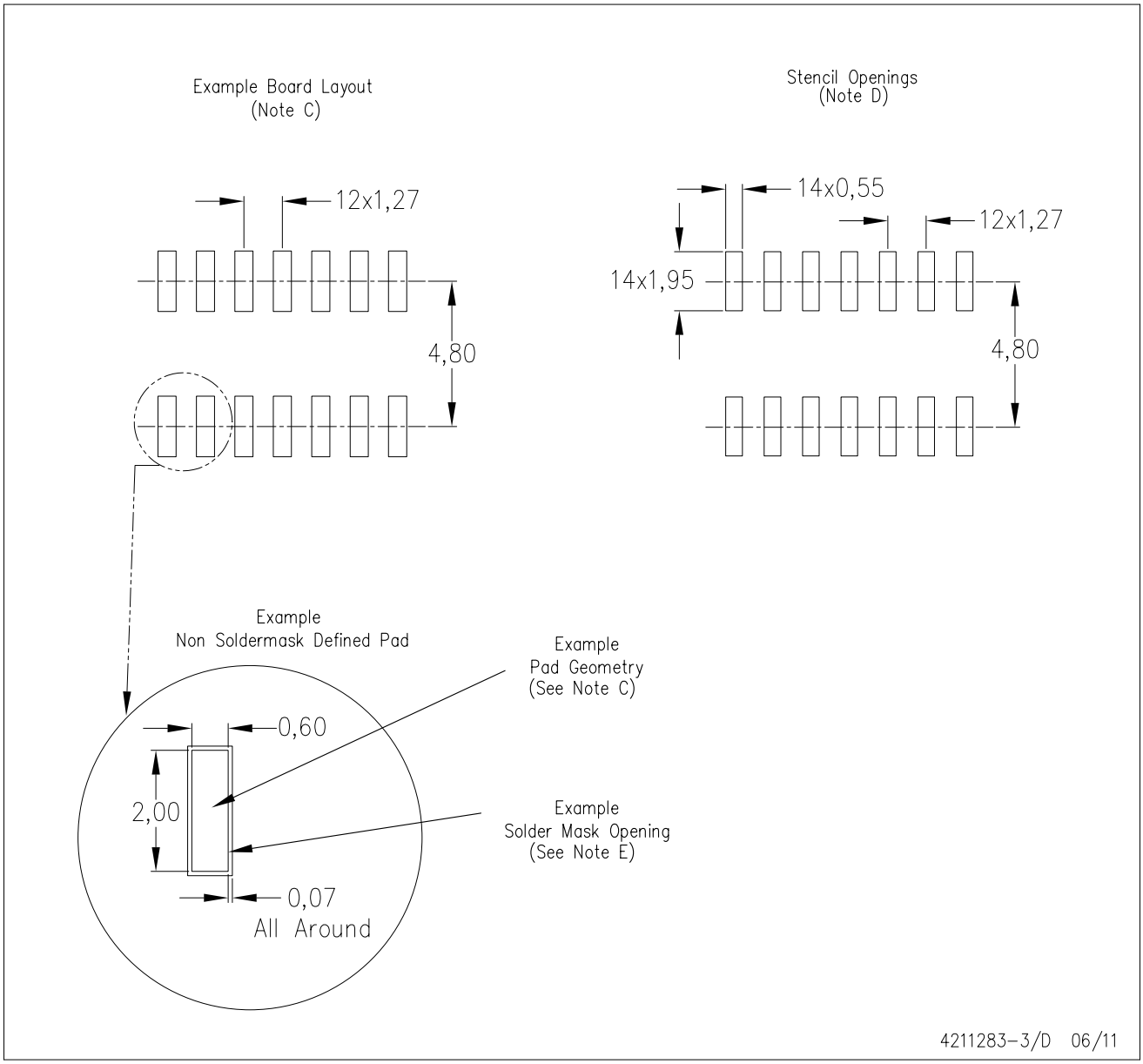
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

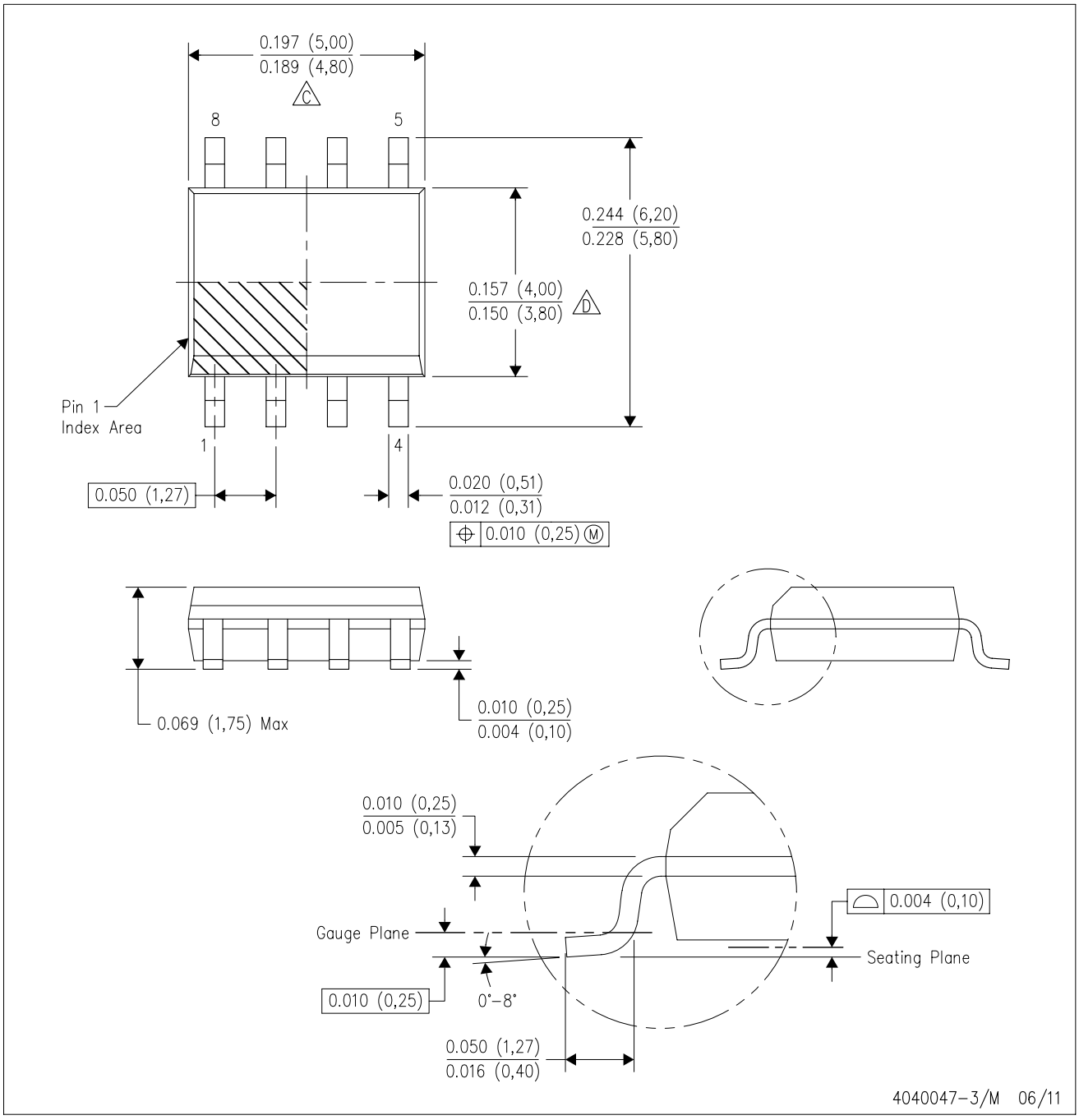
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



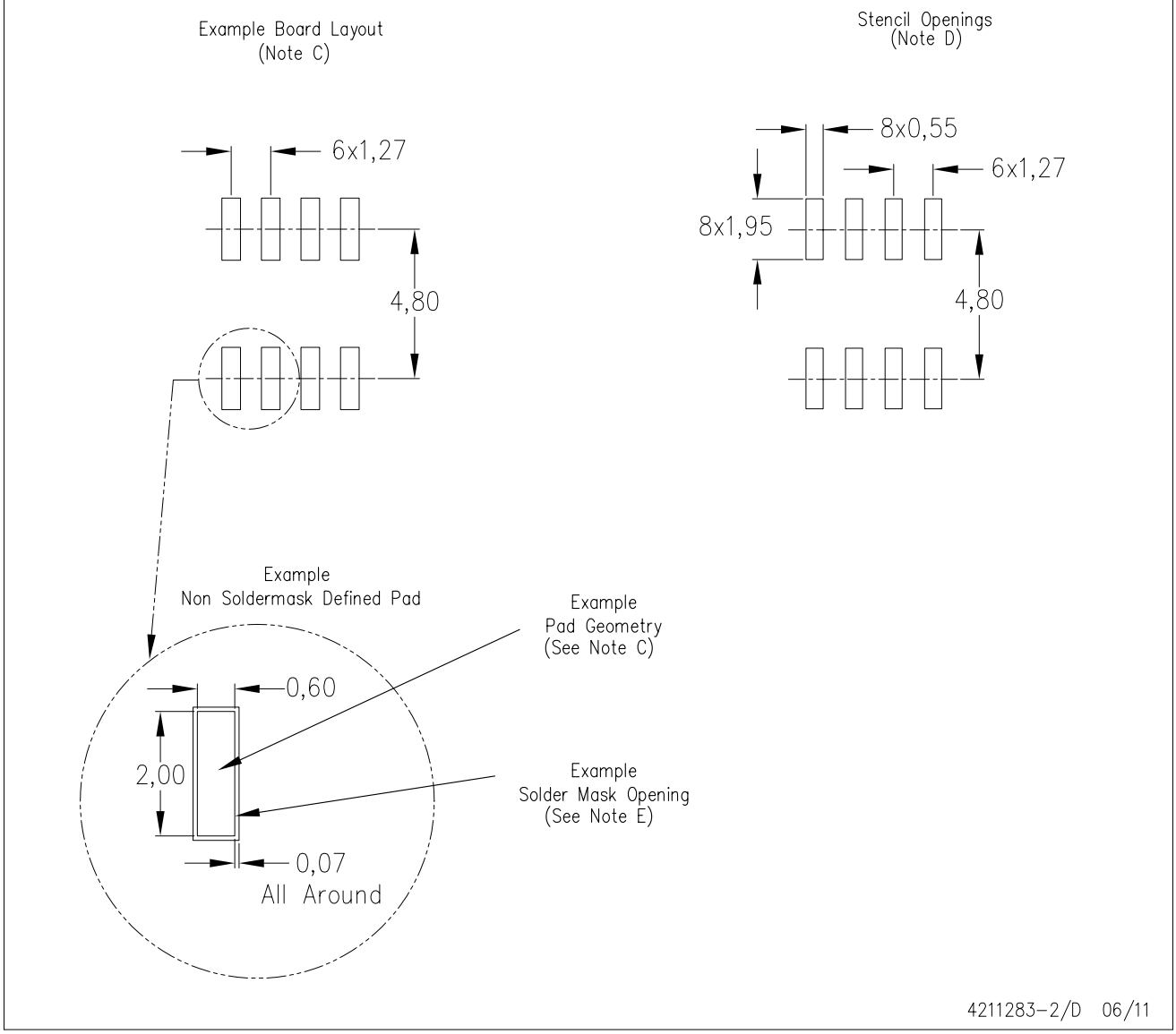
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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