DAC8771 Evaluation Module

This user's guide describes the characteristics and use of the DAC8771 evaluation board (EVM). It also discusses how to setup and configure the software and hardware for proper operation. Throughout this document, the terms *evaluation board*, *evaluation module*, and *EVM* are synonymous with the DAC8771EVM.

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1 Overview

The DAC8771 is a single-channel (quad) 16-bit precision digital-to-analog converter (DAC). The output can be configured to produce a current in output ranges of 0 to 20 mA, 0 to 24 mA, 3.5 to 23.5 mA, or ±24 mA. It can also be configured for voltage output in ranges of 0 to 5 V, 0 to 6 V, 0 to 10 V, 0 to 12 V, ±5 V, ±6 V, ±10 V, or ±12 V. The DAC8771 includes an integrated buck-boost converter to generate all necessary power supplies from a single external supply. The buck-boost converter features various operating modes that can be used to enhance power dissipation and thermal performance. The DAC8771 features additional peripherals including: HART input pins for coupling of FSK HART voltage signals, slew-rate control for the analog output, and reliability features such as CRC, watchdog timer, and conditional alarms.

1.1 EVM Kit Contents

Table 1 details the contents of the EVM kit. Contact the nearest Texas Instruments Product Information Center or visit the Texas Instruments E2E Community (http://E2E.ti.com) if any component is missing.

Table 1. Contents of DAC8771EVM Kit

Item #	Item	QTY	Description or Use
1	DAC8771EVM PCB	1	EVM hardware
2	USB Extension Cable	1	Connects PC USB port to SM-USB-DIG USB connector
3	SM-USB-DIG Platform	1	Platform used for digital communication from PC to EVM

1.2 Related Documentation From Texas Instruments

The following documents provide information regarding Texas Instruments integrated circuits used in the assembly of the DAC8771EVM. This user's guide is available from the TI website under the literature number SLAU727. Any letter appended to the literature number corresponds to the document revision that is current at the time of the writing of this document. Newer revisions may be available from the TI website at http://www.ti.com/, or by calling the Texas Instruments Literature Response Center at 1-800-477-8924 or the Product Information Center at 1-972-644-5580. When ordering identify the document by both title and literature number.

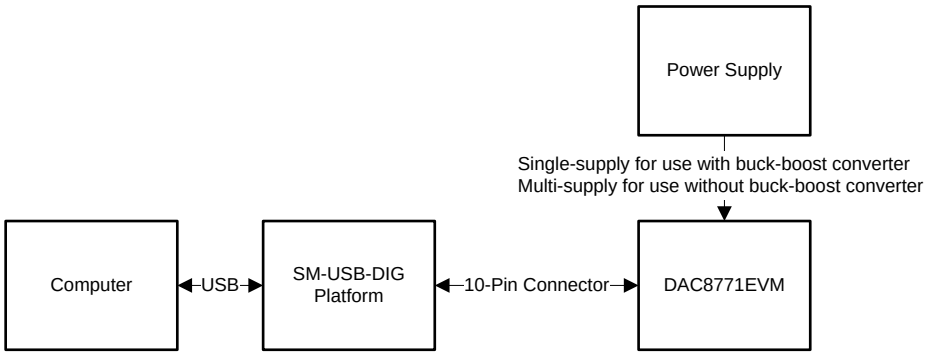
Table 2. Related Documentation

Item #	Literature Number
DAC8771 product data sheet	SLASEE2
REF5050 product data sheet	SBOS410
SM-USB-DIG platform user's guide	SBOU098

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2 EVM Hardware Overview

This section discusses the overall system setup for the EVM. A personal computer (PC) runs the software that communicates with the SM-USB-DIG platform, which provides the power and digital signals used to communicate with the EVM board. Connectors on the EVM board allow the user to connect the required external power supplies for the configuration under test. The SM-USB-DIG must be connected to the DAC8771EVM with the Texas Instruments logo facing up.

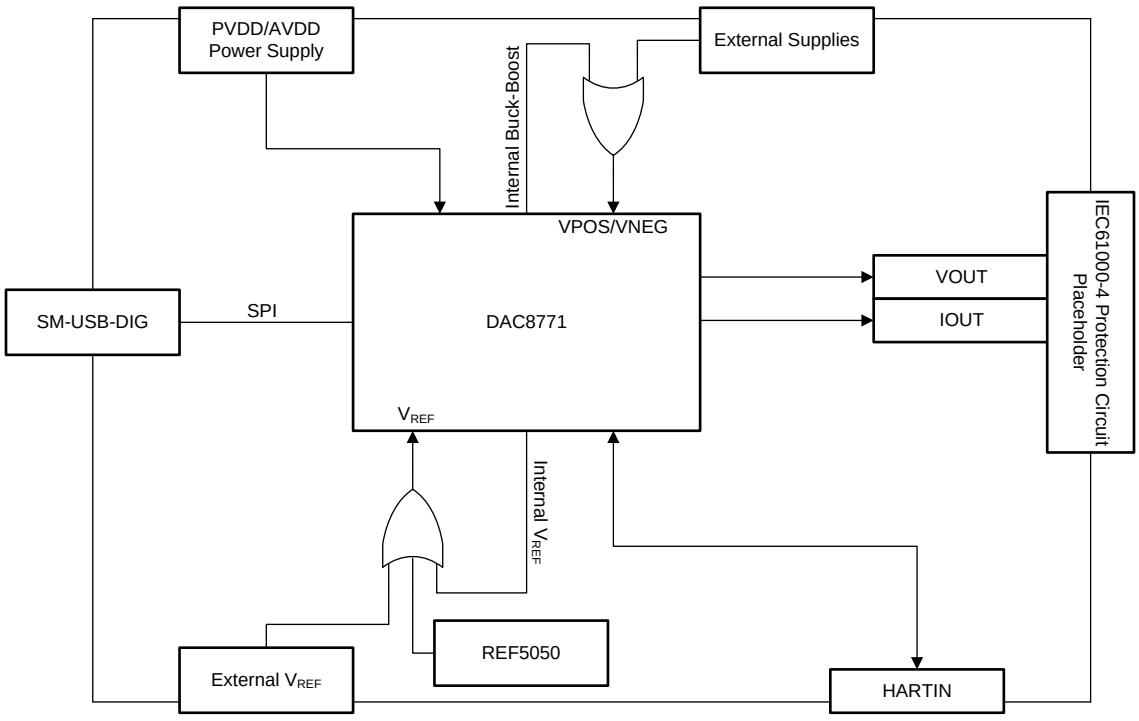


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Figure 1. DAC8771EVM Hardware Setup

2.1 EVM Board Block Diagram

A block diagram of the EVM board setup is shown in Figure 2. This board provides test points for the SPI, power, reference, ground, analog outputs, $\overline{\text{LDAC}}$, CLR, ALARM, and RESET signals. The EVM allows the user to select the internal buck-boost converter or external power supplies as sources for positive and negative supply rails of each channel. The EVM also allows the user to select the internal reference, onboard REF5050 reference, or external reference to provide the reference voltage to the DAC8771.



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Figure 2. DAC8771EVM Block Diagram

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2.2 Electrostatic Discharge Warning

Many of the components on the EVM are susceptible to damage by electrostatic discharge (ESD). Users are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

2.3 Jumper Summary

Table 3 summarizes all of the EVM jumper functionality.

Table 3. EVM Jumper Summary

Jumper Label	Default	Position	Function
JP1	1-2	1-2	Selects positive buck-boost to supply VPOS
		2-3	Selects PVDD/AVDD to supply VPOS
JP2	1-2	1-2	Selects negative buck-boost to supply VNEG
		2-3	Selects EXT_VNEG to supply VNEG
JP3	Installed	Installed	VSENSEP is shorted to VOUT onboard
		Not installed	VSENSEP is shorted to VOUT off board
JP4	Installed	Installed	Loads VOUT/IOUT with a short to GND
		Not installed	Unloads VOUT/IOUT of the short to GND
JP5	Installed	Installed	Loads VOUT/IOUT with a 249-Ω resistor
		Not installed	Unloads VOUT/IOUT of the 249-Ω resistor
JP6	Not installed	Installed	Loads VOUT/IOUT with a 624-Ω resistor
		Not installed	Unloads VOUT/IOUT of the 625-Ω resistor
JP7	Not installed	Installed	Loads VOUT/IOUT with a 1-kΩ resistor
		Not installed	Unloads VOUT/IOUT of the 1-kΩ resistor
JP8	Installed	Installed	VSENSEN is shorted to GND onboard
		Not installed	VSENSEN is shorted to GND off board
JP9	Installed	Installed	When HART_IN is not in use, AC couple to GND
		Not installed	When HART_IN is in use, disconnect from GND
JP10	Not installed	Installed	Selects the external DVDD
		Not installed	Disconnects the external DVDD
JP11	1-2	1-2	Selects the DAC8771 internal reference
		2-3	Selects the REF5050 external reference
JP12	2-3	1-2	Issues a clear command to the DAC8771
		2-3	No operation
JP13	Not installed	Installed	Issues a hardware reset to the DAC8771
		Not installed	No operation
JP14	Installed	Installed	Select asynchronous update mode
		Not installed	Select asynchronous update mode
JP15	Not installed	Installed	Disables internal DVDD LDO
		Not installed	Enables internal DVDD LDO
JP16	Not installed	Installed	Connects the SM-USB-DIG supply to DVDD
		Not installed	Disconnects SM-USB-DIG supply for DVDD
JP17	Not installed	Installed	RSET is connected to external Resistor
		Not installed	Internal current setting resistor is used

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2.4 Powering the EVM

This section describes the various power configurations that can be used by the EVM.

2.4.1 PVDD/AVDD Supply

The PVDD, the buck-boost converter supply, and AVDD, the analog supply, of the DAC8771 are connected to the same power net labeled PVDD/AVDD on the DAC8771EVM. Terminal block J3, shown in Figure 3, allows for external voltage sources to be connected to the PVDD/AVDD supply. The PVDD/AVDD supply must be provided regardless of whether the buck-boost converter is in use or not.



Figure 3. PVDD/AVDD, and DVDD Supply Connections

2.4.2 VPOS and VNEG Supplies

VPOS, the positive supply for the output signal chain, and VNEG, the negative supply for the output signal chain, may be powered by the DAC8771 internal buck-boost converters or by off-board supply voltages.

WARNING

Permanent device damage may occur if externally supplying VPOS or VNEG while the internal buck-boost supply is enabled.

When using the DAC8771 internal buck-boost converters to supply VPOS and VNEG, install JP1 and JP2 in the 1-2 position, or "inside" position, as indicated by Table 3.

When using external equipment to supply VPOS and VNEG, install JP1 and JP2 in the 2-3 position, or "outside" position, as indicated by Table 3. In this configuration, the VPOS supply is connected to the PVDD/AVDD net and the VNEG supply is connected to the EXT_VNEG. If bipolar supplies are used, connect an appropriate negative supply voltage to AVSS through terminal block J4, as shown in Figure 3. If unipolar supplies are used, connect AVSS to ground through terminal block J3.

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2.4.3 DVDD Supply

DVDD, the digital supply voltage, of the DAC8771 can be supplied by the SM-USB-DIG VDUT supply (pin 6 of J1), an external supply voltage through J5 (illustrated in Figure 3), or by the DAC8771 internal DVDD LDO. When using the SM-USB-DIG as the DVDD supply, uninstall jumper JP10 and install jumpers JP15 and JP15. To use an external supply voltage as the DVDD supply, install jumpers JP10 and JP15 and uninstall JP16. To use the DAC8771 internal LDO as the DVDD supply, uninstall jumpers JP10, JP15, and JP16.

In each DVDD supply configuration, take care to ensure that digital logic thresholds of the host and DAC8771 match and that the absolute maximum ratings of the DAC8771 are not violated.

2.5 EVM Features

This section describes some of the hardware features present on the EVM board.

2.5.1 Communication Test Points

The EVM board features test points for monitoring the communication between the SM-USB-DIG and the DAC8771. Header J2 provide test points for the LDAC, ALARM, CLR, RESET, SDIN, SCLK, $\overline{\text{SYNC}}$, and SDO pins of the DAC8771.

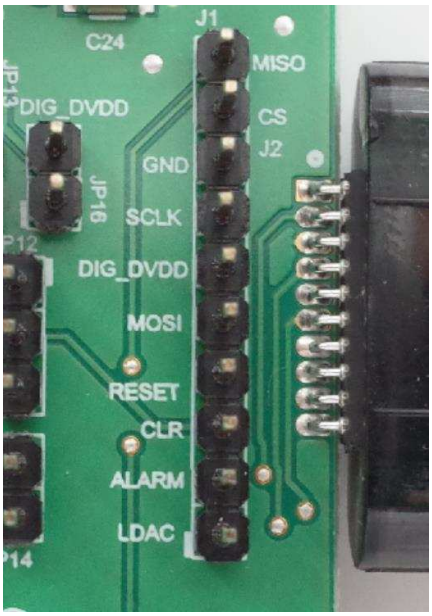


Figure 4. Digital Communication Test Points

The EVM design also allows external signals to be connected through these communication test points if the EVM is integrated into a custom evaluation setup or application-specific prototype. Note that if the SM-USB-DIG platform is not used, DVDD must be configured to use the DAC8771 internal DVDD LDO or external supplies as described in Section 2.4.3.

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2.5.2 Reference Voltage

The DAC8771 reference voltage can be supplied by the internal voltage reference, by the onboard REF5050, or by an external reference voltage.



Figure 5. Onboard Reference Supply Connections

To use the internal reference voltage, place JP11 in the 1-2 position. To use the REF5050 reference voltage, place JP11 in the 2-3 position and connect a supply voltage for the REF5050 to J6, as shown in Figure 5. To use an external reference voltage, remove JP11 and the reference can be connected to the DAC8771EVM through the center post of JP11.

2.5.3 VOUT, VSENSEP, and VSENSEN

The VOUT pins can be accessed on terminal block J7, by the OUT test points. The VSENSEP and VSENSEN sense connections may be provided onboard or externally closer to the point of load through terminal block J7. To provide the VSENSEP connections onboard, install JP3. Similarly, to provide the VSENSEN connections onboard, install JP8. Removing these jumpers requires that the sense connections are made external to the EVM board. Figure 6 shows the arrangement of the output terminal blocks.

2.5.4 IOUT

The IOUT pin can be accessed on terminal block J7 or by the test point OUT.

2.5.5 Onboard Output Loads

Four load choices are installed on the EVM board to evaluate the voltage and current outputs as well as the adaptive power management performance of the DAC8771. JP4 is available to provide a short-circuit condition on the output. JP5 provides a 250-Ω load on the output. JP6 provides a 625-Ω on the output. JP7 provides a 1-kΩ load on the output.

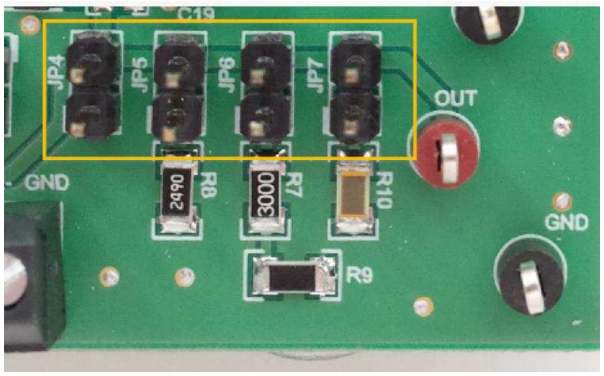


Figure 6. Output Terminal Block Connections and Load Jumpers

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2.5.6 Applying HART Signals

JP9 is available to couple external HART FSK communication signals onto the current outputs. When injecting the HART signal, remove JP9 and apply the HART signal to JP9 pin 1. When a HART signal is not being injected, install JP9 with AC coupling the HART pins to ground.

2.6 Connecting the SM-USB-DIG

To connect the EVM board and the SM-USB-DIG platform together, firmly slide the male and female ends of the 10-pin connectors together with the Texas Instruments logo of the SM-USB-DIG facing up as shown in Figure 7. Make sure that the two connectors are completely pushed together as loose connections may cause intermittent operation.



Figure 7. SM-USB-DIG Connection

2.7 Signal Definitions of J1 (10-Pin SM-USB-DIG Connector)

Table 4 shows the pin-out for the 10-pin connector used to communicate between the EVM and the SM-USB-DIG. Note that the I^2C communication lines (I2C_SCL and I2C_SDA1) are not used.

Table 4. SM-USB-DIG Connector

Pin on J1	Signal	Description
1	I2C_SCL	I^2C clock signal (SCL)
2	CTRL/MEAS4	GPIO: Control output or measure input
3	I2C_SDA1	I^2C data signal (SDA)
4	CTRL/MEAS5	GPIO: Control output or measure input
5	SPI_DOUT1	SPI data output (MOSI)
6	VDUT	Switchable DUT power supply: 3.3 V, 5 V, Hi-Z (disconnected). Note: When VDUT is Hi-Z, all digital I/Os are Hi-Z as well
7	SPI_CLK	SPI clock signal (SCLK)
8	GND	Power return (GND)
9	SPI_CS1	SPI chip-select signal (!CS)
10	SPI_DIN1	SPI data input (MISO)

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3 EVM Software Setup

This section discusses how to install the EVM software.

3.1 Operating Systems for EVM Software

The EVM software has been tested on the Microsoft® Windows® XP and Windows 7 operating systems with United States and European regional settings. The software should also function on other Windows operating systems.

3.2 EVM Software Installation

Download the EVM software by following the instructions provided external to this document. To install the software, locate and extract the file named DAC8771.zip to a specific folder (for example, C:\DAC8771\) on the hard drive.

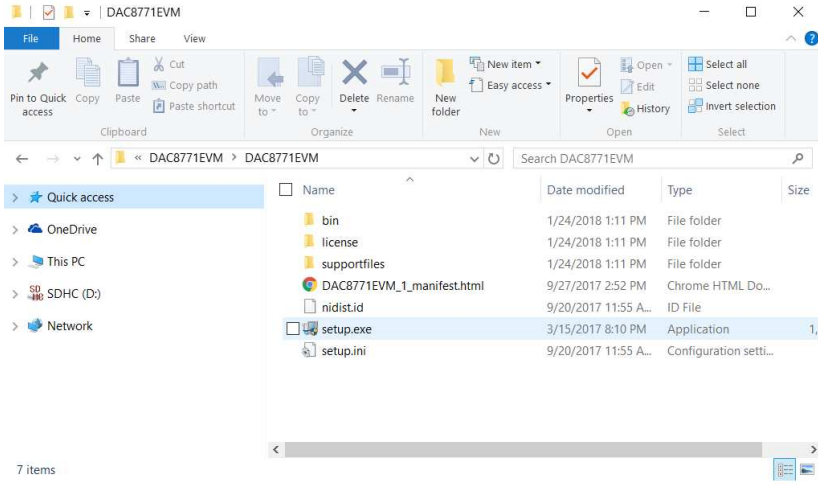


Figure 8. DAC8771EVM Installer

After the files are extracted, navigate to the folder created on the hard drive. Locate and execute the setup.exe file to start the installation. The DAC8771 software installer file then opens to begin the installation process.

After the installation process initializes, the user is given a choice of selecting the installation directory, usually defaulting to C:\Program Files(x86)\DAC8771EVM\ and C:\Program Files(x86)\National Instruments\.

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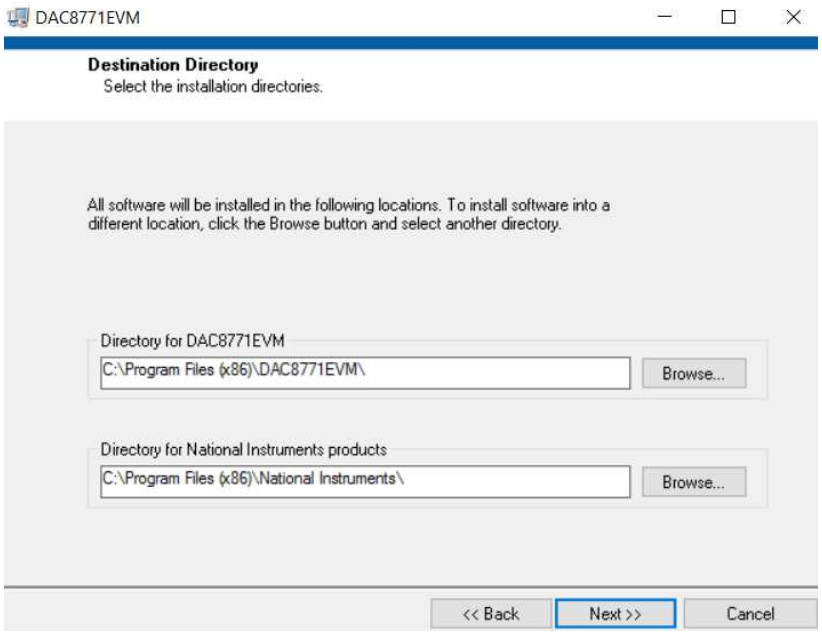


Figure 9. DAC8771EVM Install Path

After selecting the installation directory, two license agreements are presented that must be accepted.

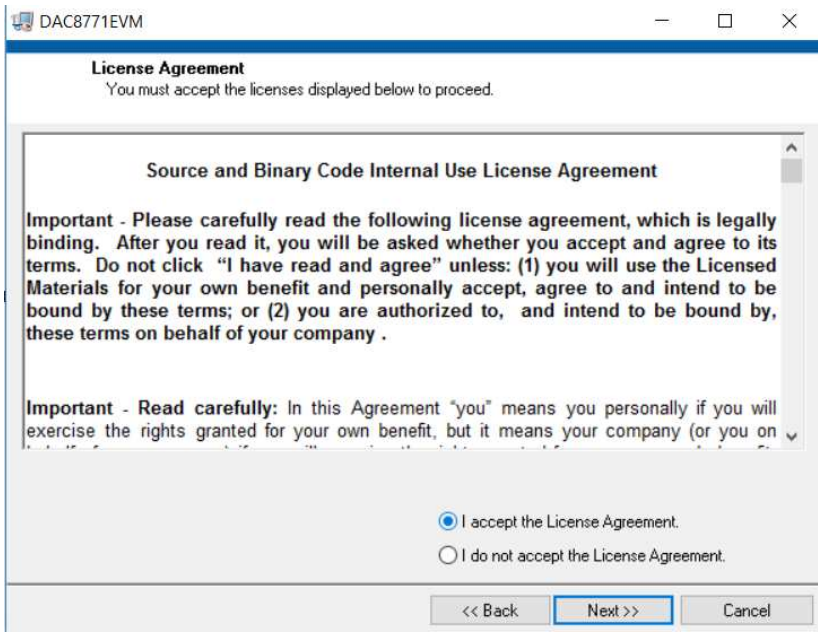


Figure 10. DAC8771EVM Software License Agreements

After accepting the Texas Instruments and National Instruments license agreements, the progress bar opens and shows the installation of the software. Once the installation process is completed, click Finish.

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4 EVM Software Overview

This section describes the use of the EVM software. Figure 11 shows the front panel of the EVM GUI.

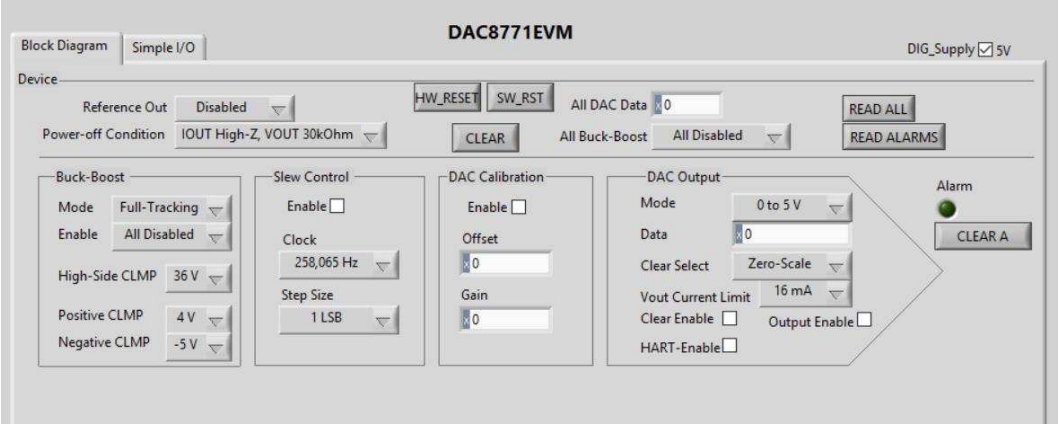


Figure 11. EVM GUI – Front Panel

4.1 Starting the EVM Software

The EVM software can be operated through the Windows start menu. From the start menu, select *All Programs*, and then select *DAC8771EVM*.

An error will appear if the PC cannot communicate with the EVM. If this error happens, first ensure that the USB cable is properly connected on both ends. This error can also occur if the USB cable is connected before the SM-USB-DIG platform power source. Another possible source for this error is a problem with the USB human interface driver on the PC. Make sure the device is recognized when the USB cable is plugged in, as indicated by a Windows-generated confirmation sound.

4.2 Reading From and Writing to Registers

The EVM software automatically reads from the DAC8771 when a reset or clear command is issued. To read from the device in other situations, press the *READ ALL* button on the EVM GUI. Write actions are carried out automatically when the value of any element on the GUI is changed.

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4.3 Device Controls

This section describes the GUI controls for the internal reference, power-on conditions, clear, software reset, and DAC broadcast functionality.

4.3.1 Internal Reference

The internal reference can be enabled or disabled using the internal reference control on the EVM GUI. By default, the internal reference is disabled.

4.3.2 Power-On Condition

By default, the power-on state of the current output is Hi-Z and the voltage output is 30 kΩ to ground after a clear or reset command. The power-on condition GUI control allows control of the voltage output power-on condition as either 30 kΩ to ground, or Hi-Z.

4.3.3 Software Reset

The *RESET* button on the GUI issues a software reset to the DAC8771, restoring the default power-on register contents. The GUI immediately reads all of the registers of the device to synchronize the GUI and hardware. A hardware reset can be issued through JP13. If a hardware issue is issued the *READ ALL* button should be pressed to synchronize the GUI and hardware.

4.3.4 Software Clear

The *CLEAR* button on the GUI issues a clear command to the DAC8771, restoring the DAC data registers to full-scale or zero-scale, based on the clear select settings and clear enable settings of each channel. After a clear command is issued, the GUI immediately reads the data registers of the device to synchronize the GUI and hardware. A hardware clear command can be issued through JP12. If a hardware clear is issued, the *READ ALL* button should be pressed to synchronize the GUI and hardware.

4.4 DAC Controls

4.4.1 DAC Output

The DAC can be configured for voltage or current output of various spans through the DAC Output *Mode* control on the GUI. The DAC output can be set to active or inactive by checking or removing the check from the *Output Enable* Boolean control on the GUI. Once an output range is selected and the output is enabled, the DAC output value can be controlled by writing values to the DAC *Data* control. The DAC *Data* control expects hexadecimal input formats. The small indicator on the left side of the DAC *Data* control can be used to change the input data format.

Output current drive can be programmatically limited for each of the voltage output modes through the *Vout Current Limit* control on the GUI. Take note that the actual current limit will be compliant to the values specified in the DAC8771 electrical characteristics table.

4.4.2 Clear Functionality

The DAC output has a *Clear Enable Boolean* that is ANDed with the *CLEAR* command. If the *Clear Enable* Boolean is checked, the output channel will respond to a clear event; conversely, if the Boolean is unchecked, the output channel will not respond to a clear event. The DAC can be programmed to clear to either zero-scale or full-scale. This behavior can be controlled by the *Clear Select* control on the GUI.

4.4.3 HART Inputs

To enable HART signals to be coupled to the current outputs through the onboard coupling path, the *HART-Enable* Boolean control must be checked.

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4.5 DAC Calibration Controls

Each DAC may use digital calibration to reduce offset and gain errors at output. By default, the calibration features are disabled. To enable the calibration features, the DAC Calibration *Enable* Boolean control must be checked. When the control is checked, offset and gain calibration may be controlled by the values written to *Offset* Calibration and *Gain* Calibration controls, respectively, on the EVM GUI. For more information concerning the calibration features, refer to *DAC8771 Single-Channel 16-Bit Voltage and Current Output DAC With Adaptive Power*.

4.6 Slew-Rate Controls

Control the slew-rate of the channel with the *Slew Control* register. By default, the slew-rate control feature is disabled. To enable the slew-rate control feature, the Slew Control *Enable* Boolean control must be checked. When the control is checked, slew-rate *Step Size* and *Clock* registers may be used to control the slew-rate of the output through the Slew Control *Step Size* and Slew Control *Clock*, respectively.

4.7 Buck-Boost Converter Controls

The buck-boost converter can be configured through the EVM GUI. The *Buck-Boost Mode* control is used to select the operating mode of the buck-boost converter and the *Buck-Boost Enable* control is used to enable the positive, negative, or both arms of the buck-boost converter. When *Buck-Boost Mode* is set to *Clamp Mode*, the *Positive CLMP* and *Negative CLMP* controls are used to set the output clamp of the arm.

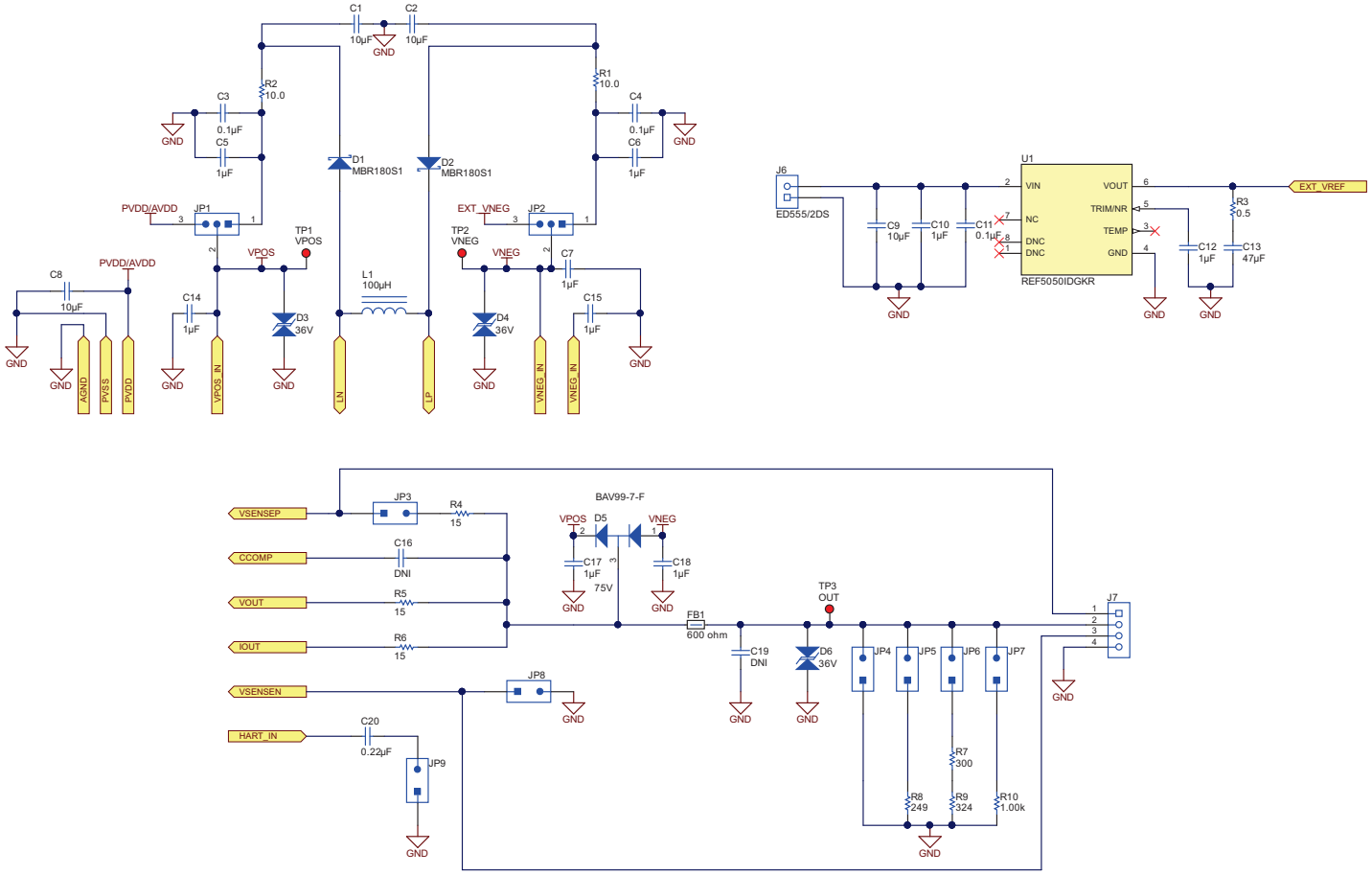
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5 EVM Documentation

This section contains the complete bill of materials and schematic diagram for the DAC8771EVM. Documentation information for the SDM-USB-DIG Platform is found in the *SDM-USB-DIG Platform User's Guide*.

5.1 EVM Board Schematic

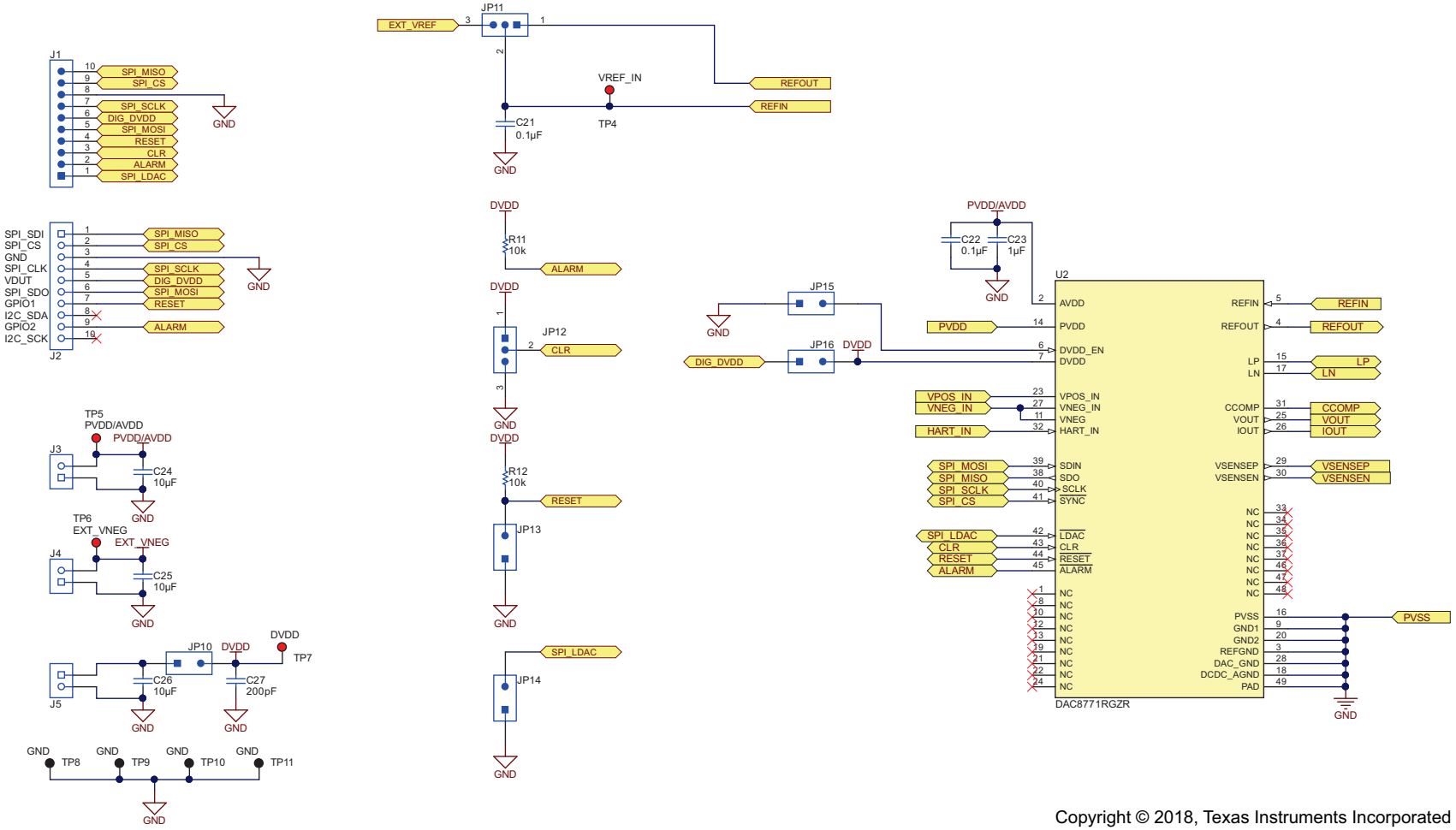
Figure 12 and Figure 13 illustrate the DAC8771EVM board schematics.



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Figure 12. Schematic 1

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Figure 13. Schematic 2

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5.2 EVM PCB Components Layout

Figure 14 shows the layout of the components for the EVM board.

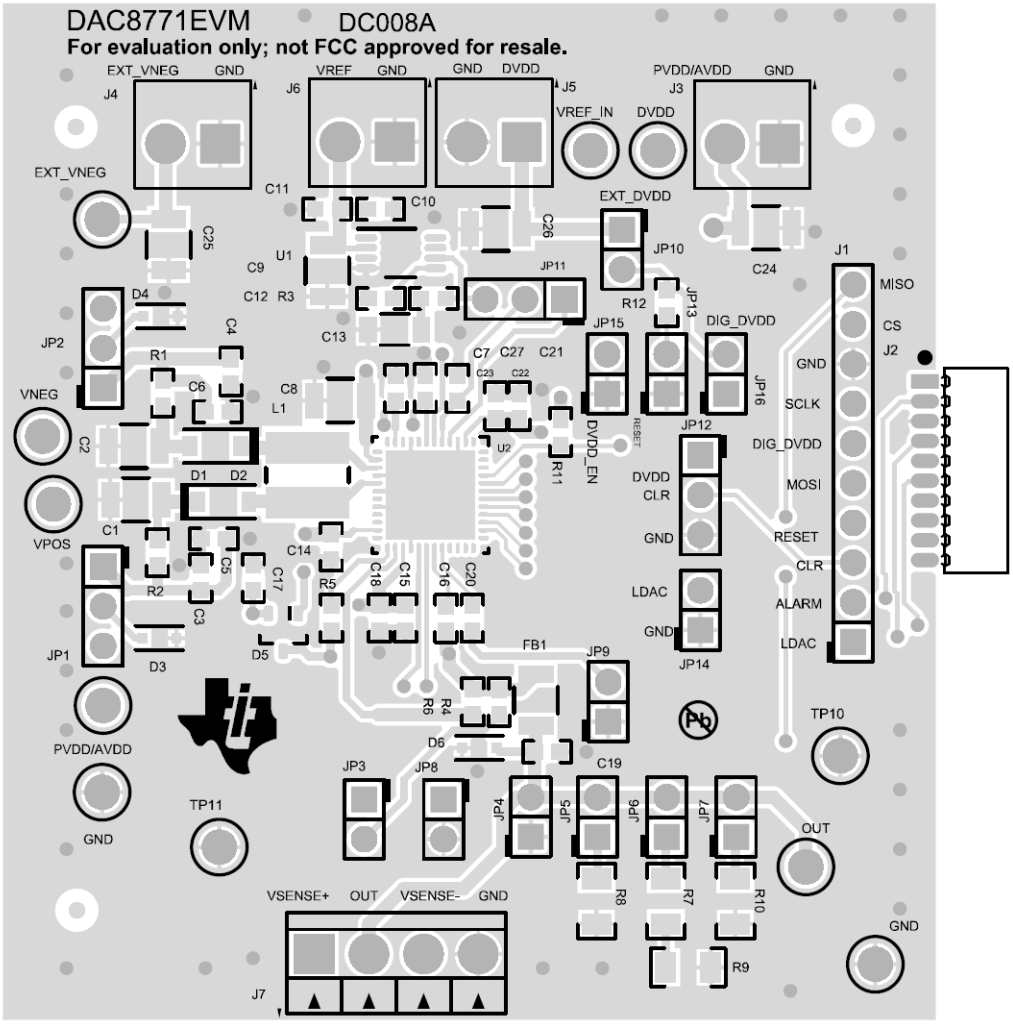


Figure 14. DAC8771EVM PCB Components Layout

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5.3 EVM Board Bill of Materials

Table 5 lists the EVM board bill of materials.

Table 5. EVM Board Bill of Materials(1)

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
!PCB1	1		Printed Circuit Board		DC008	Any		
C1, C2, C8, C9, C24, C25, C26	7	10uF	CAP, CERM, 10uF, 50V, ±10%, X7R, 1210 (H=2.5mm)	1210 (H=2.5mm)	UMK325AB7106KM-T	Taiyo Yuden		
C3, C4, C11, C21, C22	5	0.1uF	CAP, CERM, 0.1uF, 50V, ±10%, X7R, 0603	0603	GRM188R71H104KA93D	Murata		
C5, C6, C7, C10, C12, C14, C15, C17, C18, C23	10	1uF	CAP, CERM, 1uF, 50V, ±10%, X7R, 0603	0603	UMK107AB7105KA-T	Taiyo Yuden		
C13	1	47uF	CAP, CERM, 47 µF, 25 V,± 20%, X5R, 1206	1206	C3216X5R1E476M160AC	TDK		
C20	1	0.22uF	CAP, CERM, 0.22 µF, 50 V, ± 10%, X7R, 0603	0603	C1608X7R1H224K080AB	TDK		
C27	1	200pF	CAP, CERM, 200pF, 50V, ±5%, C0G/NP0, 0603	0603	GRM1885C1H201JA01D	Murata		
D1, D2	2	80V	Diode, Schottky, 60 V, 1 A, SOD-123	SOD-123	MBR180S1	Diodes Incorporated		
D3, D4, D6	3	36V	Diode, TVS, Bi, 36V, 400W, SOD323, 2-Leads, Body 1.9x1.45mm, No Polarity Mark	SOD323, 2-Leads, Body 1.9x1.45mm, No Polarity Mark	CDSOD323-T36SC	Bourns		
D5	1	75V	Diode, Switching, 75V, 0.3A, SOT-23	SOT-23	BAV99-7-F	Diodes Inc.		
FB1	1	600 ohm	Ferrite Bead, 600 ohm @ 100MHz, 3A, 1210 (H=2.5mm)	1210 (H=2.5mm)	FBMH3225HM601NT	Taiyo Yuden		
H1, H2, H3, H4	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M		
J1	1		Header, 100mil, 10x1, Gold, TH	10x1 Header	TSW-110-07-G-S	Samtec		
J2	1		Receptacle, 50mil, 10x1, Gold, R/A, TH	receptacle 10x1, 50mil	851-43-010-20-001000	Mill-Max		
J3, J4, J5, J6	4		Terminal Block, 3.5mm Pitch, 2x1, TH	7.0x8.2x6.5mm	ED555/2DS	On-Shore Technology		
J7	1		Terminal Block, 3.5mm Pitch, 4x1, TH	14x8.2x6.5mm	ED555/4DS	On-Shore Technology		
JP1, JP2, JP11, JP12	4		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec		
JP3, JP4, JP5, JP6, JP7, JP8, JP9, JP10, JP13, JP14, JP15, JP16	12		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec		
L1	1	100uH	Inductor, Shielded Drum Core, Ferrite, 100uH, 0.52A, 0.77 ohm, SMD	4.8x3.8x4.8mm	74408943101	Wurth Elektronik eiSos		
R1, R2	2	10.0	RES, 10.0 ohm, 1%, 0.1W, 0603	0603	CRCW060310R0FKEA	Vishay-Dale		
R3	1	0.5	RES, 0.5, 1%, 0.125 W, 0603	0603	CSR0603FKR500	Stackpole Electronics Inc		
R4, R5, R6	3	15	RES, 15 ohm, 5%, 0.1W, 0603	0603	CRCW060315R0JNEA	Vishay-Dale		
R7	1	300	RES, 300, 0.1%, 0.25 W, 1206	1206	ERA-8AEB301V	Panasonic		
R8	1	249	RES, 249, 0.1%, 0.25 W, 1206	1206	TNPW1206249RBEEA	Vishay-Dale		
R9	1	324	"RES, 324, 0.1%, 0.25 W,	1206"	1206	ERA-8AEB3240V	Panasonic	
R10	1	1.00k	"RES, 1.00 k, 0.1%, 1 W, 1206 resistor	1206	PHP01206E1001BST5	Vishay-Dale		
R11, R12	2	10k	RES, 10k ohm, 5%, 0.1W, 0603	0603	CRCW060310K0JNEA	Vishay-Dale		

(1) Unless otherwise noted in the *Alternate Part Number* or *Alternate Manufacturer* columns, all parts may be substituted with equivalents.

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Table 5. EVM Board Bill of Materials[(1)] (continued)

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SH-J11, SH-J12, SH-J13	13	1x2	Shunt, 100mil, Gold plated, Black	Shunt	969102-0000-DA	3M	SNT-100-BK-G	Samtec
TP1, TP2, TP3, TP4, TP5, TP6, TP7	7	Red	Test Point, Compact, Red, TH	Red Compact Testpoint	5005	Keystone		
TP8, TP9, TP10, TP11	4	Black	Test Point, Compact, Black, TH	Black Compact Testpoint	5006	Keystone		
U1	1		Low-Noise, Very Low Drift, Precision Voltage Reference, DGK0008A	DGK0008A	REF5050IDGKR	Texas Instruments	REF5050IDGKT	Texas Instruments
U2	1		Single-Channel, 16-Bit Voltage and Current Output Digital-to-Analog Converter with Adaptive Power Management, RGZ0048D (VQFN-48)	RGZ0048D	DAC8771RGZR	Texas Instruments	DAC8771RGZT	Texas Instruments
C16	0		CAP, CERM, 2200 pF, 50 V,± 5%, C0G/NP0, 0603	0603	GRM1885C1H222JA01D	Murata		
C19	0	0.1uF	CAP, CERM, 0.1uF, 50V, ±10%, X7R, 0603	0603	GRM188R71H104KA93D	Murata		
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A		

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   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

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8. *Limitations on Damages and Liability:*

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9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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