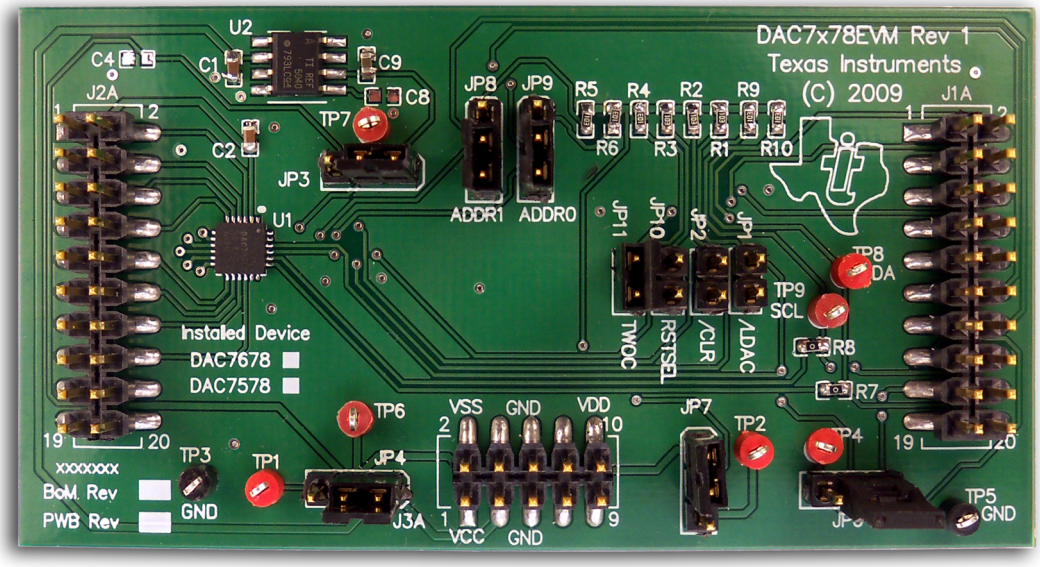
DAC7678EVM User's Guide



DAC7678EVM

This user's guide describes the characteristics, operation, and use of the DAC7678EVM. The evaluation model (EVM) is an evaluation board for the DAC7678. The DAC7678 is a low-power, voltage-output, octal, 12-bit digital-to-analog converter (DAC). The converter is controlled by an I²C™ interface that can operate at clock rates of up to 3.4MHz. Additionally, this DAC includes a 2.5V internal reference voltage (disabled by default), giving a full-scale output range of 5V. The EVM allows evaluation of all aspects of the device and allows user control over every pin on the DAC7678. Complete circuit descriptions, schematic diagrams, and bills of material are included in this document.

The following related documents are available for download through the Texas Instruments web site at http://www.ti.com.

EVM-Related Device Data Sheets

Device	Literature Number
DAC7678	SBAS493
REF5040	SBOS410D

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1 EVM Overview

1.1 Features

DAC7678EVM:

- Full-featured evaluation board for the DAC7678
- Onboard optional external reference selection
- Wide selection of digital and I/O voltages
- Hardware or software control of control logic
- Compatible with the TI Modular EVM System

This manual covers the operation of the DAC7678EVM. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the DAC7678EVM.

1.2 Introduction

The DAC7678 is a 12-bit, low-power, octal digital-to-analog converter (DAC) that operates from a single AV_{DD} supply. The DAC includes a 2.5V internal reference (disabled by default), giving a full-scale output voltage range of 5V. The DAC7678 is controlled by a two-wire I^2C interface (allowing speeds up to 3.4MHz) to communicate with a DSP or a microprocessor using a compatible interface. The DAC7678 has programmable address pins to set a custom I^2C communication address. This option allows you to use multiple devices on the same bus without having address conflicts.

The DAC7678EVM is designed to give the user access to all pins on the DAC7678. The evaluation module allows the user to control the DAC logic using on board jumpers, or digitally through the J2 header. By default, the evaluation module is configured to be used with an onboard external reference, but can be easily modified to use the DAC internal reference by changing a jumper setting and enabling the internal reference using software.

The DAC7678EVM is an evaluation module built to the TI Modular EVM System specification. It can be connected to any modular EVM system interface card.

Note that the DAC7678EVM has no microprocessor and cannot run software. To connect it to a computer, some type of interface is required.

2 Analog Interface

For maximum flexibility, the DAC7678EVM can interface to multiple analog sources. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a 10-pin, dual-row, header at J1. This header provides access to the analog input and output pins of the DAC7678. Consult Samtec at http://www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options. Table 1 summarizes the pinouts for analog interface J1A.

Table 1. J1: Analog Interface Pinout

Pin Number	Signal	Description
J1.2	$V_{OUT}A$	Analog output channel A
J1.4	$V_{OUT}C$	Analog output channel C
J1.6	$V_{OUT}E$	Analog output channel E
J1.8	$V_{OUT}G$	Analog output channel G
J1.10	$V_{OUT}H$	Analog output channel H
J1.12	$V_{OUT}F$	Analog output channel F
J1.14	$V_{OUT}D$	Analog output channel D
J1.16	$V_{OUT}B$	Analog output channel B
J1.18	N/A	—
J1.20	V_{REFIN}/V_{REFOUT}	External reference source input for V_{REFIN}/V_{REFOUT}
J1.9-1.13 (odd)	GND	Analog ground connection

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Table 1. J1: Analog Interface Pinout (continued)

Pin Number	Signal	Description
J1.17-1.19 (odd)	GND	Analog ground connection
J1.1-1.7 (odd)	N/A	—
J1.15	N/A	—

The analog interface is populated on both the top and the bottom sides of the evaluation board. All of the output pins of the DAC7678 are routed directly to the J1 connector.

The GND pins of the DAC7678 are connected directly to the ground of the evaluation board.

The DAC7678EVM is designed to allow the user to choose from using the DAC7678 internal reference, the onboard 4.096V REF5040, or a user-supplied external reference source for the DAC7678. Depending on how the DAC7678 is configured, pin J1.20 is either an input or an output. If the DAC7678 internal reference is used, then J1.20 is the output of the V_{REFIN}/V_{REFOUT} pin on the DAC7678. If an external reference is used, other than the onboard REF5025, J1.20 is used to provide the external reference voltage.

3 Digital Interface

3.1 I^2C Interface

Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a 10-pin, dual-row, header/socket combination at J2. This header/socket provides access to the digital control and I^2C data pins from both J2A (top side) and J2B (bottom side) of the connector. Consult Samtec at http://www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options. Table 2 describes the I^2C interface pins.

Table 2. J2: Serial Interface Pins

Pin No.	Signal Name	I/O Type	Pull-Up	Function
J2.1 - J2.13 odd	Unused			
J2.2	$\overline{CLR}$	In	High	DAC7678 $\overline{CLR}$ signal
J2.4	DGND	In/Out	None	Digital ground
J2.6	RSTSEL	In	High	Reset select
J2.8	TWOC	In	High	Data format for DAC input
J2.10	DGND	In/Out	None	Digital ground
J2.12	ADDR0	In	None	DAC7678 ADDR0 signal
J2.14	ADDR1	In	None	DAC7678 ADDR1 signal
J2.15	$\overline{LDAC1}$	In	High	DAC7678 $\overline{LDAC}$ signal. Switch JP6 determines $\overline{LDAC}$ control pin
J2.16	SCL	In	High	I^2C SCL line
J2.17	$\overline{LDAC2}$	In	High	DAC7678 $\overline{LDAC}$ signal. Switch JP6 determines $\overline{LDAC}$ control pin
J2.18	DGND	In/Out	None	Digital ground
J2.19	Unused	—	—	—
J2.20	SDA	In/Out	High	I^2C SDA line

The DAC7678 is controlled by a two-wire serial interface that is I^2C-compatible. Pins J2.16 (SCL) and J2.20 (SDA) are connected directly to the two control pins on the DAC7678 through 0Ω resistors. When the bus is idle, both the SDA and SCLK lines are pulled high through 10kΩ resistors built onto the EVM.

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Pins J2.2, J2.6, J2.8, J2.15, and J2.17 have weak pull-up/pull-down resistors. These resistors provide default settings for many of the control pins. These signals can be controlled through the digital interface or jumpers found directly on the EVM. By default, these signals are pulled high through 10kΩ resistors. The J2 header can be used to access these pins. See the DAC7678 product data sheet for complete details on these pins.

Pins J2.12 and J2.14 control the ADDR0 and ADDR1 pins to set the I^2C address for the DAC. Individually, the ADDR0 and ADDR1 address pins can be set to one of three positions: pulled high to AVDD, tied to ground, or left floating. The ADDR0 and ADDR1 pins can be controlled using the EVM hardware via JP8 and JP9 or through software using the J2 header.

The Load DAC ($\overline{\text{LDAC}}$) pin is connected via jumper JP6 to either the J2.15 or J2.17 pin. Updating the DAC7678 registers can be completed in two different ways. The $\overline{\text{LDAC}}$ pin can be held low and the input registers update immediately. Alternatively, $\overline{\text{LDAC}}$ can be held high and the DAC7678 registers update when $\overline{\text{LDAC}}$ is taken low. By default, $\overline{\text{LDAC}}$ is pulled high through a 10kΩ resistor. A shunt can be placed across jumper JP1 to connect $\overline{\text{LDAC}}$ to ground. See the DAC7678 product data sheet for more information on how to update the DAC7678 registers.

4 Power Supplies

J3 is the power-supply input connector. Table 3 lists the configuration details for J3. The voltage inputs to the DAC can be applied directly to the device. The DAC7678 requires only one power supply to operate.

Table 3. J3 Configuration: Power-Supply Input

Pin No.	Pin Name	Function	Required
J3.1	+VA	+VA analog supply	No
J3.2	–VA	–VA analog supply	No
J3.3	+5VA	+5V analog supply	Yes
J3.4	–5VA	-5V analog supply	No
J3.5	DGND	Digital ground input	Yes
J3.6	AGND	Analog ground input	Yes
J3.7	+1.8VD	1.8V digital supply	No
J3.8	VD1	Not used	No
J3.9	+3.3VD	3.3V digital supply	No
J3.10	+5VD	+5V	No

The digital and analog ground inputs are short-circuited internally through a ground plane.

The DAC7678EVM is designed to operate from a single +5V power supply (J3.3). This supply powers the DAC7678 itself, and the onboard REF5040 reference voltage source.

The DAC7678 can be powered from a wide range of voltages from +2.7V to +5.5V. The onboard REF5040 is powered from the +5VA supply on the J3 header. Jumper JP4 is in place to allow users to choose between the +5VA voltage to power the DAC or a separate, external power supply applied to TP1. This flexibility allows the user to be able to properly power the REF5040 while powering the DAC from any desired voltage within the specified range. The DAC7678EVM is not designed with any filters, so the use of a clean, well-regulated supply is strongly recommended.

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5 Voltage Reference

The DAC7678 can be operated using either the built-in 2.5V internal reference voltage or an external voltage option. When using external reference voltage options, the DAC7678EVM is configured with an onboard REF5040 that supplies a 4.096V external reference voltage to the DAC7678. The evaluation module also allows users to input an external reference voltage source through pin J1.20 on the analog header.

The V_{REFIN}/V_{REFOUT} pin on the DAC7678 can be configured as either an input or an output. When the 2.5V internal reference voltage is used, the pin is an output. When the DAC7678 is configured to use an external reference voltage and the internal reference is disabled, the pin is an input. Enabling and disabling the DAC7678 internal reference is controlled through digital communication. Jumper JP3 must be set accordingly, depending on the configuration of the reference voltage.

By default, the DAC7678 internal reference is disabled, and requires an external reference voltage. Jumper JP3 controls which external reference source is used. When JP3 is in the 1-2 position (default), the REF5040 is used. When JP3 is in the 2-3 position, the user can input a separate reference voltage to analog header pin J1.20; this reference will then be routed to the DAC7678.

To enable the DAC7678 internal reference voltage, make sure that jumper JP3 is either floating or connected in the 2-3 position. Then, once the internal reference is enabled by writing to the DAC, it appears on TP7.

NOTE: Do not place jumper JP3 in the 1-2 position while using the internal reference. If JP3 is in the 1-2 position when the internal reference is used, the user will be attempting to drive the V_{REFIN}/V_{REFOUT} pin externally while it is configured as the internal reference voltage output. This condition may cause permanent damage to the DAC7678.

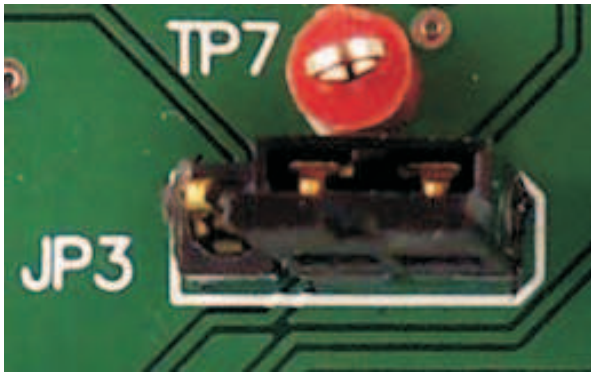


Figure 1. Reference Selection Jumper JP3 and Test Point TP7

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6 EVM Operation

This section provides information on the analog input, digital control, and general operating conditions of the DAC7678EVM.

6.1 Analog Input

The DAC7678 has eight analog outputs that are available through the J1 header. Each of these output are referenced to the board ground.

The V_{REFIN}/V_{REFOUT} pin is also routed to the J1 header. Depending on the JP3 configuration and the status of the DAC7678 internal reference, the internal reference voltage can be routed to the J1 analog header.

6.2 Digital Control

The digital control signals can be applied directly to J1 (top or bottom side). The modular DAC7678EVM can also be connected directly to a DSP or microcontroller interface board, such as the the MMB0 DSP board available from Texas Instruments.

No specific evaluation software is provided with this EVM. However, various code examples are available that show how to use EVMs with a variety of digital signal processors from Texas Instruments. Check the respective product folders on the TI web site or send an e-mail to dataconvapps@list.ti.com for a listing of available code examples. The EVM Gerber files are available on request.

6.3 Default Jumper Settings and Switch Positions

Table 4 lists the jumpers and the functionality of each that is available on the DAC7678EVM.

Table 4. DAC7678EVM Jumpers

Jumper	Name	Description
JP1	$\overline{\text{LDAC}}$ Control	$\overline{\text{LDAC}}$ control pin; pulled high by default. Apply shunt to tie pin to ground.
JP2	$\overline{\text{CLR}}$ Control	$\overline{\text{CLR}}$ control pin; pulled high by default. Apply shunt to tie pin to ground.
JP3	REF Selection	DAC reference selection control
JP4	AVDD Selection	Routes AVDD pin to either J3.3 or TP1 for an external voltage source.
JP6	$\overline{\text{LDAC}}$ Selection	Routes $\overline{\text{LDAC}}$ pin to either J2.15 or J2.17
JP7	IOVDD Selection	Selection between AVDD or an external voltage (via TP2) for the digital pull up.
JP8	ADDR1 Selection	Hardware control for the ADDR1 control pin
JP9	ADDR0 Selection	Hardware control for the ADDR0 control pin
JP10	RSTSEL Control	RSTSEL control pin; pulled high by default. Apply shunt to tie pin to ground.
JP11	TWOC Control	TWOC control pin; pulled high by default. Apply shunt to tie pin to ground.

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Figure 2 shows the default jumper conditions for the DAC7678EVM.

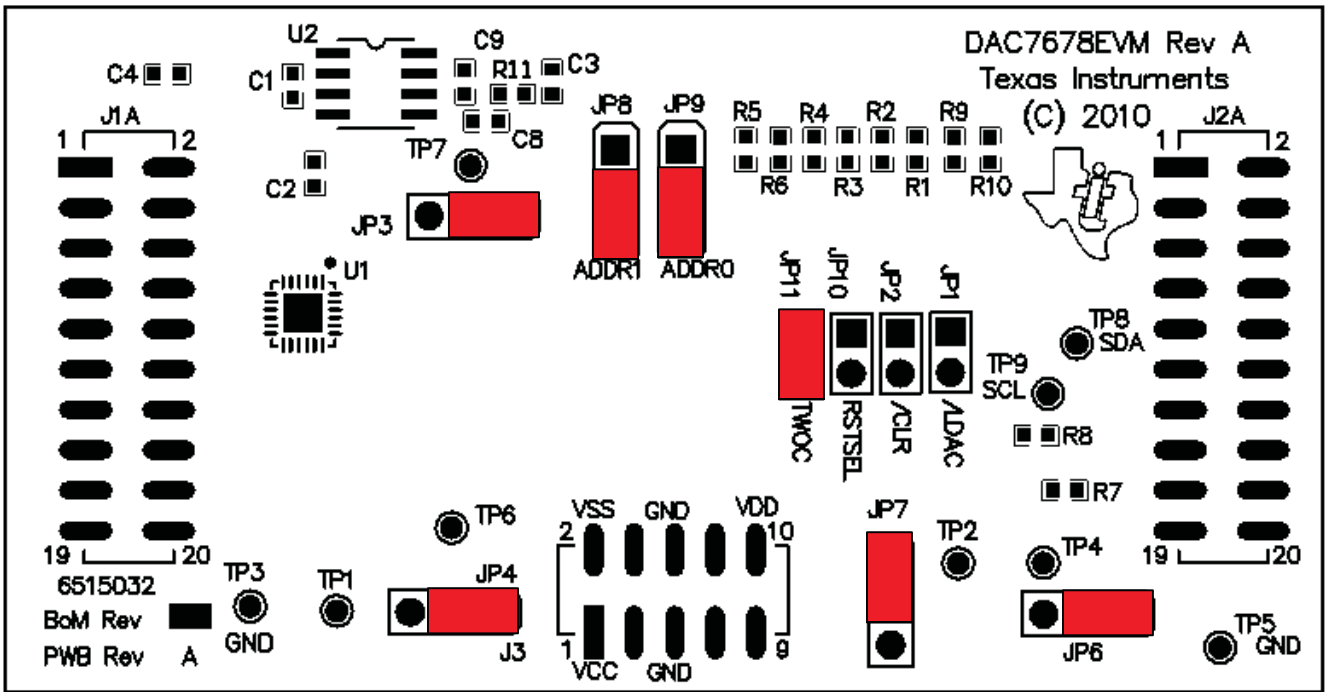


Figure 2. DAC7678EVM Default Jumper Locations

Jumpers JP1, JP2, JP10, and JP11 control the digital control inputs to the DAC7678. The $\overline{\text{LDAC}}$, $\overline{\text{CLR}}$, RSTSEL, and TWOC lines are all initially pulled high through 10kΩ resistors. A shunt can be placed along the corresponding pins to tie the signal to ground.

JP3 routes where the V_{REFIN}/V_{REFOUT} I/O pin on the DAC7678 is routed. When JP3 is in its default position, the shunt is placed across pins 1 and 2. This configuration allows the DAC7678 to use the onboard REF5040 as the external reference. When JP3 is in the 2-3 position, the user can input an external reference voltage to analog header pin J1.20, which will then be routed to the DAC7678. If the DAC7678 internal reference is enabled, the user must ensure that jumper JP3 is either floating or connected in the 2-3 position. The internal reference voltage can then appear on TP7. It is important to not have jumper JP3 in the 1-2 position while using the internal reference. You cannot drive the V_{REFIN}/V_{REFOUT} pin externally while it is configured as the internal reference voltage output. Doing so may permanently damage the DAC7678.

Jumper JP4 determines how to power the DAC AV_{DD}. By default, AV_{DD} is powered from J3.3 (JP4 position 1-2). It can also be powered from TP1 if the shunt is placed across pins 2-3.

Jumper JP6 selects where to route the $\overline{\text{LDAC}}$ signal. By default, pins JP6.1 and JP6.2 are connected to route the $\overline{\text{LDAC}}$ signal to J2.15. The shunt can be placed across JP6.2 and JP6.3 to route the $\overline{\text{LDAC}}$ signal to J2.17.

JP7 determines what voltage the pullup resistors on the digital control lines is. By default, the JP7 jumper is set to the 1-2 position to set the voltage to AVDD. If a different voltage is desired, the jumper must be set to the 2-3 position and place an external voltage at TP2.

Jumpers JP8 and JP9 set the address lines, ADDR1 and ADDR0, for the DAC7678. By default, the two address lines are pulled low (position 2-3). The ADDR1 and ADDR0 lines can be pulled high (position 1-2) or left floating (remove shunt completely) to set the address accordingly.

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7 Schematics and Layout

Schematics for the DAC7678EVM are appended to this user's guide. Figure 3 and Figure 4 are the printed circuit board (PCB) layouts. The bill of materials is provided in Table 5.

7.1 Bill of Materials

NOTE: All components should be compliant with the European Union Restriction on Use of Hazardous Substances (RoHS) Directive. Some part numbers may be either leaded or RoHS. Verify that purchased components are RoHS-compliant. (For more information about TI's position on RoHS compliance, see the Quality and Eco-Info information on the TI web site.)

Table 5. Bill of Materials

Item No.	Qty	Ref Des	Description	Vendor	Part Number
1	4	C1, C2, C3, C9	Capacitor, ceramic, 10µF, 6.3V X5R 0603	Murata	GRM188R60J106ME47D
2	2	C4, C8	Do not install	—	—
3	2	J1A, J2A (Top Side)	10-pin, l, SM header (20 Pos.)	Samtec	TSM-110-01-T-DV-P
4	2	J1B, J2B (Bottom Side)	10-pin, dual row, SM leader (20 Pos.)	Samtec	SSW-110-22-F-D-VS-K
5	1	J3A (Top Side)	5-pin, dual row, SM header (10 Pos.)	Samtec	TSM-105-01-T-DV-P
6	1	J3B (Bottom Side)	5-pin, dual row, SM header (10 Pos.)	Samtec	SSW-105-22-F-D-VS-K
7	4	JP1, JP2, JP10, JP11	Header strip, 2 pin (1x2)	Samtec	TSW-102-07-L-S
8	6	JP3, JP4, JP6, JP7, JP8, JP9	Header strip, 3 pin (1x3)	Samtec	TSW-103-07-L-S
9	8	R1, R2, R3, R4, R5, R6, R9, R10	Resistor, 10kΩ, 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ103V
10	3	R7, R8, R11	Resistor, 0Ω 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEY0R00V
11	7	TP1, TP2, TP4, TP6, TP7, TP8, TP9	Test point - Single .025 Pin, Red	Keystone	5000
12	2	TP3, TP5	Test point - Single .025 Pin, Black	Keystone	5001
13	1	U1	Octal, 12-bit, high-accuracy DAC,	Texas Instruments	DAC7678SRGET
14	1	U2	Precision voltage reference 4.096V, 8-SOIC	Texas Instruments	REF5040AID
15	10	NA	0.100 shunt - Black	Samtec	SNT-100-BK-T

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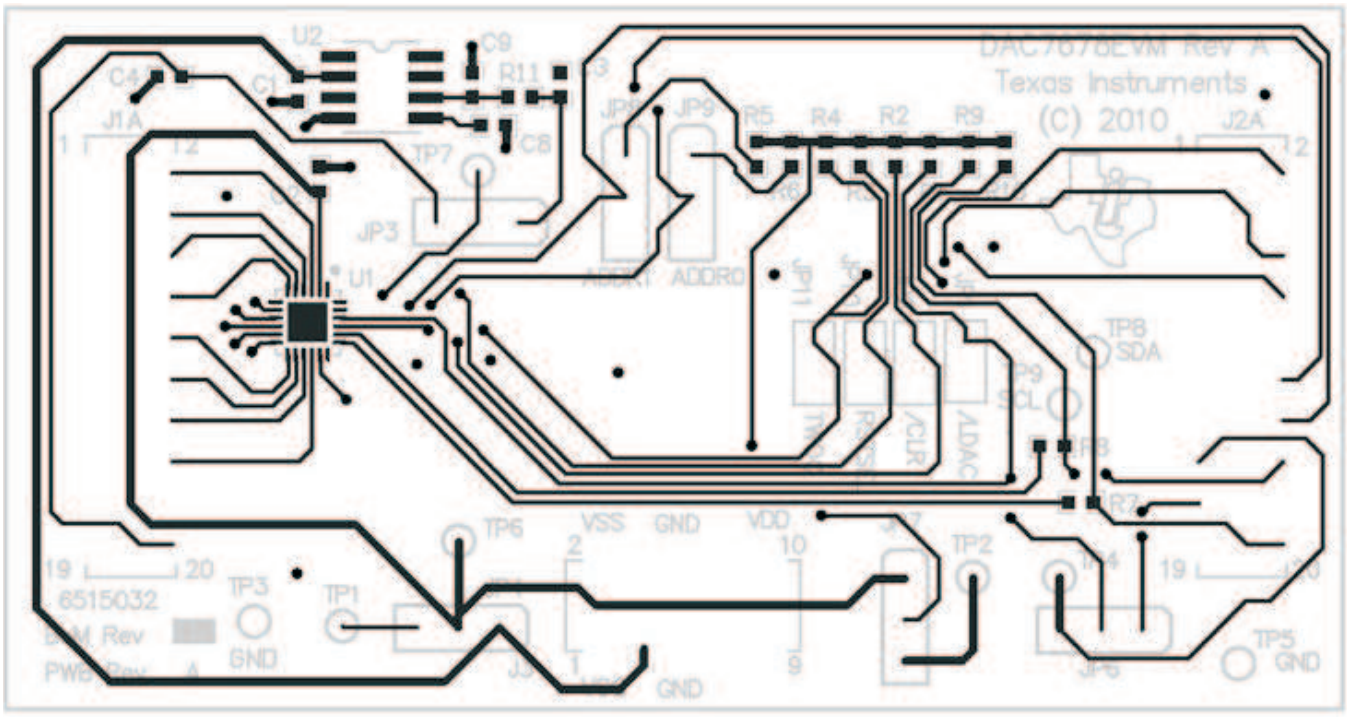


Figure 3. DAC7678EVM: Top Layer Image

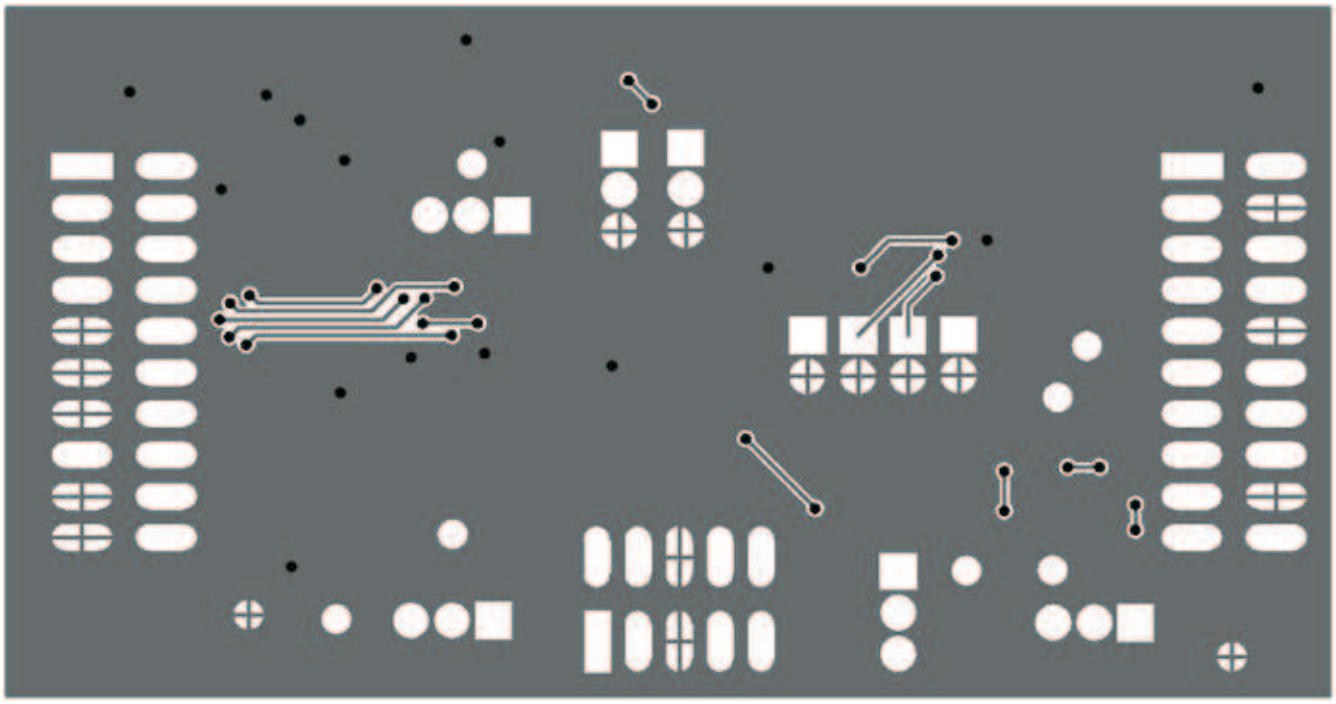


Figure 4. DAC7678EVM: Bottom Layer Image

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Revision History

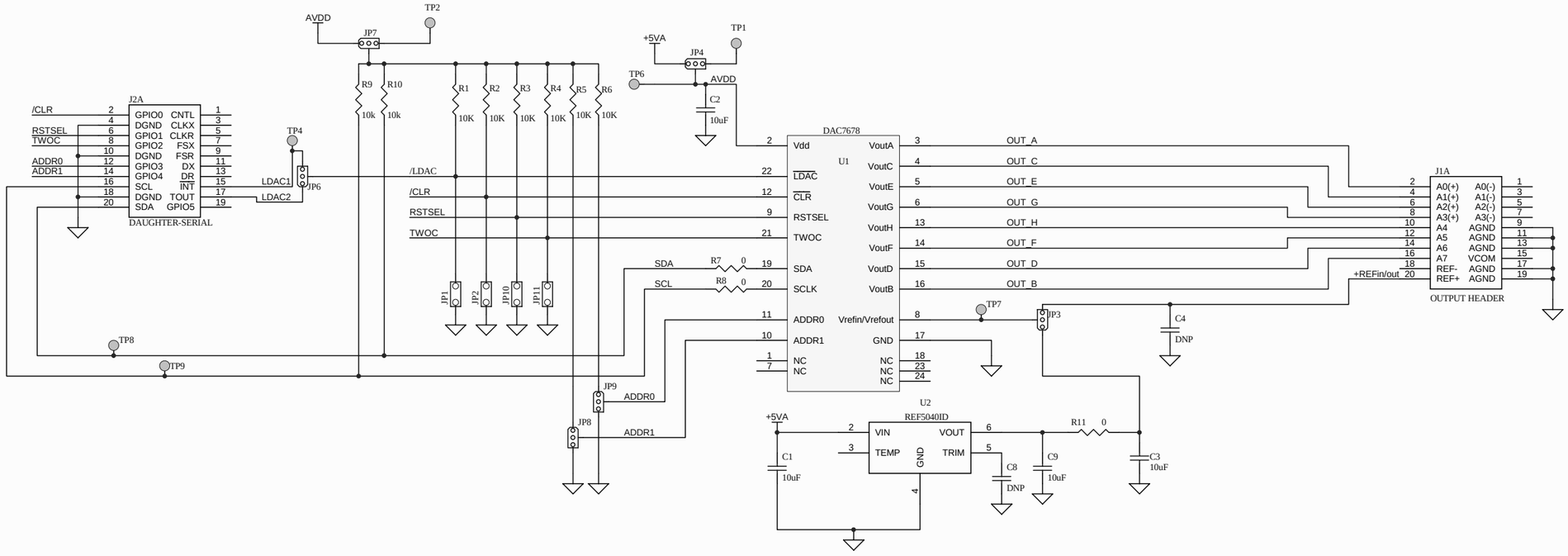
Changes from B Revision (May, 2011) to C Revision **Page**

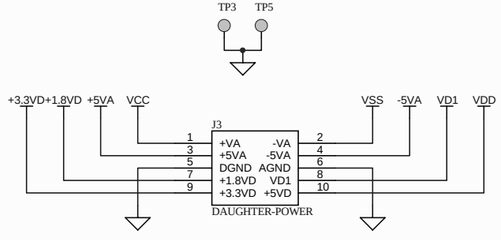
- Corrected typos and errors in *Analog Interface* section 3
- Updated Table 1 3
- Revised last paragraph of *Voltage Reference* section 6
- Changed descriptions of jumper positions and operations throughout Section 6.3 8

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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Revision History		
REV	ECN Number	Approved
1	First Proto Release	
	Production Release	





Engineer:	
Drawn By:	
FILE:	DAC7678 Rev A.Sch

TEXAS INSTRUMENTS

12500 TI Boulevard. Dallas, Texas 75243

Title: DAC7678 EVM			
DOCUMENTCONTROL # 6515032			REV: A
DATE: 5-Aug-2010	SIZE:	SHEET: 1 OF: 1	

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 0V to 5.5V and the output voltage range of 0V to 5.5V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +30°C. The EVM is designed to operate properly with certain components above +30°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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