DAC7512

SBAS156B – JULY 2002

Low-Power, Rail-to-Rail Output, 12-Bit Serial Input DIGITAL-TO-ANALOG CONVERTER

FEATURES

- ***micro*POWER OPERATION: 135µA at 5V**
- **POWER-DOWN: 200nA at 5V, 50nA at 3V**
- **POWER SUPPLY: +2.7V to +5.5V**
- **TESTED MONOTONIC BY DESIGN**
- **POWER-ON RESET TO 0V**
- **THREE POWER-DOWN FUNCTIONS**
- **LOW POWER SERIAL INTERFACE WITH SCHMITT-TRIGGERED INPUTS**
- **ON-CHIP OUTPUT BUFFER AMPLIFIER, RAIL-TO-RAIL OPERATION**
- **$\overline{\text{SYNC}}$ INTERRUPT FACILITY**
- **SOT23-6 AND MSOP-8 PACKAGES**

APPLICATIONS

- **PORTABLE BATTERY-POWERED INSTRUMENTS**
- **DIGITAL GAIN AND OFFSET ADJUSTMENT**
- **PROGRAMMABLE VOLTAGE AND CURRENT SOURCES**

DESCRIPTION

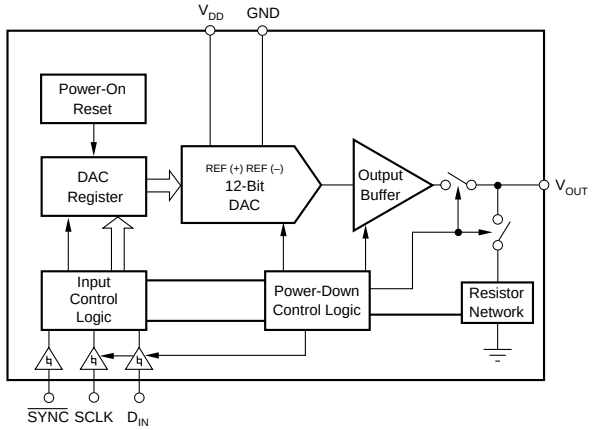
The DAC7512 is a low-power, single, 12-bit buffered voltage output Digital-to-Analog Converter (DAC). Its on-chip precision output amplifier allows rail-to-rail output swing to be achieved. The DAC7512 uses a versatile three-wire serial interface that operates at clock rates up to 30MHz and is compatible with standard SPI™, QSPI™, Microwire™, and DSP interfaces.

The reference for the DAC7512 is derived from the power supply, resulting in the widest dynamic output range possible. The DAC7512 incorporates a power-on reset circuit that ensures that the DAC output powers up at 0V and remains there until a valid write takes place in the device. The DAC7512 contains a power-down feature, accessed over the serial interface, that can reduce the current consumption of the device to 50nA at 5V.

The low power consumption of this part in normal operation makes it ideally suited to portable battery-operated equipment. The power consumption is 0.7mW at 5V reducing to 1µW in power-down mode.

The DAC7512 is available in a SOT23-6 package and an MSOP-8 package.

SPI and QSPI are registered trademarks of Motorola.
Microwire is a registered trademark of National Semiconductor.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to GND	–0.3V to +6V
Digital Input Voltage to GND	–0.3V to $+V_{DD}$ + 0.3V
V_{OUT} to GND	–0.3V to $+V_{DD}$ + 0.3V
Operating Temperature Range	–40°C to +105°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature Range (T_J max)	+150°C
SOT23 Package:	
Power Dissipation	(T_J max — T_A)/ $_{JA}$
$_{JA}$ Thermal Impedance	240°C/W
Lead Temperature, Soldering:	
Vapor Phase (60s)	+215°C
Infrared (15s)	+220°C
MSOP Package:	
Power Dissipation	(T_J max — T_A)/ $_{JA}$
$_{JA}$ Thermal Impedance	206°C/W
$_{JC}$ Thermal Impedance	44°C/W
Lead Temperature, Soldering:	
Vapor Phase (60s)	+215°C
Infrared (15s)	+220°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

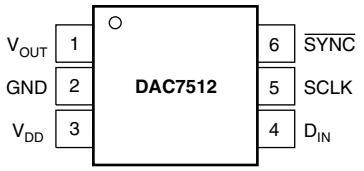
PACKAGE/ORDERING INFORMATION

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER[1]	TRANSPORT MEDIA, QUANTITY
DAC7512E	±8	±1	MSOP-8	DGK	–40°C to +105°C	D12E	DAC7512E/250	Tape and Reel, 250
"	"	"	"	"	"	"	DAC7512E/2K5	Tape and Reel, 2500
DAC7512N	±8	±1	SOT23-6	DBV	–40°C to +105°C	D12N	DAC7512N/250	Tape and Reel, 250
"	"	"	"	"	"	"	DAC7512N/3K	Tape and Reel, 3000

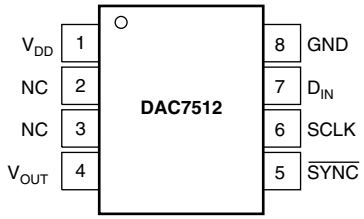
NOTES: (1) For the most current specifications and package information, refer to our web site at www.ti.com. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "DAC7512E/2K5" will get a single 2500-piece Tape and Reel.

PIN CONFIGURATIONS

Top View SOT23-6



MSOP-8

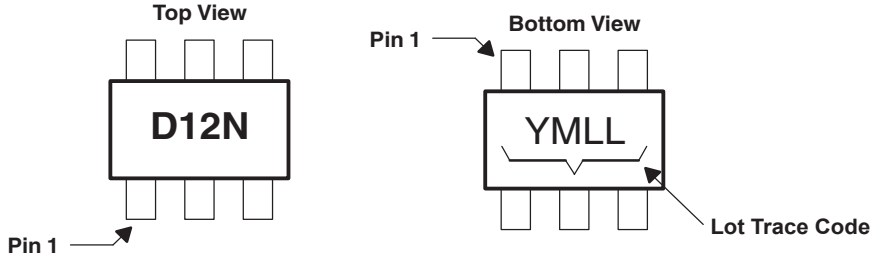


NC = No Internal Connection

PIN DESCRIPTION (SOT23-6)

PIN	NAME	DESCRIPTION
1	V_{OUT}	Analog output voltage from DAC. The output amplifier has rail-to-rail operation.
2	GND	Ground reference point for all circuitry on the part.
3	V_{DD}	Power Supply Input, +2.7V to 5.5V.
4	D_{IN}	Serial Data Input. Data is clocked into the 16-bit input shift register on the falling edge of the serial clock input.
5	SCLK	Serial Clock Input. Data can be transferred at rates up to 30MHz.
6	$\overline{SYNC}$	Level triggered control input (active LOW). This is the frame sychronization signal for the input data. When $\overline{SYNC}$ goes LOW, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 16th clock cycle unless $\overline{SYNC}$ is taken HIGH before this edge, in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC7512.

DAC7512N LOT TRACE LOCATION



ELECTRICAL CHARACTERISTICS

V_{DD} = +2.7V to +5.5V; R_L = 2ký to GND; C_L = 200pF to GND.

PARAMETER	CONDITIONS	DAC7512E, N			UNITS
		MIN	TYP	MAX	
STATIC PERFORMANCE (1)					
Resolution		12			Bits
Relative Accuracy				±8	LSB
Differential Nonlinearity	Tested Monotonic by Design			±1	LSB
Zero Code Error	All Zeroes Loaded to DAC Register		+5	+20	mV
Full-Scale Error	All Ones Loaded to DAC Register		–0.15	–1.25	% of FSR
Gain Error				±1.25	% of FSR
Zero Code Error Drift			–20		µV/°C
Gain Temperature Coefficient			–5		ppm of FSR/°C
OUTPUT CHARACTERISTICS (2)					
Output Voltage Range		0		V_{DD}	V
Output Voltage Settling Time	1/4 Scale to 3/4 Scale Change (400_H to $C00_H$)		8	10	µs
	R_L = 2kΩ; 0pF < C_L < 200pF				
	R_L = 2kΩ; C_L = 500pF		12		µs
Slew Rate		1			V/µs
Capacitive Load Stability	R_L = ×		470		pF
	R_L = 2kΩ		1000		pF
Code Change Glitch Impulse	1LSB Change Around Major Carry		20		nV-s
Digital Feedthrough			0.5		nV-s
DC Output Impedance			1		Ω
Short-Circuit Current	V_{DD} = +5V		50		mA
	V_{DD} = +3V		20		mA
Power-Up Time	Coming Out of Power-Down Mode				
	V_{DD} = +5V		2.5		µs
	Coming Out of Power-Down Mode				
	V_{DD} = +3V		5		µs
LOGIC INPUTS (2)					
Input Current				±1	µA
V_{IN}L, Input Low Voltage	V_{DD} = +5V			0.8	V
V_{IN}L, Input Low Voltage	V_{DD} = +3V			0.6	V
V_{IN}H, Input High Voltage	V_{DD} = +5V	2.4			V
V_{IN}H, Input High Voltage	V_{DD} = +3V	2.1			V
Pin Capacitance				3	pF
POWER REQUIREMENTS					
V_{DD}		2.7		5.5	V
I_{DD} (normal mode)	DAC Active and Excluding Load Current				
V_{DD} = +3.6V to +5.5V	V_{IH} = V_{DD} and V_{IL} = GND		135	200	µA
V_{DD} = +2.7V to +3.6V	V_{IH} = V_{DD} and V_{IL} = GND		115	160	µA
I_{DD} (all power-down modes)					
V_{DD} = +3.6V to +5.5V	V_{IH} = V_{DD} and V_{IL} = GND		0.2	1	µA
V_{DD} = +2.7V to +3.6V	V_{IH} = V_{DD} and V_{IL} = GND		0.05	1	µA
POWER EFFICIENCY					
I_{OUT}/I_{DD}	I_{LOAD} = 2mA. V_{DD} = +5V		93		%
TEMPERATURE RANGE					
Specified Performance		–40		+105	°C

NOTES: (1) Linearity calculated using a reduced code range of 48 to 4047; output unloaded. (2) Guaranteed by design and characterization, not production tested.

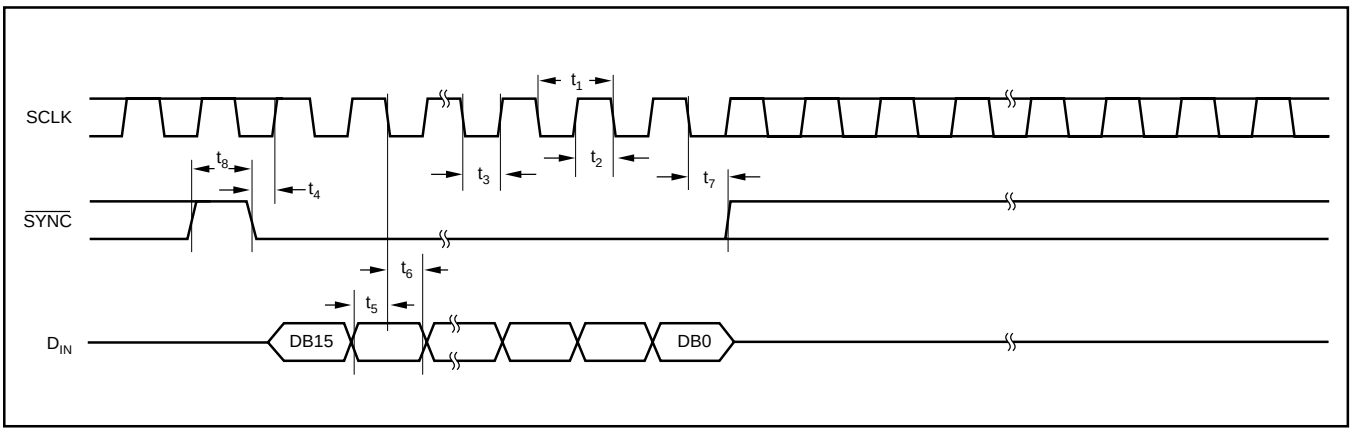
TIMING CHARACTERISTICS[1, 2]

V_{DD} = +2.7V to +5.5V; all specifications –40°C to +105°C, unless otherwise noted.

PARAMETER	DESCRIPTION	CONDITIONS	DAC7512E, N			UNITS
			MIN	TYP	MAX	
t_1[3]	SCLK Cycle Time					
		V_{DD} = 2.7V to 3.6V	50			ns
		V_{DD} = 3.6V to 5.5V	33			ns
t_2	SCLK HIGH Time					
		V_{DD} = 2.7V to 3.6V	13			ns
		V_{DD} = 3.6V to 5.5V	13			ns
t_3	SCLK LOW Time					
		V_{DD} = 2.7V to 3.6V	22.5			ns
		V_{DD} = 3.6V to 5.5V	13			ns
t_4	$\overline{SYNC}$ to SCLK Rising Edge Setup Time					
		V_{DD} = 2.7V to 3.6V	0			ns
		V_{DD} = 3.6V to 5.5V	0			ns
t_5	Data Setup Time					
		V_{DD} = 2.7V to 3.6V	5			ns
		V_{DD} = 3.6V to 5.5V	5			ns
t_6	Data Hold Time					
		V_{DD} = 2.7V to 3.6V	4.5			ns
		V_{DD} = 3.6V to 5.5V	4.5			ns
t_7	SCLK Falling Edge to $\overline{SYNC}$ Rising Edge					
		V_{DD} = 2.7V to 3.6V	0			ns
		V_{DD} = 3.6V to 5.5V	0			ns
t_8	Minimum $\overline{SYNC}$ HIGH Time					
		V_{DD} = 2.7V to 3.6V	50			ns
		V_{DD} = 3.6V to 5.5V	33			ns

NOTES: (1) All input signals are specified with $t_R = t_F$ = 5ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. (2) See Serial Write Operation timing diagram, below. (3) Maximum SCLK frequency is 30MHz at V_{DD} = +3.6V to +5.5V and 20MHz at V_{DD} = +2.7V to +3.6V.

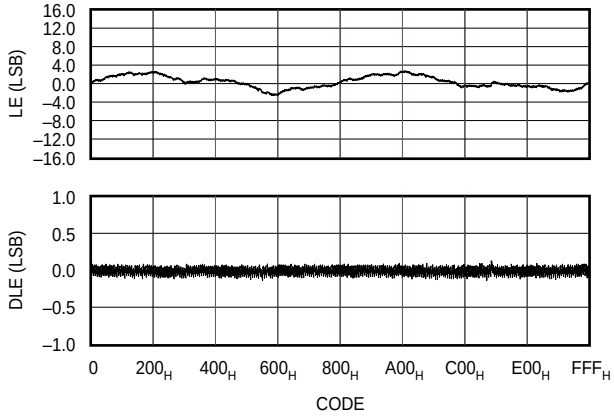
SERIAL WRITE OPERATION



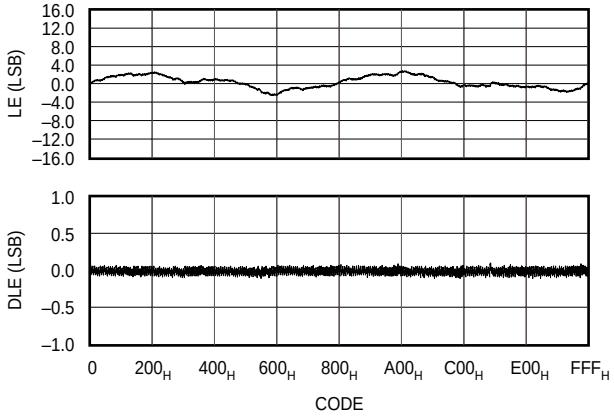
TYPICAL CHARACTERISTICS: V_{DD} = +5V

At T_A = +25°C, $+V_{DD}$ = +5V, unless otherwise noted.

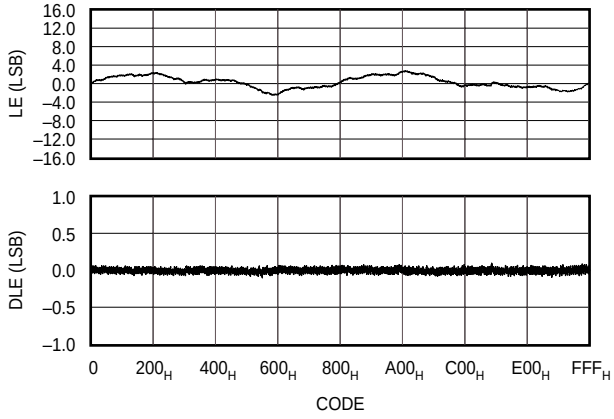
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(–40°C)



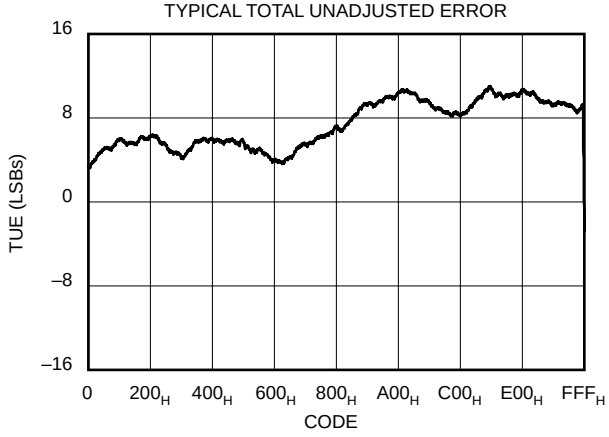
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(+25°C)



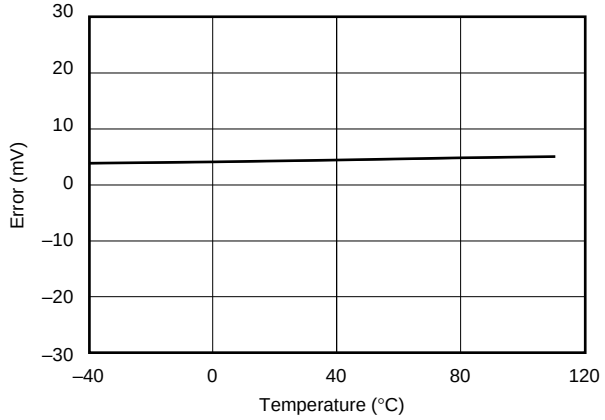
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(+105°C)



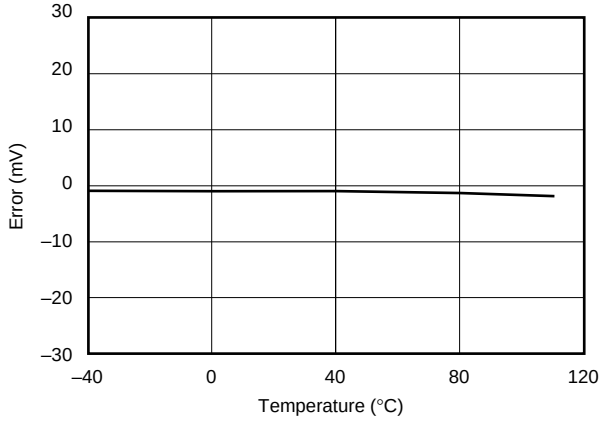
TYPICAL TOTAL UNADJUSTED ERROR



ZERO-SCALE ERROR vs TEMPERATURE

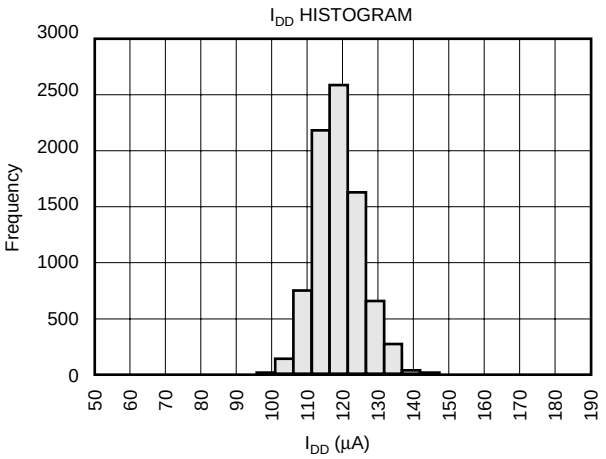


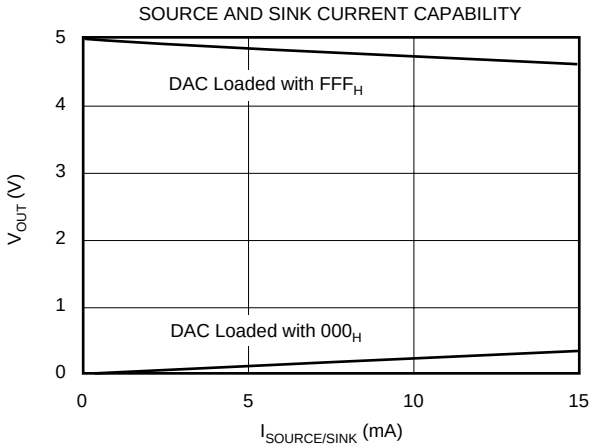
FULL-SCALE ERROR vs TEMPERATURE

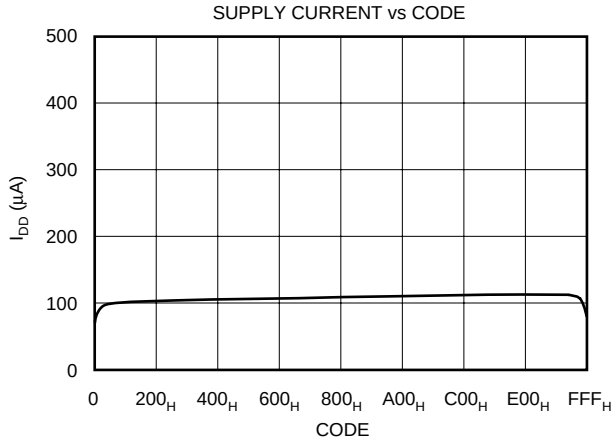


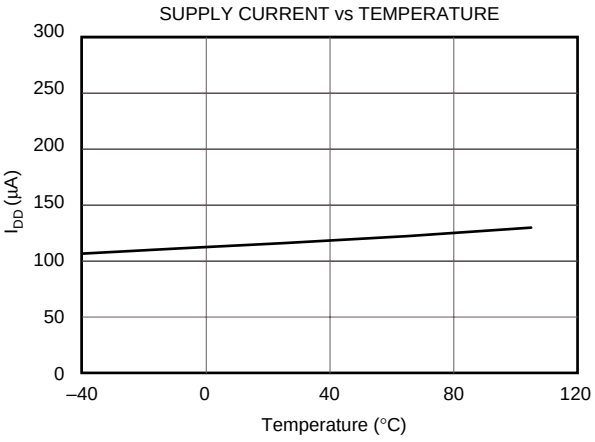
TYPICAL CHARACTERISTICS: V_{DD} = +5V (Cont.)

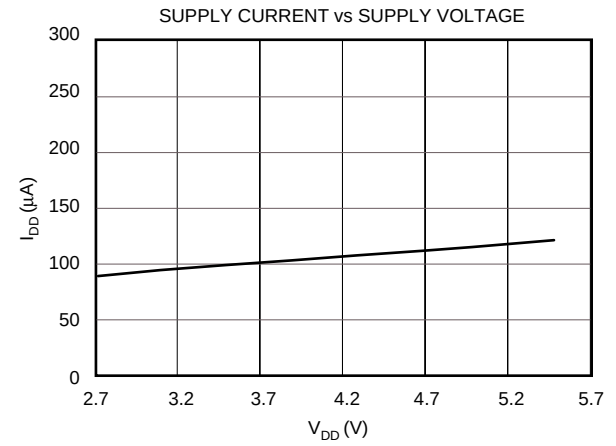
At T_A = +25°C, $+V_{DD}$ = +5V, unless otherwise noted.

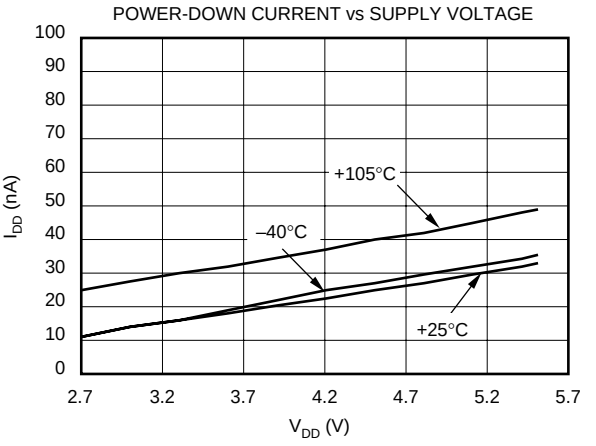








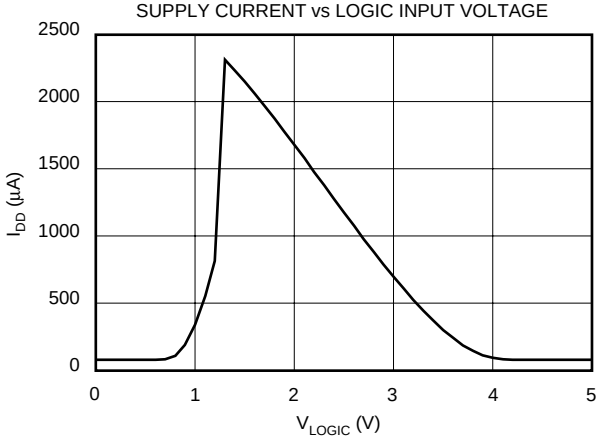




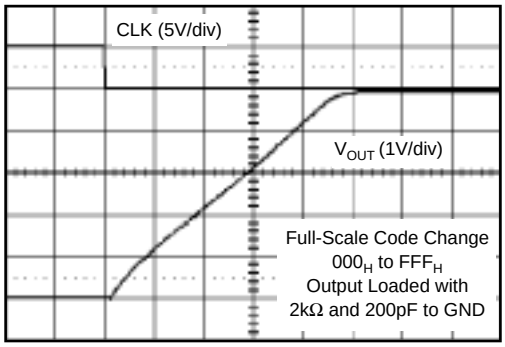
TYPICAL CHARACTERISTICS: V_{DD} = +5V (Cont.)

At T_A = +25°C, $+V_{DD}$ = +5V, unless otherwise noted.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

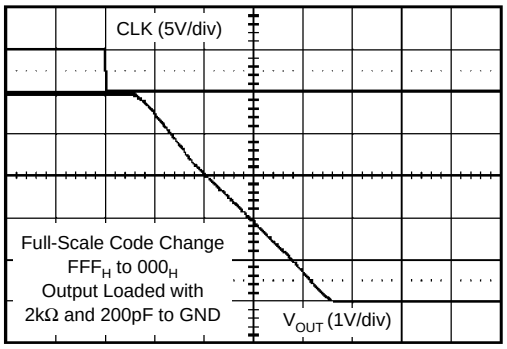


FULL-SCALE SETTLING TIME



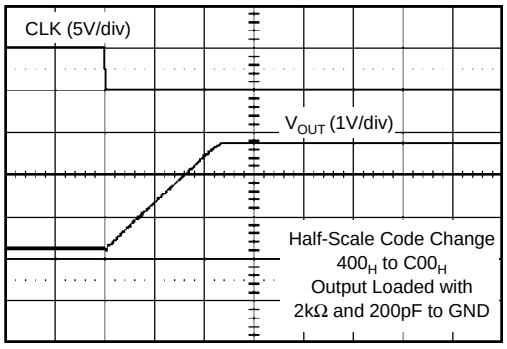
Time (1µs/div)

FULL-SCALE SETTLING TIME



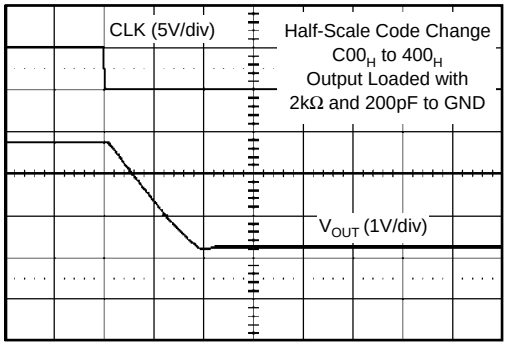
Time (1µs/div)

HALF-SCALE SETTLING TIME



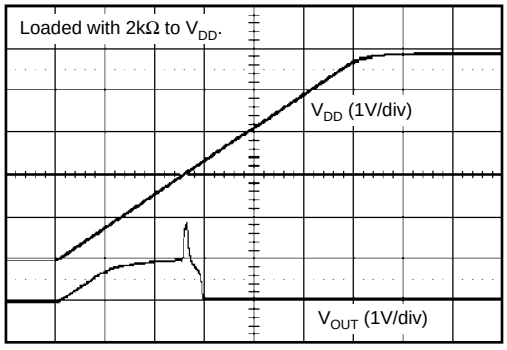
Time (1µs/div)

HALF-SCALE SETTLING TIME



Time (1µs/div)

POWER-ON RESET TO 0V

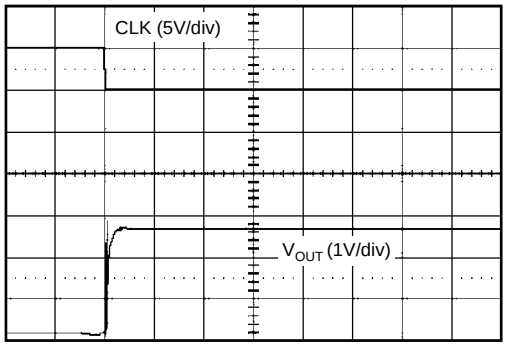


Time (20µs/div)

TYPICAL CHARACTERISTICS: V_{DD} = +5V (Cont.)

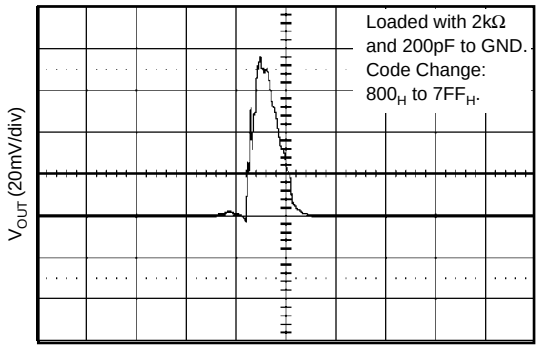
At T_A = +25°C, $+V_{DD}$ = +5V, unless otherwise noted.

EXITING POWER-DOWN
(800_H Loaded)



Time (5µs/div)

CODE CHANGE GLITCH

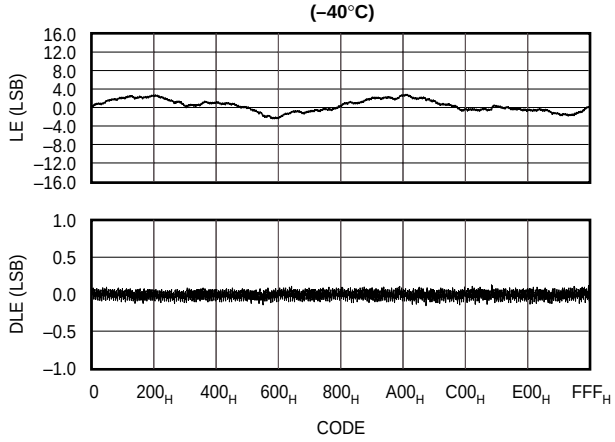


Time (0.5µs/div)

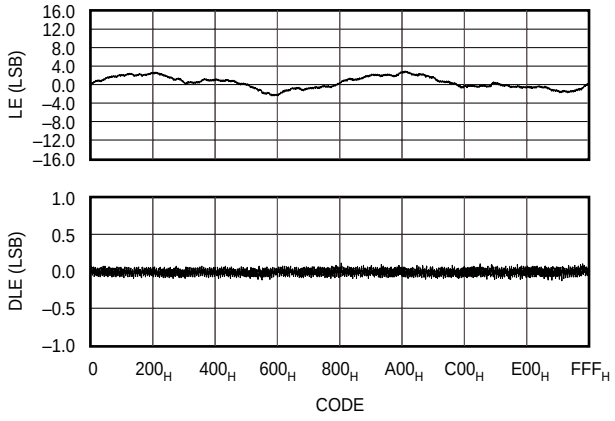
TYPICAL CHARACTERISTICS: V_{DD} = +2.7V

At T_A = +25°C, $+V_{DD}$ = +2.7V, unless otherwise noted.

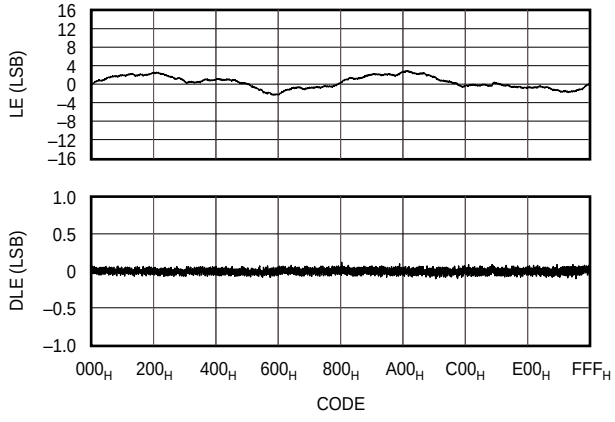
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(–40°C)



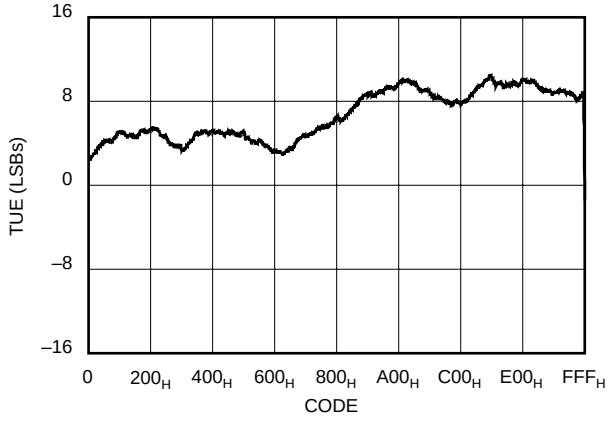
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(+25°C)



LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(+105°C)



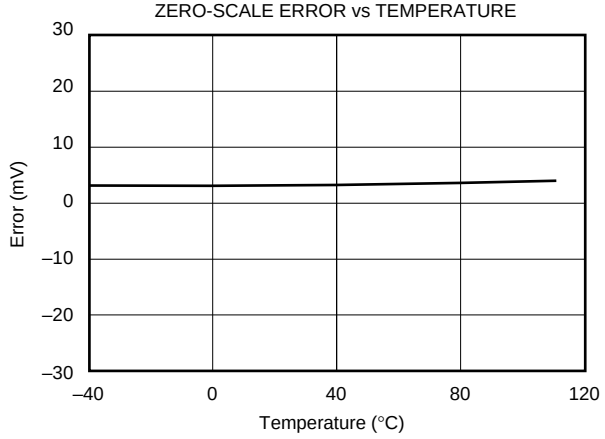
TYPICAL TOTAL UNADJUSTED ERROR



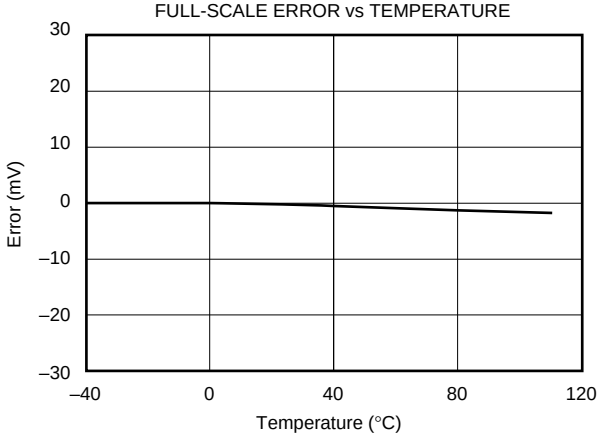
TYPICAL CHARACTERISTICS: V_{DD} = +2.7V (Cont.)

At T_A = +25°C, $+V_{DD}$ = +2.7V, unless otherwise noted.

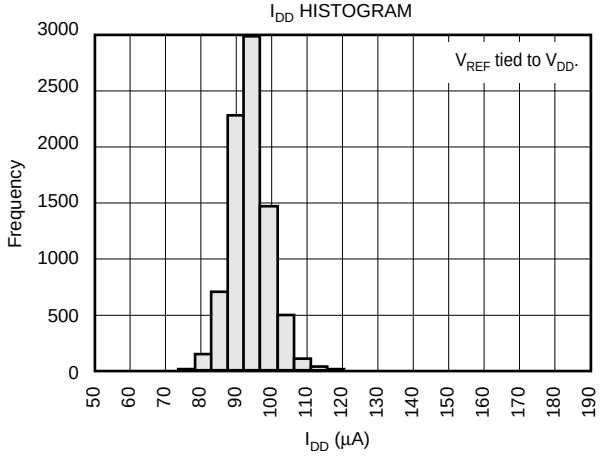
ZERO-SCALE ERROR vs TEMPERATURE



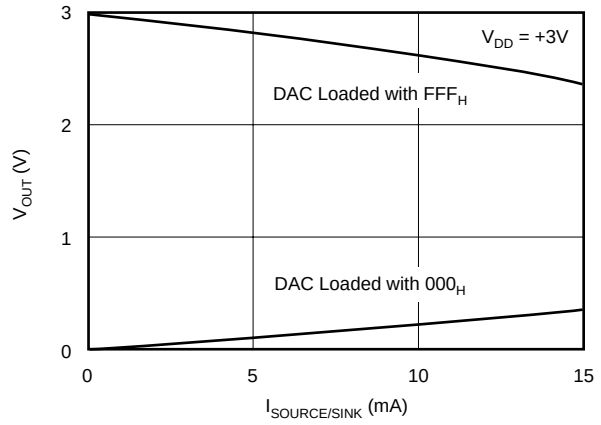
FULL-SCALE ERROR vs TEMPERATURE



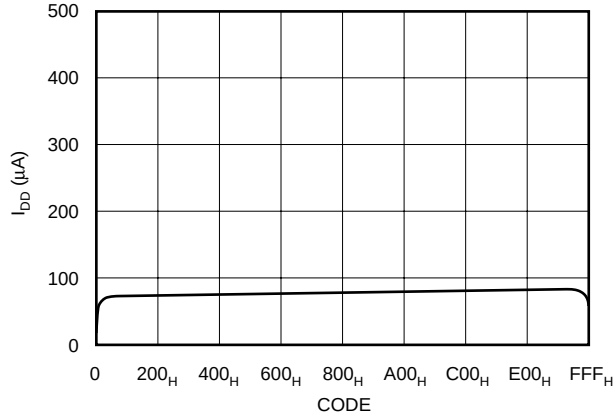
I_{DD} HISTOGRAM



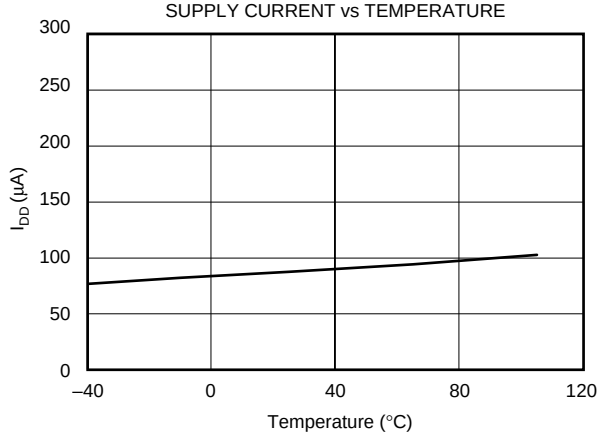
SOURCE AND SINK CURRENT CAPABILITY



SUPPLY CURRENT vs CODE



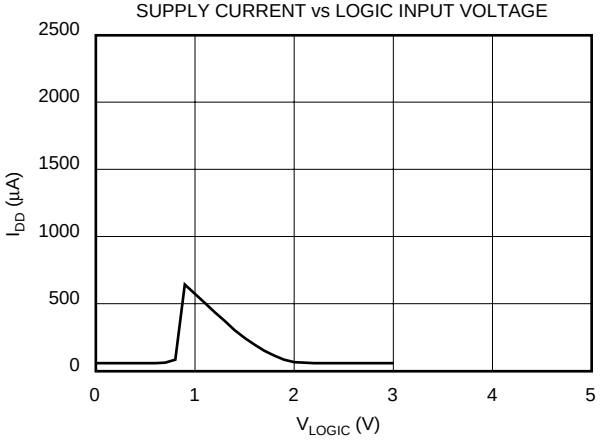
SUPPLY CURRENT vs TEMPERATURE



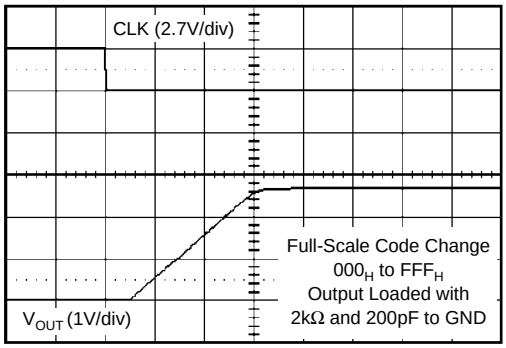
TYPICAL CHARACTERISTICS: V_{DD} = +2.7V (Cont.)

At T_A = +25°C, $+V_{DD}$ = +2.7V, unless otherwise noted.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

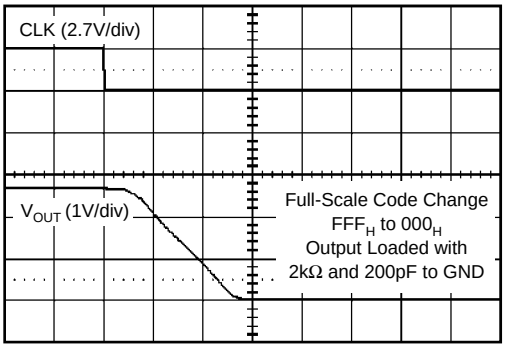


FULL-SCALE SETTLING TIME



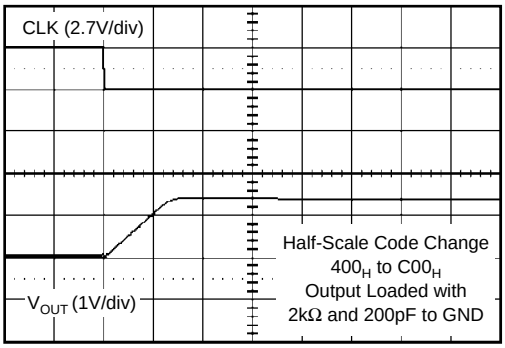
Time (1µs/div)

FULL-SCALE SETTLING TIME



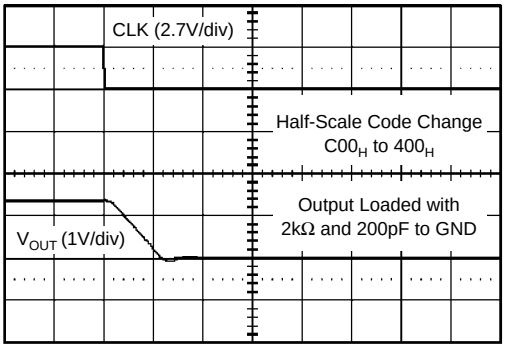
Time (1µs/div)

HALF-SCALE SETTLING TIME



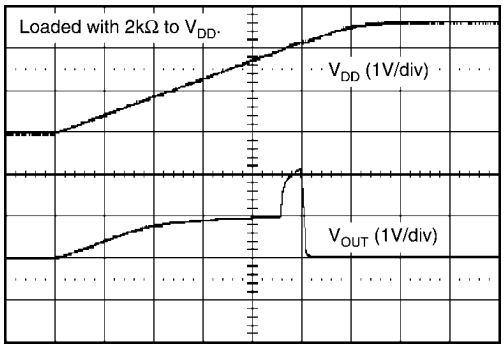
Time (1µs/div)

HALF-SCALE SETTLING TIME



Time (1µs/div)

POWER-ON RESET to 0V

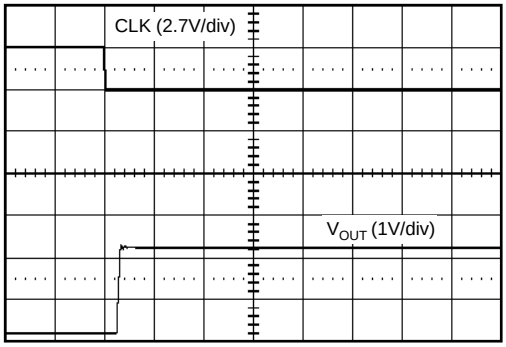


Time (20µs/div)

TYPICAL CHARACTERISTICS: V_{DD} = +2.7V (Cont.)

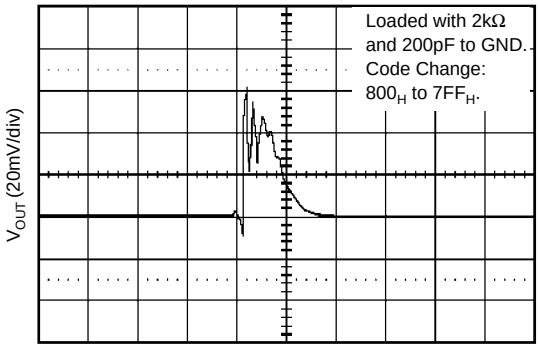
At T_A = +25°C, $+V_{DD}$ = +2.7V, unless otherwise noted.

EXITING POWER-DOWN
(800_H Loaded)



Time (5µs/div)

CODE CHANGE GLITCH



Time (0.5µs/div)

THEORY OF OPERATION

DAC SECTION

The DAC7512 is fabricated using a CMOS process. The architecture consists of a string DAC followed by an output buffer amplifier. Since there is no reference input pin, the power supply (V_{DD}) acts as the reference. Figure 1 shows a block diagram of the DAC architecture.

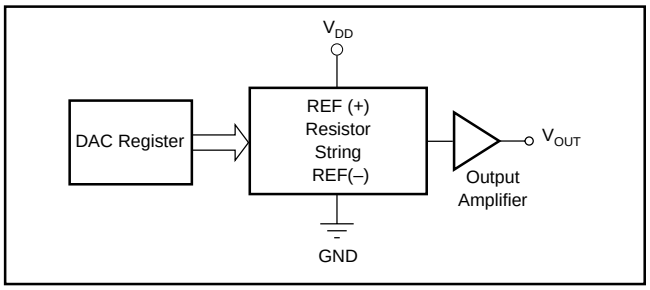


FIGURE 1. DAC7512 Architecture.

The input coding to the DAC7512 is straight binary, so the ideal output voltage is given by:

$$V_{OUT} = V_{DD} \bullet \frac{D}{4096}$$

where D = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 4095.

RESISTOR STRING

The resistor string section is shown in Figure 2. It is simply a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. It is tested monotonic because it is a string of resistors.

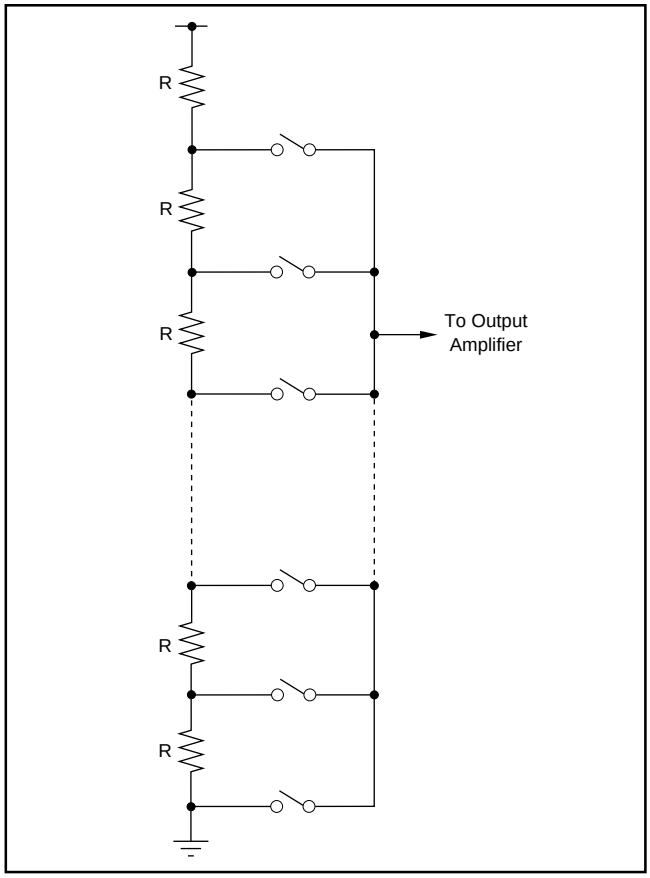


FIGURE 2. Resistor String.

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output which gives an output range of 0V to V_{DD}. It is capable of driving a load of 2kΩ in parallel with 1000pF to GND. The source and sink capabilities of the output amplifier can be seen in the typical characteristics. The slew rate is 1V/µs with a half-scale settling time of 8µs with the output unloaded.

SERIAL INTERFACE

The DAC7512 has a three-wire serial interface ($\overline{SYNC}$, SCLK, and D_{IN}), which is compatible with SPI, QSPI, and Microwire interface standards as well as most Digital Signal Processors (DSPs). See the Serial Write Operation timing diagram for an example of a typical write sequence.

The write sequence begins by bringing the $\overline{SYNC}$ line LOW. Data from the D_{IN} line is clocked into the 16-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 30MHz, making the DAC7512 compatible with high-speed DSPs. On the 16th falling edge of the serial clock, the last data bit is clocked in and the programmed function is executed (i.e., a change in DAC register contents and/or a change in the mode of operation).

At this point, the $\overline{SYNC}$ line may be kept LOW or brought HIGH. In either case, it must be brought HIGH for a minimum of 33ns before the next write sequence so that a falling edge of $\overline{SYNC}$ can initiate the next write sequence. Since the $\overline{SYNC}$ buffer draws more current when the $\overline{SYNC}$ signal is HIGH than it does when it is LOW, $\overline{SYNC}$ should be idled LOW between write sequences for lowest power operation of the part. As mentioned above, however, it must be brought HIGH again just before the next write sequence.

INPUT SHIFT REGISTER

The input shift register is 16 bits wide, as shown in Figure 3. The first two bits are “don’t cares”. The next two bits (PD1 and PD0) are control bits that control which mode of operation the part is in (normal mode or one of three power-down modes). There is a more complete description of the various modes in the Power-Down Modes section. The next 12 bits are the data bits. These are transferred to the DAC register on the 16th falling edge of SCLK.

$\overline{SYNC}$ INTERRUPT

In a normal write sequence, the $\overline{SYNC}$ line is kept LOW for at least 16 falling edges of SCLK and the DAC is updated on the 16th falling edge. However, if $\overline{SYNC}$ is brought HIGH before the 16th falling edge, this acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents or a change in the operating mode occurs, as shown in Figure 4.

POWER-ON RESET

The DAC7512 contains a power-on reset circuit that controls the output voltage during power-up. On power-up, the DAC register is filled with zeros and the output voltage is 0V; it remains there until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

POWER-DOWN MODES

The DAC7512 contains four separate modes of operation. These modes are programmable by setting two bits (PD1 and PD0) in the control register. Table I shows how the state of the bits corresponds to the mode of operation of the device.

DB13	DB12	OPERATING MODE
0	0	Normal Operation
		Power-Down Modes:
0	1	Output 1kΩ to GND
1	0	Output 100kΩ to GND
1	1	High-Z

TABLE I. Modes of Operation for the DAC7512.

When both bits are set to 0, the part works normally with its normal power consumption of 135µA at 5V. However, for the three power-down modes, the supply current falls to 200nA at 5V (50nA at 3V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. There are three different options. The output is connected internally to GND through a 1kΩ resistor, a 100kΩ resistor, or it is left open-circuited (High-Z). See Figure 5 for the output stage.

DB15															DB0
X	X	PD1	PD0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

FIGURE 3. Data Input Register.

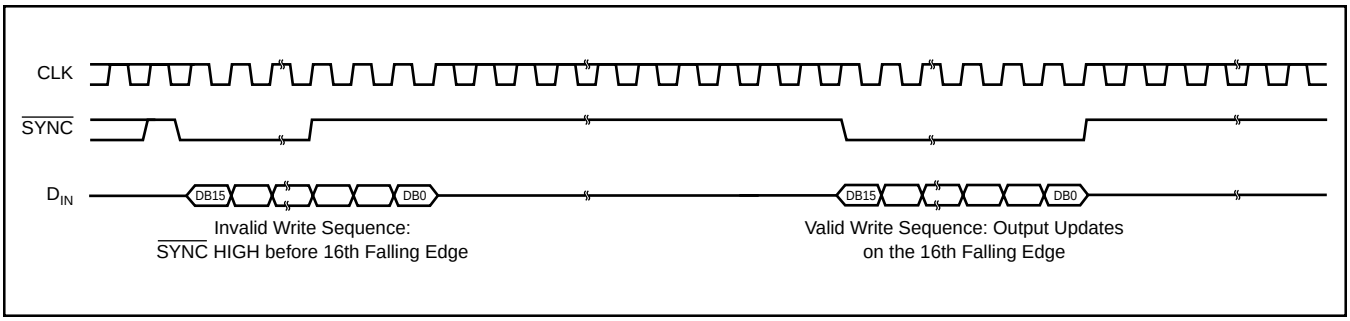


FIGURE 4. $\overline{SYNC}$ Interrupt Facility.

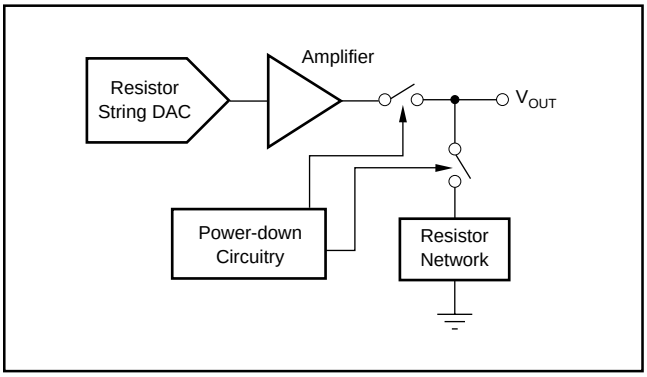


FIGURE 5. Output Stage During Power-Down.

All linear circuitry is shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 2.5µs for V_{DD} = 5V and 5µs for V_{DD} = 3V. See the Typical Characteristics for more information.

MICROPROCESSOR INTERFACING

DAC7512 TO 8051 INTERFACE

Figure 6 shows a serial interface between the DAC7512 and a typical 8051-type microcontroller. The setup for the interface is as follows: TXD of the 8051 drives SCLK of the DAC7512, while RXD drives the serial data line of the part. The $\overline{SYNC}$ signal is derived from a bit programmable pin on the port. In this case, port line P3.3 is used. When data is to be transmitted to the DAC7512, P3.3 is taken LOW. The 8051 transmits data only in 8-bit bytes; thus only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left LOW after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken HIGH following the completion of this cycle. The 8051 outputs the serial data in a format which has the LSB first. The DAC7512 requires its data with the MSB as the first bit received. The 8051 transmit routine must therefore take this into account, and "mirror" the data as needed.

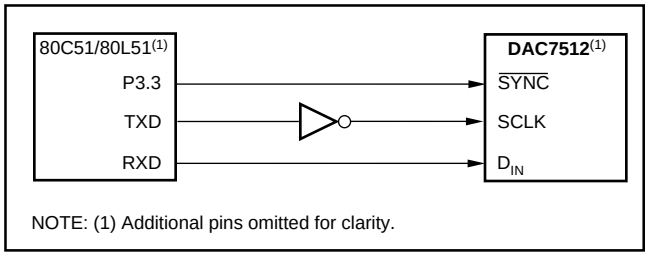


FIGURE 6. DAC7512 to 80C51/80L51 Interface.

DAC7512 TO MICROWIRE™ INTERFACE

Figure 7 shows an interface between the DAC7512 and any Microwire compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the DAC7512 on the rising edge of the SK signal.

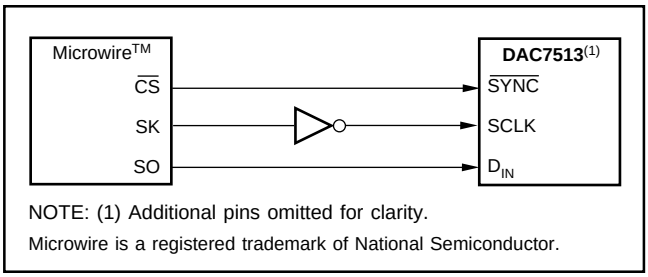


FIGURE 7. DAC7512 to Microwire Interface.

DAC7512 TO 68HC11 INTERFACE

Figure 8 shows a serial interface between the DAC7512 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DAC7512, while the MOSI output drives the serial data line of the DAC. The $\overline{SYNC}$ signal is derived from a port line (PC7), similar to what was done for the 8051.

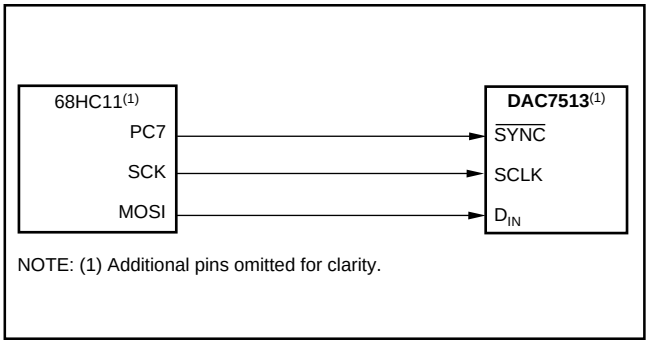


FIGURE 8. DAC7512 to 68HC11 Interface.

The 68HC11 should be configured so that its CPOL bit is a 0 and its CPHA bit is a 1. This configuration causes data appearing on the MOSI output is valid on the falling edge of SCK. When data is being transmitted to the DAC, the $\overline{SYNC}$ line is taken LOW (PC7). Serial data from the 68HC11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. In order to load data to the DAC7512, PC7 is left LOW after the first eight bits are transferred, and a second serial write operation is performed to the DAC and PC7 is taken HIGH at the end of this procedure.

APPLICATIONS

USING REF02 AS A POWER SUPPLY FOR THE DAC7512

Due to the extremely low supply current required by the DAC7512, an alternative option is to use a REF02 +5V precision voltage reference to supply the required voltage to the part, see Figure 9. This is especially useful if the power supply is too noisy or if the system supply voltages are at some value other than 5V. The REF02 will output a steady supply voltage for the DAC7512. If the REF02 is used, the current it needs to supply to the DAC7512 is 135µA. This is with no load on the output of the DAC. When the DAC output

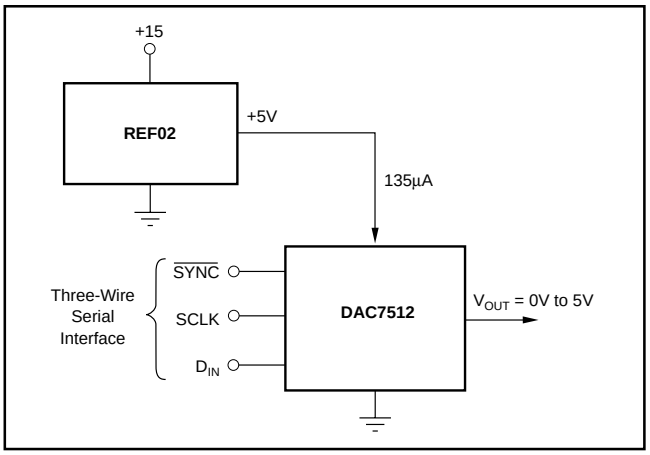


FIGURE 9. REF02 as Power Supply to DAC7512.

is loaded, the REF02 also needs to supply the current to the load. The total current required (with a 5kΩ load on the DAC output) is:

$$135\mu A + (5V/5k\Omega) = 1.14mA$$

The load regulation of the REF02 is typically 0.005%/mA, which results in an error of 285µV for the 1.14mA current drawn from it. This corresponds to a 0.2LSB error.

BIPOLAR OPERATION USING THE DAC7512

The DAC7512 has been designed for single-supply operation but a bipolar output range is also possible using the circuit in Figure 10. The circuit shown will give an output voltage range of ±5V. Rail-to-rail operation at the amplifier output is achievable using an OPA340 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = \left[V \bullet \left(\frac{D}{4096}\right) \bullet \left(\frac{R_1 + R_2}{R_1}\right) - V_{DD} \bullet \left(\frac{R_2}{R_1}\right)\right]$$

where D represents the input code in decimal (0 - 4095).

With V_{DD} = 5V, $R_1 = R_2$ = 10kΩ:

$$V_O = \left(\frac{10 \bullet D}{4096}\right) - 5V$$

This is an output voltage range of ±5V with 000_H corresponding to a –5V output and FFF_H corresponding to a +5V output.

LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

As the DAC7512 offers single-supply operation, it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it will be to achieve good performance from the converter.

Due to the single ground pin of the DAC7512, all return currents, including digital and analog return currents, must flow through the GND pin. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power entry point of the system.

The power applied to V_{DD} should be well regulated and low noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. This is particularly true for the DAC7512, as the power supply is also the reference voltage for the DAC.

As with the GND connection, V_{DD} should be connected to a +5V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. In addition, the 1µF to 10µF and 0.1µF bypass capacitors are strongly recommended. In some situations, additional bypassing may be required, such as a 100µF electrolytic capacitor or even a “Pi” filter made up of inductors and capacitors—all designed to essentially low-pass filter the +5V supply, removing the high-frequency noise.

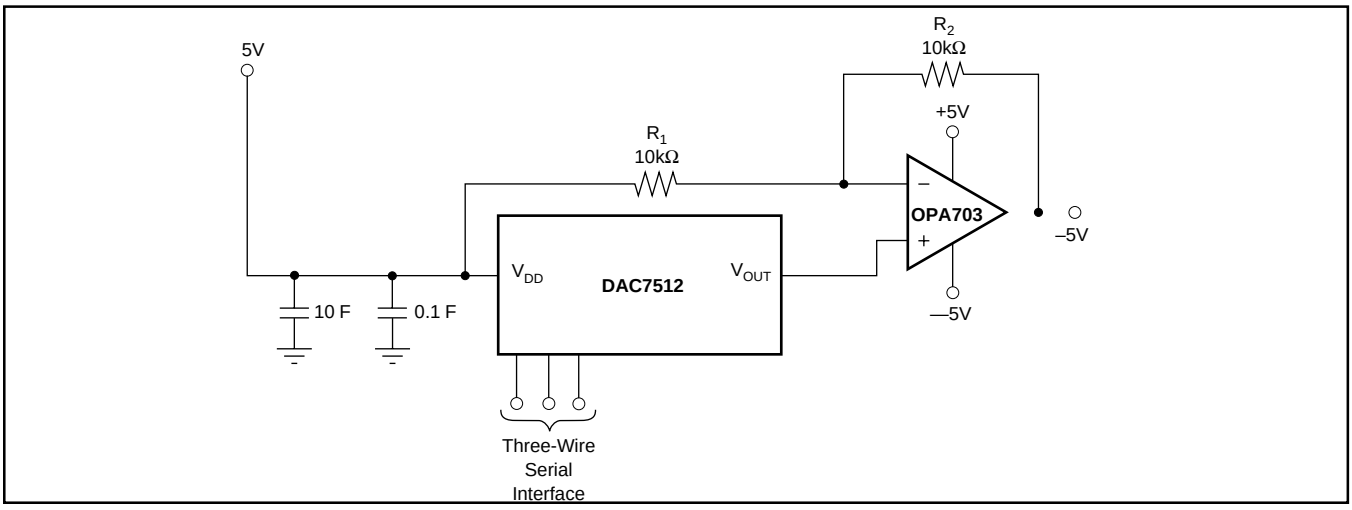
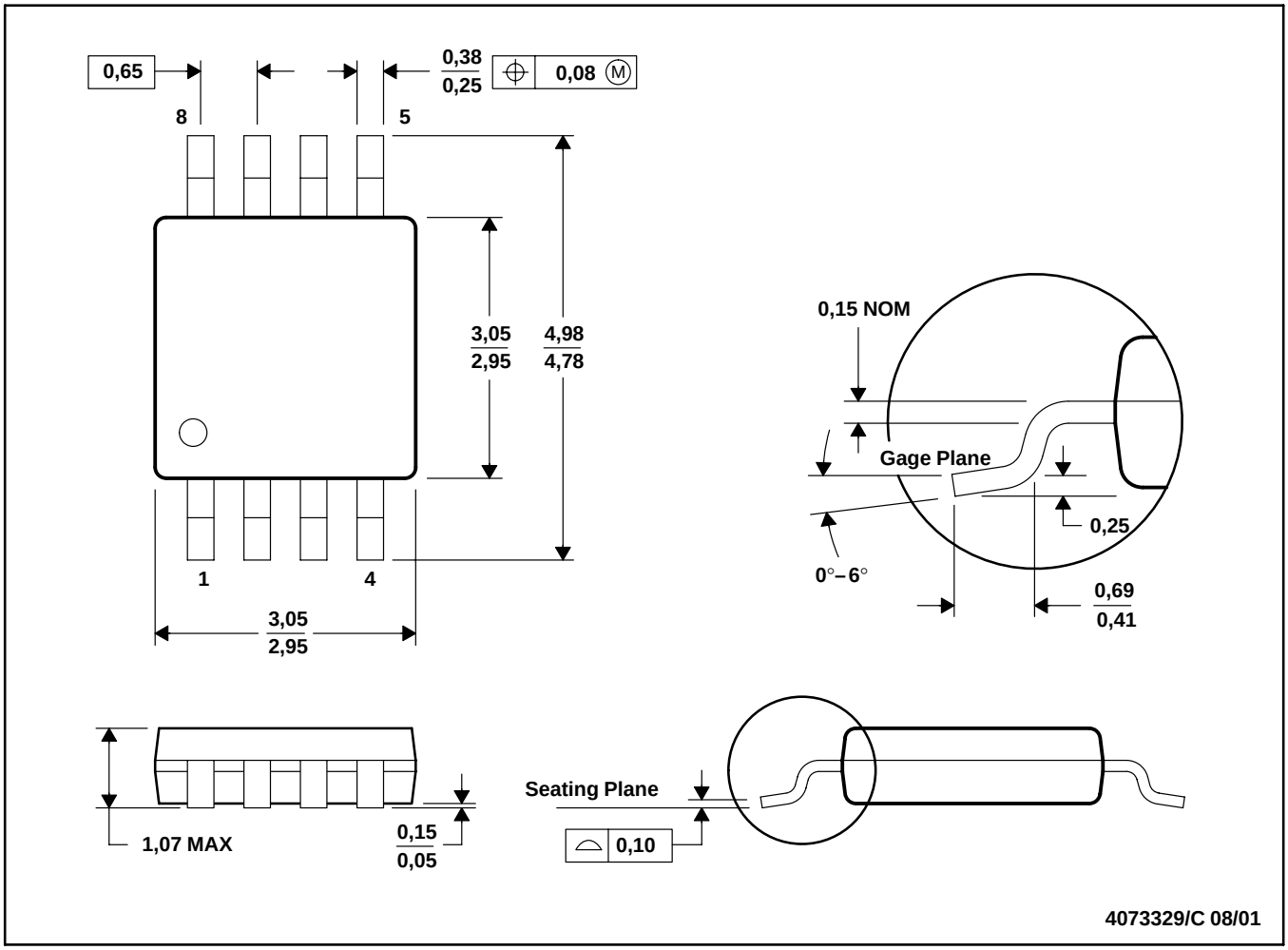


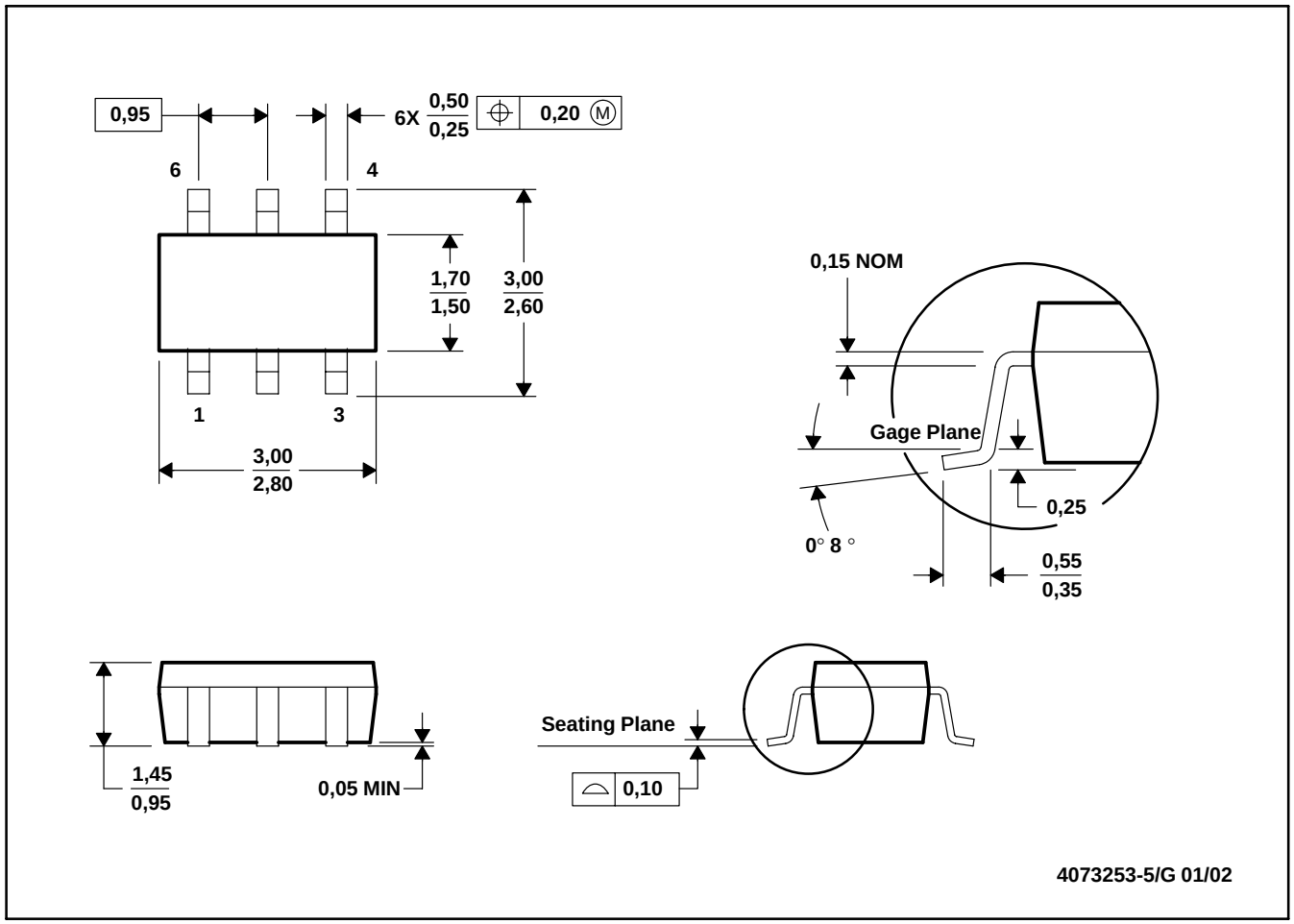
FIGURE 10. Bipolar Operation with the DAC7512.

DGK (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187

DBV (R-PDSO-G6) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Leads 1, 2, 3 may be wider than leads 4, 5, 6 for package orientation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7512E/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	D12E	Samples
DAC7512E/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	D12E	Samples
DAC7512E/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	D12E	Samples
DAC7512N/250	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	D12N	Samples
DAC7512N/250G4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	D12N	Samples
DAC7512N/3K	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	D12N	Samples
DAC7512N/3KG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	D12N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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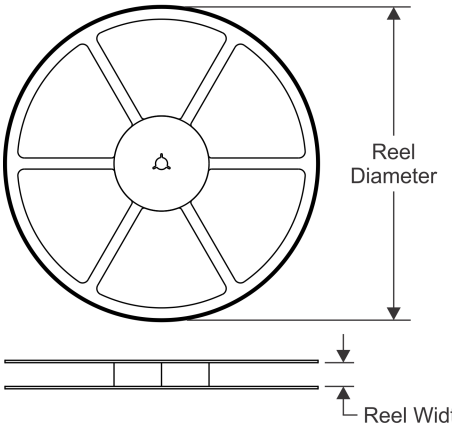
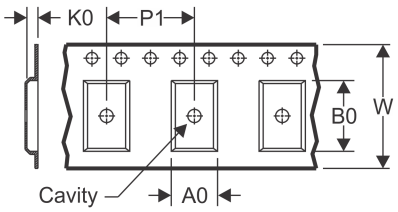
TAPE AND REEL INFORMATION

REEL DIMENSIONS

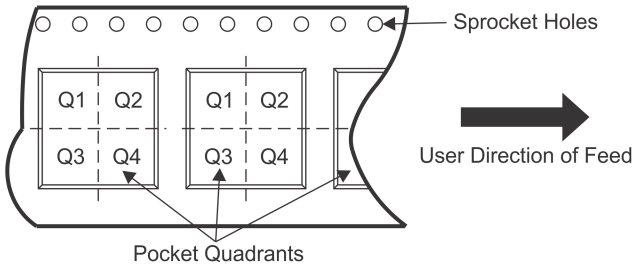


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

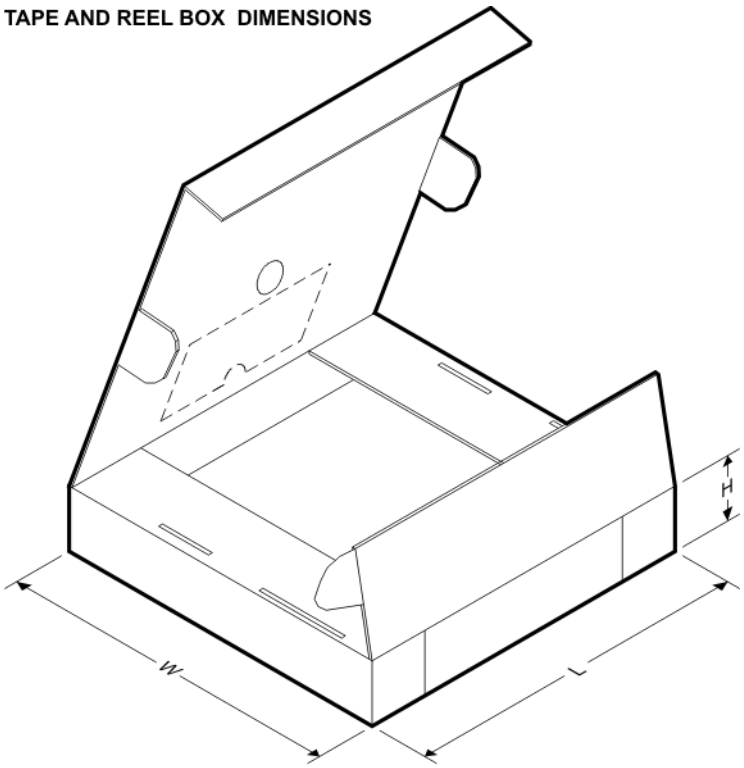
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7512E/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC7512E/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC7512N/250	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
DAC7512N/3K	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

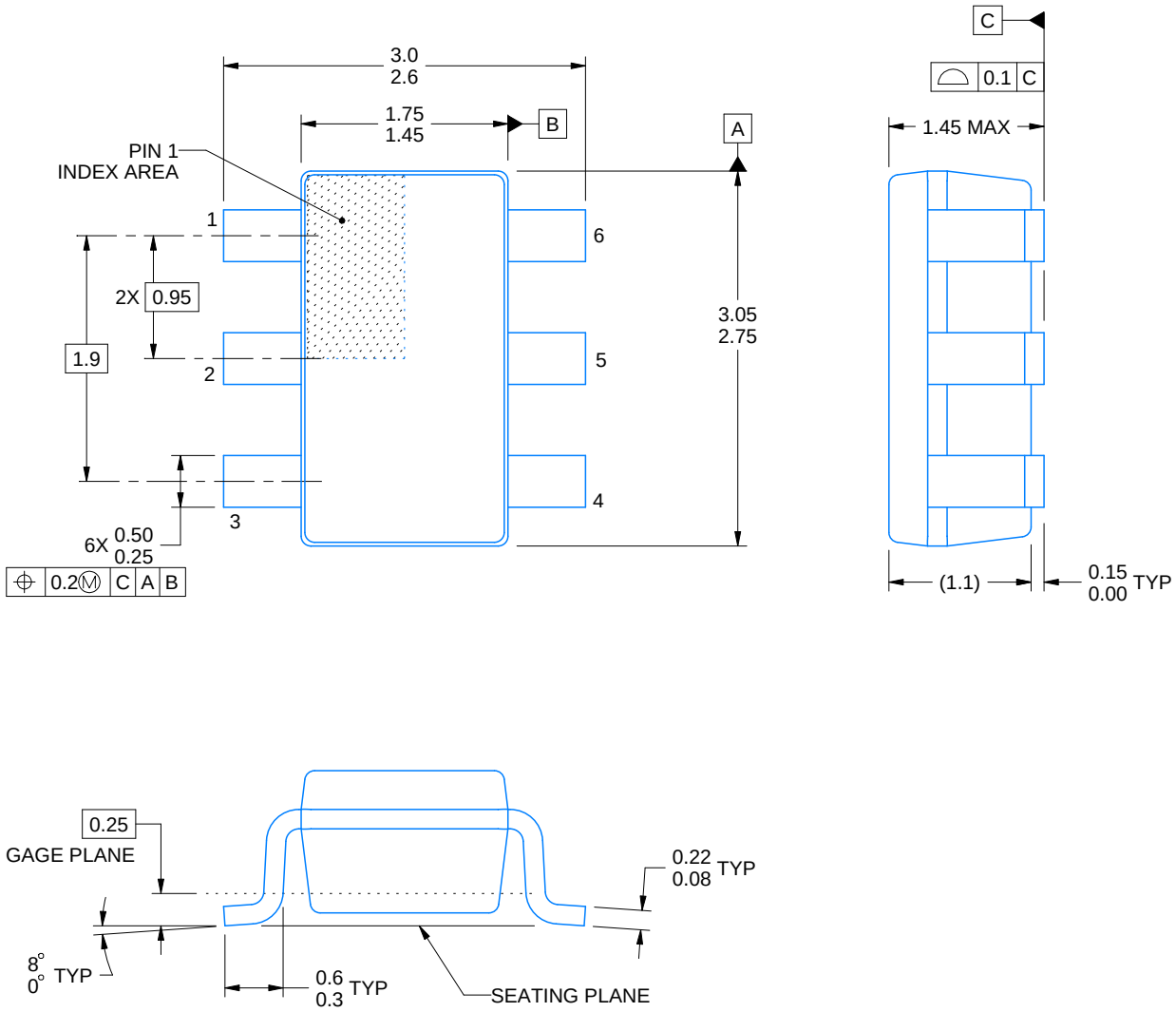
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7512E/250	VSSOP	DGK	8	250	210.0	185.0	35.0
DAC7512E/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0
DAC7512N/250	SOT-23	DBV	6	250	180.0	180.0	18.0
DAC7512N/3K	SOT-23	DBV	6	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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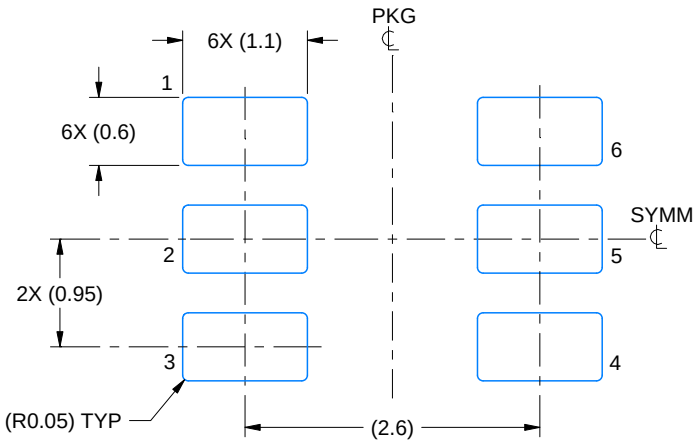
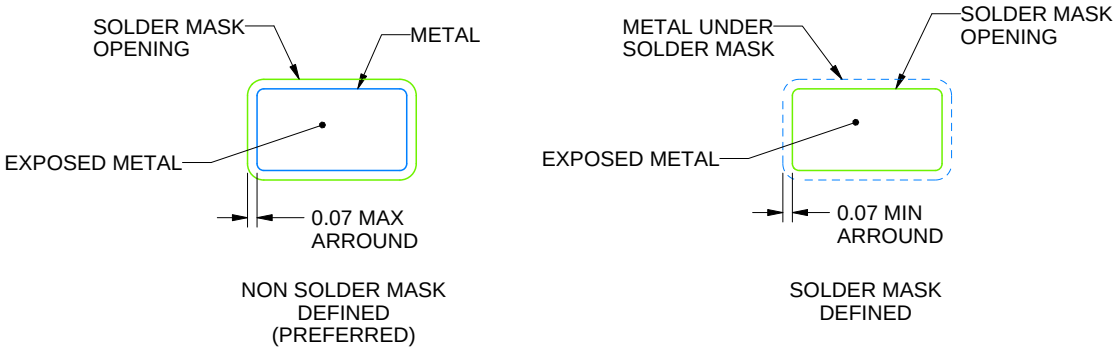
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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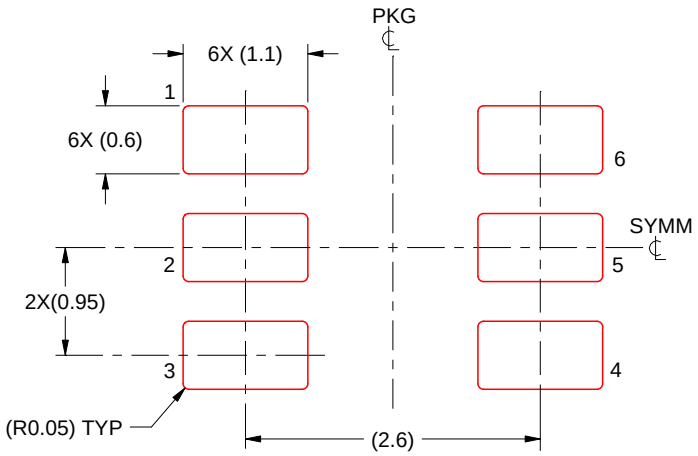
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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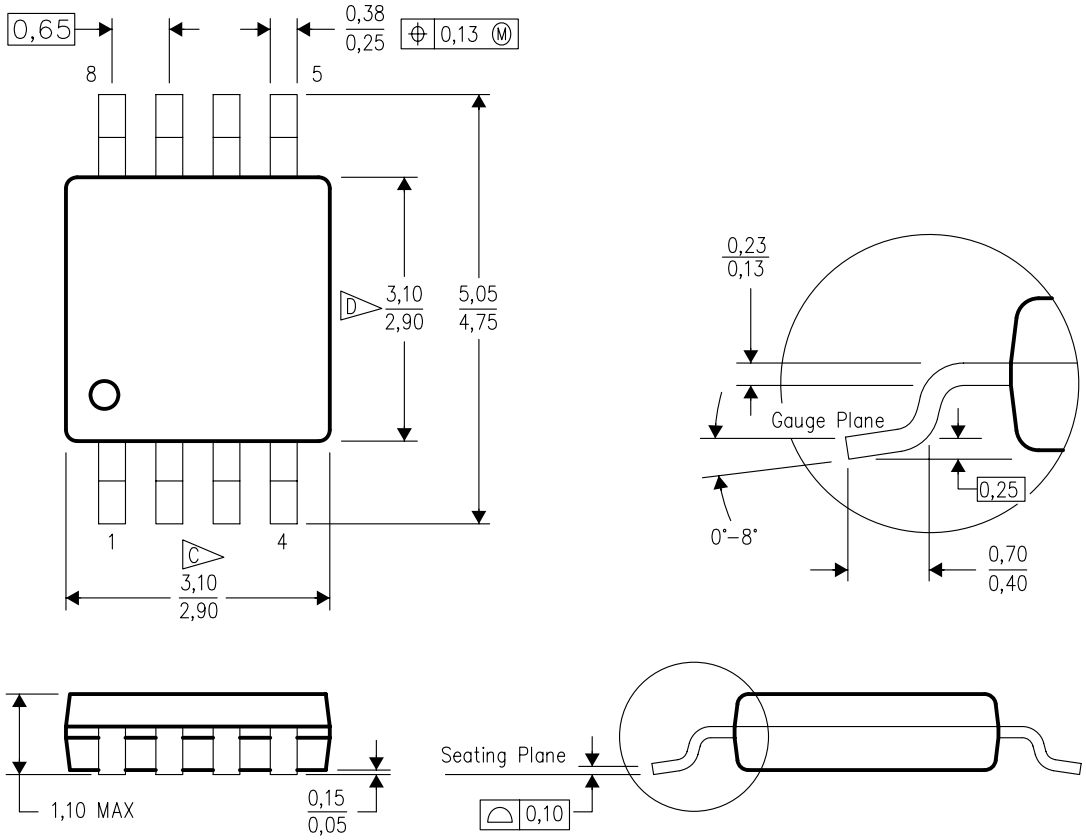
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

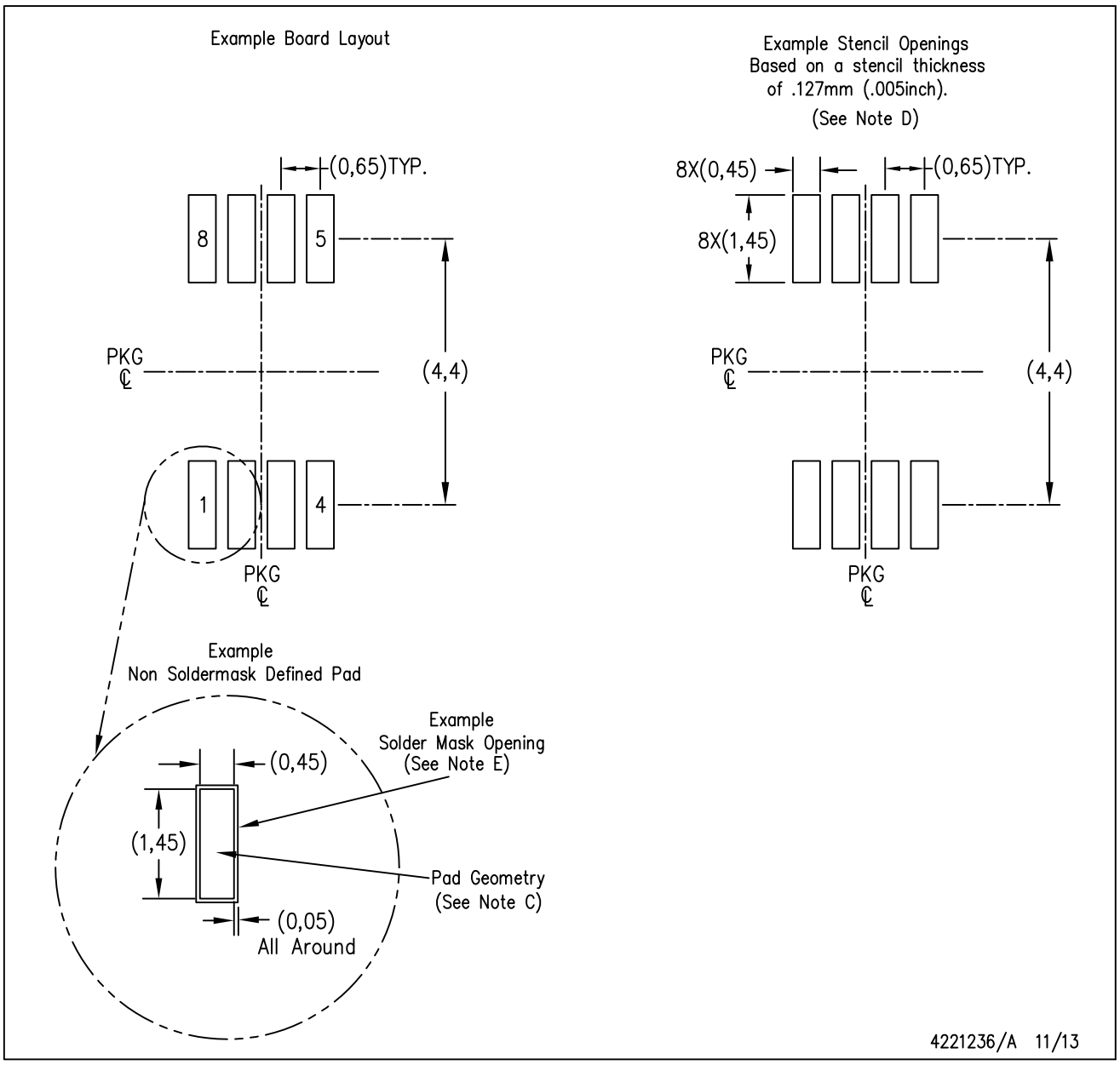
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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