DAC3283

This is the user's guide for the DAC328x EVM. The EVM includes the TRF372017 quadrature modulator to facilitate measuring the output signals at a desired RF frequency. The TRF372017 includes an integrated RF synthesizer used for the LO. The EVM also includes the CDCE62005 clocking source which provides the clocks required for the DAC, the pattern generator, and the synthesizer reference of the RF modulator. This EVM is ideally suited for mating with the TSW3100 pattern generation card for evaluating WCDMA, LTE, or other high-performance modulation schemes.

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1 EVM Block Diagram

Figure 1 shows the configuration of the EVM with the TSW3100 used for the pattern generation.

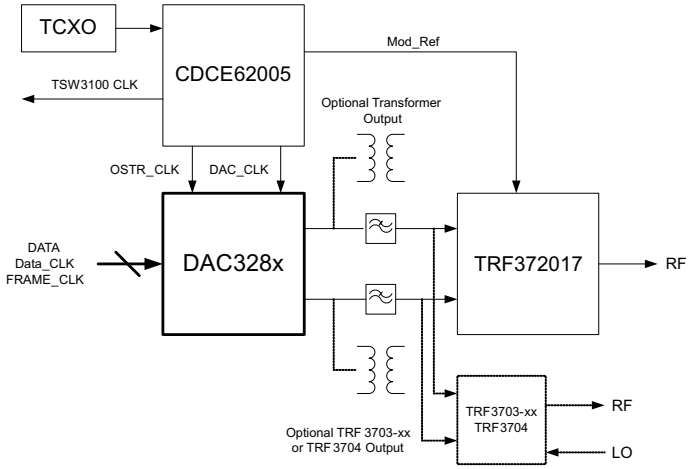


Figure 1. EVM Block Diagram

2 Software Control

2.1 Installation Instructions

1. Open folder named DAC328x_Installer_vxpx (xpx represents the latest version)
2. Run Setup.exe
3. Follow the on-screen instructions
4. Once installed, launch by clicking on the DAC328x_GUI_vxpx program in Start >Texas Instruments DACs.
5. When plugging in the USB cable for the first time, you will be prompted to install the USB drivers.

   (a) When a pop-up screen opens, select *Continue Downloading*.
   (b) Follow the on-screen instructions to install the USB drivers.
   (c) If needed, you can access the drivers directly in the install directory.

2.2 Software Operation

The software allows programming control of the DAC device, the CDC device, and the TRF device. The front panel provides a tab for full programming of each device. The Top Level tab provides a more convenient and simplified interface to the most used registers of each device. The Top Level panel of the software is shown in Figure 2.

2.2.1 DAC328x

- Interpolation: Sets the DAC interpolation factor
- DAC Gain: Adjusts the DAC gain for each channel
- Mixer: Selects the DAC mixer
- Temperature: Reads the temperature sensor inside the DAC device

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2.2.2 CDCE62005

Frequency control is determined by register values in the CDC tab. See the CDCE62005 data sheet for detailed explanations of the register configuration to change the clock frequency. Sample configuration files are provided with a variety of common clock frequency choices that can be loaded automatically (see Load Regs). The Top Level tab gives access to the dividers for each of the outputs.

- Mod Ref In Div: The divider register to set the RF synthesizer reference frequency in the TRF372017
- DAC Clock Div: The divider register to set the DAC clock frequency
- FIFO OSTR Div: The divider register that sets the FIFO output strobe clock.
  - FIFO OSTR Div = 8 × Interpolation × DAC clock divider
- TSW3100 Clk Div: The divider register that sets the clock for the TSW3100 pattern generator card
  - TSW3100 Clk Div = 8 × Interpolation × DAC clock divider / 4 {BwDDR}
- Test Port Div The divider register that sets the clock to the SMA test port

2.2.3 TRF372017

- Ref Freq (MHz): Shows the reference frequency for the synthesizer. This is automatically generated from the CDC register.
- LO Target (MHz): Sets the LO target frequency
- RF Step (MHz): Sets the synthesizer pfd frequency which determines the synthesizer resolution

2.2.4 Register Control

- Send All: Sends the register configuration to all devices
- Read All: Reads register configuration from DAC328x device
- Save Regs: Saves the register configuration for all devices
- Load Regs: Load a register file for all devices. Sample configuration files for common frequency plans are located in the install directory.
  - Select *Load Regs* button.
  - Double click on the *data* folder.
  - Double click on the desired register file.
  - Click on *Send All* to ensure all of the values are loaded properly.

2.2.5 Miscellaneous Settings

- Reset USB: Toggle this button if the USB port is not responding. This generates a new USB handle address
- Initialize: This button toggles the *Wake up* button for the CDC device and the *Cal Enable* device for the TRF372017 device
- Exit: Stops the program
- Fin (MHz): Shows the system reference frequency from the onboard TCXO; this does not need to be adjusted.
- Out Freq (MHz): Shows the VCO output frequency from the CDC device. This frequency is changed by adjusting the appropriate register configuration in the CDC tab or by loading a different configuration file.

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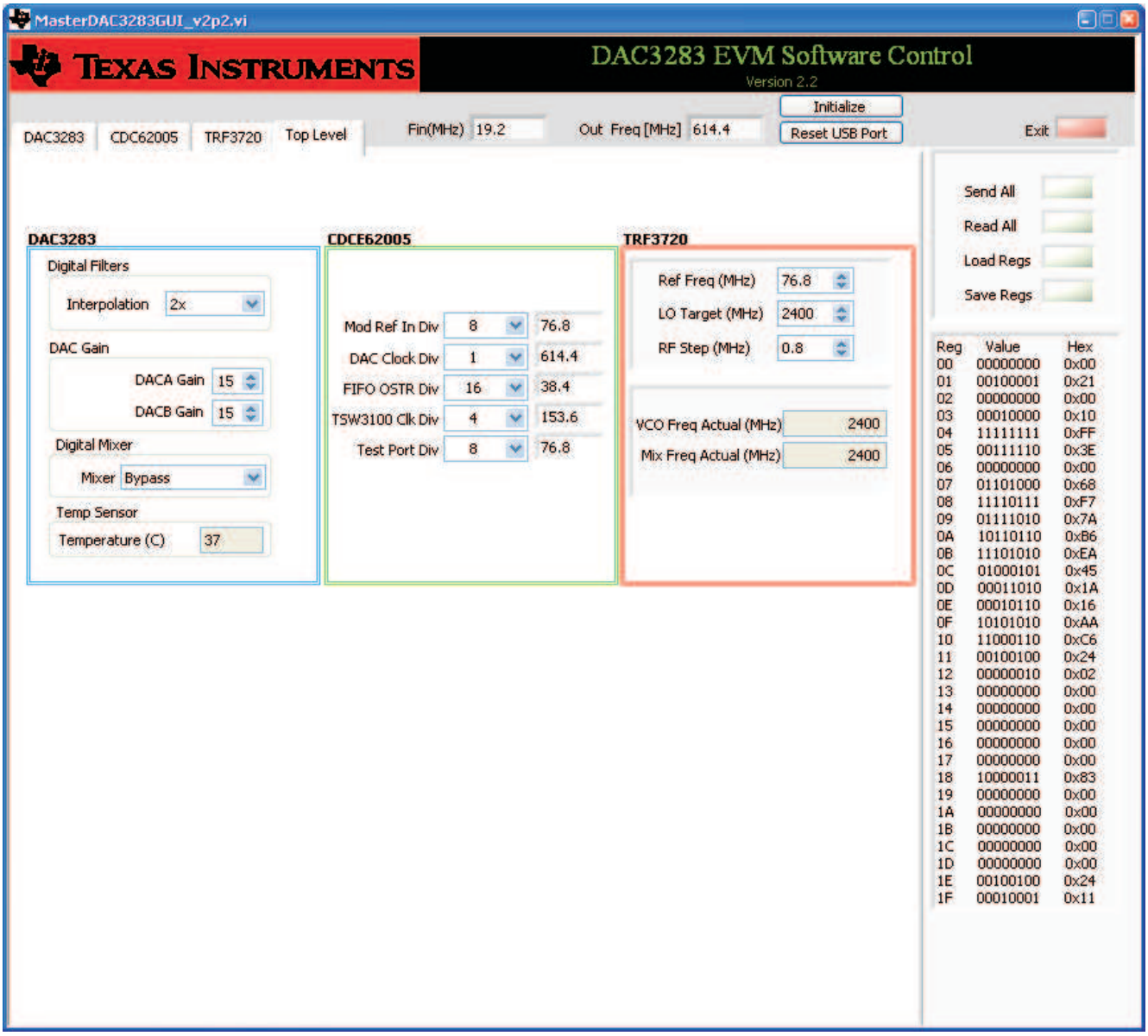


Figure 2. DAC3283 GUI Front Panel

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3 Basic Test Procedure

This section outlines the basic test procedure for testing the EVM.

3.1 Test Block Diagram

The test setup for general testing of the DAC328x with the TSW3100 pattern generation card is shown in Figure 3.

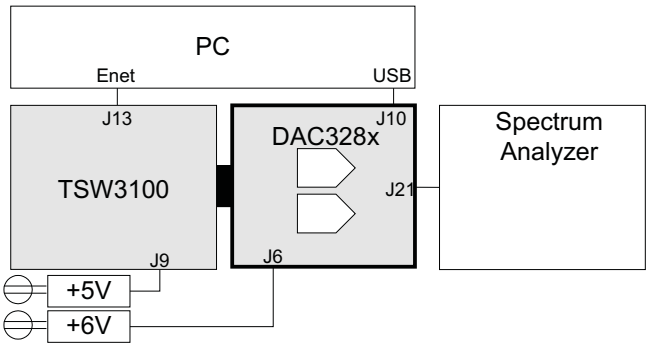


Figure 3. Test Setup Block Diagram

3.2 Test Setup Connection

1. Connect DAC328x EVM to TSW3100 EVM
2. Connect 6-V power-supply jack
3. Connect RF output to Spectrum Analyzer
4. Connect USB cable to programming computer

3.3 TSW3100 Quick-Start Operation

See the TSW3100 User's Guide for more detailed explanations of the TSW3100 setup and operation. This document assumes the TSW3100 software is installed and functioning properly. The DAC328x uses byte-wide DDR operation; hence, TSW3100 operating software version 2.2 or later is required. Also, the DAC328x can operate at higher data rates, so verify that the oscillator on the TSW3100 at Y3 is operating at 125 MHz to support the data rates above 250 MHz. The front panel of the TSW3100 is shown in Figure 4 and Figure 5. The following registers must be changed from the default settings.

Multitone Setup From Default Configuration

1. Change sample rate to equal DAC clock rate / Interpolation (i.e., 614.4 / 2 = 307.2).
2. Select desired tone groups (i.e., group 1: tone center = 20, group 2: tone center = 21)
3. Select BwDDR output button
4. Check the *LOAD and Run* box
5. Press the green *Create and Save/Run TSW3100* button

CommsSignalPattern Setup From Default Configuration (WCDMA)

1. Change Interpolation value to (DAC clock rate / Interpolation) / 3.84 [i.e., (614.4 / 2) / 3.84 = 80]
2. Enter desired offset frequency (i.e., 30 MHz) for each desired carrier
3. Select the BwDDR output button
4. Check the *LOAD and Run* box
5. Press the green *Create* button

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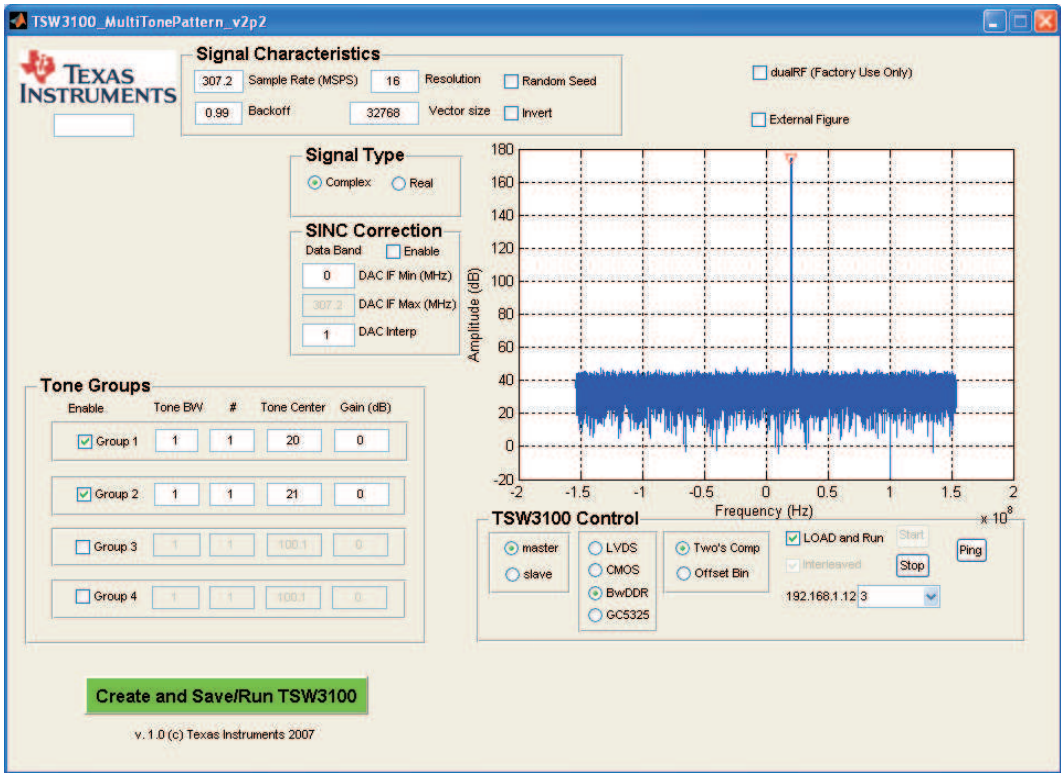


Figure 4. TSW3100 MultiTonePattern Programming GUI

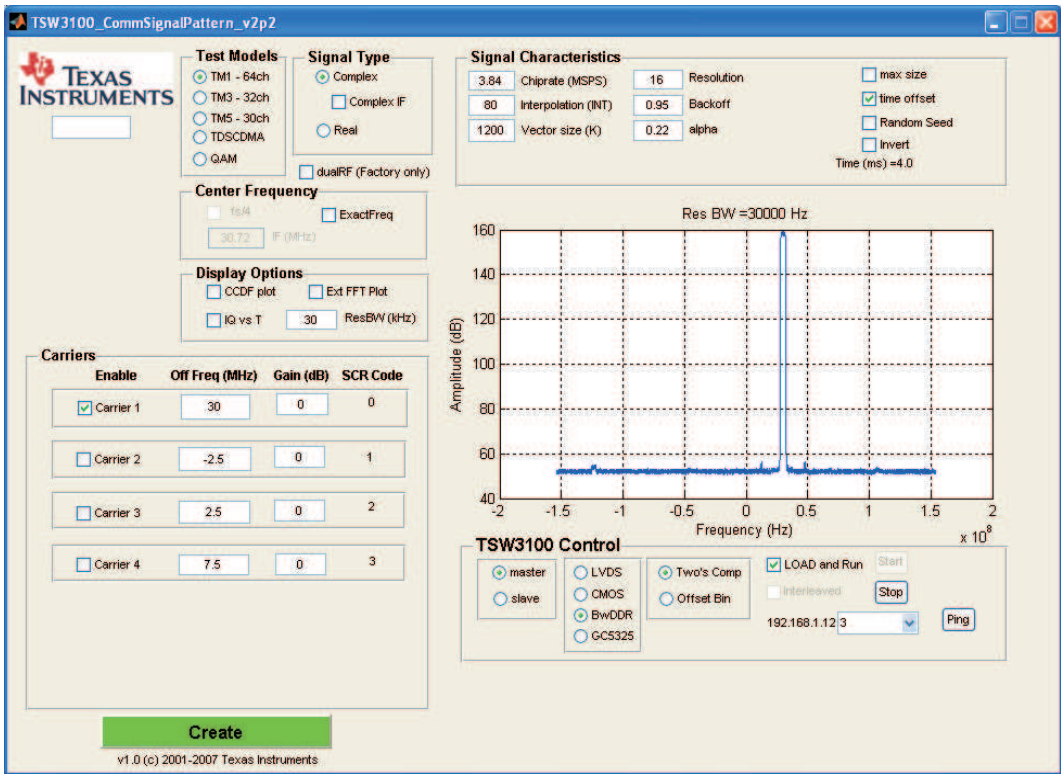


Figure 5. TSW3100 CommsSignalPattern (WCDMA) Programming GUI

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3.4 DAC328x Software Quick-Start Guide

1. Select the Top Level tab. This tab shows the most pertinent registers for the DAC, CDCE62005, and TRF372017 devices. Press the *Reset USB Port* button.
2. The default configuration uses a 614.4-MHz DAC clock.
3. Set the RF output LO to the desired output frequency.
4. Toggle the *Initialize* button. This initializes the CDCE62005 clock and the TRF372017 synthesizer.
5. Verify that the CDCE62005 LED (D4) is illuminated, indicating lock.
6. Verify that the TRF372017 LED (D5) is illuminated, indicating the synthesizer is locked.
7. Monitor the output signal at the RF output connector. If default LO frequency of 2400 MHz is used and the TSW3100 is set up with two tones at 20 MHz and 21 MHz, then the tones seen in Figure 6 are at 2420 MHz and 2421 MHz.

3.5 DA3283 Performance Results

Figure 6, Figure 7, and Figure 8 show the typical two-tone and ACPR performance of the DAC3283 EVM from the setup in Section 3.4. This performance incorporates the DAC device and the TRF372017 modulator device.

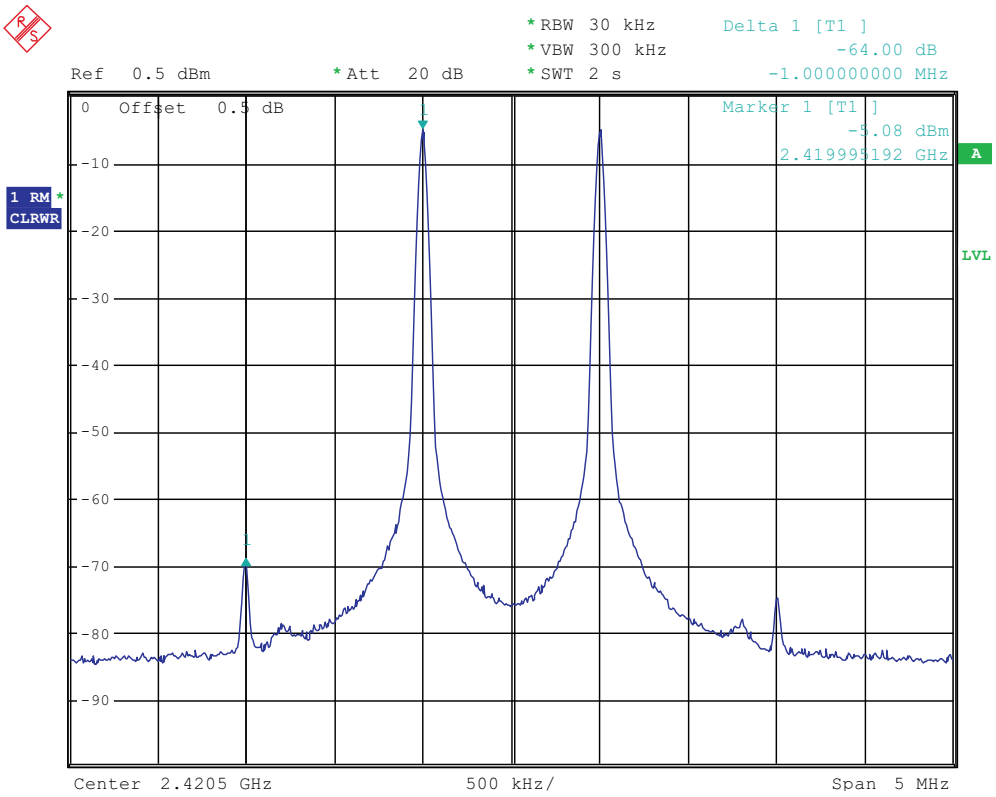


Figure 6. Two-Tone IMD Performance: LO = 2400 MHz, DAC Clk = 614.4 MHz, 2× Interpolation, IF = 20, 21 MHz

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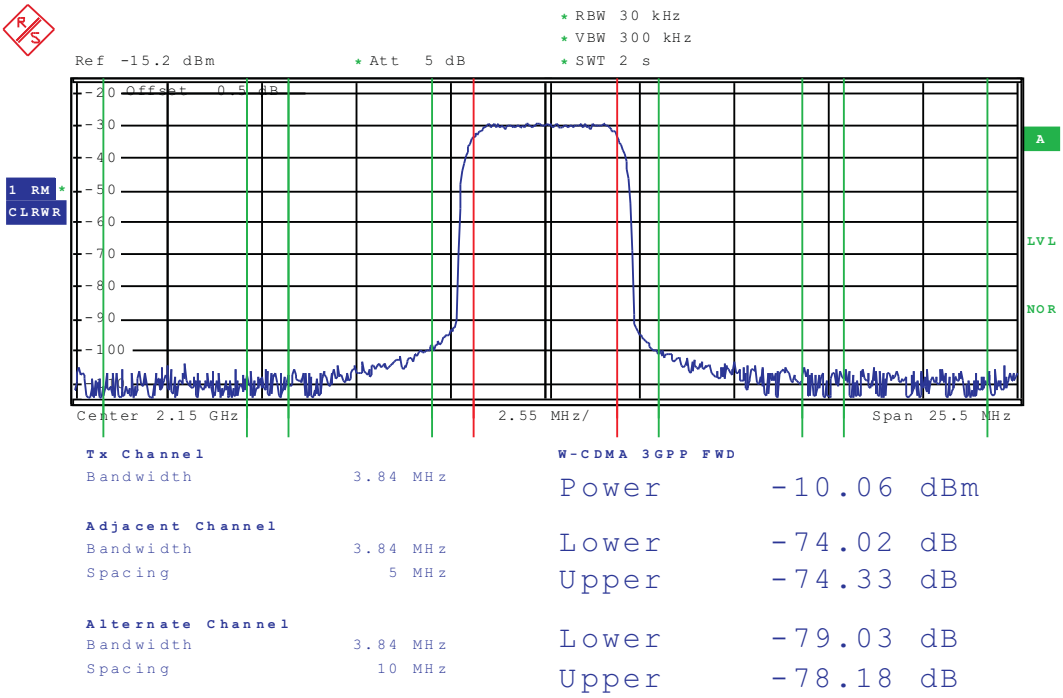


Figure 7. WCDMA ACPR: LO = 2120 MHz, DAC Clk = 614.4 MHz, 2× Interpolation, 30-MHz Offset

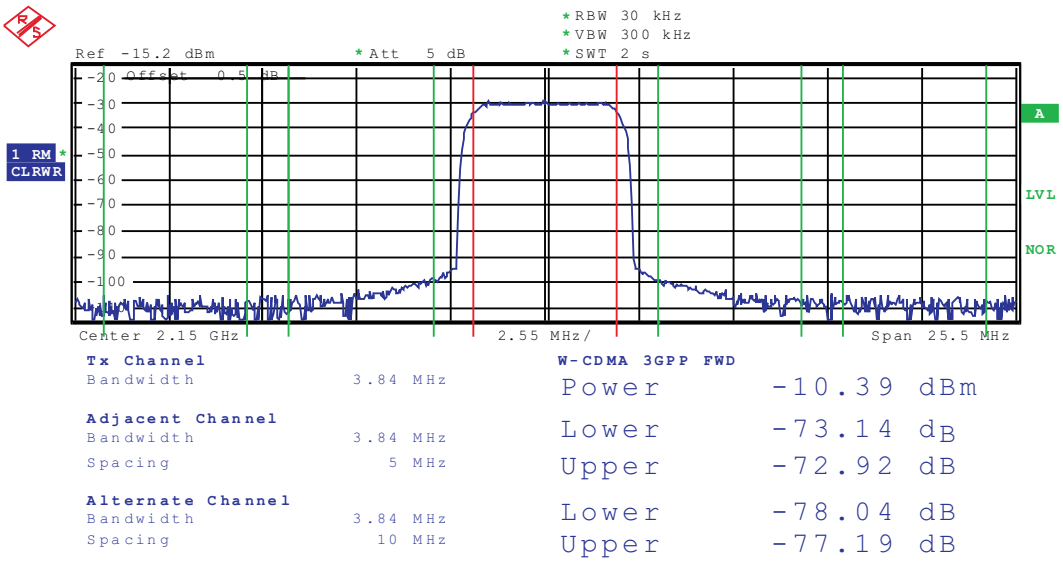


Figure 8. WCDMA ACPR: LO = 1966.4 MHz, DAC Clk = 614.4 MHz, 2× Interpolation, $f_S/4$ mixing, 30-MHz Offset

Note that there are some part-to-part performance variations that can yield significantly improved two-tone IP3 or ACPR performance. The performance plots in this document show conservative typical responses.

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4 Optional Configurations

4.1 DAC Output to 4:1 Transformer

To view the performance of the DAC by itself, move jumpers R153, R137, R156, R155 to location R136, R135, R134, R109. The DAC can be monitored at connectors J3 and J1 from the output of the transformers. The DAC-output-only performance is shown in Figure 9 and Figure 10.

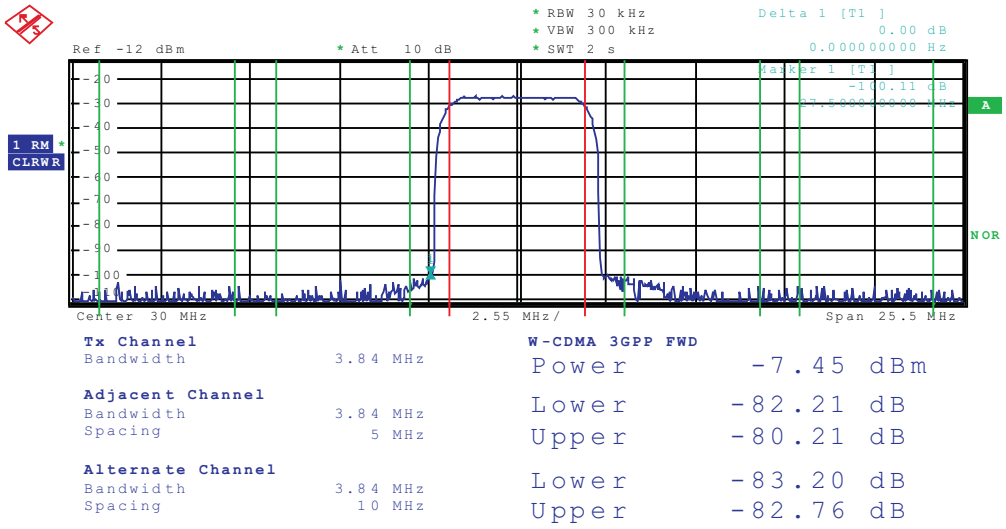


Figure 9. WCDMA ACPR (DAC Ch. B): DAC Clk = 614.4 MHz, 2× Int, 30-MHz Offset

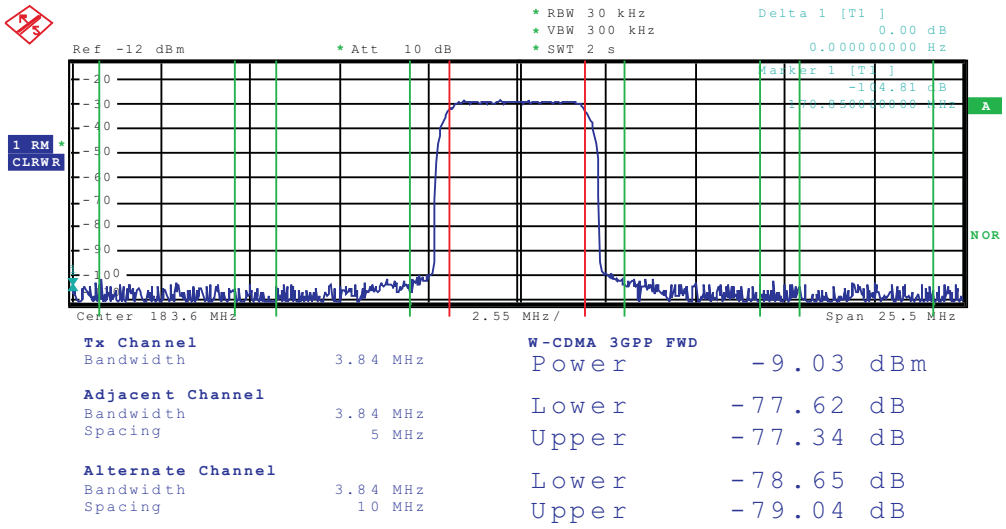


Figure 10. WCDMA ACPR (DAC Ch. B): DAC Clk = 614.4 MHz, 2× Int, $f_S/4$ Mixing, 30-MHz Offset; 183.6-MHz IF

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4.2 DAC Output to Filter Network and 4:1 Transformer

The DAC output can first go through a filter network before going to the 4:1 transformer. The network can accommodate up to a 5th order filter network. As an example, the instructions below will provide an option for a 5th order Butterworth low-pass filter with 75MHz cut-off frequency. To employ this option, please use the following settings:

1. Remove 1uF at C31, C32, C33, and C34
2. Install 0-Ω at R140, R148, R150, R151, R152, R154, R158, and R159
3. Install 270nH at L12, L17, R125, R128, L14, L19, R111, and R115
4. Install 22pF at C166 and C160
5. Install 12pF at C171, R124, R105, and C161
6. Install 0-Ω at L13, L16, L15, and L18
7. Remove 100-Ω at R7, R13, R21, and R26

Please refer to the TSW4200-DAC EVM schematic in the design package for the filter example mentioned above. Other filter component values can also be used to provide a desired frequency response.

4.3 TRF3703-33 Output

The back side of the EVM contains the TRF3703-33 quadrature modulator as an alternative to the TRF372017 device. To employ this option, please use the following settings:

1. Remove 1uF at C31, C32, C33, and C34
2. Install 0-Ω at R142, R145, R146, and R149
3. Remove 100-Ω at R126 and R114
4. Install 100-Ω at R124 and R105
5. Install L13, L16, L15, and L18
6. Move jumper at JP17 to the TRF3703 side to power up the device.

For this option, an external LO signal must be applied at J27, and the output is monitored at J24.

4.4 External LO Option for the TRF372017

The TRF372017 can be configured for external LO. Toggle the *En_EXTVCO* register on the TRF372017 tab and inject the desired LO frequency at J26.

4.5 External Clock Frequency

An external clock can be provided instead of using the internal VCO of the CDCE62005. To configure the CDC for this operation, modify the following on the CDC tab of the software.

1. Inject desired clock signal at J25 (i.e., 614.4 MHz)
2. Remove jumper at JP19.
3. Move jumper at JP22 to connect pins 2 and 3
4. Change *Input Level* to *LVPECL*
5. Change *Input Source* to *Manual_PRI-IN*
6. Change *Pri Ref PreDivider* to *Divide by 1*
7. Change *Sec Ref PreDivider* to *3-state*
8. Select *Pri Term* to *Disabled*
9. Change Output 0 through 4 from *VCO* to *Primary*
10. Toggle *Wake up* button

4.6 DC/DC Power Supply Bypass Mode

The primary DC/DC switching power supply (U14) can be completely bypassed to further minimize the switching noise of the power supply. The main 6V is stepped down initially by two TPS7A4501 LDOs (U17 and U18). To bypass the DC/DC power supply, please modify the following:

1. Remove 0-Ω at R88, R96, and R165

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2. Install 0-Ω at R131, R130, R164, and R163

5 Revision Changes

Changes from Revision D. to Revision E.

- Added DAC Output to Filter Network and Transformer
- Changed routing of 5V power to TRF372017 (U3), TRF3703 (U10), and filter network bias.
- Added DC/DC Switching Power Supply (U14) bypass option.
- Changed CDCE62005 (U4) LVPECL output termination network at DACCLK and FIFO_OSTR clocks.
- Changed CDCE62005 (U4) LVPECL input termination network at J25 for external clock mode.

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 5.5 V to 7 V and the output voltage range of 0 V to 3.3 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 55°C. The EVM is designed to operate properly with certain components above 55°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps

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