ADVANCE INFORMATION

CYWB0224ABS/CYWB0224ABM

West Bridge™ Astoria™

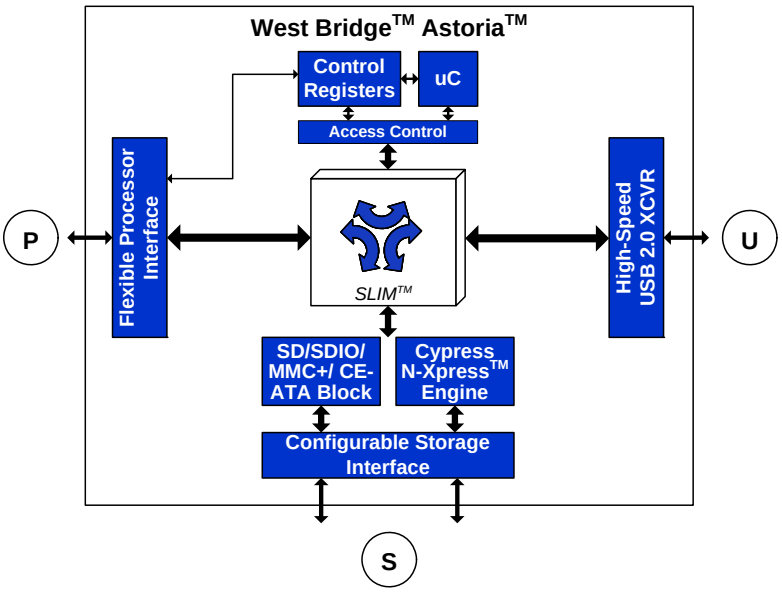
Features

- N-Xpress™ NAND Controller Technology
  - Interleave up to 16 NANDs with 8 Chip Enables (CE#) for x8 or x16 SLC (CYWB0224ABS) or MLC (CYWB0224ABM) NAND flash devices.
  - 4-bit Error Correction Coding
  - Bad Block Management
  - Static Wear Leveling
- Multimedia Device Support
  - Up to 2 SD/SDIO/MMC/MMC+/CE-ATA devices
- *SLIM*™ Architecture, allowing simultaneous and independent data paths between the processor and USB, and between the USB and Mass Storage.
- Fully backward compatible (including pin to pin) to Antioch (CYWB0124AB)
- High speed USB at 480 Mbps
  - USB 2.0 compliant
  - Integrated USB 2.0 transceiver, smart Serial Interface Engine
  - 16 programmable endpoints
- Flexible Processor Interface, which supports:
  - Multiplexing and nonMultiplexing Address and Data interface
  - SRAM Interface
  - Pseudo CRAM interface (Antioch Interface)
  - Pseudo NAND Flash interface
  - SPI (slave mode) interface
  - DMA slave support
- Ultra low power, 1.8V core operation
- Low Power Modes
- Small footprint, 6x6mm VFBGA
- Supports I2C boot and Processor Boot
- Selectable Clock Input Frequencies
  - 19.2 MHz, 24 MHz, 26 MHz, and 48 MHz

Applications

- Cellular Phones
- Portable Media Players
- Personal Digital Assistants
- Portable Navigation Devices
- Digital Cameras
- POS Terminals
- Portable Video Recorders

Logic Block Diagram



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Functional Overview

The *SLIM*™ architecture

The Simultaneous Link to Independent Multimedia (SLIM) architecture allows three different interfaces (P-port, S-port and U-port) to connect to each other independently.

With this architecture, a device using Astoria is connected to a PC through a USB, without disturbing any of the functions of the device. The device can still access Mass Storage when the PC is synchronizing with the main processor.

The SLIM architecture enables new usage models, in which a PC accesses a Mass Storage device independent of the main processor, or enumerates access to both the Mass Storage and the main processor at the same time.

In a handset using SLIM architecture, the user can do the following:

- Use the phone as a thumb drive.
- Download media files to the phone with all the functionalities still available on the phone.
- Use the same phone as a modem to connect the PC to the internet.

8051 Microprocessor

The 8051 microprocessor embedded in Astoria does basic transaction management for all transactions between the P-Port, S-Port, and the U-Port. The 8051 does not reside in the data path; it manages the path. The data path is optimized for performance. The 8051 executes firmware that supports NAND, SD, SDIO, MMC+, and CE-ATA devices at the S-Port. For the NAND device, the 8051 firmware follows the Smart Media algorithm to support the following:

- Physical to Logical Management
- ECC Correction support
- Wear Leveling
- NAND Flash bad blocks handling

Configuration and Status Registers

The West Bridge Astoria device includes configuration and status registers that are accessible as memory-mapped registers through the processor interface. The configuration registers allow the system to specify some behaviors of Astoria. For example, it can mask certain status registers from raising an interrupt. The status registers convey the status of Astoria, such as the addresses of buffers for read operations.

Processor Interface (P-Port)

Communication with the external processor is realized through a dedicated processor interface. This interface is configured to support different interface standards. This interface supports multiplexing and nonmultiplexing address or data bus in both synchronous and asynchronous pseudo CRAM-mapped, and nonmultiplexing address or data asynchronous SRAM-mapped memory accesses. The interface may be configured to pseudo NAND interface to support the processor's NAND interface. In addition, this interface may be configured to support the slave SPI interface. This ensures straightforward electrical communication with the processor, which may have other devices connected on a shared memory bus. Asynchronous accesses can reach a bandwidth of up to 66.7 MBps. Synchronous accesses are performed at 33 MHz across 16 bits for up to 66.7 MBps bandwidth.

The memory address is decoded to access any of the multiple endpoint buffers inside Astoria. These endpoints serve as buffers for data between each pair of ports, for example, between the processor port and the USB port. The processor writes and reads into these buffers through the memory interface.

Access to these buffers is controlled by using a DMA protocol or using an interrupt to the main processor. These two modes are configured by the external processor.

As a DMA slave, Astoria generates a DMA request signal to notify the main processor that a specific buffer is ready to be read from or written to. The external processor monitors this signal and polls Astoria for the specific buffers ready for a read or write operation. It then performs the appropriate read or write operations on the buffer through the processor interface. As a result, the external processor only deals with the buffers to access a multitude of storage devices connected to Astoria.

In the Interrupt mode, Astoria communicates important buffer status changes to the external processor using an interrupt signal. The external processor then polls Astoria for the specific buffers ready for read or write, and it performs the appropriate read or write operations through the processor interface.

USB Interface (U-Port)

In accordance with the USB 2.0 specification, Astoria can operate in Full-Speed USB mode in addition to High-Speed USB. The USB interface consists of the USB transceiver. The USB interface can access and be accessed by both the P-Port and the S-Port.

The Astoria USB interface supports programmable CONTROL/BULK/INTERRUPT/ISOCHRONOUS endpoints.

Mass Storage Support (S-Port)

The S-Port may be configured in three different modes, which simultaneously support the following:

- An SD/SDIO/MMC+/CE-ATA port and a x8 NAND port
- Two SD/SDIO/MMC+/CE-ATA ports
- Up to eight Chip Enable (CE#) for x8 or x16 NAND flash access port

These configurations are controlled by the 8051 firmware. The 16-bit NAND interface is used only when there is no other Mass Storage device connected to the S-Port.

N-Xpress NAND Controller (S-Port)

Astoria, as part of its Mass Storage management functions, can fully manage the SLC and MLC NAND flash devices. The embedded 8051 manages the actual reading and writing of the NAND, along with its required protocols. It performs standard NAND management functions, such as ECC and wear leveling. The Astoria supports single bit ECC for the SLC and 4-bit ECC for MLC NAND flash. SLC NAND flash devices are supported by CYWB0244ABS. CYWB0244ABM supports both SLC and MLC NAND flash devices.

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SD/SDIO/MMC+/CE-ATA Port (S-Port)

When Astoria is configured through firmware to support SD/SDIO/MMC+/CE-ATA, this interface supports the following:

- The Multimedia Card System Specification, MMCA Technical Committee, Version 4.1.
- SD Memory Card Specification - Part 1, Physical Layer Specification, SD Group, Version 1.10, October 15, 2004.
- SD Memory Card Specification - Part 1, Physical Layer Specification, SD Group, Version 2.0, May 9, 2006.
- SD Specifications - Part E1 SDIO specification, Version 1.10, August 18, 2004.
- CE-ATA Specification - CE-ATA Digital Protocol, CE-ATA Committee, Version 1.1, September, 2005

West Bridge Astoria provides support for 1-bit and 4-bit SD and SDIO cards; 1-bit, 4-bit and 8-bit MMC; MMC+ cards, and CE-ATA drive. For the SD, SDIO, MMC/MMC Plus, and CE-ATA, this block supports one card for one physical bus interface.

Astoria supports SD commands including the multisector program command, which is handled by API.

Table 1. Astoria Pin Assignments

	Pin Name					IO	Pin Description	Power Domain
	Non-multiplexing	Multiplexing	SRAM	PNAND	SPI			
P-PORT	CLK	CLK		Ext pull up	SCK	I	Clock/SPI clock	PVDDQ VGND
	CE#	CE#	CE#	CS#	SS#	I	Chip Enable/NAND Chip Select/SPI Slave Select	
	A0	Ext pull up	A0	CLE#	Ext pull up	I	Address Bus 0/PNAND Command Latch	
	A1	Ext pull up	A1	RB#	Ext pull up	IO	Address Bus 1/PNAND Ready_Buy	
	A[3:2]	set A[3:2] = 01	A[3:2]	set A[3:2] = 00	set A[3:2] = 10	I	Addr. Bus [3:2]	
	A4	Ext pull up	A4	WP#	Ext pull up	I	Addr. Bus 4/NAND Write Protect	
	A5	SCL	A5	SCL	SCL	IO	Address Bus 5/I2C clock	
	A6	SDA	A6	SDA	SDA	IO	Address Bus 6/I2C data	
	A7]	Ext pull up	A7	set A7 to 0 - LBD set A7 to 1 - SBD	Ext pull up	I	Addr. Bus 7	
	DQ[0]	AD[0]	DQ[0]	IO[0]	SDI	IO	SPI Input/Data Bus 0	
	DQ[1]	AD[1]	DQ[1]	IO[1]	SDO	IO	SPI Output/Data Bus 1	
	DQ[15:2]	AD[15:2]	DQ[15:2]	IO[15:2]	Ext pull up	IO	Data Bus	
	ADV#	ADV#		ALE#	Ext pull up	I	Address Valid	
	OE#	OE#	OE#	RE#	Ext pull up	I	Output Enable	
	WE#	WE#	WE#	WE#	Ext pull up	I	Write Enable	
	INT#	INT#	INT#	INT#	SINT	O	Interrupt Request	
	DRQ#	DRQ#	DRQ#	DRQ#	N/C	O	DMA Request	
	DACK#	DACK#	DACK#	DACK#	Ext pull up	I	DMA Acknowledgement	
U-Port	D+					IO/Z	USB D+	UVDDQ UVSSQ
	D-					IO/Z	USB D-	
	UVALID					O	External USB Switch Control	

[+] Feedback

Table 1. Astoria Pin Assignments (continued)

	Pin Name					IO	Pin Description	Power Domain
	Non-multiplexing	Multiplexing	SRAM	PNAND	SPI			
S-Port	SDIO and NAND Configuration	NAND only Configuration	Dual SDIO Configuration	NAND and GPIO Configuration	SDIO and GPIO Configuration			
S-Port	SD_D[7:0]	NAND_IO[15:8] / PD[7:0] (GPIO)	SD_D[7:0]	NAND_IO[15:8] / PD[7:0] (GPIO)	SD_D[7:0]	IO	SD Data bus/NAND Upper IO bus	SSVDDQ VGND
S-Port	SD_CLK	NAND_CE8#/NAND_R/B4#	SD_CLK	PC-7 (GPIO) / NAND_CE8# / NAND_R/B4#	SD_CLK	IO	SD Clock/NAND CE8#/NAND R/B4#	
S-Port	SD_CMD	NAND_CE7#/NAND_R/B3#	SD_CMD	PC-3 (GPIO) / NAND_CE7# / NAND_R/B3#	SD_CMD	IO	SD Command, NAND CE7#, or NAND_R/B3#	
S-Port	SD_POW	NAND_CE6#	SD_POW	PC-6 (GPIO) / NAND_CE6#	SD_POW	IO	SD Power Control/NAND CE6#	
S-Port	SD_WP	NAND_CE5#	SD_WP	PC-1 (GPIO) / NAND_CE5#	SD_WP	IO	GPIO (SD Write Protection Microswitch) or NAND CE5#	
S-Port	NAND_IO[7:0]	NAND_IO[7:0]	SD2_D[7:0]	NAND_IO[7:0]	PB[7:0] (GPIO)	IO	NAND Lower IO bus/2nd SD Data Bus	SNVDDQ VGND
S-Port	NAND_CLE	NAND_CLE	SD2_CLK	NAND_CLE	PA-6 (GPIO)	IO	CMD Latch Enable/2nd SD Clock	
S-Port	NAND_ALE	NAND_ALE	SD2_CMD	NAND_ALE	PA-7 (GPIO)	IO	Address Latch Enable/2nd SD CMD	
S-Port	NAND_CE#	NAND_CE#	SD2_POW	NAND_CE#	PC-0 (GPIO)	IO	Chip Enable/2nd SD Power Control	
S-Port	NAND_RE#	NAND_RE#	N/C	NAND_RE#	N/C	O	Read Enable	
S-Port	NAND_WE#	NAND_WE#	N/C	NAND_WE#	N/C	O	Write Enable	
S-Port	NAND_WP#	NAND_WP#	PA-5 (GPIO)	NAND_WP#	PA-5 (GPIO)	IO	Write Protect	
S-Port	NAND_R/B#	NAND_R/B#		NAND_R/B#		I	Ready/Busy/2nd SD WP	
S-Port	NAND_CE2#	NAND_CE2#	SD2_WP	NAND_CE2#	PC-2 (GPIO)	IO	Chip Enable 2	
Other	RESETOUT / NAND_R/B2#	NAND_R/B2#	RESETOUT	NAND_R/B2# / RESETOUT	RESETOUT	IO	RESET OUT/NAND Busy/Ready	GVDDQ VGND
Other	GPIO[0] / SD_CD / NAND_CE4#	NAND_CE4#	PC-4 (GPIO[0]) / SD_CD	PC-4 (GPIO[0]) / NAND_CE4#	PC-4 (GPIO[0]) / SD_CD	IO	General Input/Output 0 or SD/MMC Card Detection or NAND CE4#	
Other	GPIO[1] / NAND_CE3#	NAND_CE3#	PC-5 (GPIO[1]) / SD2_CD	PC-5 (GPIO[1]) / NAND_CE3#	PC-5 (GPIO[1])	IO	General Input/Output 1 or NAND CE3#	
Other	RESET#					I	RESET	
Other	WAKEUP					I	Wake Up Signal	
Other	XTALIN					I	Crystal/Clock IN	XVDDQ VGND
Other	XTALOUT					O	Crystal Out	
Config	XTALSLC[1:0]					I	Clock Select 0 and 1	GVDDQ VGND
Config	NANDCFG					I	S Port Configuration	
Config	TEST[2:0]					I	Test Configuration	
Power	PVDDQ					PWR	Processor interface VDD	
Power	SNVDDQ					PWR	NAND VDD	
Power	UVDDQ					PWR	USB VDD	
Power	SSVDDQ					PWR	SDIO VDD	
Power	GVDDQ					PWR	Miscellaneous IO VDD	
Power	AVDDQ					PWR	Analog VDD	
Power	XVDDQ					PWR	Crystal VDD	
Power	VDD					PWR	Core VDD	
Power	VDD33					PWR	Independent 3.3V nominal	
Power	UVSSQ					PWR	USB GND	
Power	AVSSQ					PWR	Analog GND	
Power	VGND					PWR	Core GND	

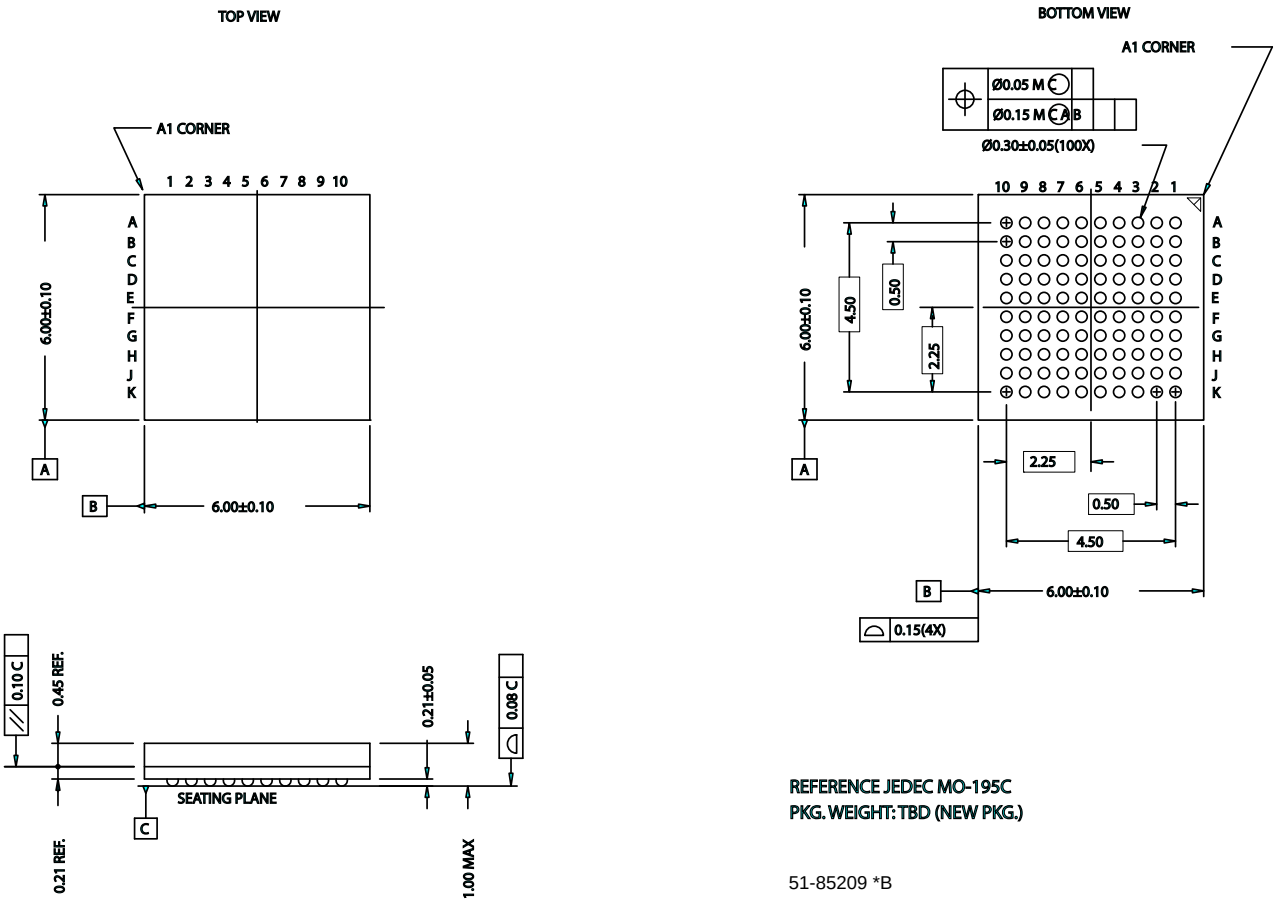
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Ordering Information

Ordering Code	Package Type	NAND Flash Support	Available Clock Input Frequencies (MHz)
CYWB0224ABS-BVXI	100 VFBGA – Pb-Free	Support SLC NAND Flash only	19.2, 24, 26, 48
CYWB0224ABM-BVXI	100 VFBGA – Pb-Free	Support SLC and MLC NAND Flash	19.2, 24, 26, 48

Package Diagram

Figure 1. 100 VFBGA (6 x 6 x 1.0 MM) BZ100A



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Document History Page

Document Title: CYWB0224ABS/CYWB0224ABM West Bridge™ Astoria™ Document Number: 001-11710				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	567055	See ECN	VSO	New data sheet
*A	1830226	See ECN	VSO/AESA	In the Feature list, adding the bullets of “N-Xpress Controller Technology” and “Multimedia Device Support” In the Feature list, removed the bullet of “Mass Storage device support” Update the bullet of Application Update Logic Block Diagram. Updated the section of “NAND Port” to N-Xpress NAND Controller” Updated the pin Assignment Table Fix the typo of VGAN in pin Assignment Table

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