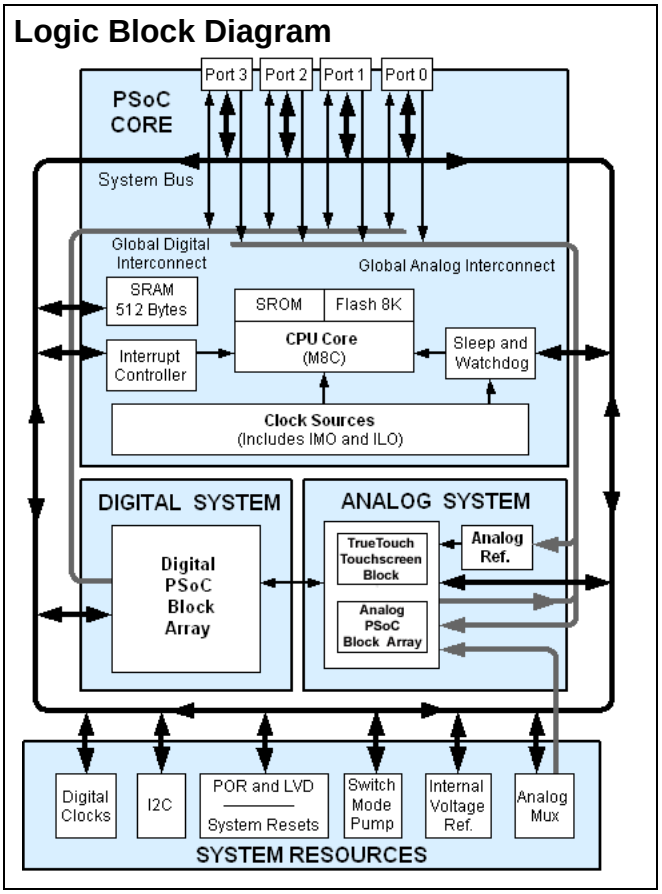
CY8CTMG110

TrueTouch™ Multi-Touch Gesture Touchscreen Controller

Features

- TrueTouch™ Capacitive Touchscreen Controller
  - Supports Single-Touch and Multi-Touch Applications
  - Supports up to 24 X/Y Sensor Inputs
  - Supports Screen Sizes 4.3” and Below (Typical)
  - Fast Scan Rates: Typical 0.5 ms per Sensor
  - High Resolution: Typical 320 x 240 for 2.6” Screen
  - Available in 32-Pin QFN Package
- Highly Configurable Sensing Circuitry
  - Allows Maximum Design Flexibility
  - Allows Trade-Off Between Scan Time and Noise Performance
- Includes Gesture Detection Library
- Allows Development of Customized Gestures
- Provides Maximum EMI Immunity
  - Selectable Spread-Spectrum Clock Source
- Low Power TrueTouch Single-Touch Touchscreen Device
  - 4 mA Average Supply Current at 8 ms Report Rate
  - 2 mA Average Supply Current at 16 ms Report Rate
- Powerful Harvard Architecture Processor
  - M8C Processor Speeds to 24 MHz
  - Low Power at High Speed
  - 2.7V to 5.25V Operating Voltage
  - Industrial Temperature Range: –40°C to +85°C
- Flexible On-Chip Memory
  - 8K Flash Program Storage, 50000 Erase/Write Cycles
  - 512 Bytes SRAM Data Storage
  - In-System Serial Programming (ISSP™)
  - Partial Flash Updates
  - Flexible Protection Modes
  - EEPROM Emulation in Flash
- Complete Development Tools
  - Free Development Software (PSoC Designer™)
  - TrueTouch Touchscreen Tuner
  - Full-Featured, In-Circuit Emulator and Programmer
  - Full Speed Emulation
  - Complex Breakpoint Structure
  - 128K Trace Memory
- Precision, Programmable Clocking
  - Internal ±2.5% 24 and 48 MHz Oscillator
  - Internal Oscillator for Watchdog and Sleep
- Programmable Pin Configurations
  - 25 mA Sink, 10 mA Drive on All GPIO
  - Pull Up, Pull Down, High Z, Strong, or Open Drain Drive Modes on All GPIO
  - Up to 8 Analog Inputs on GPIO
  - Configurable Interrupt on All GPIO
- Additional System Resources
  - I^{2}C™ Master, Slave, and Multi-Master to 400 kHz
  - Watchdog and Sleep Timers
  - User-Configurable Low Voltage Detection
  - Integrated Supervisory Circuit
  - On-Chip Precision Voltage Reference

Logic Block Diagram



TrueTouch Functional Overview

The TrueTouch family provides the fastest and most efficient way to develop and tune a capacitive touchscreen application. A TrueTouch device includes the configurable TrueTouch block, configurable analog and digital logic, and programmable interconnect. This architecture enables the user to create flexible, customized touchscreen configurations to match the requirements of each individual touchscreen application. Various configurations of Flash program memory, SRAM data memory, and configurable IO are included in a range of convenient pinouts.

The TrueTouch architecture consists of four main areas: the Core, the System Resources, the Digital System, and the TrueTouch Analog System. Configurable global bus resources allow combining all the device resources into a complete custom touchscreen system. Each CY8TMG110 TrueTouch device includes four digital blocks and the TrueTouch controller block. The CY8CTMG110 is offered in a 32-pin QFN package, with up to 28 general purpose IO (GPIO), and support of up to 24 X/Y sensors.

When designing touchscreen applications, refer to the UM data sheet for performance requirements to meet and detailed design process explanation.

The TrueTouch Core

The core encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO (Internal Main Oscillator) and ILO (Internal Low speed Oscillator). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four MIPS 8-bit Harvard architecture microprocessor.

System Resources provide the following additional capabilities:

- Digital clocks to increase the flexibility of the PSoC mixed-signal arrays.
- I2C functionality to implement an I2C master and slave.
- An internal voltage reference, MultiMaster, that provides an absolute value of 1.3V to a number of TrueTouch subsystems.
- Various system resets supported by the M8C.

The Digital System consists of an array of digital blocks that may be configured into any number of digital peripherals. The digital blocks are connected to the GPIO through a series of global buses that can route any signal to any pin, freeing designs from the constraints of a fixed peripheral controller.

The Analog System consists of four analog blocks, supporting comparators and analog-to-digital conversion up to 8 bits in precision.

Implementation of touchscreen applications allows additional digital and analog resources to be used, depending on the touchscreen design.

The Digital System

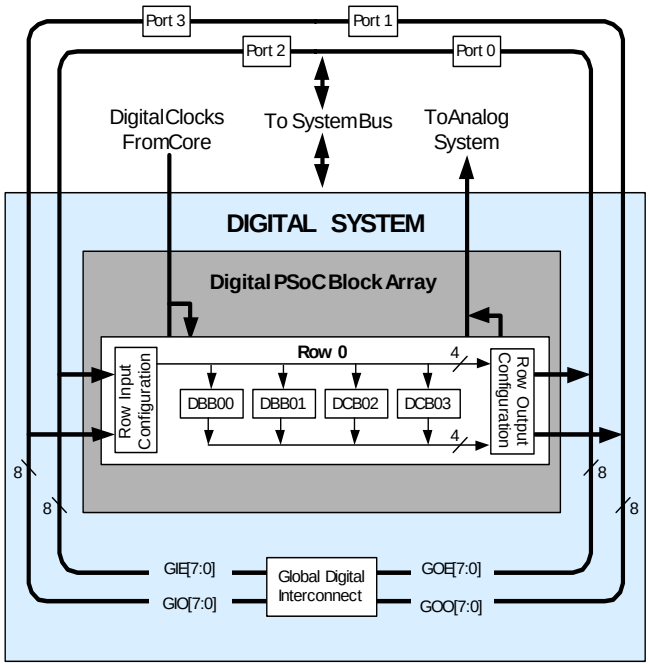
The Digital System consists of 4 digital PSoC blocks. Each block is an 8-bit resource that is used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references. Digital peripheral configurations include the following.

- PWMs (8 to 32 bit)
- PWMs with Dead band (8 to 32 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8 bit with selectable parity
- SPI master and slave
- I2C slave and multi-master
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks are connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows the optimum choice of system resources for your application. Family characteristics are shown in Table 1 on page 4.

Figure 1. Digital System Block Diagram



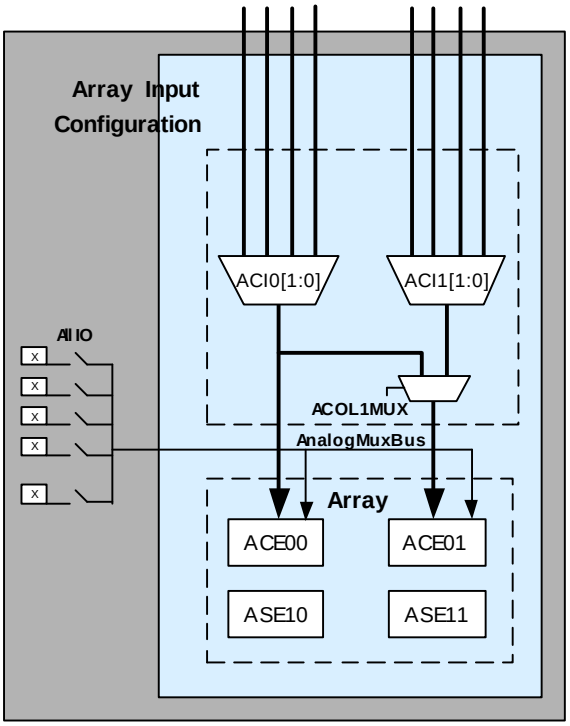
[+] Feedback

The Analog System

The Analog System consists of 4 configurable blocks that allow the creation of complex analog signal flows. Analog peripherals are very flexible and may be customized to support specific application requirements. Some of the common PSoC analog functions for this device (most available as user modules) are:

- Analog-to-digital converters (single or dual, with 8-bit resolution)
- Pin-to-pin comparator
- Single-ended comparators (up to 2) with absolute (1.3V) reference or 8-bit DAC reference
- 1.3V reference (as a System Resource)

Figure 2. Analog System Block Diagram



The Analog Multiplexer System

The Analog Mux Bus connects to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for capacitive sensing with the TrueTouch block comparator. An additional 8:1 analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Switch control logic enables selected pins to switch dynamically under hardware control. This allows capacitive measurement for the touchscreen application. Other multiplexer applications include:

- Chip-wide mux that allows analog input from any IO pin.
- Electrical connection between any IO pin combinations.

Additional System Resources

System Resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. Brief statements describing the merits of each system resource follow.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks may be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3 voltage reference provides an absolute reference for the analog system, including ADCs and DACs.
- Versatile analog multiplexer system.

[+] Feedback

Getting Started

To understand the TrueTouch device, read this data sheet and use the PSoC Designer™ Integrated Development Environment (IDE). This data sheet is an overview of the general silicon information and electrical specifications. For in depth touchscreen application information, including touchscreen specific specifications, read the touchscreen user module data sheet that is supported by this specific device.

TrueTouch Device Characteristics

Depending on your TrueTouch device selected for a touchscreen application, characteristics and capabilities of each device changes. Table 1 lists the touchscreen sensing capabilities available for specific TrueTouch devices. The TrueTouch device covered by this data sheet is highlighted in this table.

Table 1. TrueTouch Device Characteristics

TrueTouch Part Number	Sensor Inputs	Max Screen Size (Inches)	Single-Touch	Multi-Touch Gesture	Multi-Touch All-Point	Scan Speed (ms)[1]	Current Consumption[2]	Flash Size	SRAM Size
CY8CTST110	up to 24	4.3”	Y	N	N	0.5	3	8K	512 Bytes
CY8CTST120	up to 44	8.4”	Y	N	N	0.5	16	16K	1K
CY8CTMG110	up to 24	4.3”	Y	Y	N	0.5	3	8K	512 Bytes
CY8CTMG120	up to 44	8.4	Y	Y	N	0.5	16	16K	1K
CY8CTMA120	up to 37	7.3”	Y	Y	Y	0.12	16	16K	1K

Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store contains development kits, C compilers, and all accessories for PSoC development. Go to the Cypress Online Store web site at http://www.cypress.com, click the Online Store shopping cart icon at the bottom of the web page, and click *PSoC (Programmable System-on-Chip)* to view a current list of available items.

Technical Training Modules

Free PSoC technical training modules are available for users new to PSoC. Training modules cover designing, debugging, advanced analog, and CapSense. Go to http://www.cypress.com/training.

Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to http://www.cypress.com, click on Design Support located on the left side of the web page, and select CYPros Consultants.

Technical Support

PSoC application engineers take pride in fast and accurate response. They are available with a four hour guaranteed response at http://www.cypress.com/support.

Application Notes

A long list of application notes can assist you in every aspect of your design effort. To view the PSoC application notes, go to the http://www.cypress.com web site and select Application Notes under the Design Resources list located in the center of the web page. Application notes are sorted by date by default.

Development Tools

PSoC Designer is a Microsoft® Windows based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE and application runs on Windows NT 4.0, Windows 2000, Windows Millennium (Me), or Windows XP (see Figure 3 on page 5).

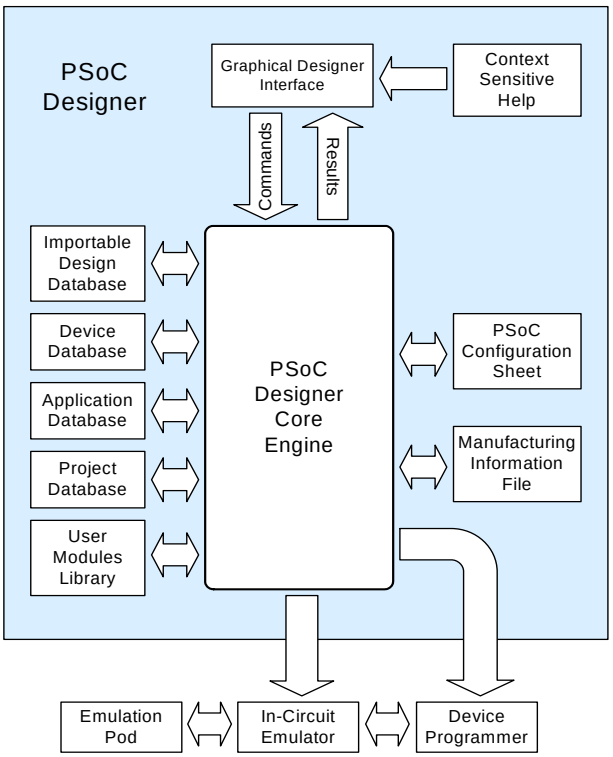
PSoC Designer helps the customer to select an operating configuration for the PSoC, write application code that uses the PSoC, and debug the application. This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and the CYASM macro assembler for the CPUs.

PSoC Designer also supports a high level C language compiler developed specifically for the devices in the family.

Notes
1. Per sensor typical. Depends on touchscreen panel. For MA120 per X/Y crossing Vcc = 3.3V.
2. Average mA supply current. Based on 8 ms report rate, except for MA120.

[+] Feedback

Figure 3. PSoC Designer Subsystems



TrueTouch Designer Software Subsystems

Device Editor

The device editor subsystem enables the user to select different onboard analog and digital components called user modules using the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration allows changing configurations at run time.

PSoC Designer sets up power on initialization tables for selected PSoC block configurations and creates source code for an application framework. The framework contains software to operate the selected components. If the project uses more than one operating configuration, then it contains routines to switch between different sets of PSoC block configurations at run time. PSoC Designer prints out a configuration sheet for a given project configuration for use during application programming in conjunction with the device data sheet. After the framework is generated, the user adds application-specific code to flesh out the framework. It is also possible to change the selected components and regenerate the framework.

Design Browser

The Design Browser enables users to select and import preconfigured designs into the user's project. Users can easily browse a catalog of preconfigured designs to facilitate time-to-design. Examples provided in the tools include a 300-baud modem, LIN Bus master and slave, fan controller, and magnetic card reader.

Application Editor

The Application Editor edits the C language and assembly language source code. It also assembles, compiles, links, and builds.

Assembler. The macro assembler allows the seamless merging of the assembly code with C code. The link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compiler. A C language compiler that supports the PSoC family of devices is available. Even if you have never worked in the C language before, the product quickly helps you create complete C programs for the PSoC family devices.

The embedded, optimizing C compiler provides all the features of C tailored to the PSoC architecture. It comes complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing the designer to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read the program and read and write data memory, read and write IO registers, read and write CPU registers, set and clear break-points, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

Hardware Tools

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

TrueTouch Touchscreen Tuner

The TrueTouch tuner is a Microsoft® Windows based graphical user interface allowing developers to set critical parameters and observe changes to the touchscreen application in real time. Optimal configuration from the tuner can be immediately applied to the TrueTouch user module settings.

Designing with User Modules

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC blocks. They implement a wide variety of user selectable functions. Each block has several registers that determine its function and connectivity to other blocks, multiplexers, buses and to the IO pins. Iterative development cycles permit you to adapt the hardware and the software. This substantially lowers the risk of selecting a different part to meet the final design requirements.

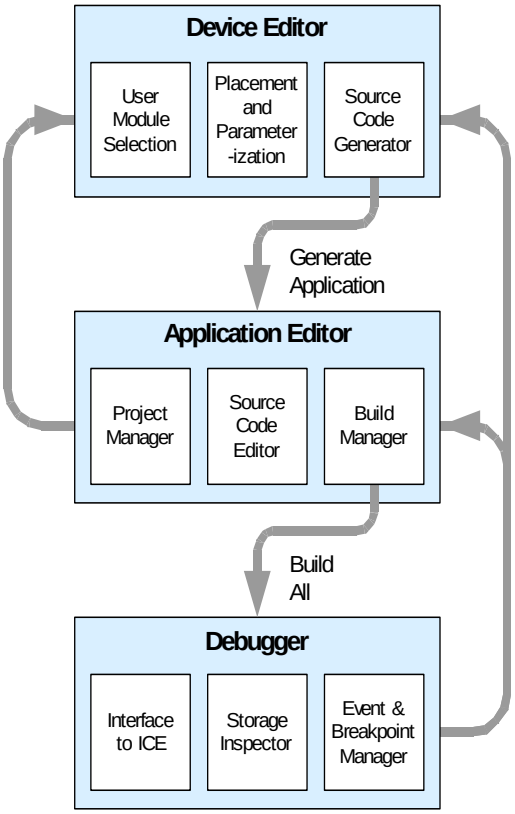
To speed the development process, the PSoC Designer IDE provides a library of pre-built, pre-tested hardware peripheral functions, called “User Modules.” User modules make selecting and implementing peripheral devices simple. They come in analog, digital, and mixed signal varieties. The standard user module library contains over 50 common peripherals such as ADCs, DACs, timers, counters, UARTs, and other uncommon peripherals, such as DTMF Generators and Bi-Quad analog filter sections.

Each user module establishes the basic register settings to implement the selected function. It also provides parameters that allow you to tailor its precise configuration to a particular application. For example, a Pulse Width Modulator User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit to establish the pulse width and duty cycle. User modules also provide tested software to cut your development time. The user module application programming interface (API) provides high level functions to control and respond to hardware events at run time. The API also provides optional interrupt service routines to adapt as needed.

The API functions are documented in user module data sheets that are viewed directly in the PSoC Designer IDE. These data sheets explain the internal operation of the user module and provide performance specifications. Each data sheet describes the use of each user module parameter and documents the setting of each register controlled by the user module.

The development process starts when you open a new project and bring up the Device Editor, a graphical user interface (GUI) for configuring the hardware. Select the user modules you need for your project and map them onto the PSoC blocks with point-and-click simplicity. Next, you build signal chains by interconnecting user modules to each other and the IO pins. At this stage, also configure the clock source connections and enter parameter values directly or by selecting values from drop down menus. When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Application” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the high level user module API functions.

Figure 4. User Module and Source Code Development Flows



The next step is to write your main program, and any sub-routines using PSoC Designer’s Application Editor subsystem. The Application Editor includes a Project Manager that allows you to open the project source code files (including all generated code files) from a hierarchal view. The source code editor provides syntax coloring and advanced edit features for both C and assembly language. File search capabilities include simple string searches and recursive “grep-style” patterns. A single mouse click invokes the Build Manager. It employs a professional-strength “makefile” system to automatically analyze all file dependencies and run the compiler and assembler as necessary. Project-level options control optimization strategies used by the compiler and linker. Syntax errors are displayed in a console window. Double click the error message to show the offending line of source code. When all is correct, the linker builds a HEX file image suitable for programming.

The last step in the development process takes place inside the PSoC Designer’s Debugger subsystem. The Debugger downloads the HEX image to the In-Circuit Emulator (ICE) where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer. This enables to define complex breakpoint events such as monitoring address and data bus values, memory locations, and external signals.

[+] Feedback

Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
FSR	full scale range
GPIO	general purpose IO
GUI	graphical user interface
HBM	human body model
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
IO	input/output
IPOR	imprecise power on reset
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
PC	program counter
PLL	phase-locked loop
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse width modulator
SC	switched capacitor
SLIMO	slow IMO
SMP	switch mode pump
SRAM	static random access memory

Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 4 on page 12 lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers are also represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or 0x are decimal.

[+] Feedback

Pinouts

The CY8CTMG110 TrueTouch device is available in a 32-pin QFN package which is listed in the following tables. Every port pin (labeled with a “P”) is capable of Digital IO and connection to the common analog bus. However, Vss, Vdd, SMP, and XRES are not capable of Digital IO.

32-Pin Part Pinout

Figure 5. CY8CTMG110 32-Pin Sawn TrueTouch Device

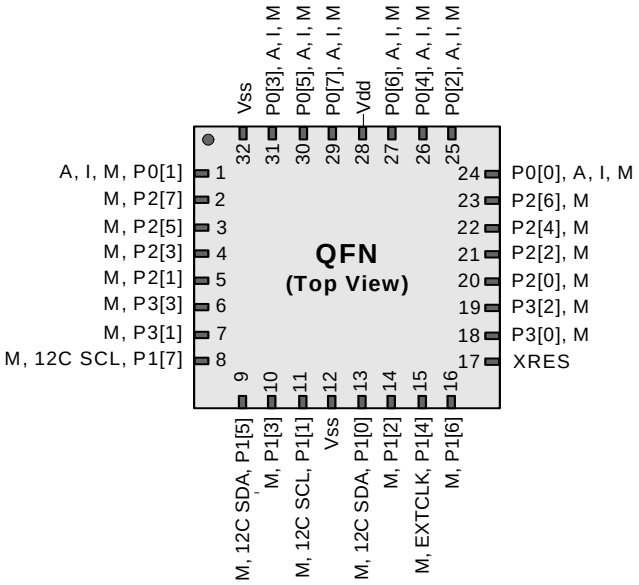


Table 2. Pin Definitions - CY8CTMG110 32-Pin (QFN)

Pin No.	Type		Name	Description
	Digital	Analog		
1	IO	I, M	P0[1]	Analog column mux input.
2	IO	M	P2[7]	
3	IO	M	P2[5]	
4	IO	M	P2[3]	
5	IO	M	P2[1]	
6	IO	M	P3[3]	
7	IO	M	P3[1]	
8	IO	M	P1[7]	I2C Serial Clock (SCL).
9	IO	M	P1[5]	I2C Serial Data (SDA).
10	IO	M	P1[3]	
11	IO	M	P1[1]	I2C Serial Clock (SCL), ISSP-SCLK[3].
12	Power		Vss	Ground. Connect to circuit ground.
13	IO	M	P1[0]	I2C Serial Data (SDA), ISSP-SDATA[3].
14	IO	M	P1[2]	
15	IO	M	P1[4]	Optional External Clock Input (EXTCLK).
16	IO	M	P1[6]	
17	Input		XRES	Active high external reset with internal pull down.
18	IO	M	P3[0]	
19	IO	M	P3[2]	

[+] Feedback

Table 2. Pin Definitions - CY8CTMG110 32-Pin (QFN) (continued)

Pin No.	Type		Name	Description
	Digital	Analog		
20	IO	M	P2[0]	
21	IO	M	P2[2]	
22	IO	M	P2[4]	
23	IO	M	P2[6]	
24	IO	I, M	P0[0]	Analog column mux input.
25	IO	I, M	P0[2]	Analog column mux input.
26	IO	I, M	P0[4]	Analog column mux input.
27	IO	I, M	P0[6]	Analog column mux input.
28	Power		Vdd	Supply voltage. Bypass to ground with 0.1 uF capacitor.
29	IO	I, M	P0[7]	Analog column mux input.
30	IO	I, M	P0[5]	Analog column mux input.
31	IO	I, M	P0[3]	Analog column mux input.
32	Power		Vss	Ground. Connect to circuit ground.
EP	Power		Vss	Exposed pad is internally connected to ground. Connect to circuit ground.

LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.

Note
3. These are the ISSP pins, that are not High Z at POR (Power On Reset). See the *PSoC Mixed Signal Array Technical Reference Manual* for details.

[+] Feedback

56-Pin Part Pinout

The 56-pin SSOP part is for the CY8CTMG110 On-Chip Debug (OCD) TrueTouch device.

Note This part is only used for in-circuit debugging. It is NOT available for production.

Figure 6. CY8CTMG110 56-Pin TrueTouch Device

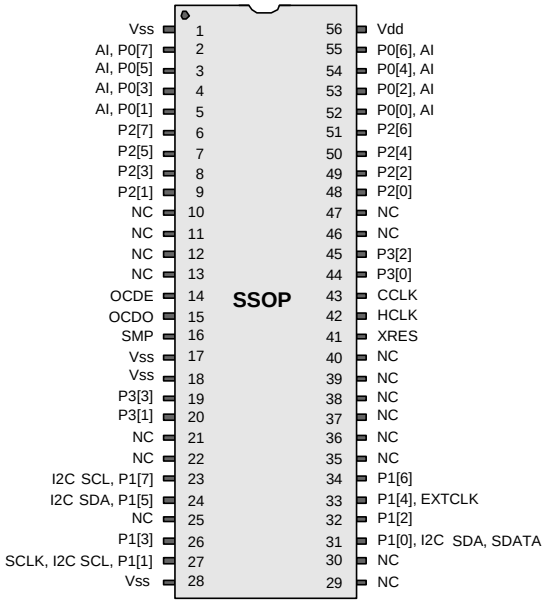


Table 3. Pin Definitions - CY8CTMG110 56-Pin (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	Power		Vss	Ground. Connect to circuit ground.
2	IO	I	P0[7]	Analog column mux input.
3	IO	I	P0[5]	Analog column mux input and column output.
4	IO	I	P0[3]	Analog column mux input and column output.
5	IO	I	P0[1]	Analog column mux input.
6	IO		P2[7]	
7	IO		P2[5]	
8	IO	I	P2[3]	Direct switched capacitor block input.
9	IO	I	P2[1]	Direct switched capacitor block input.
10			NC	No connection. Leave floating.
11			NC	No connection. Leave floating.
12			NC	No connection. Leave floating.
13			NC	No connection. Leave floating.
14	OCD		OCDE	OCD even data IO.
15	OCD		OCDO	OCD odd data output.
16	Power		SMP	Switch Mode Pump (SMP) connection to required external components.
17	Power		Vss	Ground. Connect to circuit ground.
18	Power		Vss	Ground. Connect to circuit ground.
19	IO		P3[3]	

[+] Feedback

Table 3. Pin Definitions - CY8CTMG110 56-Pin (SSOP) (continued)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
20	IO		P3[1]	
21			NC	No connection. Leave floating.
22			NC	No connection. Leave floating.
23	IO		P1[7]	I2C Serial Clock (SCL).
24	IO		P1[5]	I2C Serial Data (SDA).
25			NC	No connection. Leave floating.
26	IO		P1[3]	
27	IO		P1[1]	Crystal Input (XTALin), I2C Serial Clock (SCL), ISSP-SCLK[3].
28	Power		Vss	Ground. Connect to circuit ground.
29			NC	No connection. Leave floating.
30			NC	No connection. Leave floating.
31	IO		P1[0]	Crystal Output (XTALout), I2C Serial Data (SDA), ISSP-SDATA[3].
32	IO		P1[2]	
33	IO		P1[4]	Optional External Clock Input (EXTCLK).
34	IO		P1[6]	
35			NC	No connection. Leave floating.
36			NC	No connection. Leave floating.
37			NC	No connection. Leave floating.
38			NC	No connection. Leave floating.
39			NC	No connection. Leave floating.
40			NC	No connection. Leave floating.
41	Input		XRES	Active high external reset with internal pull down.
42	OCD		HCLK	OCD high-speed clock output.
43	OCD		CCLK	OCD CPU clock output.
44	IO		P3[0]	
45	IO		P3[2]	
46			NC	No connection. Leave floating.
47			NC	No connection. Leave floating.
48	IO	I	P2[0]	
49	IO	I	P2[2]	
50	IO		P2[4]	
51	IO		P2[6]	
52	IO	I	P0[0]	Analog column mux input.
53	IO	I	P0[2]	Analog column mux input and column output.
54	IO	I	P0[4]	Analog column mux input and column output.
55	IO	I	P0[6]	Analog column mux input.
56	Power		Vdd	Supply voltage. Bypass to ground with 0.1 uF capacitor.

LEGEND: A = Analog, I = Input, O = Output, and OCD = On-Chip Debug.

[+] Feedback

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CTMG110 TrueTouch device. For up to date electrical specifications, visit the web site http://www.cypress.com/psoc.

Specifications are valid for -40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C as specified, except where noted.

Refer Table 18 on page 19 for the electrical specifications on the internal main oscillator (IMO) using SLIMO mode.

Figure 7. Voltage versus CPU Frequency

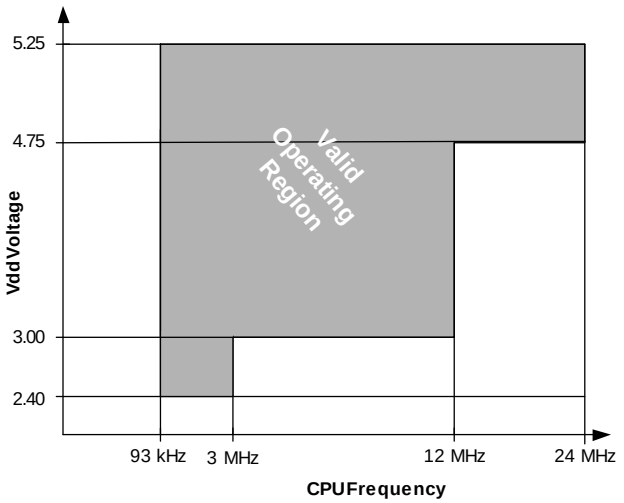


Figure 8. IMO Frequency Trim Options

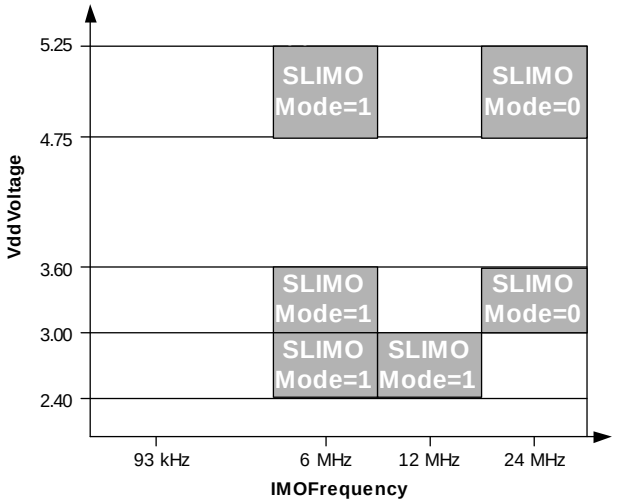


Table 4 lists the units of measure that are used in this section.

Table 4. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	µW	microwatts
dB	decibels	mA	milli-ampere
fF	femto farad	ms	milli-second
Hz	hertz	mV	milli-volts
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	Ω	ohm
MHz	megahertz	pA	picoampere
MΩ	megaohm	pF	picofarad
µA	microampere	pp	peak-to-peak
µF	microfarad	ppm	parts per million
µH	microhenry	ps	picosecond
µs	microsecond	sps	samples per second
µV	microvolts	s	sigma: one standard deviation
µVrms	microvolts root-mean-square	V	volts

[+] Feedback

Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	25	+100	^{o}C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25^{o}C ± 25^{o}C. Extended duration storage temperatures above 65^{o}C degrade reliability.
T_A	Ambient Temperature with Power Applied	-40	–	+85	^{o}C	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss - 0.5	–	Vdd + 0.5	V	
V_{IOZ}	DC Voltage Applied to Tri-state	Vss - 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
ESD	Electro Static Discharge Voltage[4]	2000	–	–	V	Human Body Model ESD.
LU	Latch-up Current	–	–	200	mA	

Operating Temperature

Table 6. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature[5]	-40	–	+85	^{o}C	
T_J	Junction Temperature	-40	–	+100	^{o}C	The temperature rise from ambient to junction is package specific. See Table 33 on page 28. The user must limit the power consumption to comply with this requirement.

Notes
4. See the user module data sheet for touchscreen application related ESD testing.
5. See the user module data sheet for touchscreen application related temperature testing.

[+] Feedback

DC Electrical Characteristics

The below electrical characteristics are for proper CPU core and I/O operation. For capacitive touchscreen electrical characteristics, refer to the touchscreen user module data sheet.

DC Chip Level Specifications

Table 7 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.7V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only.

Table 7. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd	Supply Voltage	2.40	–	5.25	V	See Table 16 on page 17.
I_{DD}	Supply Current, IMO = 24 MHz	–	3	4	mA	Conditions are Vdd = 5.0V, T_A = 25°C, CPU = 3 MHz, 48 MHz disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz.
I_{DD3}	Supply Current, IMO = 6 MHz using SLIMO Mode	–	1.2	2	mA	Conditions are Vdd = 3.3V, T_A = 25°C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz.
I_{DD27}	Supply Current, IMO = 6 MHz using SLIMO Mode	–	1.1	1.5	mA	Conditions are Vdd = 2.55V, T_A = 25°C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz.
I_{SB27}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and Internal Slow Oscillator Active. Mid temperature range	–	2.6	4.	µA	Vdd = 2.55V, 0°C ≤ T_A ≤ 40°C.
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and Internal Slow Oscillator Active	–	2.8	5	µA	Vdd = 3.3V, -40°C ≤ T_A ≤ 85°C.
V_{REF}	Reference Voltage (Bandgap)	1.28	1.30	1.32	V	Trimmed for appropriate Vdd. Vdd = 3.0V to 5.25V.
V_{REF27}	Reference Voltage (Bandgap)	1.16	1.30	1.33	V	Trimmed for appropriate Vdd. Vdd = 2.4V to 3.0V.
AGND	Analog Ground	V_{REF} - 0.003	V_{REF}	V_{REF} + 0.003	V	

DC General Purpose IO Specifications

Table 8 and Table 9 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C. These are for design guidance only.

Table 8. 5V and 3.3V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull Up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull Down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vdd - 1.0	–	–	V	IOH = 10 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])).
V_{OL}	Low Output Level	–	–	0.75	V	IOL = 25 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])).
V_{IL}	Input Low Level	–	–	0.8	V	Vdd = 3.0 to 5.25.
V_{IH}	Input High Level	2.1	–		V	Vdd = 3.0 to 5.25.

[+] Feedback

Table 8. 5V and 3.3V DC GPIO Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
V_H	Input Hysteresis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.

Table 9. 2.7V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull Up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull Down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vdd - 0.4	–	–	V	IOH = 2.5 mA (6.25 Typ), Vdd = 2.4 to 3.0V (16 mA maximum, 50 mA Typ combined IOH budget).
V_{OL}	Low Output Level	–	–	0.75	V	IOL = 10 mA, Vdd = 2.4 to 3.0V (90 mA maximum combined IOL budget).
V_{IL}	Input Low Level	–	–	0.75	V	Vdd = 2.4 to 3.0.
V_{IH}	Input High Level	2.0	–	–	V	Vdd = 2.4 to 3.0.
V_H	Input Hysteresis	–	90	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.

DC Operational Amplifier Specifications

Table 10, Table 11, and Table 12 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only.

Table 10. 5V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (Absolute Value)	–	2.5	15	mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	10	–	μV/°C	
I_{EBOA}[6]	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 μA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range	0.0	–	Vdd - 1	V	
G_{OLOA}	Open Loop Gain	–	80	–	dB	
I_{SOA}	Amplifier Supply Current	–	10	30	μA	

Note
6. Atypical behavior: I_{EBOA} of Port 0 Pin 0 is below 1 nA at 25°C; 50 nA over temperature. Use Port 0 Pins 1-7 for the lowest leakage of 200 nA.

[+] Feedback

Table 11. 3.3V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	10	–	µV/°C	
I_{EBOA}[6]	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range	0	–	Vdd - 1	V	
G_{OLOA}	Open Loop Gain	–	80	–	dB	
I_{SOA}	Amplifier Supply Current	–	10	30	µA	

Table 12. 2.7V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	10	–	µV/°C	
I_{EBOA}[6]	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range	0	–	Vdd - 1	V	
G_{OLOA}	Open Loop Gain	–	80	–	dB	
I_{SOA}	Amplifier Supply Current	–	10	30	µA	

DC Low Power Comparator Specifications

Table 13 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V at 25°C. These are for design guidance only.

Table 13. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low Power Comparator (LPC) Reference Voltage Range	0.2	–	Vdd - 1	V	
I_{SLPC}	LPC Supply Current	–	10	40	µA	
V_{OSLPC}	LPC Voltage Offset	–	2.5	30	mV	

DC Analog Mux Bus Specifications

Table 14 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only.

Table 14. DC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{SW}	Switch Resistance to Common Analog Bus	–	–	400 800	W W	Vdd ≥ 2.7V 2.4V ≤ Vdd ≤ 2.7V
R_{VDD}	Resistance of Initialization Switch to Vdd	–	–	800	W	

[+] Feedback

DC IDAC Resolution

Table 15 lists IDAC typical resolution. Typical parameters apply to 5V at 25°C. These are for design guidance only.

Table 15. DC IDAC Resolution

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DAC}	Current Output of 1 LSB (1x Setting)	-	90	-	nA	

DC POR and LVD Specifications

Table 16 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only.

Table 16. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	Vdd Value for PPOR Trip					Vdd must be greater than or equal to 2.5V during startup, reset from the XRES pin, or reset from Watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b		2.82	2.95	V	
V_{PPOR2}	PORLEV[1:0] = 10b		4.55	4.70	V	
	Vdd Value for LVD Trip					
V_{LVD0}	VM[2:0] = 000b	2.40	2.45	2.51[7]	V	
V_{LVD1}	VM[2:0] = 001b	2.85	2.92	2.99[8]	V	
V_{LVD2}	VM[2:0] = 010b	2.95	3.02	3.09	V	
V_{LVD3}	VM[2:0] = 011b	3.06	3.13	3.20	V	
V_{LVD4}	VM[2:0] = 100b	4.37	4.48	4.55	V	
V_{LVD5}	VM[2:0] = 101b	4.50	4.64	4.75	V	
V_{LVD6}	VM[2:0] = 110b	4.62	4.73	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.81	4.95	V	
	Vdd Value for PUMP Trip					
V_{PUMP0}	VM[2:0] = 000b	2.45	2.55	2.62[9]	V	
V_{PUMP1}	VM[2:0] = 001b	2.96	3.02	3.09	V	
V_{PUMP2}	VM[2:0] = 010b	3.03	3.10	3.16	V	
V_{PUMP3}	VM[2:0] = 011b	3.18	3.25	3.32[10]	V	
V_{PUMP4}	VM[2:0] = 100b	4.54	4.64	4.74	V	
V_{PUMP5}	VM[2:0] = 101b	4.62	4.73	4.83	V	
V_{PUMP6}	VM[2:0] = 110b	4.71	4.82	4.92	V	
V_{PUMP7}	VM[2:0] = 111b	4.89	5.00	5.12	V	

Notes
7. Always greater than 50 mV above V_{PPOR} (PORLEV = 00) for falling supply.
8. Always greater than 50 mV above V_{PPOR} (PORLEV = 01) for falling supply.
9. Always greater than 50 mV above V_{LVD0}.
10. Always greater than 50 mV above V_{LVD3}

[+] Feedback

DC Programming Specifications

Table 17 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only.

Table 17. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd_{IWRITE}	Supply Voltage for Flash Write Operations	2.70	–	–	V	
I_{DDP}	Supply Current During Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[11]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

Note

11. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

[+] Feedback

AC Electrical Characteristics

AC Chip Level Specifications

Table 18 and Table 19 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only.

Table 18. 5V and 3.3V AC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	Internal Main Oscillator Frequency for 24 MHz	23.4	24	24.6[12,13,14]	MHz	Trimmed for 5V or 3.3V operation using factory trim values. See Figure 8 on page 12. SLIMO mode = 0.
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.75	6	6.35[12,13,14]	MHz	Trimmed for 5V or 3.3V operation using factory trim values. See Figure 8 on page 12. SLIMO mode = 1.
F_{CPU1}	CPU Frequency (5V Nominal)	0.93	24	24.6[12,13]	MHz	24 MHz only for SLIMO mode = 0.
F_{CPU2}	CPU Frequency (3.3V Nominal)	0.93	12	12.3[13,14]	MHz	
F_{BLK5}	Digital PSoC Block Frequency (5V Nominal)	0	48	49.2[12,13,15]	MHz	Refer to the AC digital block specifications.
F_{BLK33}	Digital PSoC Block Frequency (3.3V Nominal)	0	24	24.6[13,15]	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
Jitter32k	32 kHz RMS Period Jitter	–	100	200	ns	
Jitter32k	32 kHz Peak-to-Peak Period Jitter	–	1400	–		
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Fout48M	48 MHz Output Frequency	46.8	48.0	49.2[12,14]	MHz	Trimmed. Using factory trim values.
Jitter24M1	24 MHz Peak-to-Peak Period Jitter (IMO)	–	600		ps	
F_{MAX}	Maximum Frequency of signal on row input or row output	–	–	12.3	MHz	
T_{RAMP}	Supply Ramp Time	0	–	–	µs	

Table 19. 2.7V AC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO12}	Internal Main Oscillator Frequency for 12 MHz	11.5	12	12.7[13,16,17],	MHz	Trimmed for 2.7V operation using factory trim values. See Figure 8 on page 12. SLIMO mode = 1.
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.75	6	6.35[13,16,17]	MHz	Trimmed for 2.7V operation using factory trim values. See Figure 8 on page 12. SLIMO mode = 1.
F_{CPU1}	CPU Frequency (2.7V Nominal)	0.093	3	3.15[13,16]	MHz	24 MHz only for SLIMO mode = 0.
F_{BLK27}	Digital PSoC Block Frequency (2.7V Nominal)	0	12	12.5[13,16,17]	MHz	Refer to the AC digital block specifications.

Notes
12. 4.75V < Vdd < 5.25V.
13. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
14. 3.0V < Vdd < 3.6V. See Application Note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3V.
15. See the individual user module data sheets for information on maximum frequencies for user modules.

[+] Feedback

Table 19. 2.7V AC Chip Level Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
F_{32K1}	Internal Low Speed Oscillator Frequency	8	32	96	kHz	
Jitter32k	32 kHz RMS Period Jitter	–	150	200	ns	
Jitter32k	32 kHz Peak-to-Peak Period Jitter	–	1400	–		
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
F_{MAX}	Maximum Frequency of signal on row input or row output.	–	–	12.3	MHz	
T_{RAMP}	Supply Ramp Time	0	–	–	µs	

Figure 9. 24 MHz Period Jitter (IMO) Timing Diagram

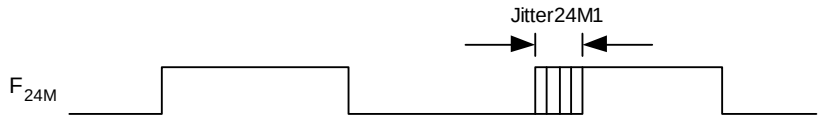
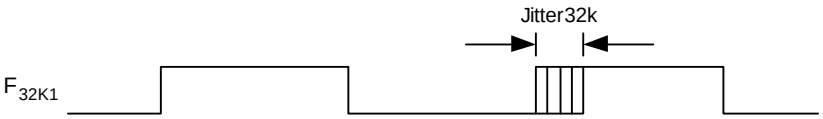


Figure 10. 32 kHz Period Jitter (ILO) Timing Diagram



Notes
16. 2.4V < Vdd < 3.0V.
17. See Application Note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on maximum frequency for user modules.

[+] Feedback

AC General Purpose IO Specifications

Table 20 and Table 21 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only.

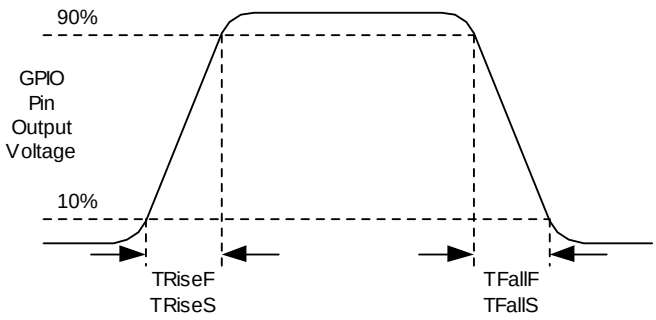
Table 20. 5V and 3.3V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	7	27	–	ns	Vdd = 3 to 5.25V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	7	22	–	ns	Vdd = 3 to 5.25V, 10% - 90%

Table 21. 2.7V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	3	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	6	–	50	ns	Vdd = 2.4 to 3.0V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	6	–	50	ns	Vdd = 2.4 to 3.0V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	18	40	120	ns	Vdd = 2.4 to 3.0V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	18	40	120	ns	Vdd = 2.4 to 3.0V, 10% - 90%

Figure 11. GPIO Timing Diagram



AC Operational Amplifier Specifications

Table 22 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only.

Table 22. AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{COMP}	Comparator Mode Response Time, 50 mV Overdrive			100 200	ns ns	Vdd ≥ 3.0V. 2.4V < Vcc < 3.0V.

[+] Feedback

AC Low Power Comparator Specifications

Table 23 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V at 25°C. These are for design guidance only.

Table 23. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RLPC}	LPC Response Time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}.

AC Analog Mux Bus Specifications

Table 24 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only.

Table 24. AC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{SW}	Switch Rate	–	–	3.17	MHz	

AC Digital Block Specifications

Table 25 and Table 26 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only.

Table 25. 5V and 3.3V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All Functions	Maximum Block Clocking Frequency (> 4.75V)			49.2	MHz	4.75V < Vdd < 5.25V.
	Maximum Block Clocking Frequency (< 4.75V)			24.6	MHz	3.0V < Vdd < 4.75V.
Timer	Capture Pulse Width	50[18]	–	–	ns	
	Maximum Frequency, No Capture	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, With or Without Capture	–	–	24.6	MHz	
Counter	Enable Pulse Width	50	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, Enable Input	–	–	24.6	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50	–	–	ns	
	Disable Mode	50	–	–	ns	
	Maximum Frequency	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	24.6	MHz	
SPIM	Maximum Input Clock Frequency	–	–	8.2	MHz	Maximum data rate at 4.1 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.1	MHz	
	Width of SS_ Negated Between Transmissions	50	–	–	ns	

Note
18. 50 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

[+] Feedback

Table 25. 5V and 3.3V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
Transmitter	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
	Maximum Input Clock Frequency with Vdd ≥ 4.75V, 2 Stop Bits	–	–	49.2	MHz	Maximum data rate at 6.15 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
	Maximum Input Clock Frequency with Vdd ≥ 4.75V, 2 Stop Bits	–	–	49.2	MHz	Maximum data rate at 6.15 MHz due to 8 x over clocking.

Table 26. 2.7V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All Functions	Maximum Block Clocking Frequency			12.7	MHz	2.4V < Vdd < 3.0V.
Timer	Capture Pulse Width	100[19]	–	–	ns	
	Maximum Frequency, With or Without Capture	–	–	12.7	MHz	
Counter	Enable Pulse Width	100	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	12.7	MHz	
	Maximum Frequency, Enable Input	–	–	12.7	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	100	–	–	ns	
	Disable Mode	100	–	–	ns	
	Maximum Frequency	–	–	12.7	MHz	
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	12.7	MHz	
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	12.7	MHz	
SPIM	Maximum Input Clock Frequency	–	–	6.35	MHz	Maximum data rate at 3.17 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.1	MHz	
	Width of SS_ Negated Between Transmissions	100	–	–	ns	
Transmitter	Maximum Input Clock Frequency	–	–	12.7	MHz	Maximum data rate at 1.59 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency	–	–	12.7	MHz	Maximum data rate at 1.59 MHz due to 8 x over clocking.

Note
19. 100 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

[+] Feedback

AC External Clock Specifications

Table 27, Table 28, and Table 29 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only.

Table 27. 5V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz
–	High Period	20.6	–	5300	ns
–	Low Period	20.6	–	–	ns
–	Power Up IMO to Switch	150	–	–	µs

Table 28. 3.3V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU Clock divide by 1	0.093	–	12.3	MHz	Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU Clock divide by 2 or greater	0.186	–	24.6	MHz	If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High Period with CPU Clock divide by 1	41.7	–	5300	ns	
–	Low Period with CPU Clock divide by 1	41.7	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

Table 29. 2.7V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU Clock divide by 1	0.093	–	3.08	MHz	Maximum CPU frequency is 3 MHz at 2.7V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU Clock divide by 2 or greater	0.186	–	6.35	MHz	If the frequency of the external clock is greater than 3 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High Period with CPU Clock divide by 1	160	–	5300	ns	
–	Low Period with CPU Clock divide by 1	160	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

[+] Feedback

AC Programming Specifications

Table 30 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only.

Table 30. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Setup Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash Erase Time (Block)	–	15	–	ms	
T_{WRITE}	Flash Block Write Time	–	30	–	ms	
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns	3.6 < Vdd
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	50	ns	3.0 ≤ Vdd ≤ 3.6
T_{DSCLK2}	Data Out Delay from Falling Edge of SCLK	–	–	70	ns	2.4 ≤ Vdd ≤ 3.0

AC I^2C Specifications

Table 31 and Table 32 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C. These are for design guidance only.

Table 31. AC Characteristics of the I^2C SDA and SCL Pins for Vdd ≥ 3.0V

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs
$T_{SUSTAI2C}$	Set-up Time for a Repeated START Condition	4.7	–	0.6	–	µs
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs
$T_{SUDATI2C}$	Data Set-up Time	250	–	100[20]	–	ns
$T_{SUSTOI2C}$	Set-up Time for STOP Condition	4.0	–	0.6	–	µs
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs
T_{SPI2C}	Pulse Width of Spikes are Suppressed by the Input Filter.	–	–	0	50	ns

Note

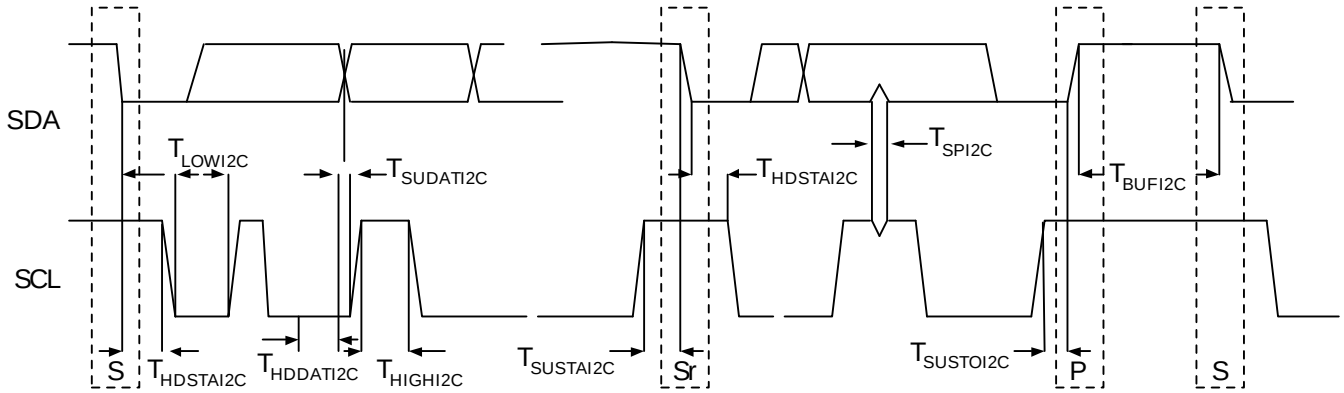
20. A Fast-Mode I2C-bus device may be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

[+] Feedback

Table 32. 2.7V AC Characteristics of the I²C SDA and SCL Pins (Fast Mode not Supported)

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL Clock Frequency	0	100	–	–	kHz
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	–	–	µs
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	–	–	µs
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	–	–	µs
$T_{SUSTAI2C}$	Setup Time for a Repeated START Condition	4.7	–	–	–	µs
$T_{HDDATI2C}$	Data Hold Time	0	–	–	–	µs
$T_{SUDATI2C}$	Data Setup Time	250	–	–	–	ns
$T_{SUSTOI2C}$	Setup Time for STOP Condition	4.0	–	–	–	µs
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	–	–	µs
T_{SPI2C}	Pulse Width of Spikes are Suppressed by the Input Filter.	–	–	–	–	ns

Figure 12. Definition for Timing for Fast/Standard Mode on the I²C Bus



[+] Feedback

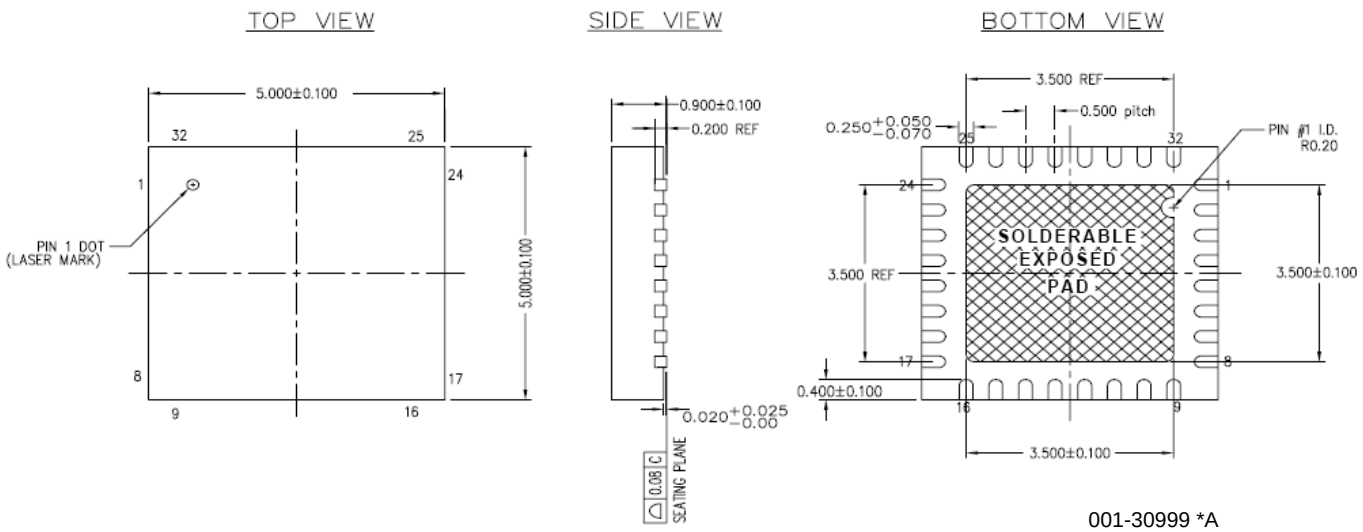
Packaging Information

This section shows the packaging specifications for the CY8CTMG110 TrueTouch device with the thermal impedances for each package.

It is important to note that emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR10161.

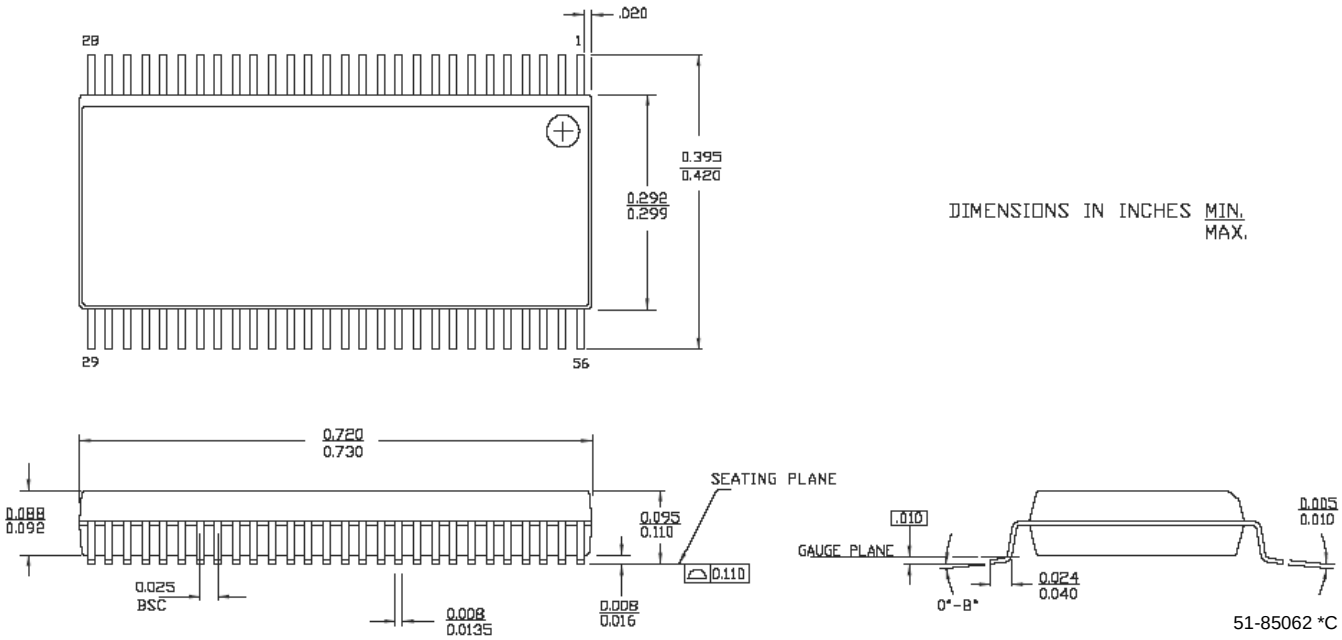
For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

Figure 13. 32-Pin Sawn QFN Package



[+] Feedback

Figure 14. 56-Pin (300-Mil) SSOP



Thermal Impedances

Table 33. Thermal Impedances per Package

Package	Typical θ_{JA} [21]	Typical θ_{JC}
32 QFN[21] 5x5 mm 0.93 MAX	22 °C/W	12 °C/W

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 34. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature[23]	Maximum Peak Temperature
32 QFN	240°C	260°C

Notes
21. $T_J = T_A$ + Power x θ_{JA}.
22. To achieve the thermal impedance specified for the ** package, the center thermal pad is soldered to the PCB ground plane.
23. Higher temperatures is required based on the solder melting point. Typical temperatures for solder are 220 ± 5oC with Sn-Pb or 245 ± 5oC with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

[+] Feedback

Development Tool Selection

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. Used by thousands of PSoC developers, this robust software has been facilitating PSoC designs for half a decade. PSoC Designer is available free of charge at http://www.cypress.com under Design Resources > Software and Drivers.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer or PSoC Express. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com/psocprogrammer.

Hi-Tech C Lite Compiler

Hi-Tech C Lite is an ANSI C compiler optimized for PSoC to deliver dense, efficient executable code for a smaller-than-ever footprint. Hi-Tech C Lite can be downloaded at http://www.cypress.htsoft.com. To install the HI-TECH Lite version, download the complier installation file from HI-TECH and choose the Lite option when prompted for a registration key. The Lite version can be upgraded to the 45-day full featured evaluation version or the PRO version at any time, however the PRO version can only be enabled with a purchased registration key.

Hi-Tech C Pro Compiler

Hi-Tech C Pro is an optional upgrade to PSoC Designer that offers all of the benefits of Hi-Tech C Lite with additional features. Hi-Tech C Pro is available for purchase either at the Cypress Online Store or at http://www.cypress.htsoft.com. Hi-Tech C Pro is recommended for touchscreen applications using the Multi-Touch All-Point CY8CTMA120 device.

CY3202-C iMAGEcraft C Compiler

CY3202 is the optional upgrade to PSoC Designer that enables the iMAGEcraft C compiler. It can be purchased from the Cypress Online Store. At http://www.cypress.com, click the Online Store shopping cart icon at the bottom of the web page, and click *PSoC (Programmable System-on-Chip)* to view a current list of available items.

Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows a user to program PSoC devices through the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC through a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- 3 Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.
Note CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

[+] Feedback

Accessories (Emulation and Programming)

Third Party Tools

Several tools have been specially designed by the following third party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at http://www.cypress.com under Design Resources > Evaluation Boards.

Build a PSoC Emulator into Your Board

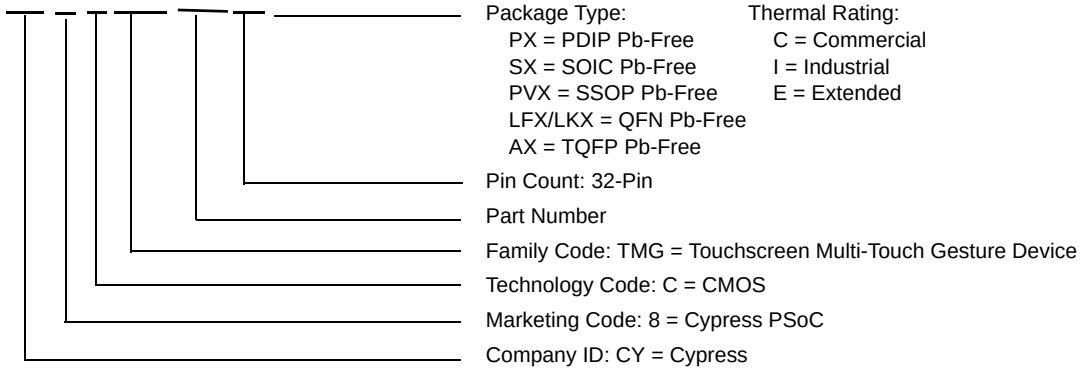
For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, see application note AN2323 “Debugging - Build a PSoC Emulator into Your Board”.

Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Temperature Range	Single-Touch Enabled	Multi-Touch Gesture Enabled	Multi-Touch All-Point Enabled	X/Y Sensor Inputs
32-Pin (5x5 mm 0.93 MAX) SAWN QFN	CY8CTMG110-32LTXI	8K	512	-40°C to +85°C	Y	Y	N	Up to 24
32-Pin (5x5 mm 0.93 MAX) SAWN QFN (Tape and Reel)	CY8CTMG110-32LTXIT	8K	512	-40°C to +85°C	Y	Y	N	Up to 24
56-Pin OCD SSOP	CY8CTMG110-00PVXI	8K	512	-40°C to +85°C	Y	Y	N	Up to 24

Ordering Code Definitions

CY 8 C TMG xxx-32xx



[+] Feedback

Document History Page

Document Title: CY8CTMG110 TrueTouch™ Multi-Touch Gesture Touchscreen Controller Document Number: 001-46928				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2518134	DSO/AESA	06/18/08	New data sheet
*A	2523303	DSO/PYRS	07/01/08	Updated X/Y sensor inputs to 24 and supported screen sizes to 4.6” and below Changed operating voltage range to 2.7V to 5.25V.
*B	2549257	YOM/PYRS	08/06/08	Added other sections based on PSoC data sheets

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