CY7C53150
CY7C53120

Neuron® Chip Network Processor

Features

- **Three eight-bit pipelined processors for concurrent processing of application code and network traffic**
- **11-pin I/O port programmable in 34 modes for fast application program development**
- **Two 16-bit timer/counters for measuring and generating I/O device waveforms**
- **Five-pin communication port that supports direct connect and network transceiver interfaces**
- **Programmable pull-ups on IO4–IO7 and 20-mA sink current on IO0–IO3**
- **Unique 48-bit ID number in every device to facilitate network installation and management**
- **Low operating current; sleep mode operation for reduced current consumption[1]**
- **0.35-μm Flash process technology**
- **5.0V operation**
- **On-chip LVD circuit to prevent nonvolatile memory corruption during voltage drops**
- **2,048 bytes of SRAM for buffering network data, system, and application data storage**
- **512 bytes (CY7C53150), 2048 bytes (CY7C53120E2), 4096 bytes (CY7C53120E4) of Flash memory with on-chip charge pump for flexible storage of configuration data and application code**
- **Addresses up to 58 KB of external memory (CY7C53150)**
- **10 KB (CY7C53120E2), 12 KB (CY7C53120E4) of ROM containing LonTalk® network protocol firmware**
- **Maximum input clock operation of 20 MHz (CY7C53150), 10 MHz (CY7C53120E2), 40 MHz (CY7C53120E4) over a –40°C to 85°C[2] temperature range**
- **64-pin TQFP package (CY7C53150)**
- **32-pin SOIC or 44-pin TQFP package (CY7C53120)**

Functional Description

The CY7C531x0 Neuron® chip implements a node for LonWorks® distributed intelligent control networks. It incorporates, on a single chip, the necessary communication and control functions, both in hardware and firmware, that facilitate the design of a LonWorks node.

The CY7C531x0 contains a very flexible five-pin communication port that can be configured to interface with a wide variety of media transceivers at a wide range of data rates. The most common transceiver types are twisted-pair, powerline, RF, IR, fiber-optics, and coaxial.

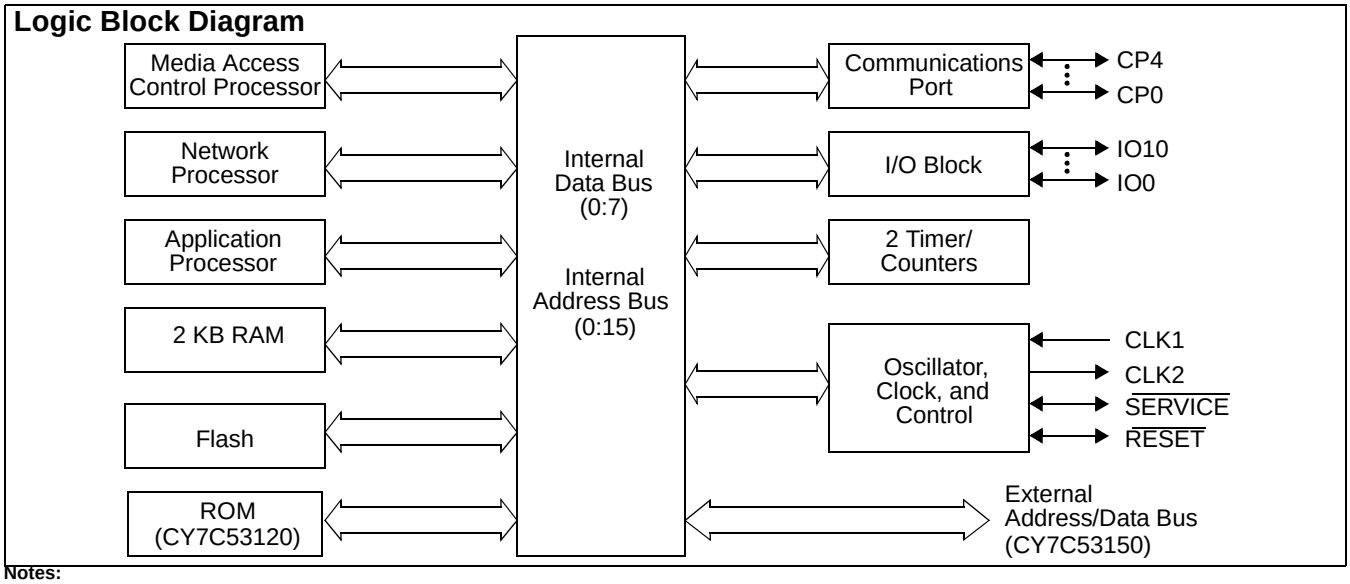
The CY7C531x0 is manufactured using state-of-the-art 0.35-μm Flash technology, providing to designers the most cost-effective Neuron chip solution.

Services at every layer of the OSI networking reference model are implemented in the LonTalk firmware-based protocol stored in 10-KB ROM (CY7C53120E2), 12-KB ROM (CY7C53120E4), or off-chip memory (CY7C53150). The firmware also contains 34 preprogrammed I/O drivers, greatly simplifying application programming. The application program is stored in the Flash memory (CY7C53120) and/or off-chip memory (CY7C53150), and may be updated by downloading over the network.

The CY7C53150 incorporates an external memory interface that can address up to 64 KB with 6 KB of the address space mapped internally. LonWorks nodes that require large application programs can take advantage of this external memory capability.

The CY7C53150 Neuron chip is an exact replacement for the Motorola MC143150Bx and Toshiba TMPN3150B1 devices. The CY7C53120E2 Neuron chip is an exact replacement for the Motorola MC143120E2 device since it contains the same firmware in ROM.

Logic Block Diagram

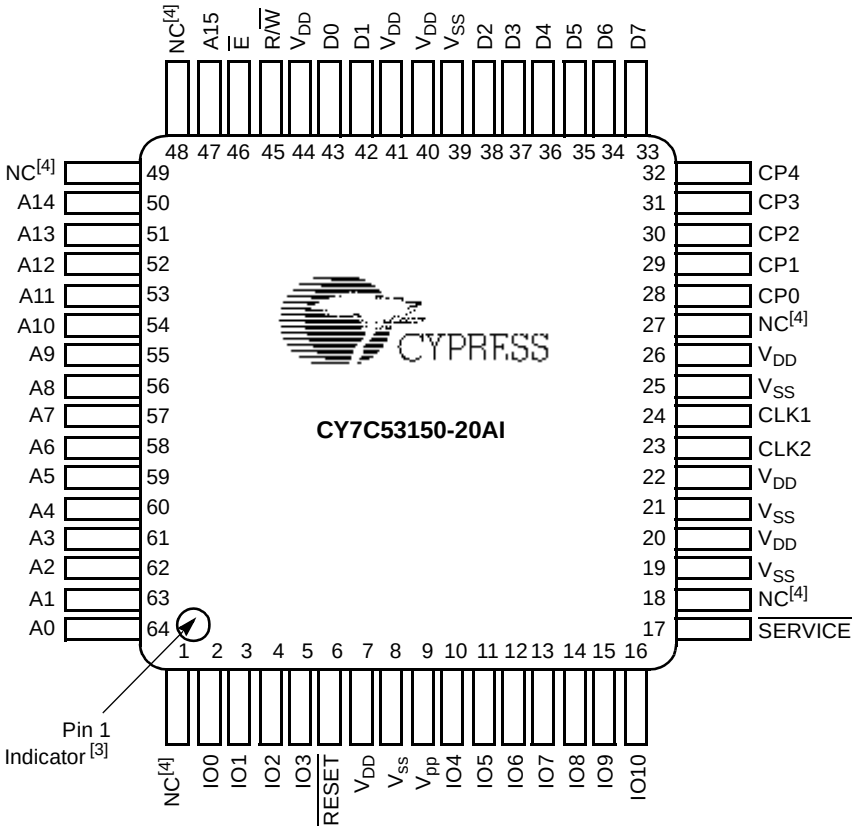


Notes:

1. Rare combinations of wake-up events occurring during the go to sleep sequence could produce unexpected sleep behavior. For details please refer to Cypress's *Neuron Metastability Description* application note.
2. Maximum Junction Temperature is 105°C. $T_{Junction} = T_{Ambient} + V \bullet I \bullet \theta_{JA}$. 32-pin SOIC θ_{JA} = 51C/W. 44-pin TQFP θ_{JA} = 43C/W. 64-pin TQFP θ_{JA} = 44C/W.

Pin Configurations

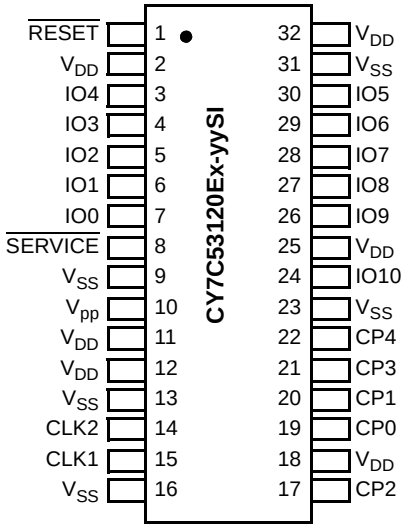
CY7C53150
64-lead Thin Quad Flat Pack



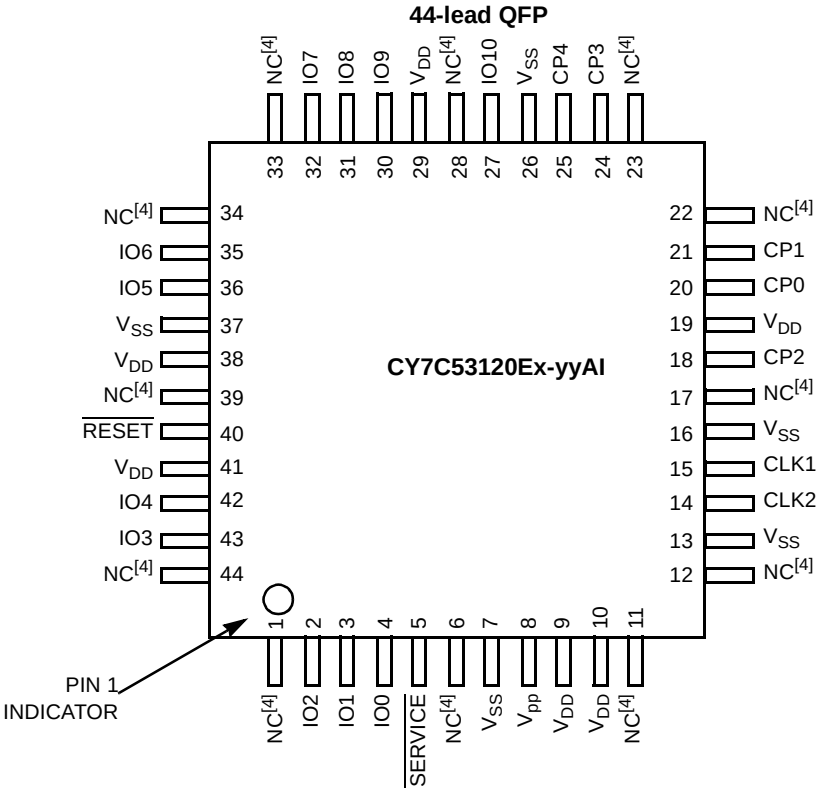
Notes:
3. The smaller dimple at the bottom left of the marking indicates pin 1.
4. No Connect (NC) — Should not be used. (These pins may be used for internal testing.)

Pin Configurations (continued)

32-lead SOIC



44-lead QFP



Pin Descriptions

Pin Name	I/O	Pin Function	CY7C53150 TQFP-64 Pin No.	CY7C53120xx SOIC-32 Pin No.	CY7C53120xx TQFP-44 Pin No.
CLK1	Input	**Oscillator connection or external clock input**.	24	15	15
CLK2	Output	**Oscillator connection**. Leave open when external clock is input to CLK1. Maximum of one external load.	23	14	14
$\overline{\text{RESET}}$	I/O (Built-In Pull-up)	**Reset pin (active LOW)**. Note. The allowable external capacitance connected to the RESET pin is 100 –1000 pF.	6	1	40
$\overline{\text{SERVICE}}$	I/O (Built-In Configurable Pull-up)	**Service pin (active LOW)**. Alternates between input and output at a 76-Hz rate.	17	8	5
IO0–IO3	I/O	**Large current-sink capacity (20 mA)**. General I/O port. The output of timer/ counter 1 may be routed to IO0. The output of timer/counter 2 may be routed to IO1.	2, 3, 4, 5	7, 6, 5, 4	4, 3, 2, 43
IO4–IO7	I/O (Built-In Configurable Pull-ups)	**General I/O port**. The input to timer/counter 1 may be derived from one of IO4–IO7. The input to timer/counter 2 may be derived from IO4.	10, 11, 12, 13	3, 30, 29, 28	42, 36, 35, 32
IO8–IO10	I/O	**General I/O port**. May be used for serial communication under firmware control.	14, 15, 16	27, 26, 24	31, 30, 27
D0–D7	I/O	**Bidirectional memory data bus**.	43, 42, 38, 37, 36, 35, 34, 33	N/A	N/A
R/$\overline{\text{W}}$	Output	**Read/write control output for external memory**.	45	N/A	N/A
$\overline{\text{E}}$	Output	**Enable clock control output for external memory**.	46	N/A	N/A
A0–A15	Output	**Memory address output port**.	64, 63, 62, 61, 60, 59, 58, 57, 56, 55, 54, 53, 52, 51, 50, 47	N/A	N/A
V_{DD}	Input	**Power input (5V nom)**. All V_{DD} pins must be connected together externally.	7, 20, 22, 26, 40, 41, 44	2, 11, 12, 18, 25, 32	9, 10, 19, 29, 38, 41
V_{SS}	Input	**Power input (0V, GND)**. All V_{SS} pins must be connected together externally.	8,19, 21, 25, 39	9, 13, 16, 23, 31	7,13, 16, 26, 37
Vpp	Input	**In-circuit test mode control**. If Vpp is high when $\overline{\text{RESET}}$ is asserted, the I/O, address and data buses become Hi-Z.	9	10	8
CP0–CP4	Communication Network Interface	**Bidirectional port supporting communications in three modes**.	28, 29, 30, 31, 32	19, 20, 17, 21, 22	20, 21, 18, 24, 25
NC	—	**No connect**. Must not be connected on the user's PC board, since they may be connected internal to the chip.	1, 18, 27, 48, 49	N/A	1, 6, 11, 12, 17, 22, 23, 28, 33, 34, 39, 44

Memory Usage

All Neuron chips require system firmware to be present when they are powered up. In the case of the CY7C53120 family, this firmware is preprogrammed in the factory in an on-chip ROM. In the case of the CY7C53150, the system firmware must be present in the first 16 KB of an off-chip nonvolatile memory such as Flash, EPROM, EEPROM, or NVRAM. These devices must be programmed in a device programmer before board assembly. Because the system firmware implements the network protocol, it cannot itself be downloaded over the network.

For the CY7C53120 family, the user application program is stored in on-chip Flash memory. It may be programmed using a device programmer before board assembly, or may be

downloaded and updated over the LonTalk network from an external network management tool.

For the CY7C53150, the user application program is stored in on-chip Flash Memory and also in off-chip memory. The user program may initially be programmed into the off-chip memory device using a device programmer.

Flash Memory Retention and Endurance

Data and code stored in Flash Memory is guaranteed to be retained for at least 10 years for programming temperature range of –25°C to 85°C.

The Flash Memory can typically be written 100,000 times without any data loss.[5] An erase/write cycle takes 20 ms. The system firmware extends the effective endurance of Flash memory in two ways. If the data being written to a byte of Flash memory is the same as the data already present in that byte, the firmware does not perform the physical write. So for example, an application that sets its own address in Flash memory after every reset will not use up any write cycles if the address has not changed. In addition, system firmware version 13.1 or higher is able to aggregate writes to eight successive address locations into a single write for CY7C53120E4 devices. For example, if 4 KB of code is downloaded over the network, the firmware would execute only 512 writes rather than 4,096.

40-MHz 3120 Operation

The CY7C53120E4-40 device was designed to run at frequencies up to 40 MHz using an external clock oscillator. It is important to note that external oscillators may typically take on the order of 5 ms to stabilize after power-up. The Neuron chip should be held in reset until the CLK1 input is stable. With some oscillators, this may require the use of a reset-stretching Low-Voltage Detection chip/circuit. Check the oscillator vendor's specification for more information about start-up stabilization times.

Low-Voltage Inhibit Operation

The on-chip Low-voltage Inhibit circuit trips the Neuron chip whenever the V_{DD} input is less than 4.1 ± 0.3V. This feature prevents the corruption of nonvolatile memory during voltage drops.

Communications Port

The Neuron chip includes a versatile 5-pin communications port that can be configured in three different ways. In Single-Ended Mode, pin CP0 is used for receiving serial data, pin CP1 for transmitting serial data, and pin CP2 enables an external transceiver. Data is communicated using Differential Manchester encoding.

In Special Purpose Mode, pin CP0 is used for receiving serial data, pin CP1 for transmitting serial data, pin CP2 transmits a bit clock, and pin CP4 transmits a frame clock for use by an external intelligent transceiver. In this mode, the external transceiver is responsible for encoding and decoding the data stream.

In Differential Mode, pins CP0 and CP1 form a differential receiver with built-in programmable hysteresis and low-pass filtering. Pins CP2 and CP3 form a differential driver. Serial data is communicated using Differential Manchester encoding. The following tables describe the communications port when used in Differential Mode.

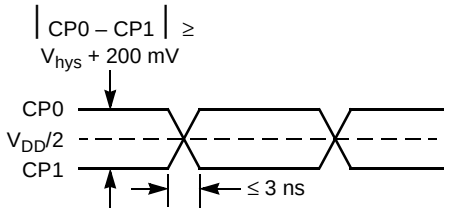


Figure 1. Receiver Input Waveform

Programmable Hysteresis Values
(Expressed as differential peak-to-peak voltages in terms of V_{DD})

Hysteresis[6]	V_{hys} Min.	V_{hys} Typ.	V_{hys} Max.
0	0.019 V_{DD}	0.027 V_{DD}	0.035 V_{DD}
1	0.040 V_{DD}	0.054 V_{DD}	0.068 V_{DD}
2	0.061 V_{DD}	0.081 V_{DD}	0.101 V_{DD}
3	0.081 V_{DD}	0.108 V_{DD}	0.135 V_{DD}
4	0.101 V_{DD}	0.135 V_{DD}	0.169 V_{DD}
5	0.121 V_{DD}	0.162 V_{DD}	0.203 V_{DD}
6	0.142 V_{DD}	0.189 V_{DD}	0.236 V_{DD}
7	0.162 V_{DD}	0.216 V_{DD}	0.270 V_{DD}

Programmable Glitch Filter Values[7]
(Receiver (end-to-end) filter values expressed as transient pulse suppression times)

Filter (F)	Min.	Typ.	Max.	Unit
0	10	75	140	ns
1	120	410	700	ns
2	240	800	1350	ns
3	480	1500	2600	ns

Receiver[8] **(End-to-End) Absolute Asymmetry**
(Worst case across hysteresis)

Filter (F)	Max ($\lvert t_{PLH} - t_{PHL} \rvert$)	Unit
0	35	ns
1	150	ns
2	250	ns
3	400	ns

Differential Receiver (End-to-End) Absolute Symmetry[9, 10]

Filter (F)	Hysteresis (H)	Max ($\lvert t_{PLH} - t_{PHL} \rvert$)	Unit
0	0	24	ns

Notes:
5. For detailed information about data retention after 100K cycles, please see Cypress qualification report.
6. Hysteresis values are on the condition that the input signal swing is 200 mV greater than the programmed value.
7. Must be disabled if data rate is 1.25 Mbps or greater.
8. Receiver input, $V_D = V_{CP0} – V_{CP1}$, at least 200 mV greater than hysteresis levels. See *Figure 1*.
9. CP0 and CP1 inputs each 0.60 Vp – p, 1.25 MHz sine wave 180° out of phase with each other as shown in *Figure 8*. V_{DD} = 5.00 V ± 5%.
10. t_{PLH}: Time from input switching states from low to high to output switching states. t_{PHL}: Time from input switching states from high to low to output switching states.

Electrical Characteristics (V_{DD} = 4.5V–5.5V)

Parameter	Description	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage				V
	IO0–IO10, CP0, CP3, CP4, $\overline{\text{SERVICE}}$, D0-D7, $\overline{\text{RESET}}$	—	—	0.8	
	CP0, CP1 (Differential)	—	—	Programmable	
V_{IH}	Input High Voltage				V
	IO0–IO10, CP0, CP3, CP4, $\overline{\text{SERVICE}}$, D0-D7,$\overline{\text{RESET}}$	2.0	—	—	
	CP0, CP1 (Differential)	Programmable	—	—	
V_{OL}	Low-Level Output Voltage				V
	I_{out} < 20 µA	—	—	0.1	
	Standard Outputs (I_{OL} = 1.4 mA)[11]	—	—	0.4	
	High Sink (IO0–IO3), $\overline{\text{SERVICE}}$, $\overline{\text{RESET}}$ (I_{OL} = 20 mA)	—	—	0.8	
	High Sink (IO0–IO3), $\overline{\text{SERVICE}}$, $\overline{\text{RESET}}$ (I_{OL} = 10 mA)	—	—	0.4	
	Maximum Sink (CP2, CP3) (I_{OL} = 40 mA)	—	—	1.0	
	Maximum Sink (CP2, CP3) (I_{OL} = 15 mA)	—	—	0.4	
V_{OH}	High-Level Output Voltage				V
	I_{out} < 20 µA	V_{DD} – 0.1	—	—	
	Standard Outputs (I_{OH} = –1.4 mA)[11]	V_{DD} – 0.4	—	—	
	High Sink (IO0 – IO3), $\overline{\text{SERVICE}}$ (I_{OH} = –1.4 mA)	V_{DD} – 0.4	—	—	
	Maximum Source (CP2, CP3) (I_{OH} = –40 mA)	V_{DD} – 1.0	—	—	
	Maximum Source (CP2, CP3) (I_{OH} = –15 mA)	V_{DD} – 0.4	—	—	
V_{hys}	Hysteresis (Excluding CLK1)	175	—	—	mV
I_{in}	Input Current (Excluding Pull-Ups) (V_{SS} to V_{DD})[12]	—	—	±10	µA
I_{pu}	Pull-Up Source Current (V_{out} = 0 V, Output = High-Z)[12]	60	—	260	µA
I_{DD}	Operating Mode Supply Current[13]40-MHz Clock[14]	—	—	55	mA
	20-MHz Clock	—	—	32	
	10-MHz Clock	—	—	20	
	5-MHz Clock	—	—	12	
	2.5-MHz Clock	—	—	8	
	1.25-MHz Clock	—	—	7	
	0.625-MHz Clock[14]	—	—	3	
$I_{DDsleep}$	Sleep Mode Supply Current[1, 13]	—	—	100	µA

LVI Trip Point (V_{DD})

Part Number	Min.	Typ.	Max.	Unit
CY7C53120E2, CY7C53120E4, and CY7C53150	3.8	4.1	4.4	V

Notes:

11. Standard outputs are IO4–IO10, CP0, CP1, and CP4. ($\overline{\text{RESET}}$ is an open drain input/output. CLK2 must have ≤ 15 pF load.) For CY7C53150, standard outputs also include A0–A15, D0–D7, E, and R/W.
12. IO4–IO7 and $\overline{\text{SERVICE}}$ have configurable pull-ups. $\overline{\text{RESET}}$ has a permanent pull-up.
13. Supply current measurement conditions: V_{DD} = 5V, all outputs under no-load conditions, all inputs ≤ 0.2V or ≥ (V_{DD} – 0.2V), configurable pull-ups off, crystal oscillator clock input, differential receiver disabled. The differential receiver adds approximately 200 µA typical and 600 µA maximum when enabled. It is enabled on either of the following conditions:
    - Neuron chip in Operating mode **and** Comm Port in Differential mode.
    - Neuron chip in Sleep mode **and** Comm Port in Differential mode **and** Comm Port Wake-up not masked.
14. Supported through an external oscillator only.

External Memory Interface Timing — CY7C53150, V_{DD} ± 10% (V_{DD} = 4.5V to 5.5 V, T_A = –40°C to+ 85°C [2])

Parameter	Description	Min.	Max.	Unit
t_{cyc}	Memory Cycle Time (System Clock Period)[15]	100	3200	ns
PW_{EH}	Pulse Width, $\overline{E}$ High[16]	$t_{cyc}/2 – 5$	$t_{cyc}/2 + 5$	ns
PW_{EL}	Pulse Width, $\overline{E}$ Low[16]	$t_{cyc}/2 – 5$	$t_{cyc}/2 + 5$	ns
t_{AD}	Delay, $\overline{E}$ High to Address Valid[20]	—	35	ns
t_{AH}	Address Hold Time After $\overline{E}$ High[20]	10	—	ns
t_{RD}	Delay, $\overline{E}$ High to R/$\overline{W}$ Valid Read[20]	—	25	ns
t_{RH}	R/$\overline{W}$ Hold Time Read After $\overline{E}$ High	5	—	ns
t_{WR}	Delay, $\overline{E}$ High to R/$\overline{W}$ Valid Write	—	25	ns
t_{WH}	R/$\overline{W}$ Hold Time Write After $\overline{E}$ High	5	—	ns
t_{DSR}	Read Data Setup Time to $\overline{E}$ High	15	—	ns
t_{DHR}	Data Hold Time Read After $\overline{E}$ High	0	—	ns
t_{DHW}	Data Hold Time Write After $\overline{E}$ High[17, 18]	10	—	ns
t_{DDW}	Delay, $\overline{E}$ Low to Data Valid	—	12	ns
t_{DHZ}	Data Three State Hold Time After $\overline{E}$ Low[19]	0	—	ns
t_{DDZ}	Delay, $\overline{E}$ High to Data Three-State[18]	—	42	ns
t_{acc}	External Memory Access Time ($t_{acc} = t_{cyc} – t_{AD} – t_{DSR}$) at 20-MHz input clock	50	—	ns

Differential Transceiver Electrical Characteristics

Characteristic	Min.	Max.	Unit
Receiver Common Mode Voltage Range to maintain hysteresis[21]	1.2	$V_{DD} – 2.2$	V
Receiver Common Mode Range to operate with unspecified hysteresis	0.9	$V_{DD} – 1.75$	V
Input Offset Voltage	$–0.05V_{hys} – 35$	$0.05V_{hys} + 35$	mV
Propagation Delay (F = 0, $V_{ID} = V_{hys}/2 + 200$ mV)	—	230 ns	ns
Input Resistance	5	—	MΩ
Wake-up Time	—	10	µs
Differential Output Impedance for CP2 and CP3[22]		35	Ω

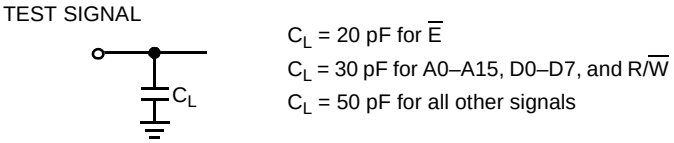


Figure 2. Signal Loading for Timing Specifications Unless Otherwise Specified

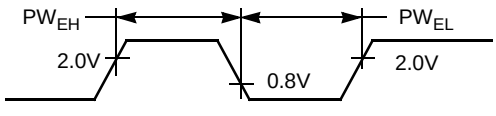
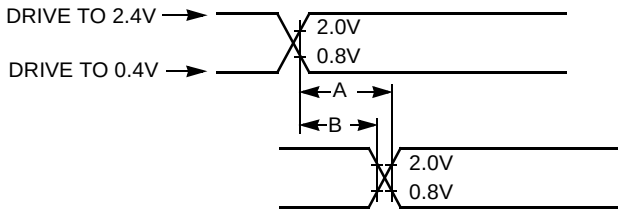


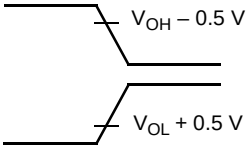
Figure 3. Test Point Levels for $\overline{E}$ Pulse Width Measurements

Notes:
15. t_{cyc} = 2(1/f), where f is the input clock (CLK1) frequency (20, 10, 5, 2.5, 1.25, or 0.625 MHz).
16. Refer to *Figure 3* for detailed measurement information.
17. The data hold parameter, t_{DHW}, is measured to the disable levels shown in *Figure 5*, rather than to the traditional data invalid levels.
18. Refer to *Figure 6* and *Figure 5* for detailed measurement information.
19. The three-state condition is when the device is not actively driving data. Refer to *Figure 2* and *Figure 5* for detailed measurement information.
20. To meet the timing above for 20-MHz operation, the loading on A0–A15, D0–D7, and R/W is 30 pF. Loading on E is 20 pF.
21. Common mode voltage is defined as the average value of the waveform at each input at the time switching occurs.
22. Z_0 = |V[CP2]-V[CP3] |/40mA for $4.75 \le V_{DD} \le 5.25V$.



A — Signal valid-to-signal valid specification (maximum or minimum)
B — Signal valid-to-signal invalid specification (maximum or minimum)

Figure 4. Drive Levels and Test Point Levels for Timing Specifications Unless Otherwise Specified



V_{OH} – Measured high output drive level
V_{OL} – Measured low output drive level

Figure 5. Test Point Levels for Driven-to-Three-State Time Measurements

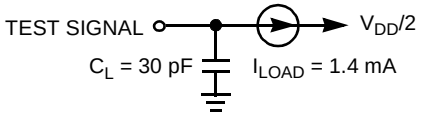


Figure 6. Signal Loading for Driven-to-Three-State Time Measurements

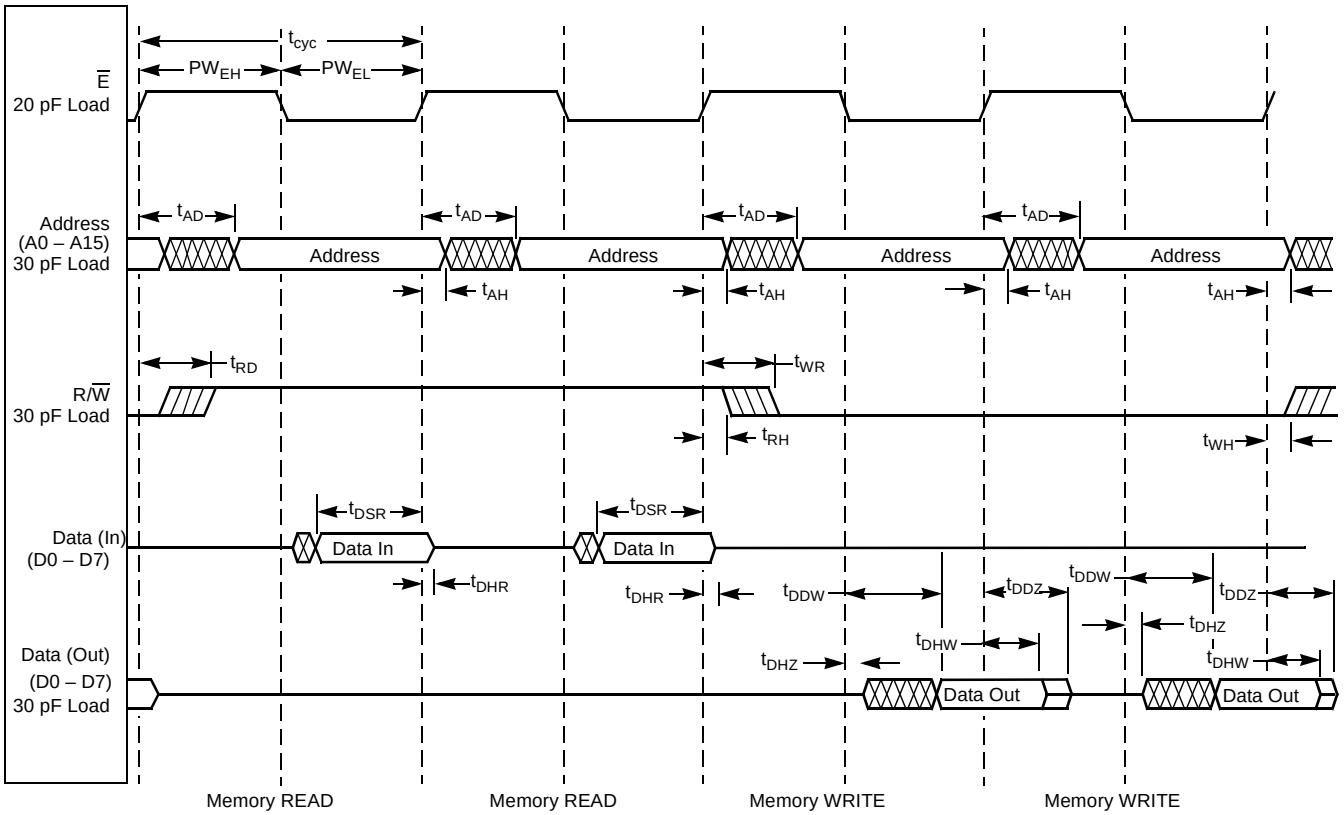
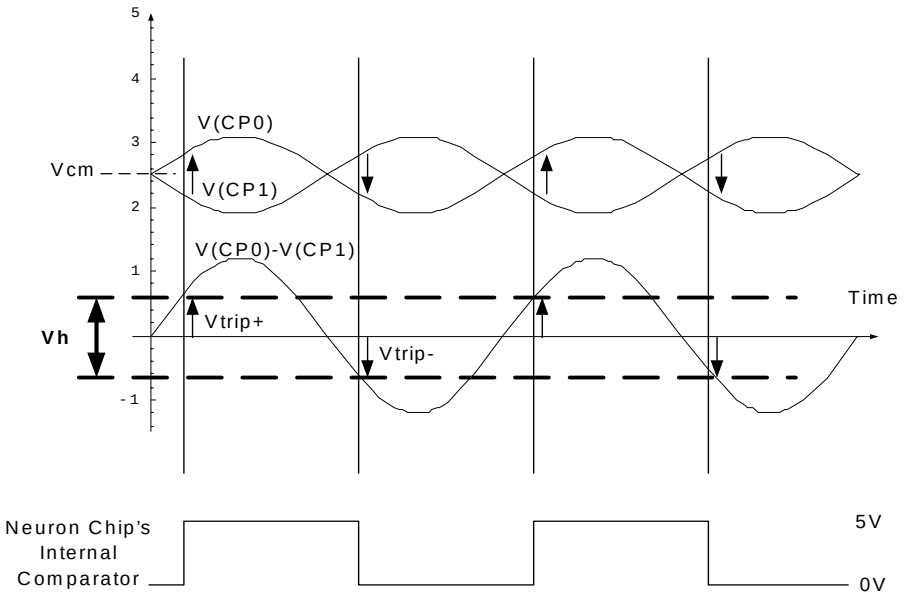


Figure 7. External Memory Interface Timing Diagram



Common-Mode voltage: Vcm = (V(CP0) + V(CP1)) / 2

Hysteresis Voltage: Vh = [Vtrip+] - [Vtrip-]

Figure 8. Differential Receiver Input Hysteresis Voltage Measurement Waveforms

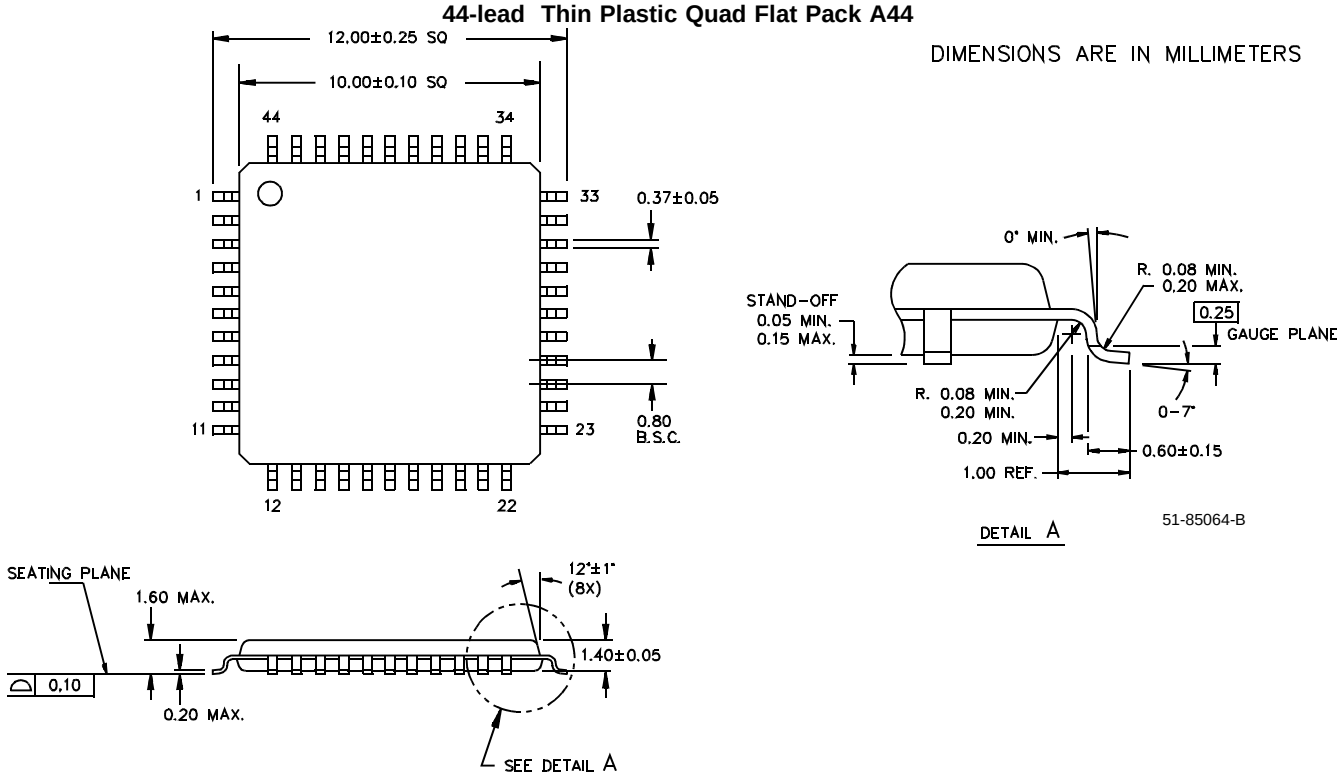
Ordering Information[23]

Part Number	Flash (KB)	ROM (KB)	Firmware Version	Max. Input Clock (MHz)	Package Name	Package Type
CY7C53150-20AI	0.5	0	N/A	20[25]	A65	64-lead Thin Plastic Quad Flat Pack
CY7C53120E2-10SI[24]	2	10	6	10	S34	32-lead (450 mil) Molded SOIC
CY7C53120E4-40SI[26]	4	12	12	40	S34	32-lead (450 mil) Molded SOIC
CY7C53120E2-10AI[24]	2	10	6	10	A44	44-lead Thin Plastic Quad Flat Pack
CY7C53120E4-40AI[26]	4	12	12	40	A44	44-lead Thin Plastic Quad Flat Pack

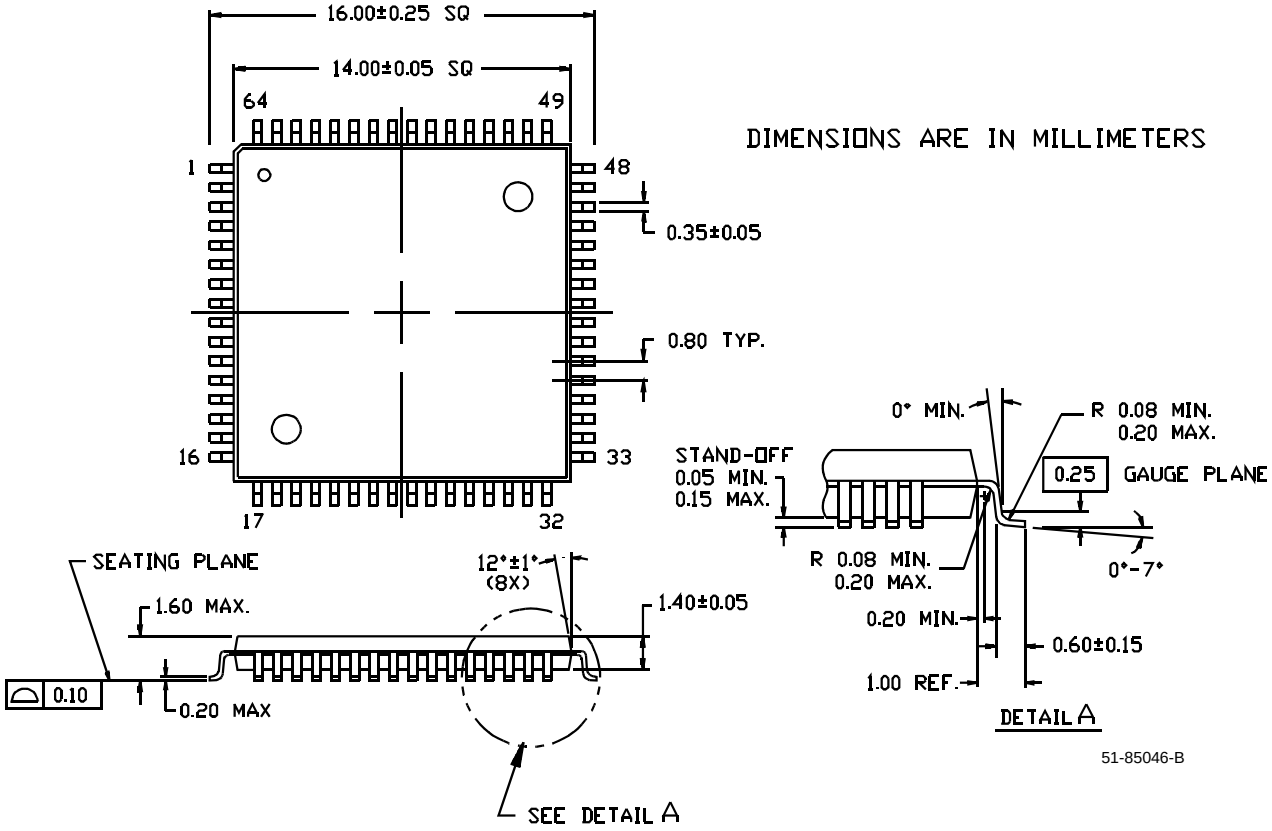
Notes:
23. All parts contain 2KB of SRAM.
24. CY7C53120E2 firmware is bit-for-bit identical with Motorola MC143120E2 firmware.
25. CY7C53150 may be used with 20-MHz input clock only if the firmware in external memory is version 13 or later.
26. CY7C53120E4 requires upgraded LonBuilder and NodeBuilder software.

Package Diagrams

44-lead Thin Plastic Quad Flat Pack A44

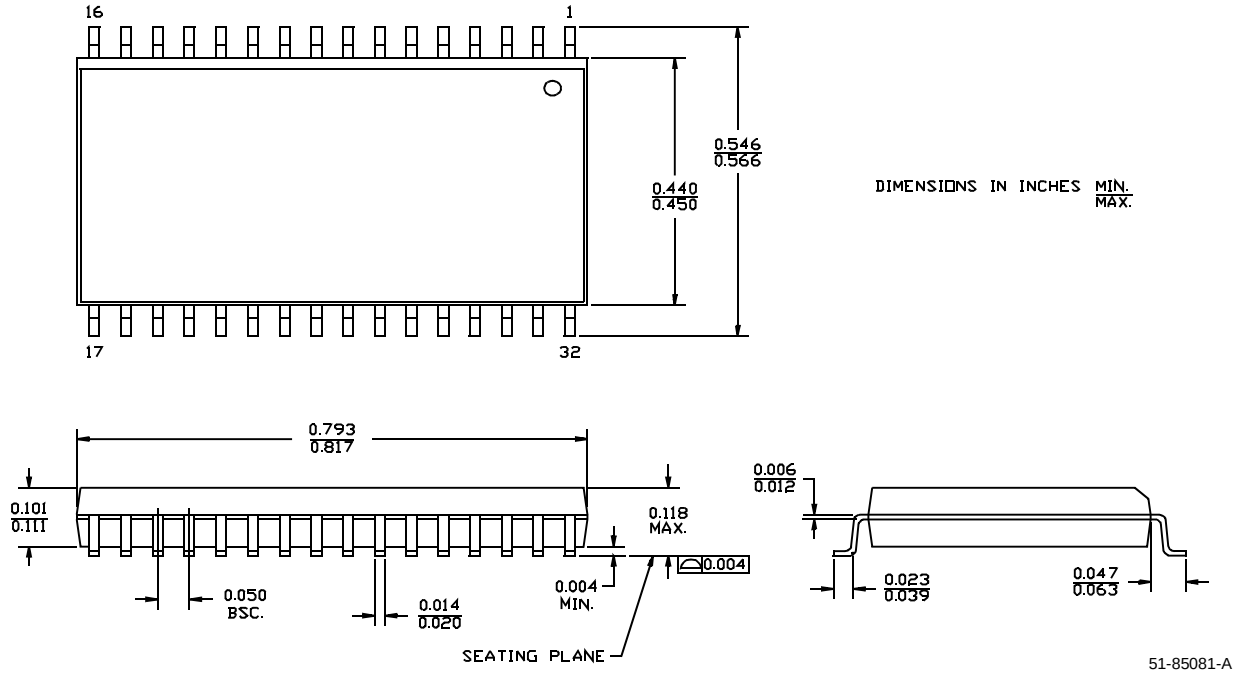


64-lead Thin Plastic Quad Flat Pack (14 × 14 × 1.4 mm) A65



Package Diagrams (continued)

32-lead (450-mil) Molded SOIC S34



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Document History Page

Document Title: CY7C53150/CY7C53120 Neuron® Chip Network Processor Document Number: 38-10001				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111472	11/28/01	DSG	Change from Spec number: 38-00891 to 38-10001
*A	111990	02/06/02	CFB	Changed the max. cur rent values Specified the Flash endurance of “100K typical” with reference to qual report Fixed some incorrect footnotes and figure numbering
*B	114465	04/24/02	KBO	Added Sleep Metastability footnote Added Junction Temperature footnote Added maximum sleep current footnote Changed “EEPROM” references to “Flash Memory”
*C	115269	04/26/02	KBO	Repositioned Note 3
*D	124450	03/25/03	KBO	Removed Note 2 regarding data retention Removed Note 16 regarding max sleep current Changed the system image firmware version from V12 to V13.1