CY7C408A
CY7C409A

64 x 8 Cascadable FIFO
64 x 9 Cascadable FIFO

Features

- **64 x 8 and 64 x 9 first-in first-out (FIFO) buffer memory**
- **35-MHz shift in and shift out rates**
- **Almost Full/Almost Empty and Half Full flags**
- **Dual-port RAM architecture**
- **Fast (50-ns) bubble-through**
- **Independent asynchronous inputs and outputs**
- **Output enable (CY7C408A)**
- **Expandable in word width and FIFO depth**
- **5V ± 10% supply**
- **TTL complete**
- **Capable of withstanding greater than 2001V electro-static discharge voltage**
- **300-mil, 28-pin DIP**

Functional Description

The CY7C408A and CY7C409A are 64-word deep by 8- or 9-bit wide first-in first-out (FIFO) buffer memories. In addition to the industry-standard handshaking signals, almost full/almost empty (AFE) and half-full (HF) flags are provided.

AFE is HIGH when the FIFO is almost full or almost empty, otherwise AFE is LOW. HF is HIGH when the FIFO is half full, otherwise HF is LOW.

The CY7C408A has an output enable (OE) function.

The memory accepts 8- or 9-bit parallel words as its inputs (DI_0 – DI_8) under the control of the shift in (SI) input when the input ready (IR) control signal is HIGH. The data is output, in the same order as it was stored on the DO_0 – DO_8 output pins under the control of the shift out (SO) input when the output ready (OR) control signal is HIGH. If the FIFO is full (IR LOW), pulses at the SI input are ignored; if the FIFO is empty (OR LOW), pulses at the SO input are ignored.

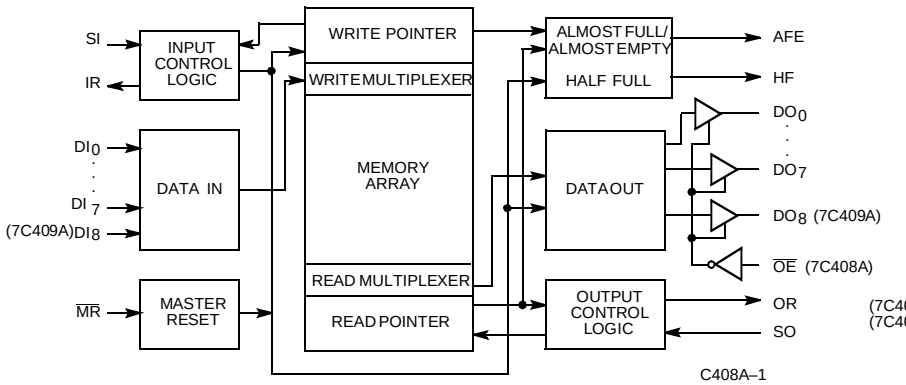
The IR and OR signals are also used to connect the FIFOs in parallel to make a wider word or in series to make a deeper buffer, or both.

Parallel expansion for wider words is implemented by logically ANDing the IR an OR outputs (respectively) of the individual FIFOs together (*Figure 5*). The AND operation insures that all of the FIFOs are either ready to accept more data (IR HIGH) or ready to output data (OR HIGH) and thus compensate for variations in propagation delay times between devices.

Serial expansion (cascading) for deeper buffer memories is accomplished by connecting data outputs of the FIFO closet to the data source (upstream device) to the data inputs of the following (downstream) FIFO (*Figure 4*). In addition, to insure proper operation, the SO signal of the upstream FIFO must be connected to the OR output of the upstream FIFO. In this serial expansion configuration, the IR and OR signals are used to pass data through the FIFOs.

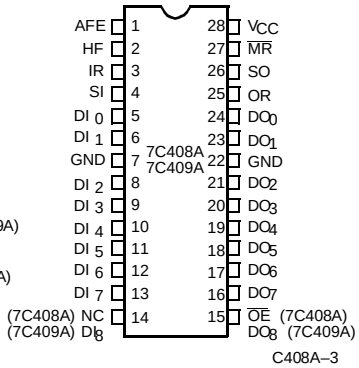
Reading and writing operations are completely asynchronous, allowing the FIFO to be used as a buffer between two digital machines of widely differing operating frequencies. The high shift in and shift out rates of these FIFOs, and their throughput rate due to the fast bubblethrough time, which is due to their dual-port RAM architecture, make them ideal for high-speed communications and controllers.

Logic Block Diagram

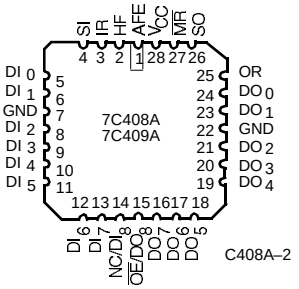


C408A–1

Pin Configurations



C408A–3



C408A–2

Flag Definitions

HF	AFE	Words Stored
L	H	0 - 8
L	L	9 - 31
H	L	32 - 55
H	H	56 - 64

Selection Guide

		7C408A-15 7C409A-15	7C408A-25 7C409A-25	7C408A-35 7C409A-35
Maximum Shift Rate (MHz)		15	25	35
Maximum Operating Current (mA)[1]	Commercial	115	125	135
	Military	140	150	N/A

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State (7C408A)..... –0.5V to +7.0V

DC Input Voltage ..... –3.0V to +7.0V

Power Dissipation..... 1.0W

Output Current, into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[2]	–55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range (Unless Otherwise Noted)[3]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			–3.0	0.8	V
I_{IX}	Input Leakage Current	$GND \le V_I \le V_{CC}$		–10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			–90	mA
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $V_{IN} \le V_{IL}$, $V_{IN} \ge V_{IH}$	Commercial		100	mA
			Military		125	
I_{CC}	Power Supply Current	$I_{CC} = I_{CCQ} + 1\ mA/MHz \times (f_{SI} + f_{SO})/2$				

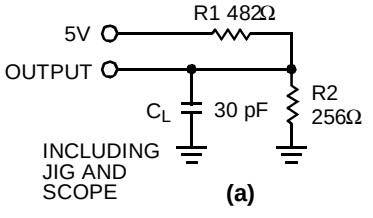
Capacitance[5]

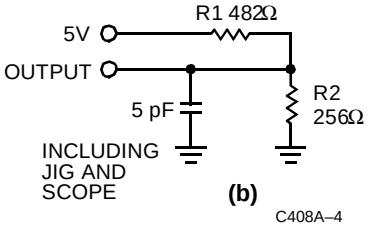
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	5	pF
C_{OUT}	Output Capacitance		7	pF

Notes:

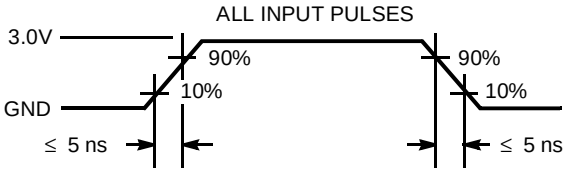
1. $I_{CC} = I_{CCQ} + 1\ mA/MHz \times (f_{SI} + f_{SO})/2$
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



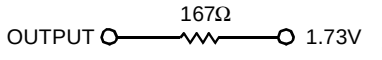


C408A–4



C408A–5

Equivalent to: THÉVENIN EQUIVALENT



C408A–6

Switching Characteristics Over the Operating Range[3, 6]

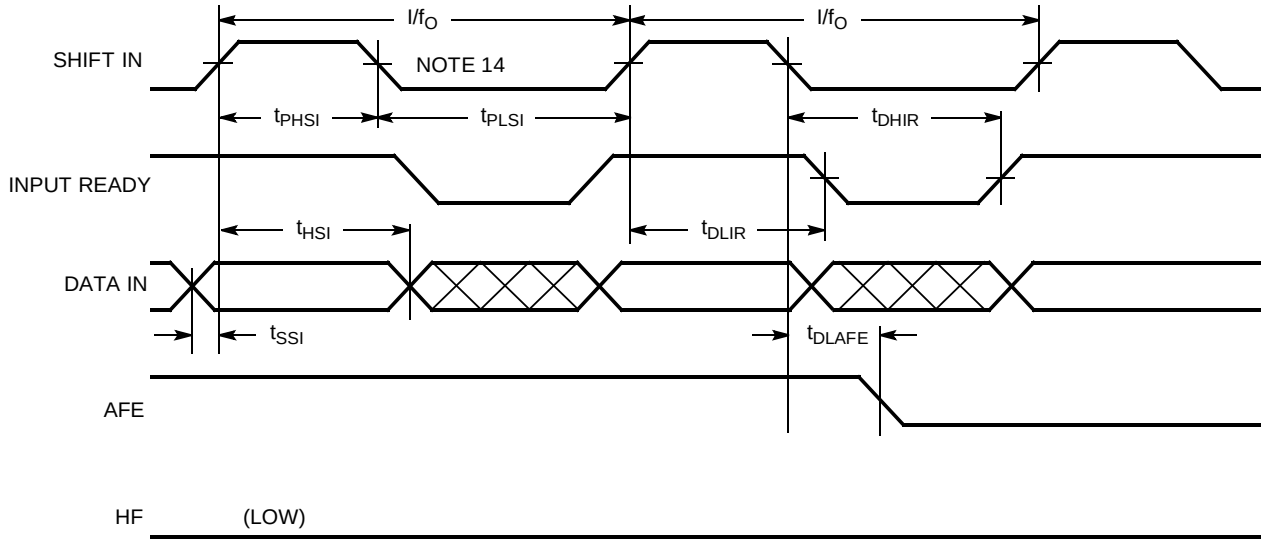
Parameter	Description	Test Conditions	7C408A-15 7C409A-15		7C408A-25 7C409A-25		7C408A-35 7C409A-35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
f_O	Operating Frequency	Note 7		15		25		35	MHz
t_{PHSI}	SI HIGH Time	Note 7	23		11		9		ns
t_{PLSI}	SI LOW Time	Note 7	25		24		17		ns
t_{SSI}	Data Set-Up to SI	Note 8	0		0		0		ns
t_{HSI}	Data Hold from SI	Note 8	30		20		12		ns
t_{DLIR}	Delay, SI HIGH to IR LOW			35		21		15	ns
t_{DHIR}	Delay, SI LOW to IR HIGH			40		23		16	ns
t_{PHSO}	SO HIGH Time	Note 7	23		11		9		ns
t_{PLSO}	SO LOW Time	Note 7	25		24		17		ns
t_{DLOR}	Delay, SO HIGH to OR LOW			35		21		15	ns
t_{DHOR}	Delay, SO LOW to OR HIGH			40		23		16	ns
t_{SOR}	Data Set-Up to OR HIGH		0		0		0		ns
t_{HSO}	Data Hold from SO LOW		0		0		0		ns
t_{BT}	Fall-through, Bubble-back Time		10	65	10	60	10	50	ns
t_{SIR}	Data Set-Up to IR	Note 9	5		5		5		ns
t_{HIR}	Data Hold from IR	Note 9	30		20		20		ns
t_{PIR}	Input Ready Pulse HIGH	Note 10	6		6		6		ns
t_{POR}	Output Ready Pulse HIGH	Note 11	6		6		6		ns
t_{DLZOE}	OE LOW to LOW Z (7C408A)	Note 12		35		30		25	ns
t_{DHZOE}	OE HIGH to HIGH Z (7C408A)	Note 7		35		30		25	ns
t_{DHHF}	SI LOW to HF HIGH			65		55		45	ns
t_{DLHF}	SO LOW to HF LOW			65		55		45	ns
t_{DLAFE}	SO or SI LOW to AFE LOW			65		55		45	ns
t_{DHAFE}	SO or SI LOW to AFE HIGH			65		55		45	ns
t_{PMR}	$\overline{MR}$ Pulse Width		55		45		35		ns
t_{DSI}	$\overline{MR}$ HIGH to SI HIGH		25		10		10		ns
t_{DOR}	$\overline{MR}$ LOW to OR LOW			55		45		35	ns
t_{DIR}	$\overline{MR}$ LOW to IR HIGH			55		45		35	ns
t_{LZMR}	$\overline{MR}$ LOW to Output LOW	Note 13		55		45		35	ns
t_{AFE}	$\overline{MR}$ LOW to AFE HIGH			55		45		35	ns
t_{HF}	$\overline{MR}$ LOW to HF LOW			55		45		35	ns
t_{OD}	SO LOW to Next Data Out Valid			28		20		16	ns

Notes:

6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance, as in parts (a) and (b) of AC Test Loads and Waveforms.
7. $1/f_O \geq (t_{PHSI} + t_{PLSI})$, $1/f_O \geq (t_{PHSO} + t_{PLSO})$.
8. t_{SSI} and t_{HSI} apply when memory is not full.
9. t_{SIR} and t_{HIR} apply when memory is full, SI is high and minimum bubble-through (t_{BT}) conditions exist.
10. At any given operating condition $t_{PIR} \geq (t_{PHSO}$ required).
11. At any given operating condition $t_{POR} \geq (t_{PHSI}$ required).
12. t_{DHZOE} and t_{DLZOE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. t_{DHZOE} transition is measured ±500 mV from steady-state voltage. t_{DLZOE} transition is measured ±100 mV from steady-state voltage. These parameters are guaranteed and not 100% tested.
13. All data outputs will be at LOW level after reset goes HIGH until data is entered into the FIFO.

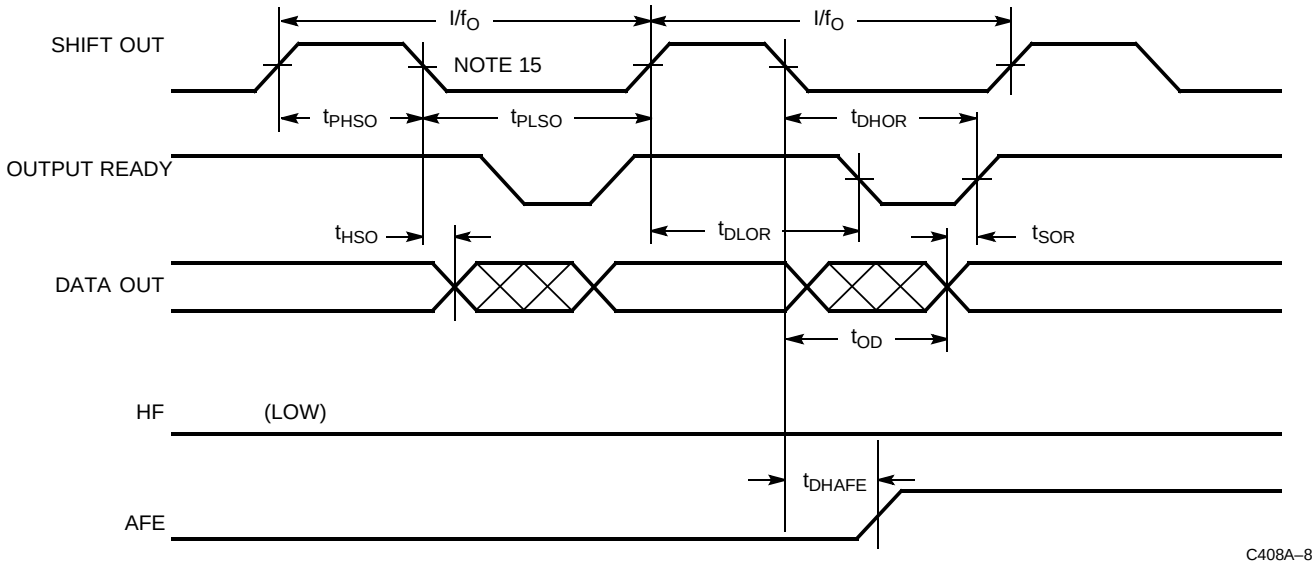
Switching Waveforms

Data In Timing Diagram



C408A–7

Data Out Timing Diagram

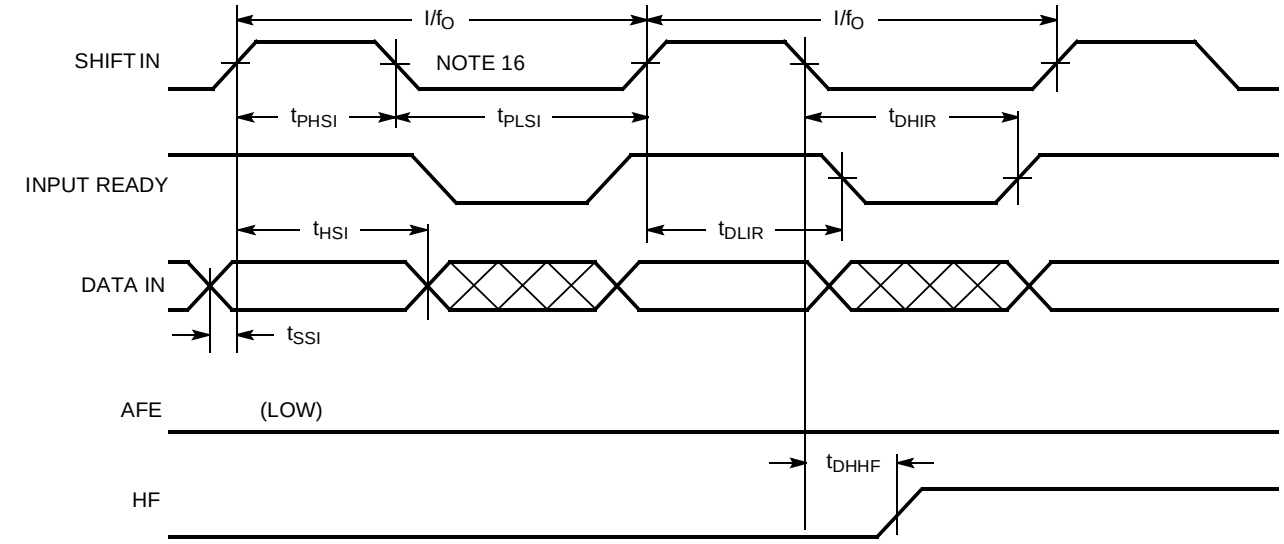


C408A–8

Notes:
14. FIFO contains 8 words.
15. FIFO contains 9 words.

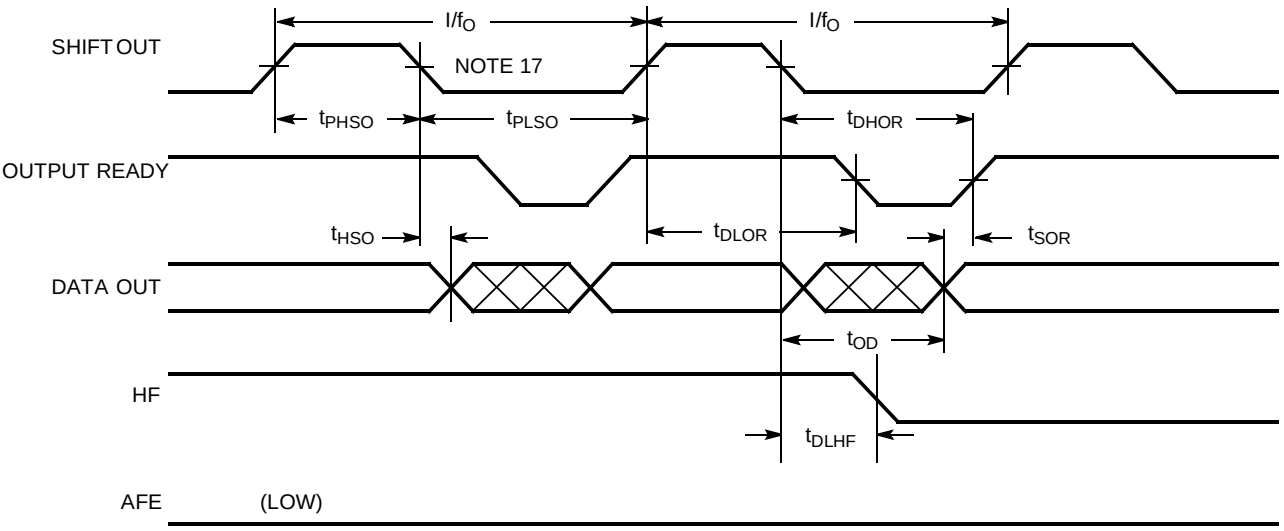
Switching Waveforms (continued)

Data In Timing Diagram



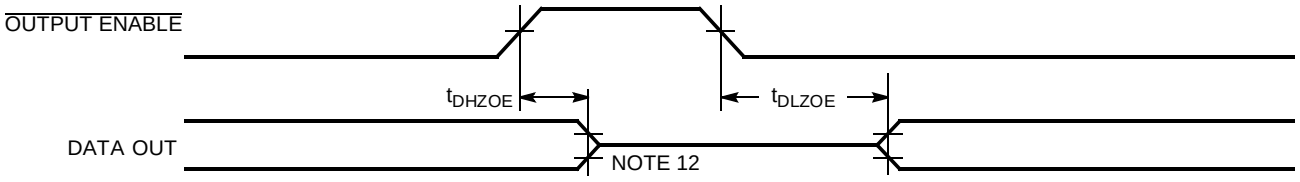
C408A–9

Data Out Timing Diagram



C408A–10

Output Enable (CY7C408A only)

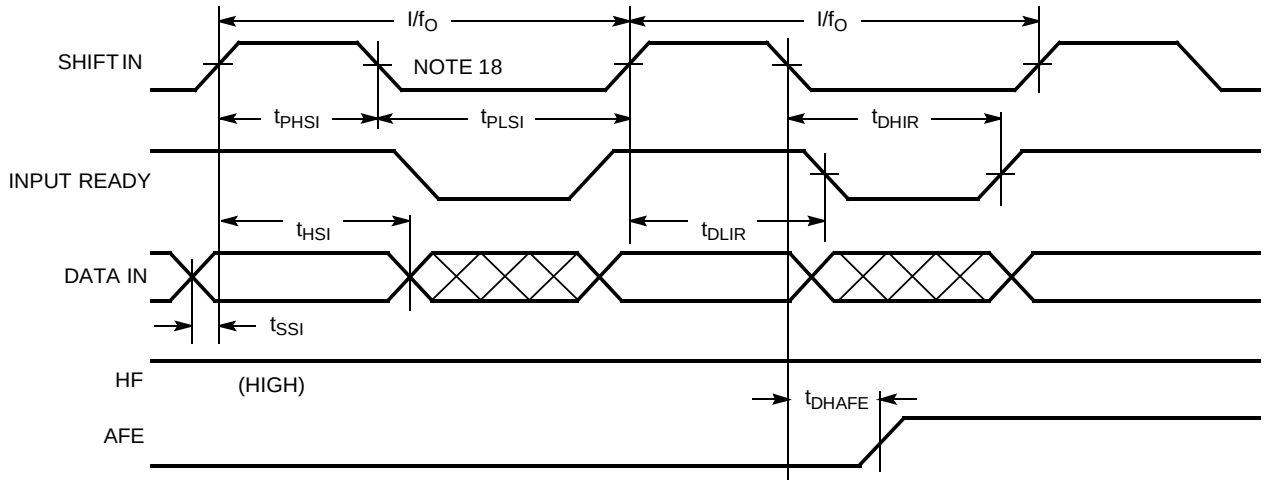


C408A–11

Notes:
16. FIFO contains 31 words.
17. FIFO contains 32 words.

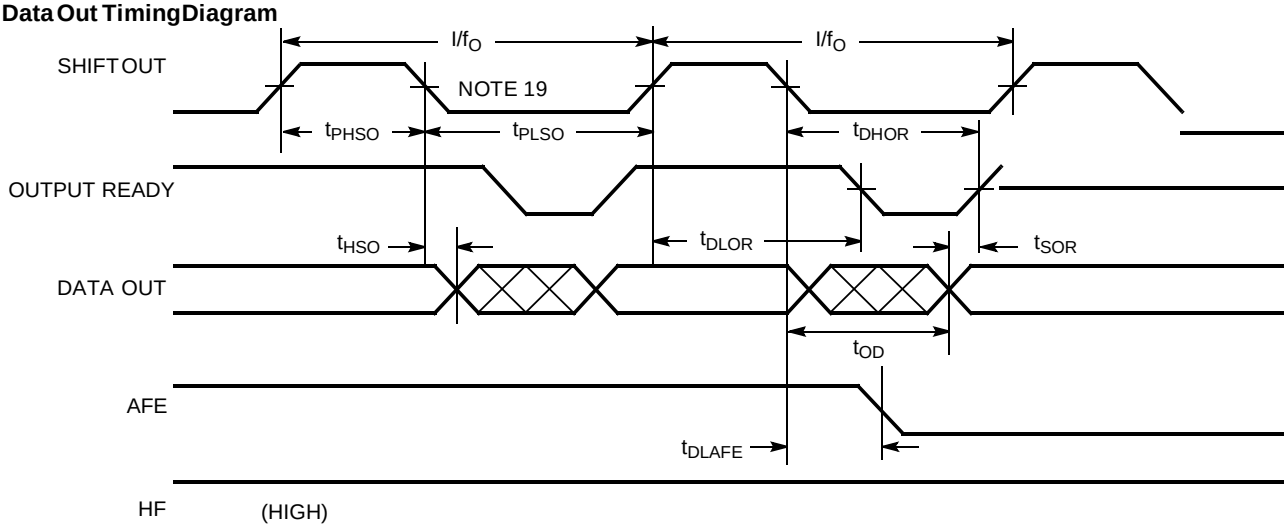
Switching Waveforms (continued)

Data In Timing Diagram



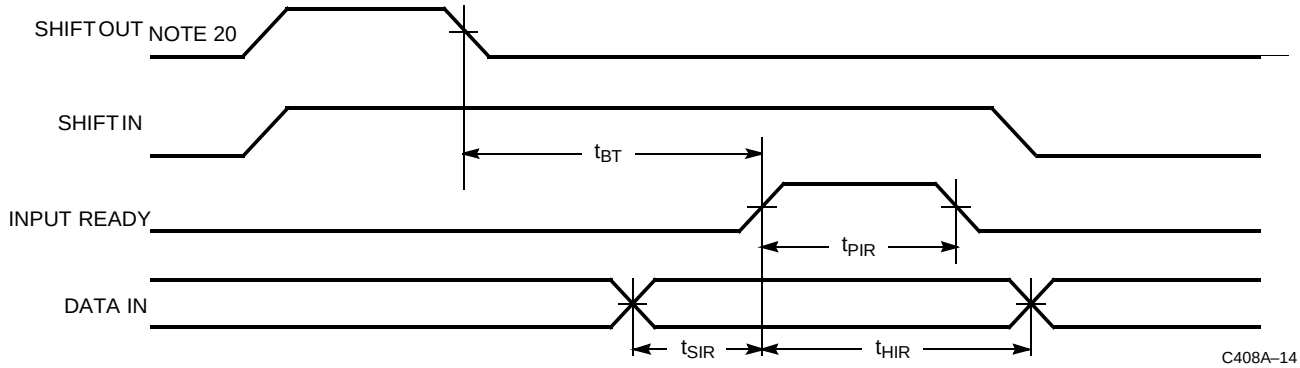
C408A–12

Data Out Timing Diagram



C408A–13

Bubble-Back, Data Out To Data In Diagram

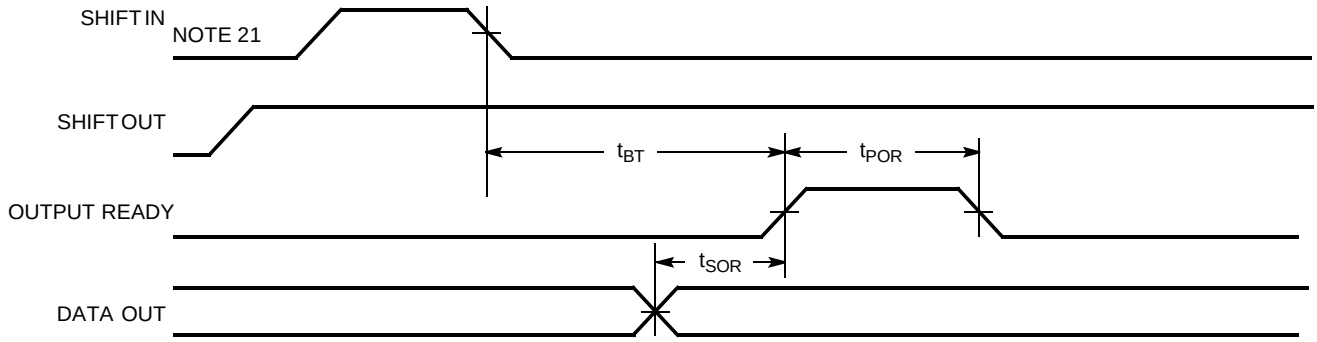


C408A–14

Notes:
18. FIFO contains 55 words.
19. FIFO contains 56 words.
20. FIFO contains 64 words.

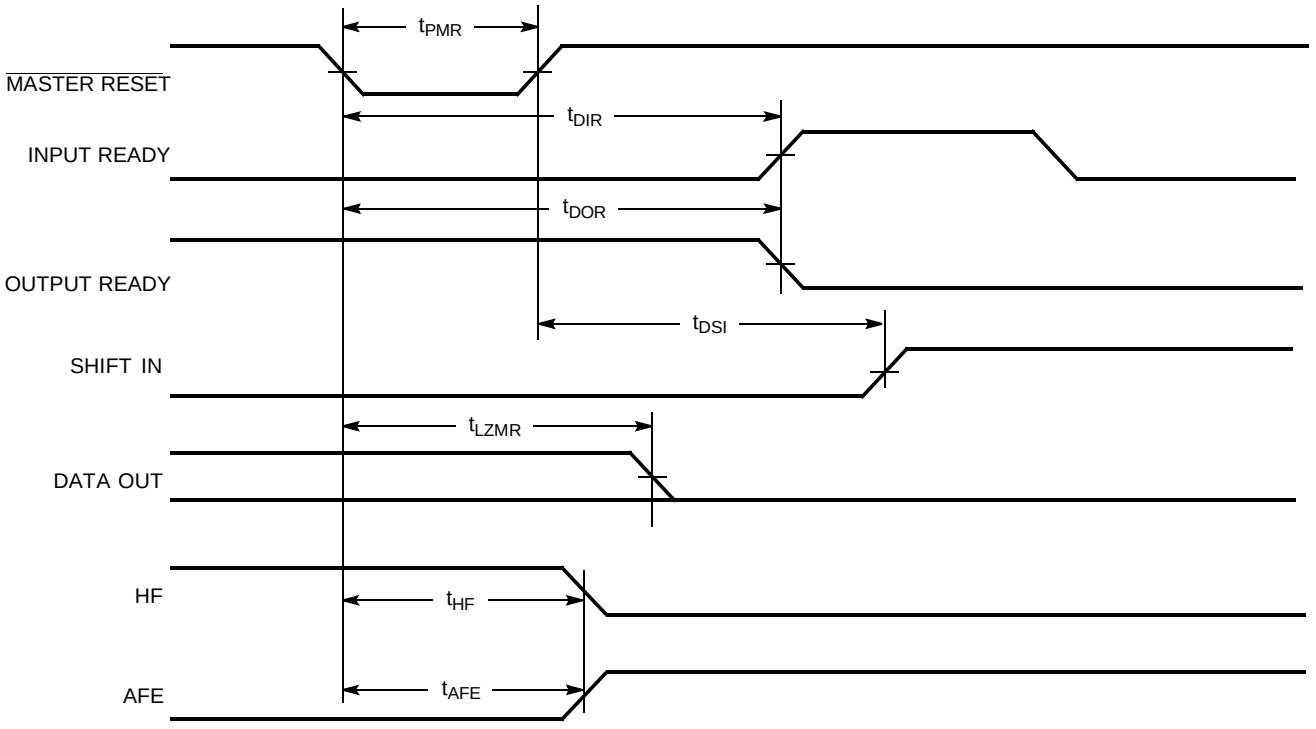
Switching Waveforms (continued)

Fall-Through, Data In to Data Out Diagram



C408A–15

Master Reset Timing Diagram



C408A–16

Notes:
21. FIFO is empty.

Architecture of the CY7C408A and CY7C409A

The CY7C408A and CY7C409A FIFOs consist of an array of 64 words of 8 or 9 bits each (which are implemented using a dual-port RAM cell), a write pointer, a read pointer, and the control logic necessary to generate the handshaking (SI/IR, SO/OR) signals as well as the almost full/almost empty (AFE) and half full (HF) flags. The handshaking signals operate in a manner identical to those of the industry standard CY7C401/402/403/404 FIFOs.

Dual-Port RAM

The dual-port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data to propagate through the memory, which it would have to do if the memory were implemented using the conventional register array architecture.

Fall-Through and Bubble-Back

The time required for data to propagate from the input to the output of an initially empty FIFO is defined as the fall-through time.

The time required for an empty location to propagate from the output to the input of an initially full FIFO is defined as the bubble-back time.

The maximum rate at which data can be passed through the FIFO (called the throughput) is limited by the fall-through time when it is empty (or near empty) and by the bubble-back time when it is full (or near full).

The conventional definitions of fall-through and bubble-back do not apply to the CY7C408A and CY7C409A FIFOs because the data is not physically propagated through the memory. The read and write pointers are incremented instead of moving the data. However, the parameter is specified because it does represent the worst-case propagation delay for the control signals. That is, the time required to increment the write pointer and propagate a signal from the SI input to the OR output of an empty FIFO or the time required to increment the read pointer and propagate a signal from the SO input to the IR output of a full FIFO.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a master reset ($\overline{MR}$) signal. This causes the device to enter the empty condition, which is signified by the OR signal being LOW at the same time that the IR signal is HIGH. In this condition, the data outputs (DO_0 – DO_8) will be LOW. The AFE flag will be HIGH and the HF flag will be LOW.

Shifting Data Into the FIFO

The availability of an empty location is indicated by the HIGH state of the input ready (IR) signal. When IR is HIGH a LOW to HIGH transition on the shift in (SI) pin will clock the data on the DI_0 - DI_8 inputs into the FIFO. Data propagates through the device at the falling edge of SI.

The IR output will then go LOW, indicating that the data has been sampled. The HIGH-to-LOW transition of the SI signal initiates the LOW-to-HIGH transition of the IR signal if the FIFO is not full. If the FIFO is full, IR will remain LOW.

Shifting Data Out of the FIFO

The availability of data at the outputs of the FIFO is indicated by the HIGH state of the output ready (OR) signal. After the FIFO is reset all data outputs (DO_0 – DO_8) will be in the LOW state. As long as the FIFO remains empty, the OR signal will be LOW and all SO pulses applied to it will be ignored. After data is shifted into the FIFO, the OR signal will go HIGH. The external control logic (designed by the user) should use the HIGH state of the OR signal to generate a SO pulse. The data outputs of the FIFO should be sampled with edge-sensitive type D flip-flops (or equivalent), using the SO signal as the clock input to the flip-flop.

AFE and HF Flags

Two flags, almost full/almost empty (AFE) and half full (HF), describe how many words are stored in the FIFO. AFE is HIGH when there are 8 or fewer or 56 or more words stored in the FIFO. Otherwise the AFE flag is LOW. HF is HIGH when there are 32 or more words stored in the FIFO, otherwise the HF flag is LOW. Flag transitions occur relative to the falling edges of SI and SO (*Figures 1* and *2*).

Due to the asynchronous nature of the SI and SO signals, it is possible to encounter specific timing relationships which may cause short pulses on the AFE and HF flags. These pulses are entirely due to the dynamic relationship of the SI and SO signals. The flags, however, will always settle to their correct state after the appropriate delay (t_{DHAFE}, t_{DLAFE}, t_{DHHF}, or t_{DLHF}). Therefore, use of level-sensitive rather than edge-sensitive flag detection devices is recommended to avoid false flag encoding.

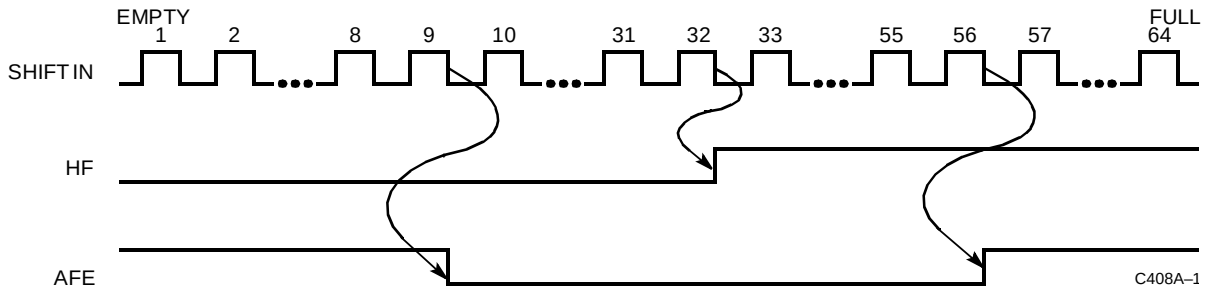


Figure 1. Shifting Words In.

Possible Minimum Pulse Width Violation at the Boundary Conditions

If the handshaking signals IR and OR are not properly used to generate the SI and SO signals, it is possible to violate the minimum (effective) SI and SO positive pulse widths at the full and empty boundaries.

Cascading the 7C408/9A-35 Above 25 MHz

First, the capacity of N cascaded FIFOs is decreased from N $\times$ 64 to (N $\times$ 63) + 1.

If cascaded FIFOs are to be operated with an external clock rate greater than 25 MHz, the interface IR signal must be inverted before being fed back to the interface SO pin (*Figure 3*). Two things should be noted when this configuration is implemented.

Secondly, the frequency at the cascade interface is less than the 35 MHz rate at which the external clocks may operate. Therefore, the first device has its data shifted in faster than it is shifted out, and eventually this device becomes momentarily full. When this occurs, the maximum sustainable external clock frequency changes from 35 MHz to the cascade interface frequency.[28]

When data packets[29] are transmitted, this phenomenon does not occur unless more than three FIFOs are depth cascaded. For example, if two FIFOs are cascaded, a packet of 127 (=2 $\times$ 63 + 1) words may be shifted in at up to 35 MHz and then the entire packet may be shifted out at up to 35 MHz.

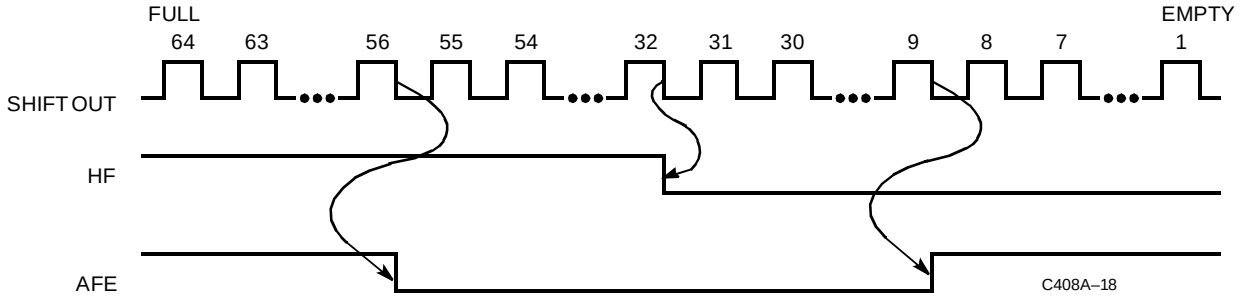


Figure 2. Shifting Words Out.

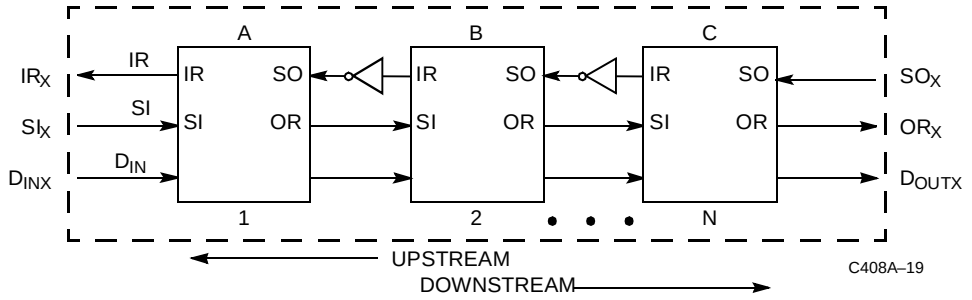


Figure 3. Cascaded Configuration Above 25 MHz.

128 x 9 Configuration

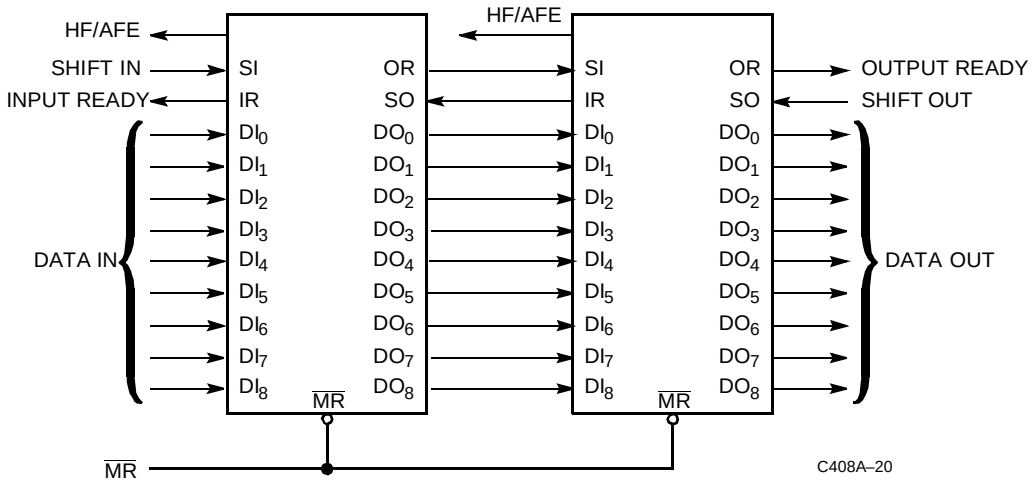


Figure 4. Cascaded Configuration at or below 25 MHz [22,23,24,25,26].

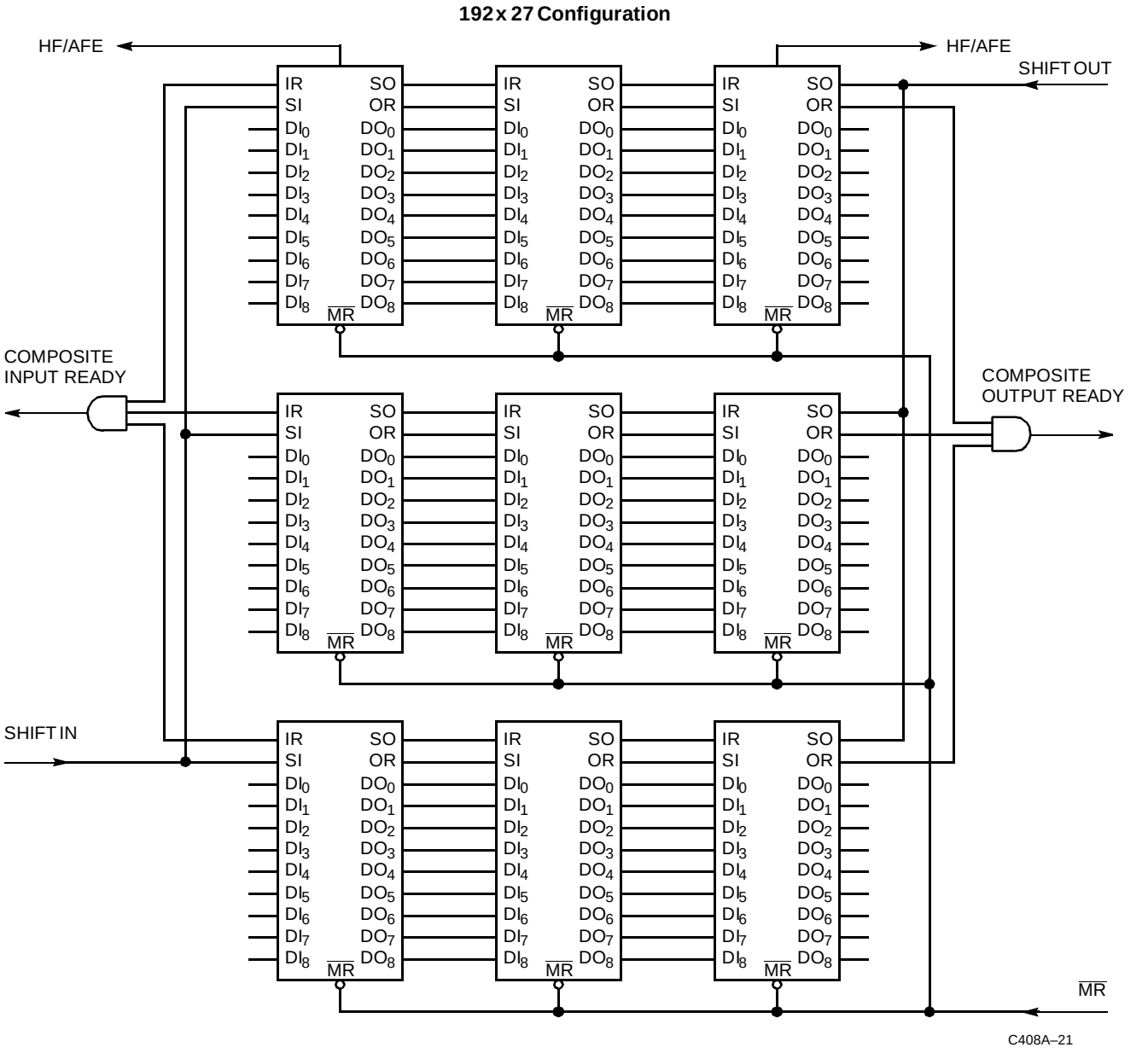


Figure 5. Depth and Width Expansion[23,24,25,26,27].

Notes:

22. FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.
23. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output.
24. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid stable data on the outputs.
25. If SO is held HIGH while the memory is empty and a word is written into the input, that word will fall through the memory to the output. OR will go HIGH for one internal cycle (at least t_{POR}) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
26. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH, and OR goes LOW.
27. FIFOs are expandable in depth and width. However, in forming wider words, two external gates are required to generate composite input ready and output ready flags. This need is due to the variation of delays of the FIFOs
28. Because the data throughput in the cascade interface is dependent on the inverter delay, it is recommended that the fastest available inverter be used.
29. Transmission of data packets assumes that up to the maximum cumulative capacity of the FIFOs is shifted in without simultaneous shift out clock occurring. The complement of this holds when data is shifted out as a packet.

If data is to be shifted out simultaneously with the data being shifted in, the concept of "virtual capacity" is introduced. Virtual capacity is simply how large a packet of data can be shifted in at a fixed frequency, e.g., 35 MHz, simultaneously with data being shifted out at any given frequency. *Figure 6* is a graph of packet size[30] vs. shift out frequency (f_{SOx}) for two different values of shift in frequency (f_{SIx}) when two FIFOs are cascaded.

The exact complement of this occurs if the FIFOs initially contain data and a high shift out frequency is to be maintained, i.e., a 35 MHz f_{SOx} can be sustained when reading data packets from devices cascaded two or three deep.[31] If data is shifted in simultaneously, *Figure 6* applies with f_{SIx} and f_{SOx} interchanged.

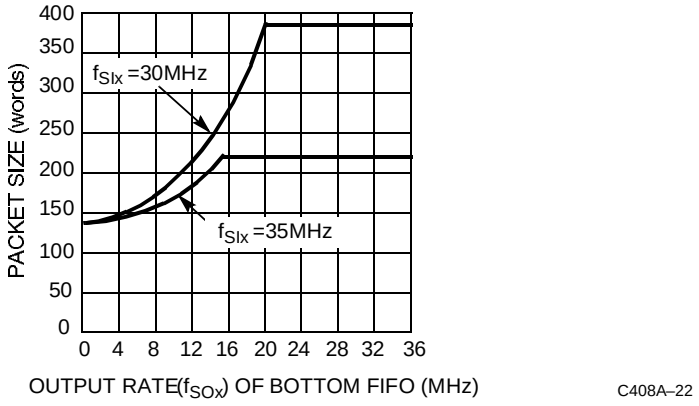
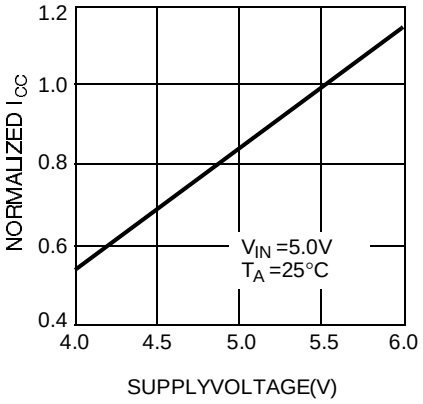


Figure 6. Virtual Capacity vs. Output Rate for Two FIFOs Cascaded Using an Inverter.

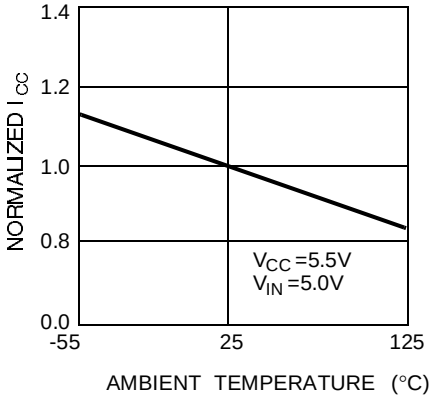
Notes:
30. These are typical packet sizes using an inverter whose delay is 4 ns.
31. Only devices with the same speed grade are specified to cascade together.

Typical DC and AC Characteristics

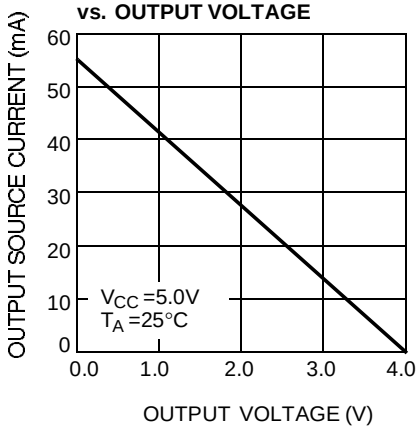
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



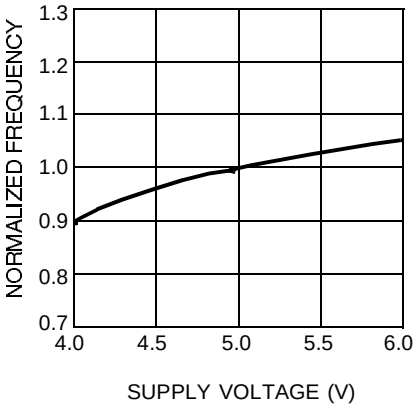
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



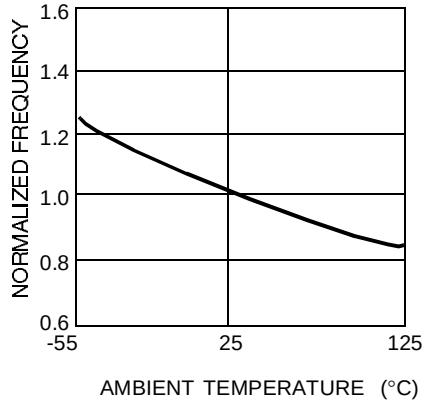
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



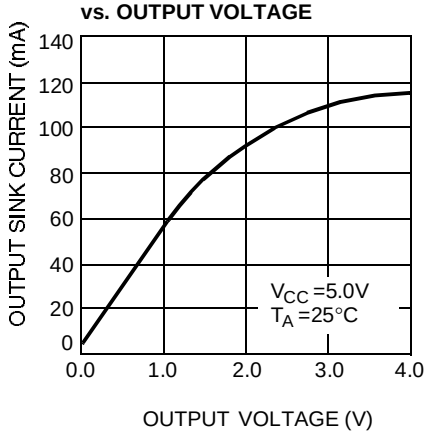
NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE



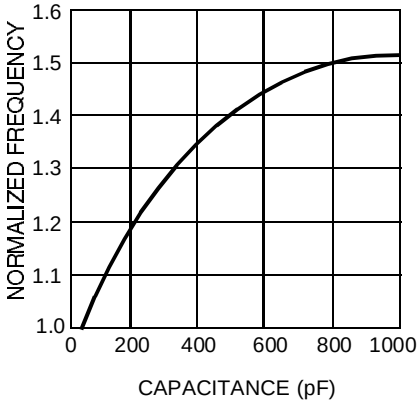
NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE



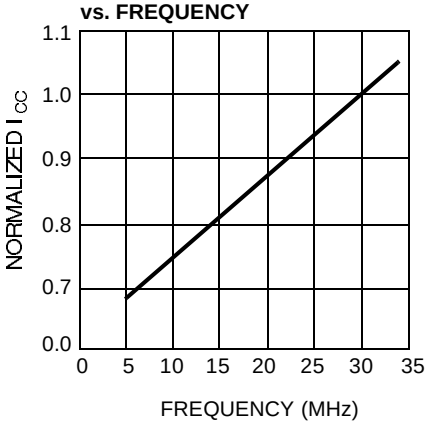
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



TYPICAL FREQUENCY CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



C408A–23

Ordering Information

Frequency (MHz)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C408A-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C408A-15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C408A-15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C408A-15LMB	L64	28-Square Leadless Chip Carrier	
25	CY7C408A-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C408A-25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C408A-25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C408A-25LMB	L64	28-Square Leadless Chip Carrier	
35	CY7C408A-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C408A-35VC	V21	28-Lead (300-Mil) Molded SOJ	

Frequency (MHz)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C409A-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C409A-15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C409A-15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C409A-15LMB	L64	28-Square Leadless Chip Carrier	
25	CY7C409A-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C409A-25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C409A-25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C409A-25LMB	L64	28-Square Leadless Chip Carrier	
35	CY7C409A-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C409A-35VC	V21	28-Lead (300-Mil) Molded SOJ	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CCQ}	1, 2, 3

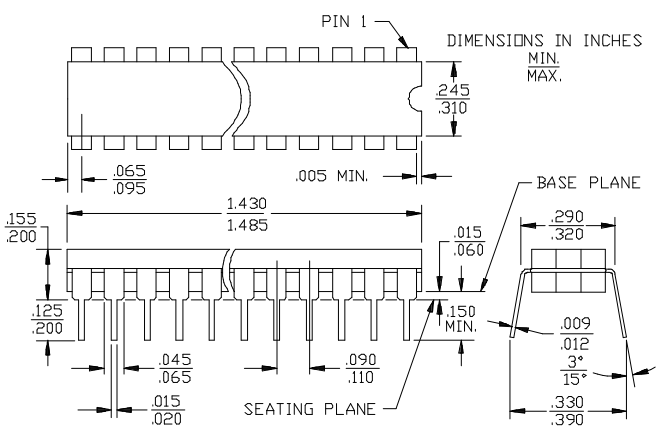
Switching Characteristics

Parameters	Subgroups
f_O	7, 8, 9, 10, 11
t_{PHSI}	7, 8, 9, 10, 11
t_{PLSI}	7, 8, 9, 10, 11
t_{SSI}	7, 8, 9, 10, 11
t_{HSI}	7, 8, 9, 10, 11
t_{DLIR}	7, 8, 9, 10, 11
t_{DHIR}	7, 8, 9, 10, 11
t_{PHSO}	7, 8, 9, 10, 11
t_{PLSO}	7, 8, 9, 10, 11
t_{DLOR}	7, 8, 9, 10, 11
t_{DHOR}	7, 8, 9, 10, 11
t_{SOR}	7, 8, 9, 10, 11
t_{HSO}	7, 8, 9, 10, 11
t_{BT}	7, 8, 9, 10, 11
t_{SIR}	7, 8, 9, 10, 11
t_{HIR}	7, 8, 9, 10, 11
t_{PIR}	7, 8, 9, 10, 11
t_{POR}	7, 8, 9, 10, 11
t_{SIIR}	7, 8, 9, 10, 11
t_{SOOR}	7, 8, 9, 10, 11
t_{DLZOE}	7, 8, 9, 10, 11
t_{DHZOE}	7, 8, 9, 10, 11
t_{DHHF}	7, 8, 9, 10, 11
t_{DLHF}	7, 8, 9, 10, 11
t_{DLAFE}	7, 8, 9, 10, 11
t_{DHAFE}	7, 8, 9, 10, 11
t_B	7, 8, 9, 10, 11
t_{OD}	7, 8, 9, 10, 11
t_{PMR}	7, 8, 9, 10, 11
t_{DSI}	7, 8, 9, 10, 11
t_{DOR}	7, 8, 9, 10, 11
t_{DIR}	7, 8, 9, 10, 11
t_{LZMR}	7, 8, 9, 10, 11
t_{AFE}	7, 8, 9, 10, 11
t_{HF}	7, 8, 9, 10, 11

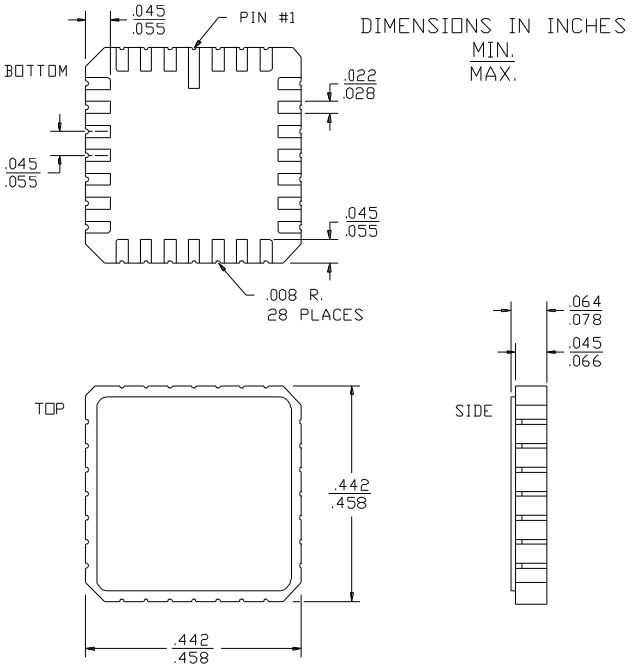
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Package Diagrams

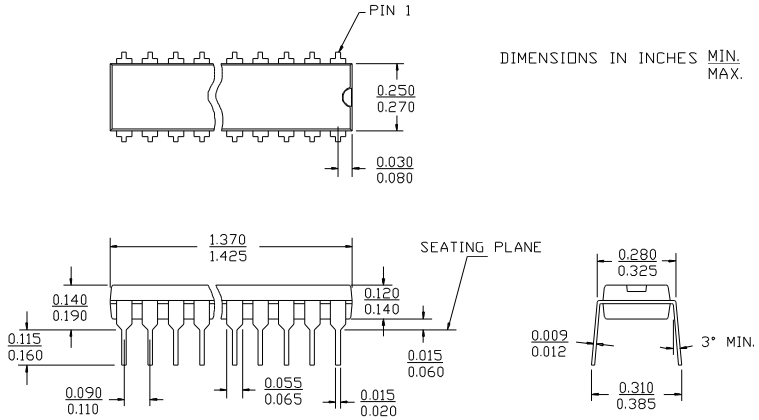
28-Lead (300-Mil) CerDIP D22
MIL-STD-1835 D-15 Config.A



28-Square Leadless Chip Carrier L64
MIL-STD-1835 C-4

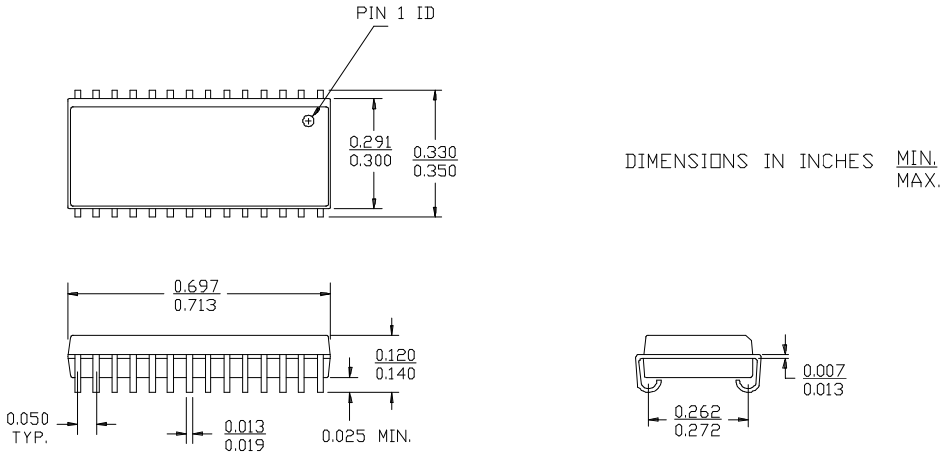


28-Lead (300-Mil) Molded DIP P21



Package Diagrams (continued)

28-Lead (300-Mil) Molded SOJ V21



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