CY7C371

UltraLogic™ 32-Macrocell Flash CPLD

Features

- **32 macrocells in two logic blocks**
- **32 I/O pins**
- **6 dedicated inputs including 2 clock pins**
- **No hidden delays**
- **High speed**
  - **— f_{MAX} = 143 MHz**
  - **— t_{PD}= 8.5 ns**
  - **— t_S = 5 ns**
  - **— t_{CO} = 6 ns**
- **Electrically alterable FLASH technology**
- **Available in 44-pin PLCC, CLCC, and TQFP packages**
- **Pin compatible with the CY7C372**

Functional Description

The CY7C371 is a Flash erasable Complex Programmable Logic Device (CPLD) and is part of the FLASH370 family of high-density, high-speed CPLDs. Like all members of the FLASH370 family, the CY7C371 is designed to bring the ease of use and high performance of the 22V10 to high-density CPLDs.

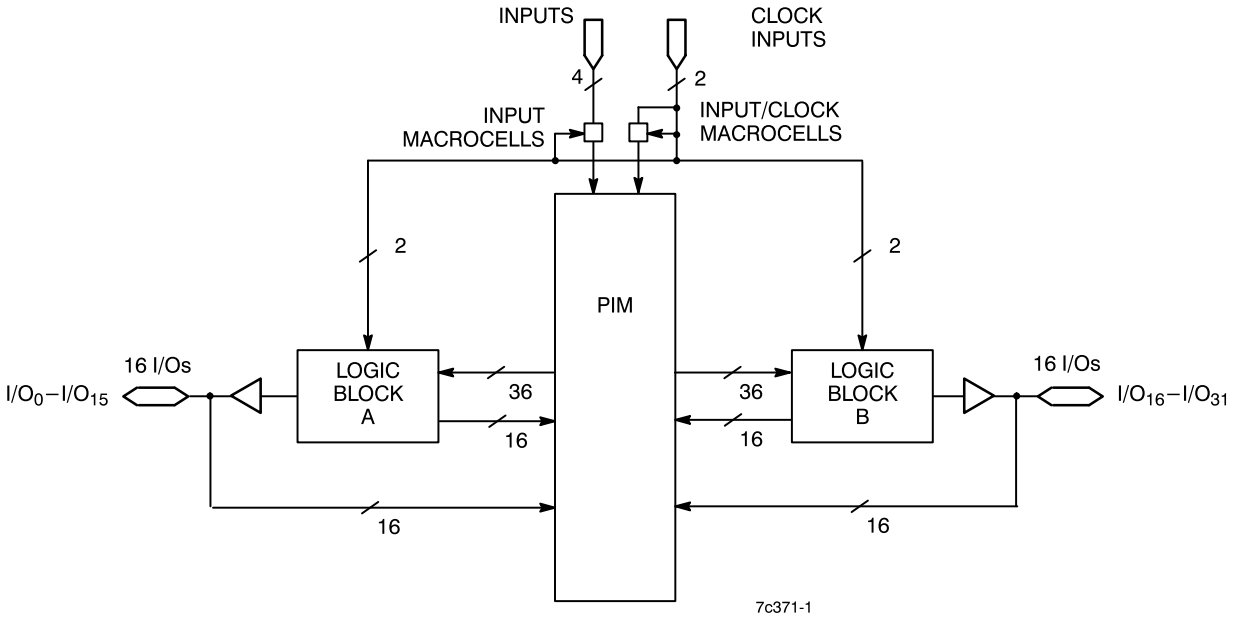
The 32 macrocells in the CY7C371 are divided between two logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370 family, the CY7C371 is rich in I/O resources. Each macrocell in the device features an associated I/O pin, resulting in 32 I/O pins on the CY7C371. In addition, there are four dedicated inputs and two input/clock pins.

Finally, the CY7C371 features a very simple timing model. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C371 remain the same.

Logic Block Diagram



Selection Guide

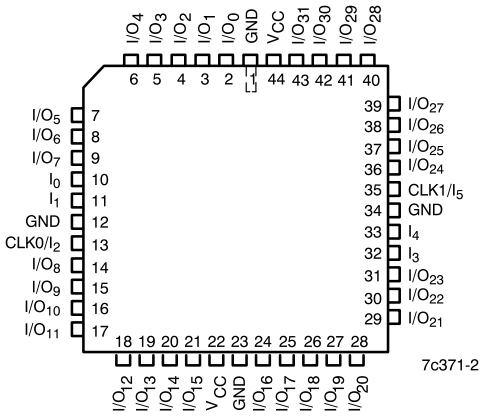
		7C371–143	7C371–110	7C371–83	7C371L–83	7C371–66	7C371L–66
Maximum Propagation Delay, t_{PD} (ns)		8.5	10	12	12	15	15
Minimum Set-Up, t_S (ns)		5	6	10	10	12	12
Maximum Clock to Output, t_{CO} (ns)		6	6.5	10	10	12	12
Maximum Supply Current, I_{CC} (mA)	Commercial	220	175	175	90	175	90
	Military/Ind.			220	110	220	110

Shaded area contains preliminary information.

CY7C371

Pin Configurations

PLCC/CLCC
Top View



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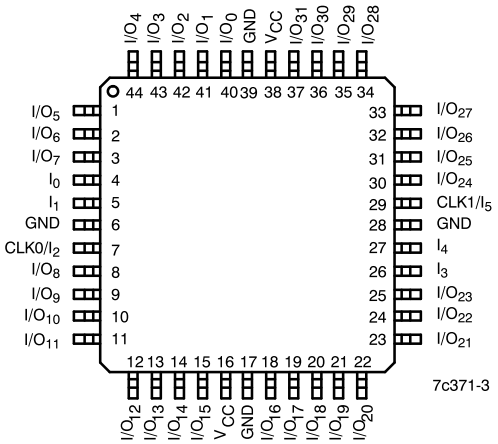
TQFP
Top View



7c371-3

Logic Block

The number of logic blocks distinguishes the members of the FLASH370 family. The CY7C371 includes two logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

Product Term Array

The product term array in the FLASH370 logic block includes 36 inputs from the PIM and outputs 86 product terms to the product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72 x 86. This large array in each logic block allows for very complex functions to be implemented in a single pass through the device.

Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product terms to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370 CPLDs. Note that product term allocation is handled by software and is invisible to the user.

I/O Macrocell

Each of the macrocells on the CY7C371 has a separate associated I/O pin. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The macrocell includes a register that can be optionally bypassed. It also has polarity control, and two global clocks to trigger the register. The macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is used as an input.

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the two logic blocks on the CY7C371 to the inputs and to each other. All inputs (including feedbacks) travel through the PIM. There is no speed penalty incurred by signals traversing the PIM.

Design Tools

Development software for the CY7C371 is available from Cypress's *Warp2*, *Warp2+*, and *Warp3* software packages. All of these products are based on the IEEE-standard VHDL language. Cypress also actively supports third-party design tools such as ABEL™, CUPL™, MINC, and LOG/iC™. Please contact your local Cypress representative for further information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

DC Program Voltage 12.5V

Output Current into Outputs (LOW) ..... 16 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Military[1]	−55°C to +125°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%

Note:
1. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −3.2 mA (Com'l/Ind)	2.4		V
			I_{OH} = −2.0 mA (Mil)			V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 16 mA (Com'l/Ind)		0.5	V
			I_{OL} = 12 mA (Mil)			V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all inputs[3]		2.0	7.0	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all inputs[2]		−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−50	+50	µA
I_{OS}	Output Short Circuit Current[4, 5]	V_{CC} = Max., V_{OUT} = 0.5V		−30	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = 1 mHz, V_{IN} = GND, V_{CC}[6]	Com'l		175	mA
			Com'l "L" −66, −83		90	
			Com'l−143, Mil/Ind		220	
			Ind "L" −66, −83		110	

Capacitance[4]

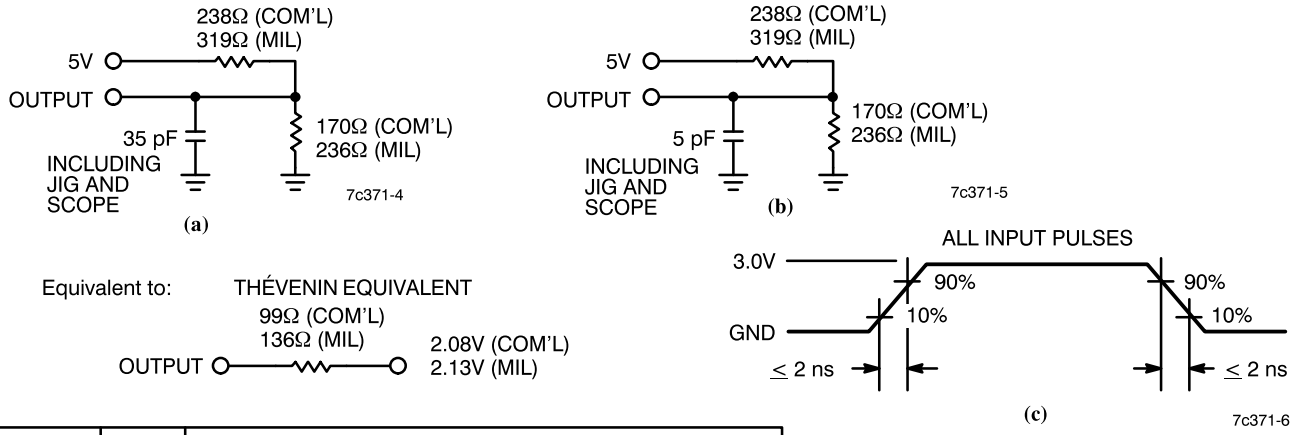
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 5.0V at f=1 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 5.0V at f = 1 MHz	12	pF

Endurance Characteristics[4]

Parameter	Description	Test Conditions	Min.	Max.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions	100		Cycles

Notes:
1. See the last page of this specification for Group A subgroup testing information.
2. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Tested initially and after any design or process changes that may affect these parameters.
5. Measured with 16-bit counter programmed into each logic block.

AC Test Loads and Waveforms



Parameter	V_X	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	V_{OH}, 0.5V, V_X 7c371-7
$t_{ER(+)}$	2.6V	V_{OL}, 0.5V, V_X 7c371-8
$t_{EA(+)}$	1.5V	V_X, 0.5V, V_{OH} 7c371-9
$t_{EA(-)}$	V_{thc}	V_X, 0.5V, V_{OL} 7c371-10

(d) Test Waveforms

Switching Characteristics Over the Operating Range[7]

Parameter	Description	7C371−143		7C371−110		7C371−83 7C371L−83		7C371−66 7C371L−66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters										
t_{PD}	Input to Combinatorial Output		8.5		10		12		15	ns
t_{PDL}	Input to Output Through Transparent Input or Output Latch		11.5		13		18		22	ns
t_{PDLL}	Input to Output Through Transparent Input and Output Latches		13.5		15		20		24	ns
t_{EA}	Input to Output Enable		13		14		19		24	ns
t_{ER}	Input to Output Disable		13		14		19		24	ns
Input Registered/Latched Mode Parameters										
t_{WL}	Clock or Latch Enable Input LOW Time[4]	2.5		3		4		5		ns
t_{WH}	Clock or Latch Enable Input HIGH Time[4]	2.5		3		4		5		ns
t_{IS}	Input Register or Latch Set-Up Time	2		2		3		4		ns
t_{IH}	Input Register or Latch Hold Time	2		2		3		4		ns
t_{ICO}	Input Register Clock or Latch Enable to Combinatorial Output		12		14		19		24	ns
t_{ICOL}	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		14		16		21		26	ns

Shaded area contains preliminary information.

Note:

6. All AC parameters are measured with 16 outputs switching.
7. This specification is intended to guarantee interface compatibility of the other members of the CY7C370 family with the CY7C371. This specification is met for the devices operating at the same ambient temperature and at the same power supply voltage.

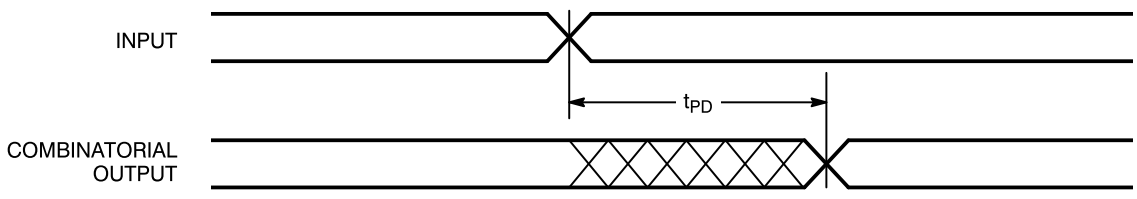
Switching Characteristics Over the Operating Range[6] (continued)

Parameter	Description	7C371−143		7C371−110		7C371−83 7C371L−83		7C371−66 7C371L−66		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Output Registered/Latched Mode Parameters										
t_{CO}	Clock or Latch Enable to Output		6		6.5		10		12	ns
t_S	Set-Up Time from Input to Clock or Latch Enable	5		6		10		12		ns
t_H	Register or Latch Data Hold Time	0		0		0		0		ns
t_{CO2}	Output Clock or Latch Enable to Output Delay (Through Memory Array)		12		14		19		24	ns
t_{SCS}	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	7		9		12		15		ns
t_{SCS2}	Output Clock Through Array to Output Clock (2-Pass Delay)[4]	13		16.5		21		27		ns
t_{SL}	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch Enable	9		10		12		15		ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		0		ns
f_{MAX1}	Maximum Frequency with Internal Feedback (Least of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[4]	143		111		83.3		66.6		MHz
f_{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)[4]	166.7		153.8		100		83.3		MHz
f_{MAX3}	Maximum Frequency with external feedback (Lesser of $1/(t_{CO} + t_S)$ and $1/(t_{WL} + t_{WH})$)[4]	91		80		50		41.6		MHz
$t_{OH} - t_{IH}$ 37x	Output Data Stable from Output clock Minus Input Register Hold Time for 7C37x[4, 8]	0		0		0		0		ns
Pipelined Mode Parameters										
t_{ICS}	Input Register Clock to Output Register Clock	7		9		12		15		ns
f_{MAX4}	Maximum Frequency in Pipelined Mode (Least of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)	125		111		76.9		62.5		MHz
Reset/Preset Parameters										
t_{RW}	Asynchronous Reset Width[4]	8		10		15		20		ns
t_{RR}	Asynchronous Reset Recovery Time[4]	10		12		17		22		ns
t_{RO}	Asynchronous Reset to Output		14		16		21		26	ns
t_{PW}	Asynchronous Preset Width[4]	8		10		15		20		ns
t_{PR}	Asynchronous Preset Recovery Time[4]	10		12		17		22		ns
t_{PO}	Asynchronous Preset to Output		14		16		21		26	ns
t_{POR}	Power-On Reset[4]		1		1		1		1	µs

Shaded area contains preliminary information.

Switching Waveforms

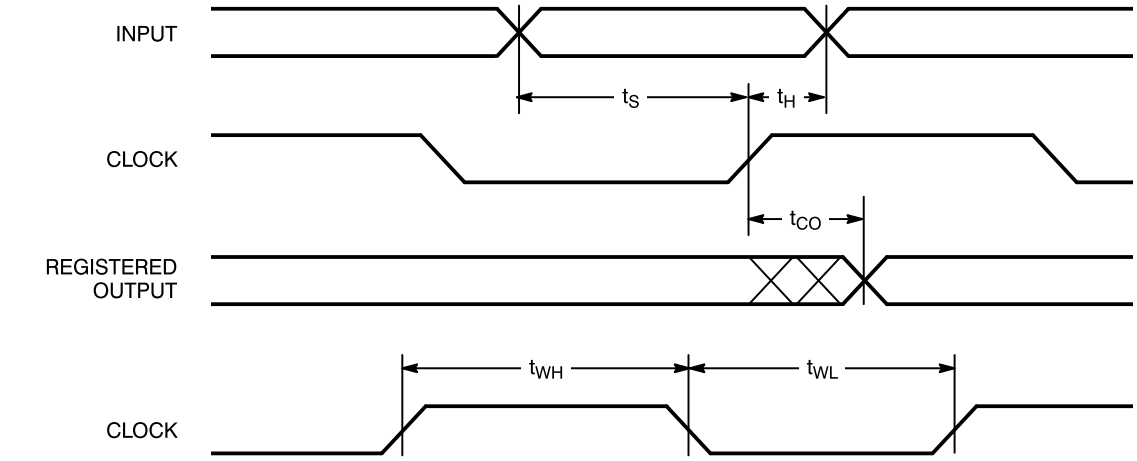
Combinatorial Output



7c371-11

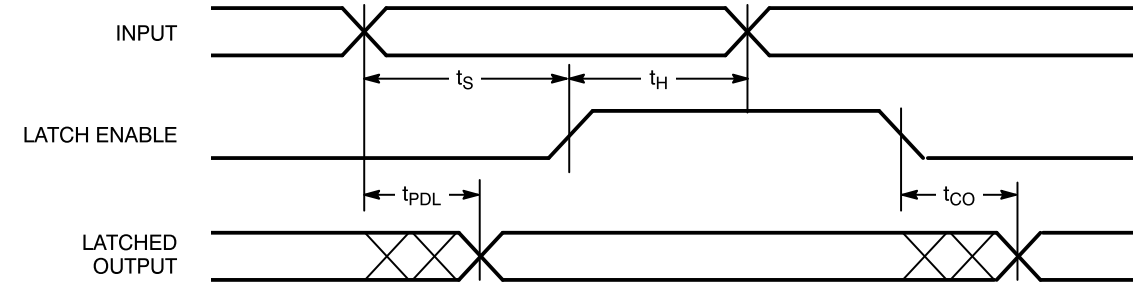
Switching Waveforms (continued)

Registered Output



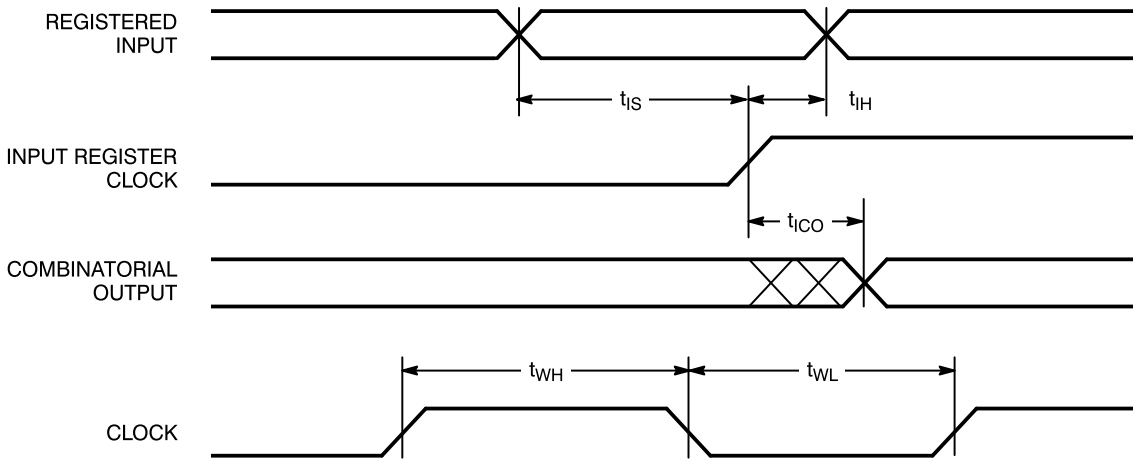
7c371-12

Latched Output



7c371-13

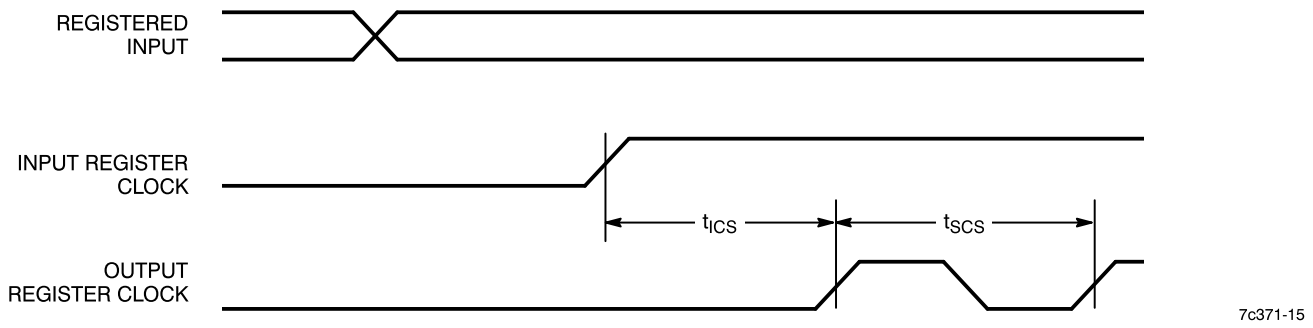
Registered Input



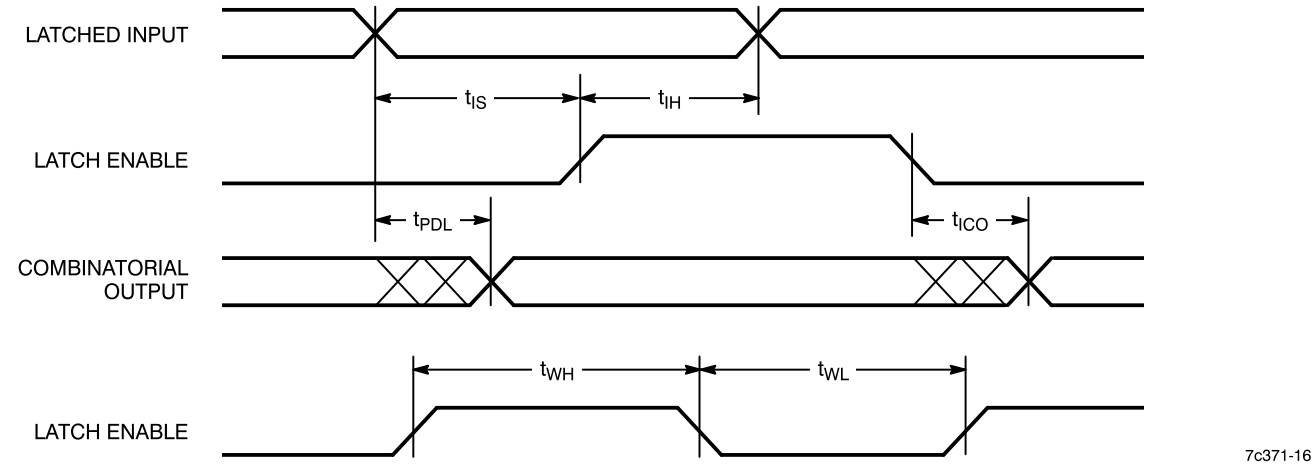
7c371-14

Switching Waveforms (continued)

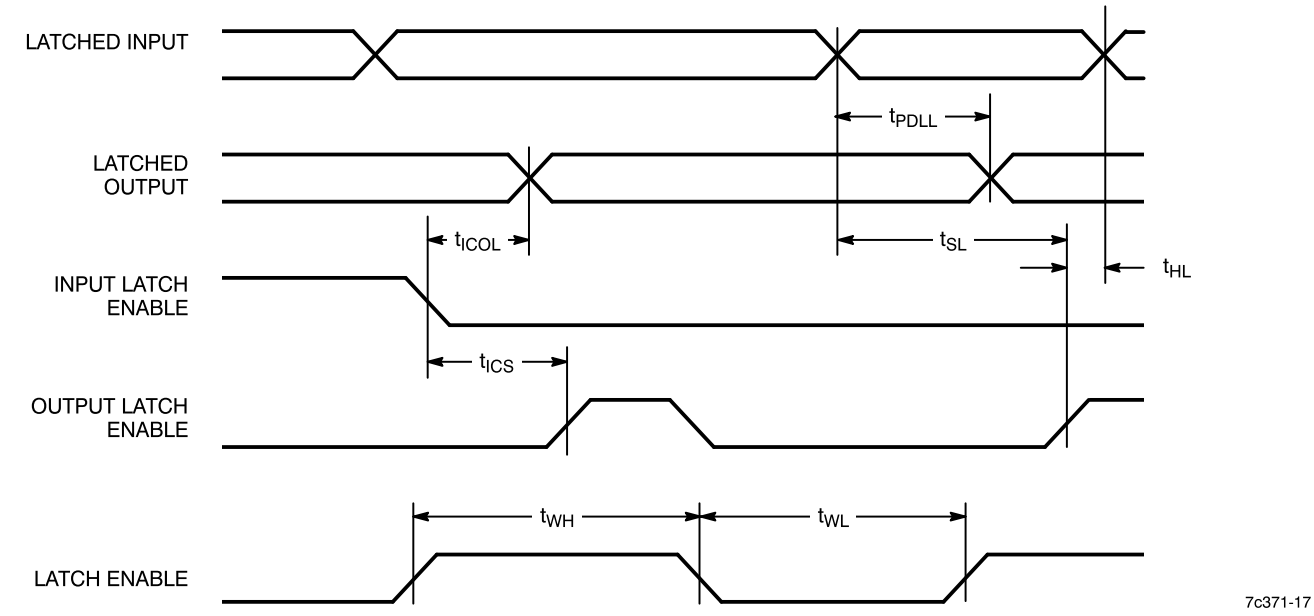
Clock to Clock



Latched Input

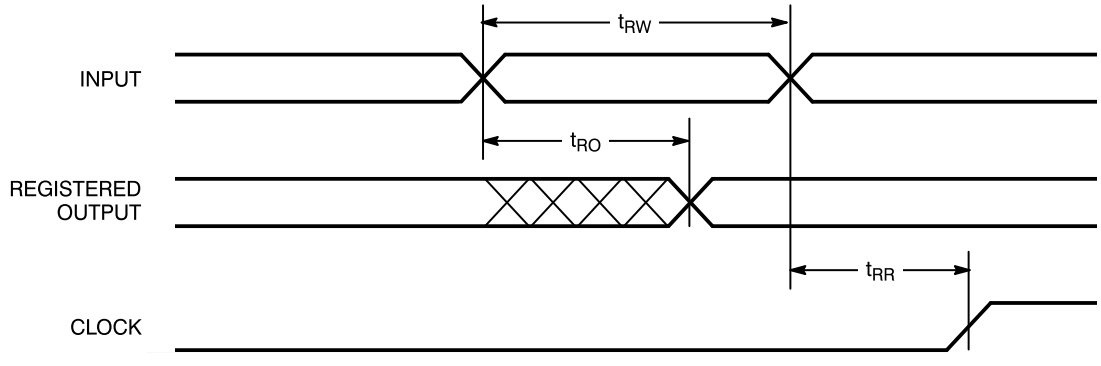


Latched Input and Output

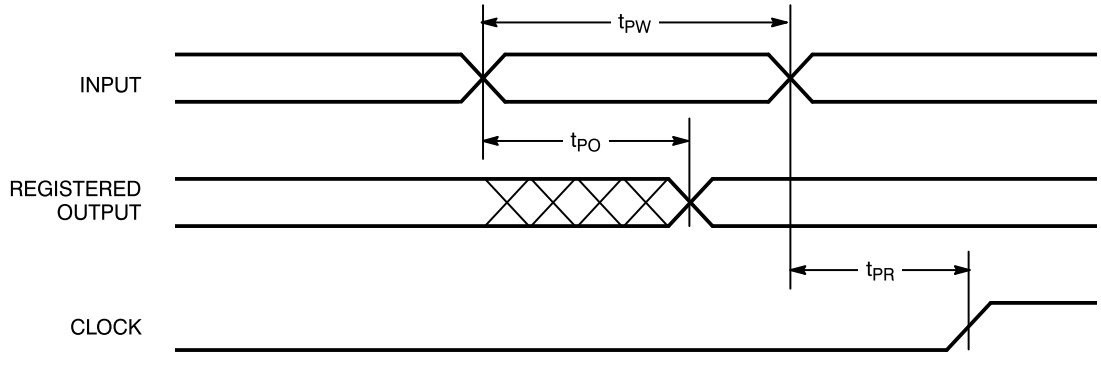


Switching Waveforms (continued)

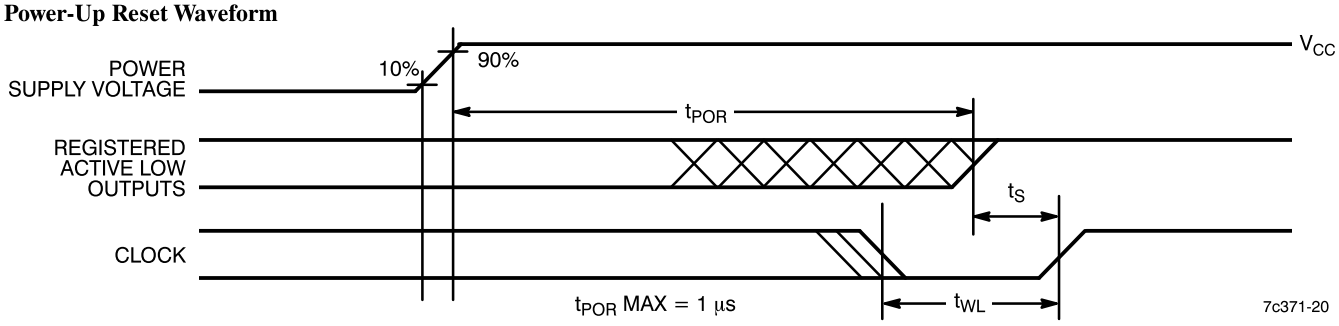
Asynchronous Reset



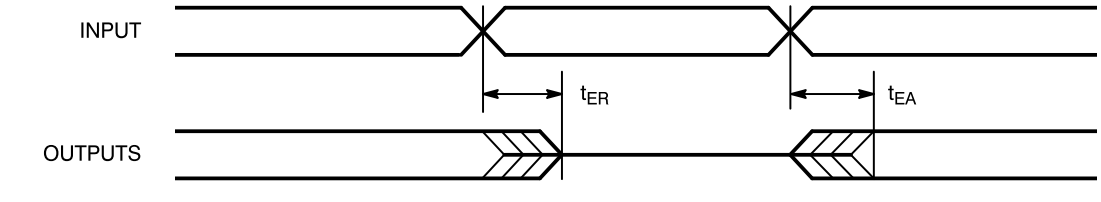
Asynchronous Preset



Power-Up Reset Waveform



Output Enable/Disable



Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
143	CY7C371−143AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371−143JC	J67	44-Lead Plastic Leaded Chip Carrier	
110	CY7C371−110AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371−110JC	J67	44-Lead Plastic Leaded Chip Carrier	
83	CY7C371−83AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371L−83AC	A44	44-Lead Thin Plastic Quad Flat Pack	
	CY7C371−83JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371L−83JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371−83AI	A44	44-Lead Thin Plastic Quad Flat Pack	Industrial
	CY7C371L−83AI	A44	44-Lead Thin Plastic Quad Flat Pack	
	CY7C371−83JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371L−83JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371−83YMB	Y67	44-Lead Ceramic Leaded Chip Carrier	Military
66	CY7C371−66AC	A44	44-Lead Thin Plastic Quad Flat Pack	Commercial
	CY7C371L−66AC	A44	44-Lead Thin Plastic Quad Flat Pack	
	CY7C371−66JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371L−66JC	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371−66AI	A44	44-Lead Thin Plastic Quad Flat Pack	Industrial
	CY7C371L−66AI	A44	44-Lead Thin Plastic Quad Flat Pack	
	CY7C371−66JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371L−66JI	J67	44-Lead Plastic Leaded Chip Carrier	
	CY7C371−66YMB	Y67	44-Lead Ceramic Leaded Chip Carrier	Military

Shaded areas contain preliminary information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{CO}	9, 10, 11
t_{ICO}	9, 10, 11
t_{S}	9, 10, 11
t_{H}	9, 10, 11
t_{IS}	9, 10, 11
t_{IH}	9, 10, 11
t_{ICS}	9, 10, 11

Document #: 38−00212−E

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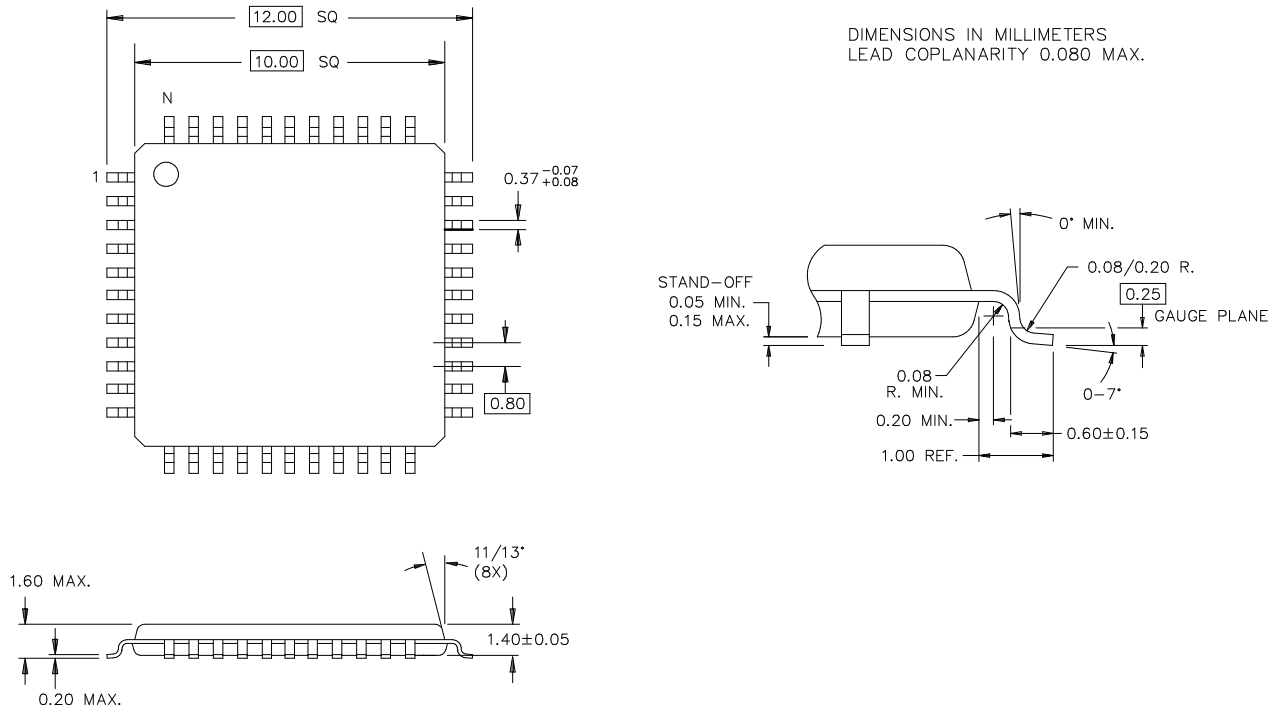
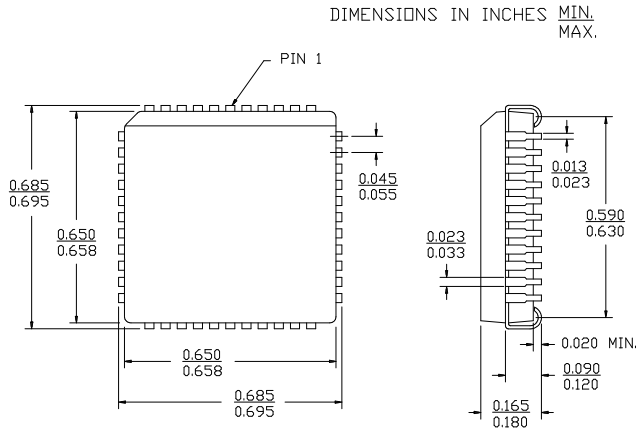
LOG/iC is a trademark of Isdata Corporation.
CUPL is a trademark of Logical Devices Incorporated.

Package Diagrams

44-Lead Thin Plastic Quad Flat Pack A44



44-Lead Plastic Leaded Chip Carrier J67



Package Diagrams (continued)

44-Pin Ceramic Leaded Chip Carrier Y67