CY7C199C

32K x 8 Static RAM

Features

- **Fast access time: 12 ns, 15 ns, 20 ns, and 25 ns**
- **Wide voltage range: 5.0V ± 10% (4.5V to 5.5V)**
- **CMOS for optimum speed/power**
- **TTL–compatible Inputs and Outputs**
- **Available in 28 DIP, 28 SOJ, and 28 TSOP I.**
- **2.0V Data Retention**
- **Low CMOS standby power**
- **Automated Power–down when deselected**

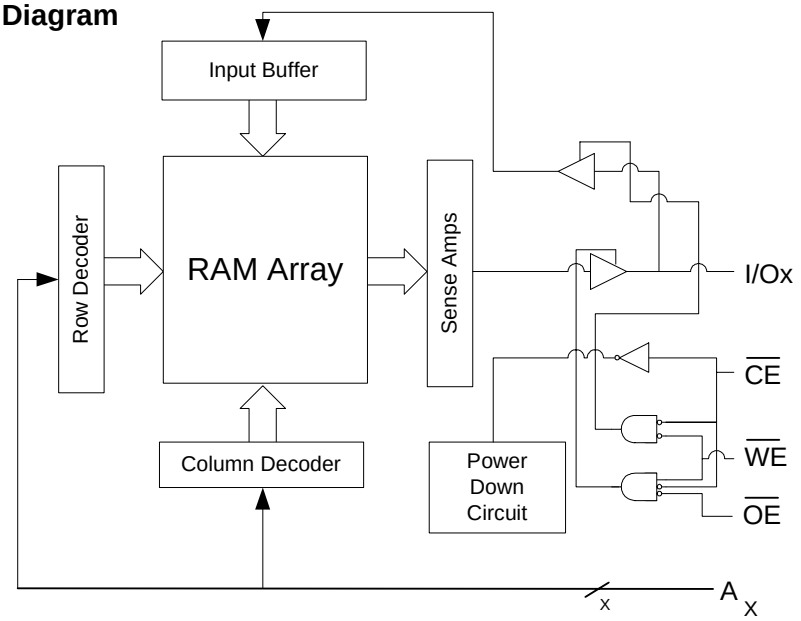
General Description[1]

The CY7C199C is a high–performance CMOS Asynchronous SRAM organized as 32K by 8 bits that supports an asynchronous memory interface. The device features an automatic power–down feature that significantly reduces power consumption when deselected.

See the Truth Table in this datasheet for a complete description of read and write modes.

The CY7C199C is available in 28 DIP, 28 SOJ, and 28 TSOP I package(s).

Logic Block Diagram



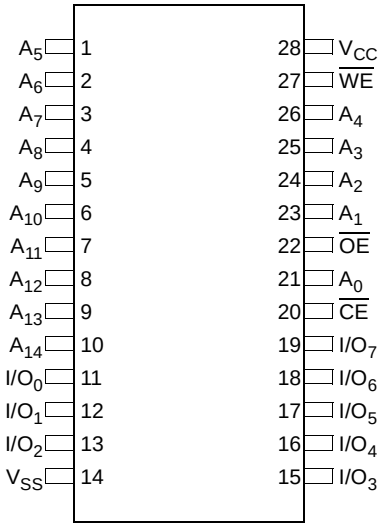
Product Portfolio

	12 ns	15 ns	20 ns	25 ns	Unit
Maximum Access Time	12	15	20	25	ns
Maximum Operating Current	85	80	75	75	mA
Maximum CMOS Standby Current (low power)	500	500	500	500	uA

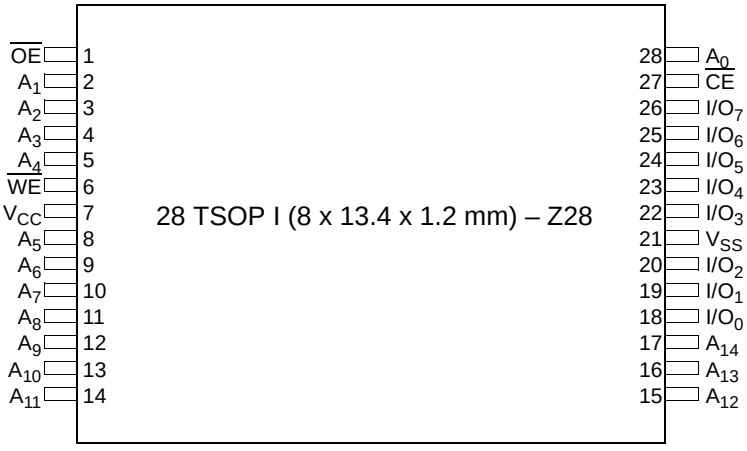
Notes:
1. For best–practices recommendations, please refer to the Cypress application note *System Design Guidelines* on www.cypress.com.

Pin Layout and Specifications

28 DIP (6.9 x 35.6 x 3.5 mm) – P21

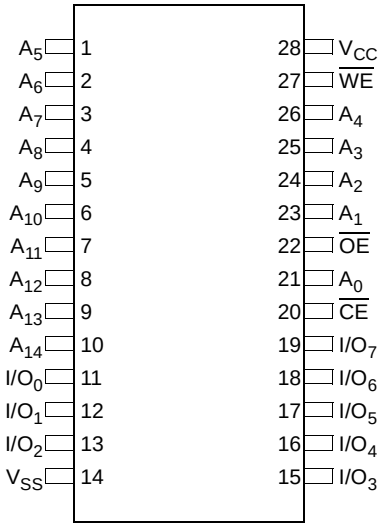


28 TSOP I (8 x 13.4 x 1.2 mm) – Z28



Pin Layout and Specifications (continued)

28 SOJ (8 x 18 x 3.5 mm) – V21



Pin Description

Pin	Type	Description	DIP	SOJ	TSOP I
A_X	Input	Address Inputs.	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 21, 23, 24, 25, 26	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 21, 23, 24, 25, 26	2, 3, 4, 5, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 28
$\overline{CE}$	Control	Chip Enable.	20	20	27
I/O_X	Input or Output	Data Input/Outputs.	11, 12, 13, 15, 16, 17, 18, 19	11, 12, 13, 15, 16, 17, 18, 19	18, 19, 20, 22, 23, 24, 25, 26
$\overline{OE}$	Control	Output Enable.	22	22	1
V_{CC}	Supply	Power (5.0V).	28	28	7
V_{SS}	Supply	Ground.	14	14	21
$\overline{WE}$	Control	Write Enable.	27	27	6

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/Ox	Mode	Power
H	X	X	High Z	Deselect / Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, outputs disabled	Active (I_{CC})

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested.)

Parameter	Description	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_{AMB}	Ambient Temperature with Power Applied (i.e. case temperature)	–55 to +125	°C
V_{CC}	Core Supply Voltage Relative to V_{SS}	–0.5 to +7.0	V
V_{IN}, V_{OUT}	DC Voltage Applied to any Pin Relative to V_{SS}	–0.5 to V_{CC} + 0.5	V
I_{OUT}	Output Short–Circuit Current	20	mA
V_{ESD}	Static Discharge Voltage (per MIL–STD–883, Method 3015)	> 2001	V
I_{LU}	Latch–up Current	> 200	mA

Operating Range

Range	Ambient Temperature (T_A)	Voltage Range (V_{CC})
Commercial	0°C to 70°C	5.0V ± 10%
Industrial	–40°C to 85°C	5.0V ± 10%

DC Electrical Characteristics Over the Operating Range (–12, –15)[2]

Parameter	Description	Condition	Power	12 ns		15 ns		Unit
				Min.	Max.	Min.	Max.	
V_{IH}	Input HIGH Voltage		–	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		–	–0.5	0.8	–0.5	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	–	2.4	–	2.4	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	–	–	0.4	–	0.4	V
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = F_{MAX} = $1/t_{RC}$	–	–	85	–	80	mA
I_{SB1}	Automatic $\overline{CE}$ Power–down Current TTL Inputs	Max. V_{CC}, $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = F_{MAX}	–	–	30	–	30	mA
			L	–	10	–	10	mA
I_{SB2}	Automatic $\overline{CE}$ Power–down Current CMOS Inputs	Max. V_{CC}, $\overline{CE} \geq V_{CC}$ – 0.3V, $V_{IN} \geq V_{CC}$ – 0.3V, or $V_{IN} \leq$ 0.3V, f = 0	–	–	10	–	10	mA
			L	–	500	–	500	uA
I_{OZ}	Output Leakage Current	GND ≤ Vi ≤ V_{CC}, Output Disabled	–	–5	+5	–5	+5	uA
I_{IX}	Input Load Current	GND ≤ Vi ≤ V_{CC}	–	–5	+5	–5	+5	uA

DC Electrical Characteristics Over the Operating Range (–20, –25)[3]

Parameter	Description	Condition	Power	20 ns		25 ns		Unit
				Min	Max	Min	Max	
V_{IH}	Input HIGH Voltage		–	2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		–	–0.5	0.8	–0.5	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	–	2.4	–	2.4	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	–	–	0.4	–	0.4	V

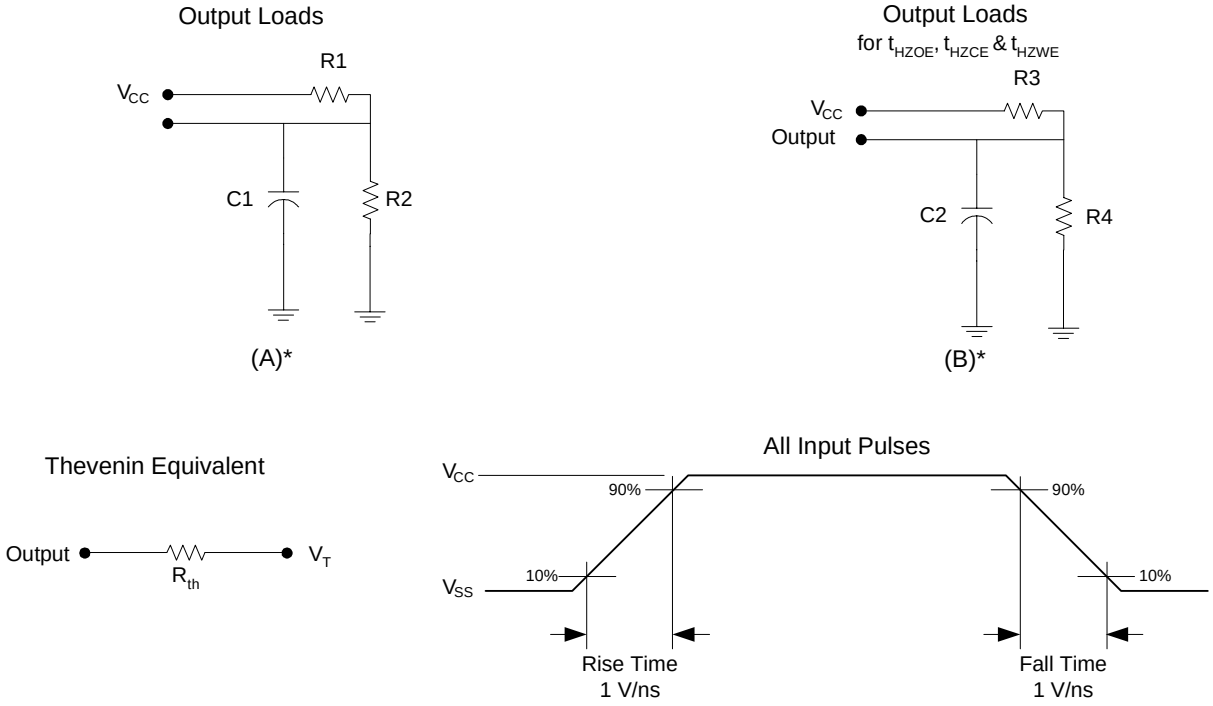
Notes:
2. V_{IL} (min) = –2.0V for pulse durations of less than 20 ns.
3. V_{IL} (min) = –2.0V for pulse durations of less than 20 ns.

Parameter	Description	Condition	Power	20 ns		25 ns		Unit
				Min	Max	Min	Max	
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = F_{MAX} = $1/t_{RC}$	–	–	75	–	75	mA
I_{SB1}	Automatic $\overline{CE}$ Power–down Current TTL Inputs	Max. V_{CC}, $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = F_{MAX}	–	–	30	–	30	mA
			L	–	10	–	10	mA
I_{SB2}	Automatic $\overline{CE}$ Power–down Current CMOS Inputs	Max. V_{CC}, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V$, f = 0	–	–	10	–	10	mA
			L	–	500	–	500	uA
I_{OZ}	Output Leakage Current	GND ≤ Vi ≤ V_{CC}, Output Disabled	–	–5	+5	–5	+5	uA
I_{IX}	Input Load Current	GND ≤ Vi ≤ V_{CC}	–	–5	+5	–5	+5	uA

Capacitance[4]

Parameter	Description	Conditions	Max	Unit
			ALL – PACKAGES	
C_{IN}	Input Capacitance	T_A = 25C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		8	

AC Test Loads



* including scope and jig capacitance

Notes:
4. Tested initially and after any design or process change that may affect these parameters.

AC Test Conditions

Parameter	Description	Nom.	Unit
C1	Capacitor 1	30	pF
C2	Capacitor 2	5	
R1	Resistor 1	480	Ω
R2	Resistor 2	255	
R3	Resistor 3	480	
R4	Resistor 4	255	
R_{TH}	Resistor Thevenin	167	
V_{TH}	Voltage Thevenin	1.73	V

Thermal Resistance[5]

Parameter	Description	Conditions	TSOP I	SOJ	DIP	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 square inch, two–layer printed circuit board	88.6	79	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		21.94	41.42	TBD	

AC Electrical Characteristics[6, 7, 8]

Parameter	Description	12 ns		15 ns		20 ns		25 ns		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	12	–	15	–	20	–	25	–	ns
t_{AA}	Address to Data Valid	–	12	–	15	–	20	–	25	ns
t_{OHA}	Data Hold from Address Change	3	–	3	–	3	–	3	–	ns
t_{ACE}	$\overline{CE}$ to Data Valid	–	12	–	15	–	20	–	25	ns
t_{DOE}	$\overline{OE}$ to Data Valid	–	5	–	7	–	9	–	9	ns
t_{LZOE}	$\overline{OE}$ to Low Z	0	–	0	–	0	–	0	–	ns
t_{HZOE}	$\overline{OE}$ to High Z	–	5	–	7	–	9	–	9	ns
t_{LZCE}	$\overline{CE}$ to Low Z	3	–	3	–	3	–	3	–	ns
t_{HZCE}	$\overline{CE}$ to High Z	–	5	–	7	–	9	–	9	ns
t_{PU}	$\overline{CE}$ to Power–Up	0	–	0	–	0	–	0	–	ns
t_{PD}	$\overline{CE}$ to Power–Down	–	12	–	15	–	20	–	20	ns
t_{WC}	Write Cycle Time	12	–	15	–	20	–	25	–	ns
t_{SCE}	$\overline{CE}$ to Write End	9	–	10	–	15	–	15	–	ns
t_{AW}	Address Set–Up to Write End	9	–	10	–	15	–	15	–	ns
t_{HA}	Address Hold from Write End	0	–	0	–	0	–	0	–	ns

Notes:

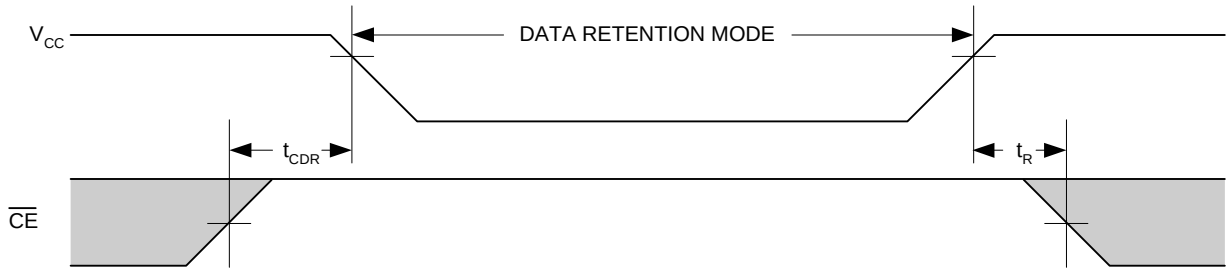
5. Test Conditions assume a transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set–up and hold timing should be referenced to the leading edge of the signal that terminates the write.
8. t_{HZOE}, t_{HZCE}, t_{HZWE} are specified as in part (b) of the A/C Test Loads. Transitions are measured ± 200 mV from steady state voltage.

Parameter	Description	12 ns		15 ns		20 ns		25 ns		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{SA}	Address Set–Up to Write Start	0	–	0	–	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse Width	8	–	9	–	15	–	15	–	ns
t_{SD}	Data Set–Up to Write End	8	–	9	–	10	–	10	–	ns
t_{HD}	Data Hold from Write End	0	–	0	–	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z	–	7	–	7	–	10	–	10	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3	–	3	–	3	–	3	–	ns

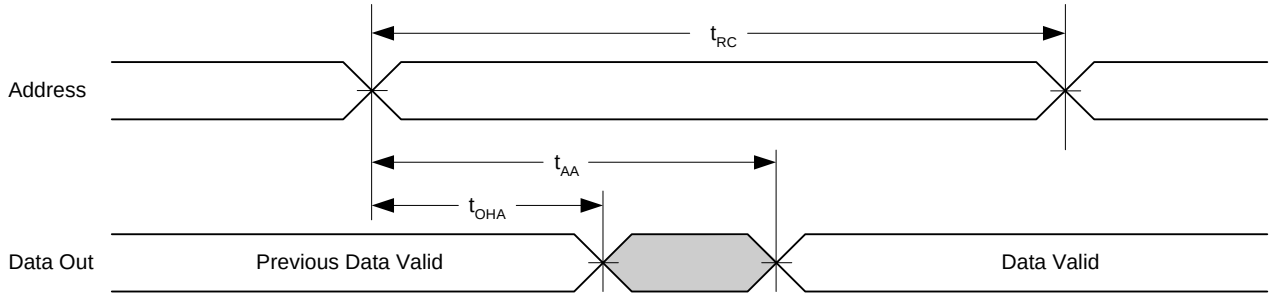
Data Retention Characteristics[9]

Parameter	Description	Condition	ALL		Unit
			Min	Max	
V_{DR}	V_{CC} for Data Retention		2.0	–	V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR}$=2.0V, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	–	150	uA
t_{CDR}	Chip Deselect to Data Retention Time		0	–	ns
t_R	Operation Recovery Time		200	–	us

Timing Waveforms
Data Retention Waveform

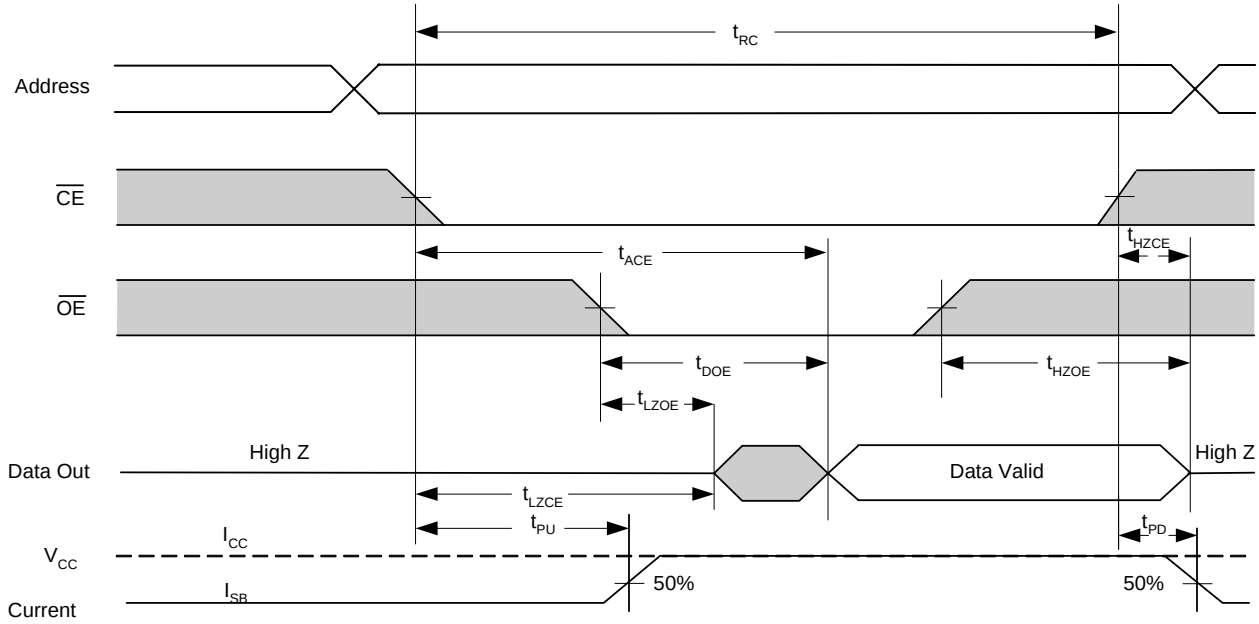


Read Cycle No. 1 [10, 11]

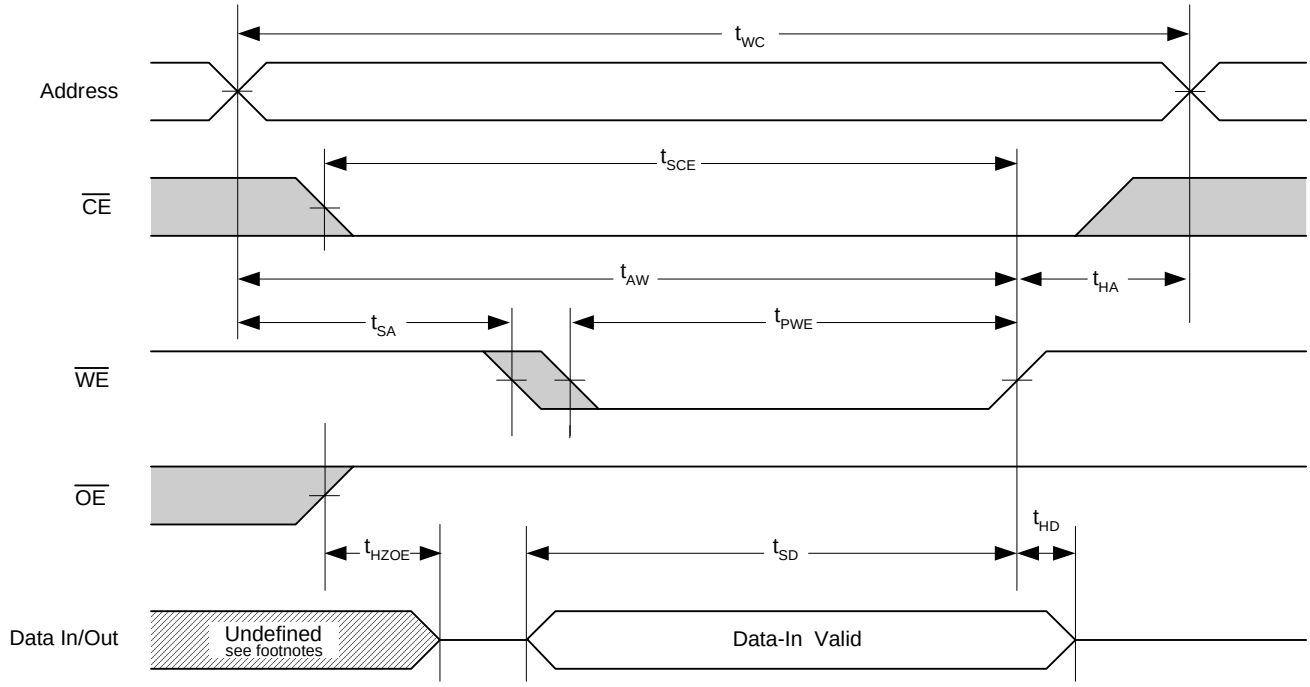


Notes:
9. L–version only.
10. Device is continuously selected. $\overline{OE} = V_{IL} = \overline{CE}$.
11. $\overline{WE}$ is HIGH for Read Cycle.

Read Cycle No. 2 [12, 13]



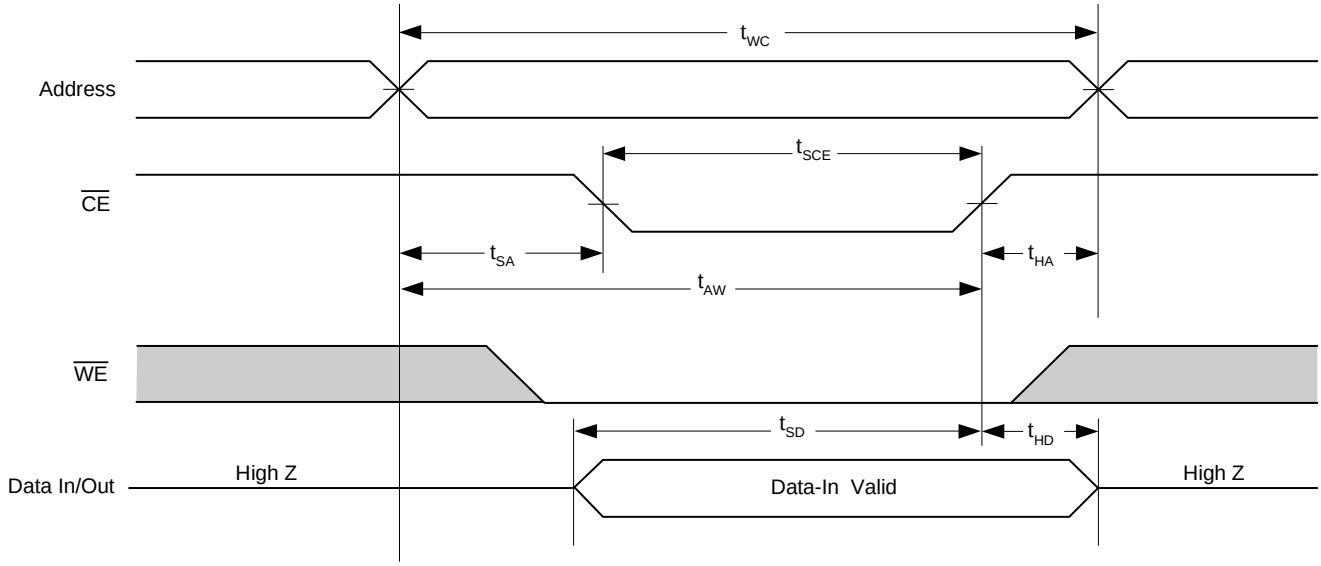
Write Cycle No. 1 ($\overline{WE}$ Controlled)[14, 15, 16]



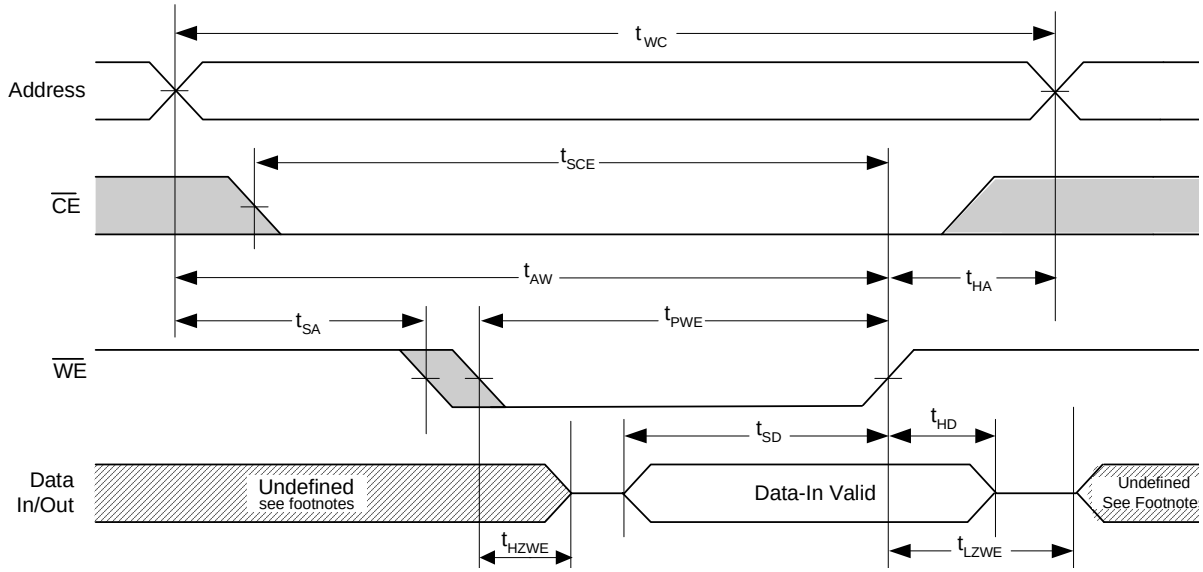
Notes:

12. This cycle is $\overline{OE}$ Controlled and $\overline{WE}$ is HIGH read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
14. This cycle is $\overline{WE}$ controlled, $\overline{OE}$ is HIGH during write.
15. Data In/Out is high impedance if $\overline{OE} = V_{IH}$.
16. During this period the I/Os are in output state and input signals should not be applied.

Write Cycle No. 2 ($\overline{CE}$ Controlled)[17, 18, 19]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ Low)[20]



Notes:

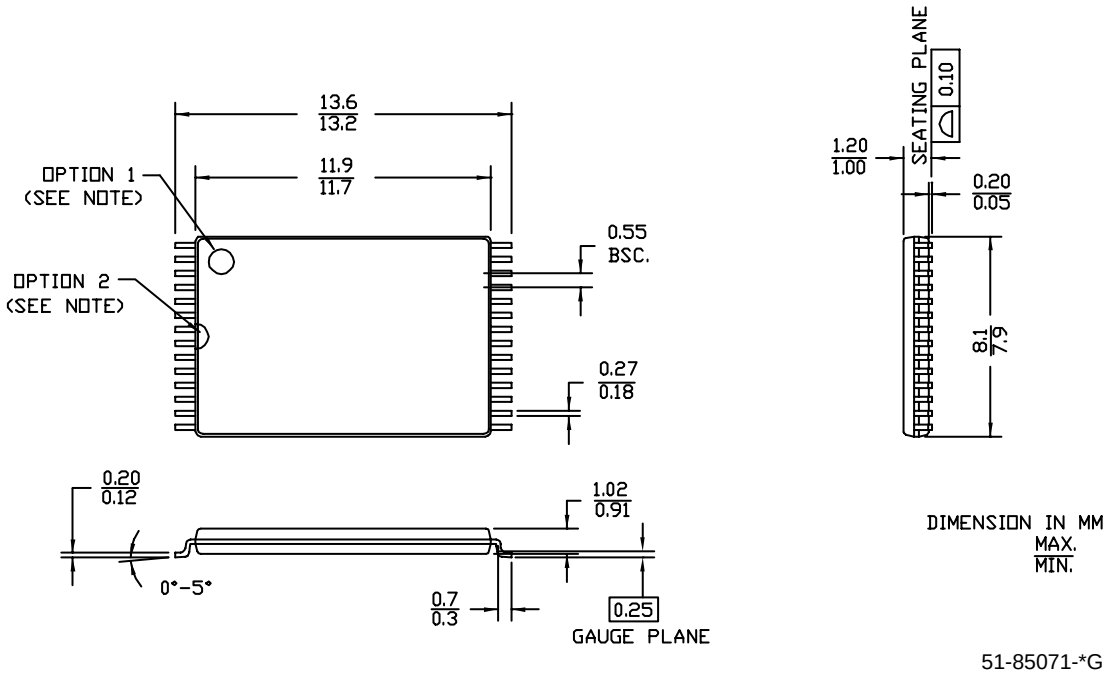
17. This cycle is $\overline{CE}$ controlled.
18. Data In/Out is high impedance if $\overline{OE} = V_{IH}$.
19. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high–impedance state.
20. The cycle is $\overline{WE}$ controlled, $\overline{OE}$ low. The minimum write cycle time is the sum of t_{HZWE} and t_{SD}.

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Power Option	Operating Range
12 ns	CY7C199C–12VC	V21	28 SOJ (8 x 18 x 3.5 mm)	Standard	Commercial
12 ns	CY7C199C–12ZC	Z28	28 TSOP I (8 x 13.4 x 1.2 mm)	Standard	Commercial
12 ns	CY7C199C–12VI	V21	28 SOJ (8 x 18 x 3.5 mm)	Standard	Industrial
15 ns	CY7C199C–15PC	P21	28 DIP (6.9 x 35.6 x 3.5 mm)	Standard	Commercial
15 ns	CY7C199C–15VC	V21	28 SOJ (8 x 18 x 3.5 mm)	Standard	Commercial
15 ns	CY7C199C–15ZC	Z28	28 TSOP I (8 x 13.4 x 1.2 mm)	Standard	Commercial
15 ns	CY7C199C–15VI	V21	28 SOJ (8 x 18 x 3.5 mm)	Standard	Industrial
15 ns	CY7C199CL–15VC	V21	28 SOJ (8 x 18 x 3.5 mm)	Low Power	Commercial
15 ns	CY7C199CL–15ZC	Z28	28 TSOP I (8 x 13.4 x 1.2 mm)	Low Power	Commercial
15 ns	CY7C199CL–15VI	V21	28 SOJ (8 x 18 x 3.5 mm)	Low Power	Industrial
20 ns	CY7C199C–20VC	V21	28 SOJ (8 x 18 x 3.5 mm)	Standard	Commercial
20 ns	CY7C199C–20ZI	Z28	28 TSOP I (8 x 13.4 x 1.2 mm)	Standard	Industrial
25 ns	CY7C199C–25PC	P21	28 DIP (6.9 x 35.6 x 3.5 mm)	Standard	Commercial

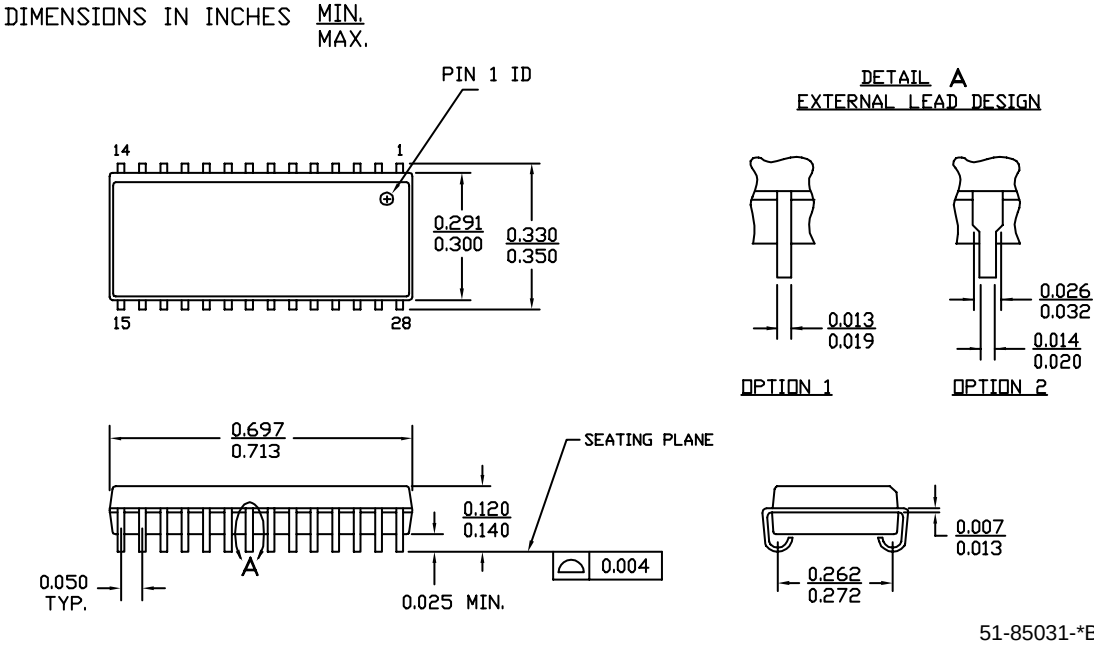
Package Diagram

28 TSOP I (8 × 13.4 × 1.2 mm) – Z28

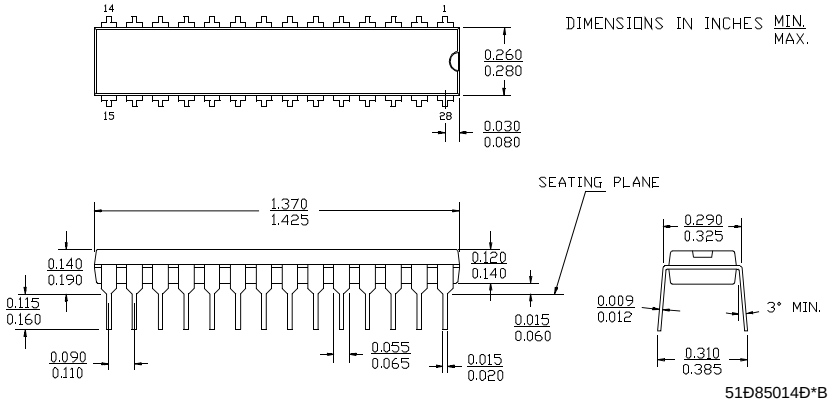


Package Diagram (continued)

28 SOJ (8 × 18 × 3.5 mm) – V21



28-Lead (300-Mil) Molded DIP P21



All product and company names mentioned in this document may be the trademarks of their respective holders.

Document History Page

Document Title: CY7C199C 32K x 8 Static RAM Document Number: 38-05408				
REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	129233	09/11/03	HGK	New Data Sheet
*A	129697	09/15/03	KKV	Minor change: Move Product Portfolio from page 4 to page 1 Move Truthtable from page 9 to page 3