CY7C1399

32K x 8 3.3V Static RAM

Features

- **Single 3.3V power supply**
- **Ideal for low-voltage cache memory applications**
- **High speed**
  - **12/15 ns**
- **Low active power**
  - **255 mW (max.)**
- **Low CMOS standby power (L)**
  - **180 µW (max.), f=f_{MAX}**
- **2.0V data retention (L)**
  - **40 µW**
- **Low-power alpha immune 6T cell**
- **Plastic SOJ and TSOP packaging**

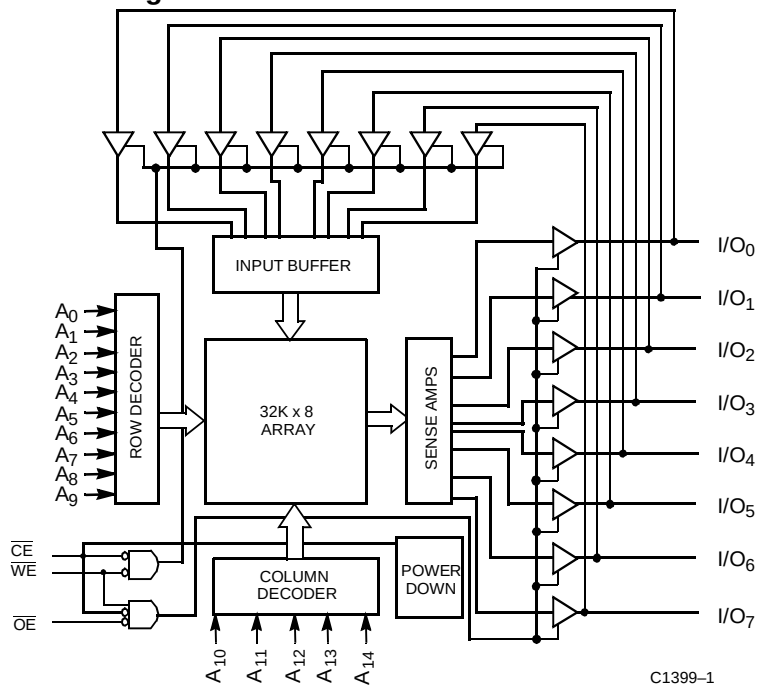
Functional Description

The CY7C1399 is a high-performance 3.3V CMOS Static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$) and active LOW Output Enable ($\overline{OE}$) and three-state drivers. The device has an automatic power-down feature, reducing the power consumption by more than 95% when deselected.

An active LOW Write Enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and Write Enable ($\overline{WE}$) is HIGH. The CY7C1399 is available in 28-pin standard 300-mil-wide SOJ and TSOP Type I packages.

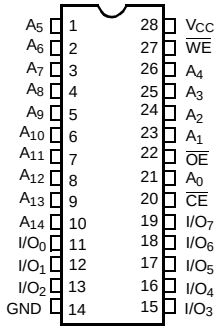
Logic Block Diagram



C1399–1

Pin Configurations

SOJ
Top View



C1399–2

Selection Guide

		7C1399–12	7C1399–15	7C1399–20	7C1399–25	7C1399–35
Maximum Access Time (ns)		12	15	20	25	35
Maximum Operating Current (mA)		60	55	50	45	40
Maximum CMOS Standby Current (µA)		500	500	500	500	500
Maximum CMOS Standby Current (µA)	L	50	50	50	50	50

Pin Configuration

TSOP
Top View



C1399–3

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[1] .... –0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State[1]..... –0.5V to V_{CC} + 0.5V

DC Input Voltage[1]..... –0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ±300 mV
Industrial	–40°C to +85°C	3.3V ±300 mV

Electrical Characteristics Over the Operating Range[1]

Parameter	Description	Test Conditions		7C1399–12 Min.	7C1399–12 Max.	7C1399–15 Min.	7C1399–15 Max.	7C1399–20 Min.	7C1399–20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage			–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current			–1	+1	–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		–5	+5	–5	+5	–5	+5	µA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max., V_{OUT} = GND			–300		–300		–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$			60		55		50	mA
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH}, or V_{IN} ≤ V_{IL}, f = f_{MAX}			5		5		5	mA
			L		3		3		3	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs[3]	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, WE ≥ V_{CC} – 0.3V or WE ≤ 0.3V, f = f_{MAX}			500		500		500	µA
			L		50		50		50	

Notes:
1. Minimum voltage is equal to –2.0V for pulse durations of less than 20 ns.
2. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
3. Device draws low standby current regardless of switching on the addresses.

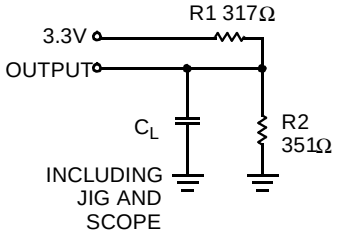
Electrical Characteristics Over the Operating Range(continued)

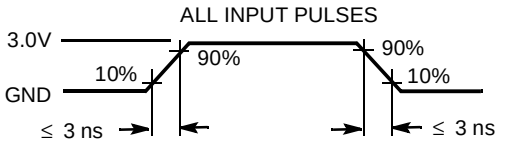
Parameter	Description	Test Conditions		7C1399–25 Min.	7C1399–25 Max.	7C1399–35 Min.	7C1399–35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage			–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current			–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		–5	+5	–5	+5	µA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max., V_{OUT} = GND			–300		–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$			45		40	mA
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH}, or V_{IN} ≤ V_{IL}, f = f_{MAX}			5		5	mA
			L		3		3	mA
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs[3]	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC}–0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, WE≥V_{CC}–0.3V or WE≤ 0.3V, f=f_{MAX}			500		500	µA
			L		50		50	µA

Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	5	pF
C_{IN}: Controls			6	pF
C_{OUT}	Output Capacitance		6	pF

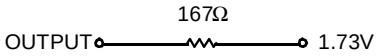
AC Test Loads and Waveforms





C1399–4

Equivalent to: THÉVENIN EQUIVALENT



Note:
4. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[5]

Parameter	Description	7C1399–12		7C1399–15		7C1399–20		7C1399–25		7C1399–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	12		15		20		25		35		ns
t_{AA}	Address to Data Valid		12		15		20		25		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6		7		8		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[6]	0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		5		6		6		7		7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		6		7		7		8		8	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		25		35	ns
WRITE CYCLE[8, 9]												
t_{WC}	Write Cycle Time	12		15		20		25		35		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		10		12		15		20		ns
t_{AW}	Address Set-Up to Write End	8		10		12		15		20		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		10		12		15		20		ns
t_{SD}	Data Set-Up to Write End	7		8		10		11		12		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8]		7		7		7		7		7	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	3		3		3		3		3		ns

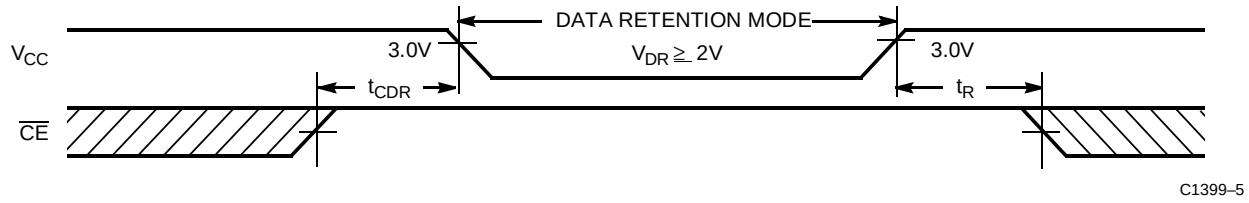
Data Retention Characteristics (Over the Operating Range)

Parameter	Description		Conditions	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention			2.0		V
I_{CCDR}	Data Retention Current		$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		200	µA
		L			20	µA
t_{CDR}[4]	Chip Deselect to Data Retention Time			0		ns
t_R[4]	Operation Recovery Time			t_{RC}		ns

Notes:

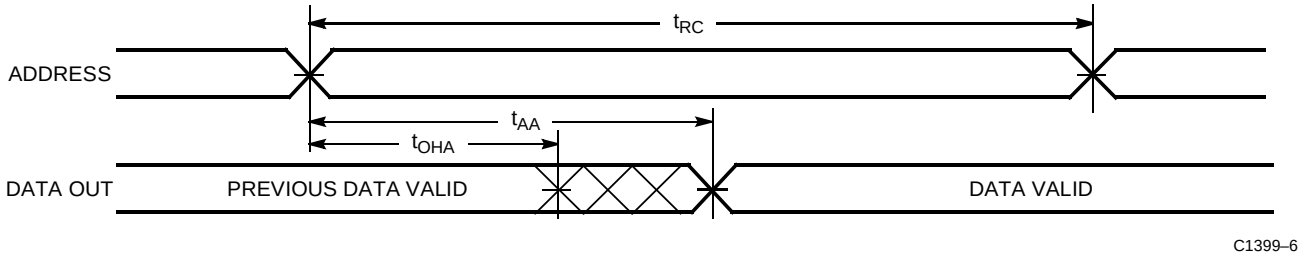
5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and capacitance C_L = 30 pF.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE}, t_{HZCE}, t_{HZWE} are specified with C_L = 5 pF as in AC Test Loads. Transition is measured ±500 mV from steady state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Waveform

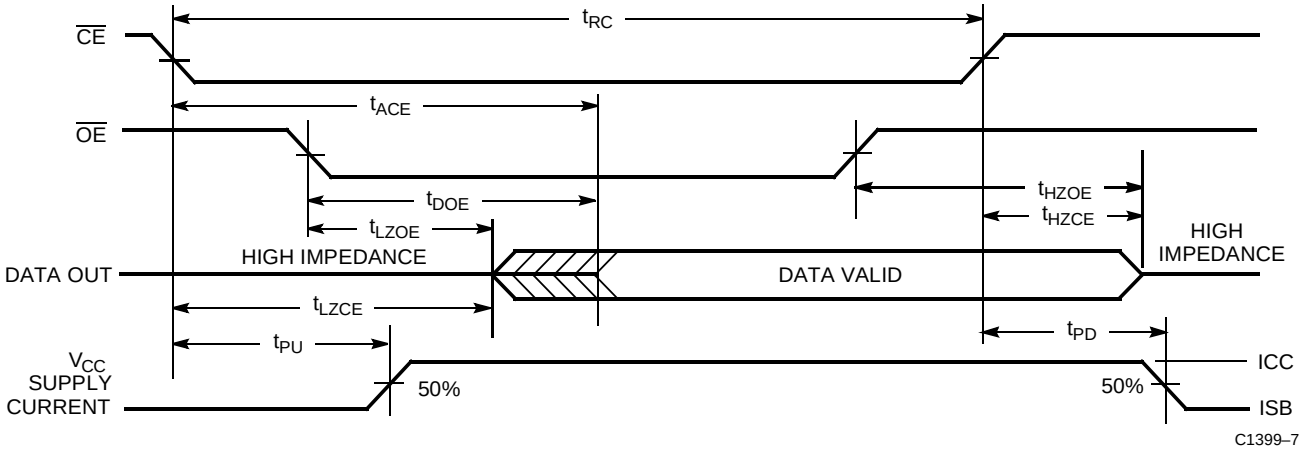


Switching Waveforms

Read Cycle No. 1[10, 11]



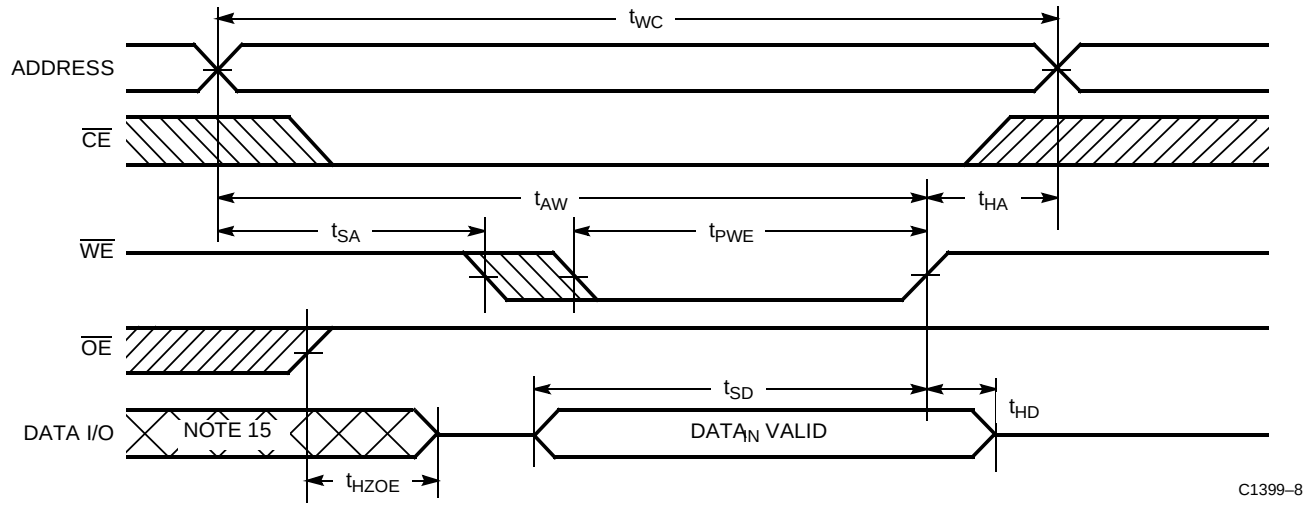
Read Cycle No. 2[11, 12]



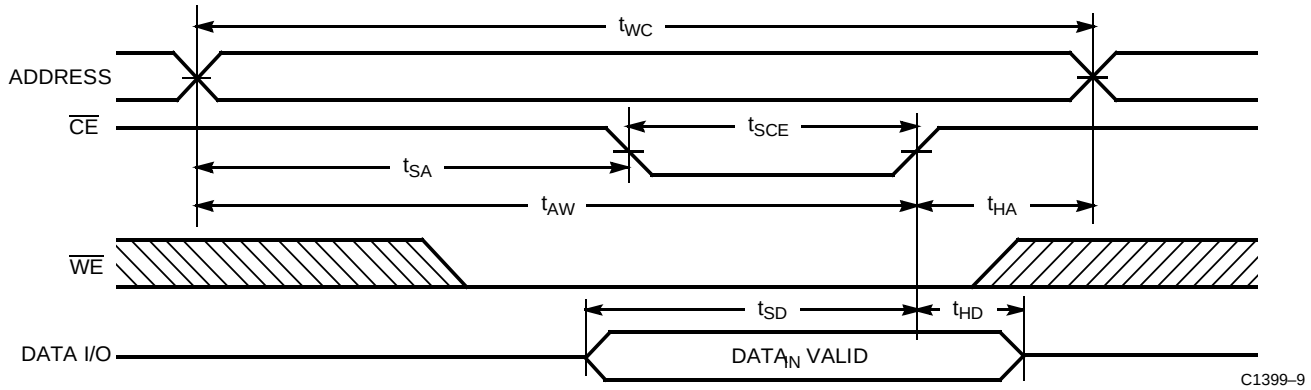
Notes:
10. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
11. $\overline{WE}$ is HIGH for read cycle.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

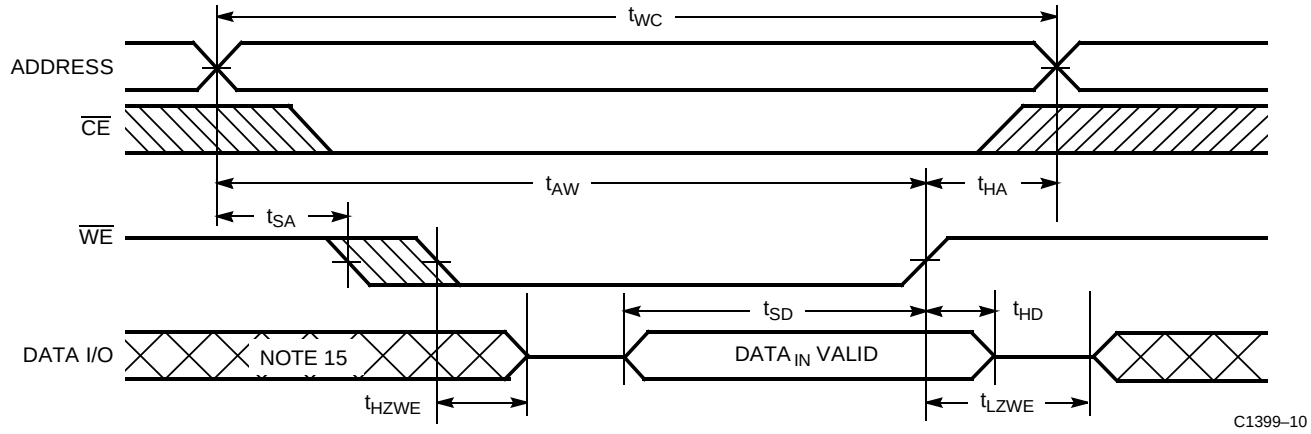
Write Cycle No. 1 ($\overline{WE}$ Controlled)[8, 13, 14]



Write Cycle No. 2 ($\overline{CE}$ Controlled)[8, 13, 14]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[9, 14]



Notes:
13. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
15. During this period, the I/Os are in the output state and input signals shold not be applied.

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output Disabled	Active (I_{CC})

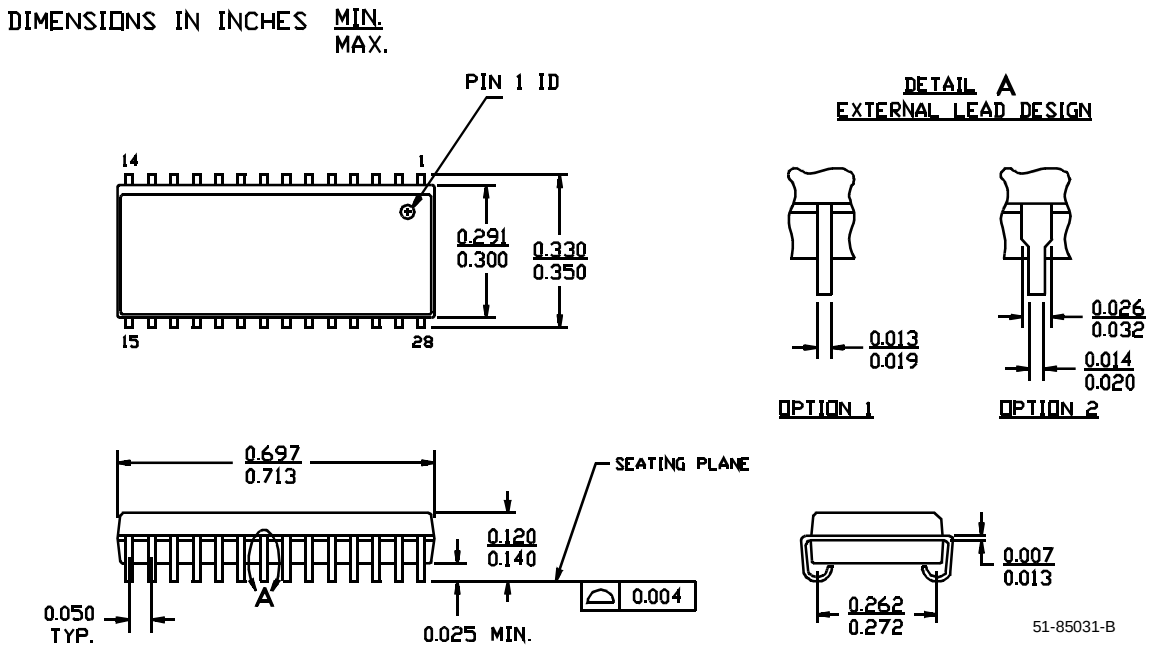
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1399–12VC	V21	28-Lead Molded SOJ	Commercial
	CY7C1399L–12VC	V21	28-Lead Molded SOJ	
	CY7C1399–12ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C1399L–12ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C1399–12VI	V21	28-Lead Molded SOJ	Industrial
	CY7C1399–12ZI	Z28	28-Lead Thin Small Outline Package	
15	CY7C1399–15VC	V21	28-Lead Molded SOJ	Commercial
	CY7C1399L–15VC	V21	28-Lead Molded SOJ	
	CY7C1399–15ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C1399L–15ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C1399–15VI	V21	28-Lead Molded SOJ	Industrial
	CY7C1399–15ZI	Z28	28-Lead Thin Small Outline Package	
	CY7C1399L–15ZI	Z28	28-Lead Thin Small Outline Package	
20	CY7C1399–20VC	V21	28-Lead Molded SOJ	Commercial
	CY7C1399L–20VC	V21	28-Lead Molded SOJ	
	CY7C1399–20ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C1399L–20ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C1399–20VI	V21	28-Lead Molded SOJ	Industrial
25	CY7C1399–25VC	V21	28-Lead Molded SOJ	Commercial
	CY7C1399L–25VC	V21	28-Lead Molded SOJ	
	CY7C1399–25ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C1399L–25ZC	Z28	28-Lead Thin Small Outline Package	
35	CY7C1399–35VC	V21	28-Lead Molded SOJ	Commercial
	CY7C1399L–35VC	V21	28-Lead Molded SOJ	
	CY7C1399–35ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C1399L–35ZC	Z28	28-Lead Thin Small Outline Package	

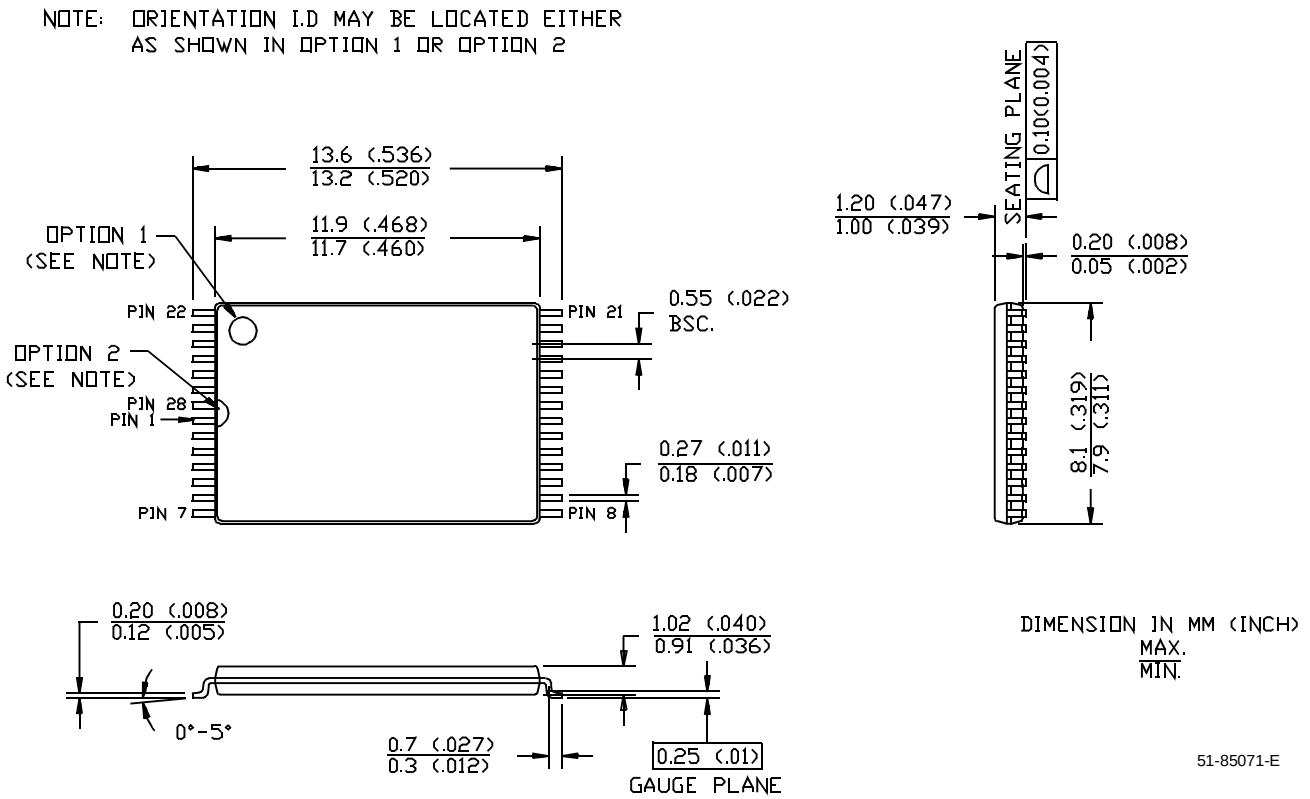
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Package Diagrams

28-Lead (300-Mil) Molded SOJ V21



28-Lead Thin Small Outline Package Z28



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