CY7C12411KV18, CY7C12561KV18
CY7C12431KV18, CY7C12451KV18

36-Mbit QDR® II+ SRAM 4-Word Burst Architecture (2.0 Cycle Read Latency)

Features

- Separate Independent Read and Write Data Ports
  - Supports concurrent transactions
- 450 MHz Clock for High Bandwidth
- 4-word Burst for Reducing Address Bus Frequency
- Double Data Rate (DDR) Interfaces on both Read and Write Ports (Data transferred at 900 MHz) at 450 MHz
- Available in 2.0 Clock Cycle Latency
- Two Input Clocks (K and $\overline{K}$) for Precise DDR Timing
  - SRAM uses rising edges only
- Echo Clocks (CQ and $\overline{CQ}$) simplify Data Capture in High Speed Systems
- Data Valid Pin (QVLD) to indicate Valid Data on the Output
- Single Multiplexed Address Input Bus Latches Address Inputs for Read and Write Ports
- Separate Port Selects for Depth Expansion
- Synchronous Internally Self Timed Writes
- QDR® II+ operates with 2.0 Cycle Read Latency when $\overline{DOFF}$ is asserted HIGH
- Operates similar to QDR-I Device with 1 Cycle Read Latency when $\overline{DOFF}$ is asserted LOW
- Available in x8, x9, x18, and x36 Configurations
- Full Data Coherency, providing most Current Data
- Core V_{DD} = 1.8V± 0.1V; I/O V_{DDQ} = 1.4V to V_{DD}[1]
  - Supports both 1.5V and 1.8V I/O supply
- HSTL Inputs and Variable Drive HSTL Output Buffers
- Available in 165-Ball FBGA Package (13 x 15 x 1.4 mm)
- Offered in both Pb-free and non Pb-free Packages
- JTAG 1149.1 Compatible Test Access Port
- Phase Locked Loop (PLL) for Accurate Data Placement

Configurations

With Read Cycle Latency of 2.0 cycles:

CY7C12411KV18 – 4M x 8

CY7C12561KV18 – 4M x 9

CY7C12431KV18 – 2M x 18

CY7C12451KV18 – 1M x 36

Functional Description

The CY7C12411KV18, CY7C12561KV18, CY7C12431KV18, and CY7C12451KV18 are 1.8V Synchronous Pipelined SRAMs, equipped with QDR II+ architecture. Similar to QDR II architecture, QDR II+ architecture consists of two separate ports: the read port and the write port to access the memory array. The read port has dedicated data outputs to support read operations and the write port has dedicated data inputs to support write operations. QDR II+ architecture has separate data inputs and data outputs to eliminate the need to “turnaround” the data bus that exists with common I/O devices. Each port is accessed through a common address bus. Addresses for read and write addresses are latched on alternate rising edges of the input (K) clock. Accesses to the QDR II+ read and write ports are completely independent of one another. To maximize data throughput, both read and write ports are equipped with DDR interfaces. Each address location is associated with four 8-bit words (CY7C12411KV18), 9-bit words (CY7C12561KV18), 18-bit words (CY7C12431KV18), or 36-bit words (CY7C12451KV18) that burst sequentially into or out of the device. Because data is transferred into and out of the device on every rising edge of both input clocks (K and $\overline{K}$), memory bandwidth is maximized while simplifying system design by eliminating bus “turnarounds”.

Depth expansion is accomplished with port selects, which enables each port to operate independently.

All synchronous inputs pass through input registers controlled by the K or $\overline{K}$ input clocks. All data outputs pass through output registers controlled by the K or $\overline{K}$ input clocks. Writes are conducted with on-chip synchronous self-timed write circuitry.

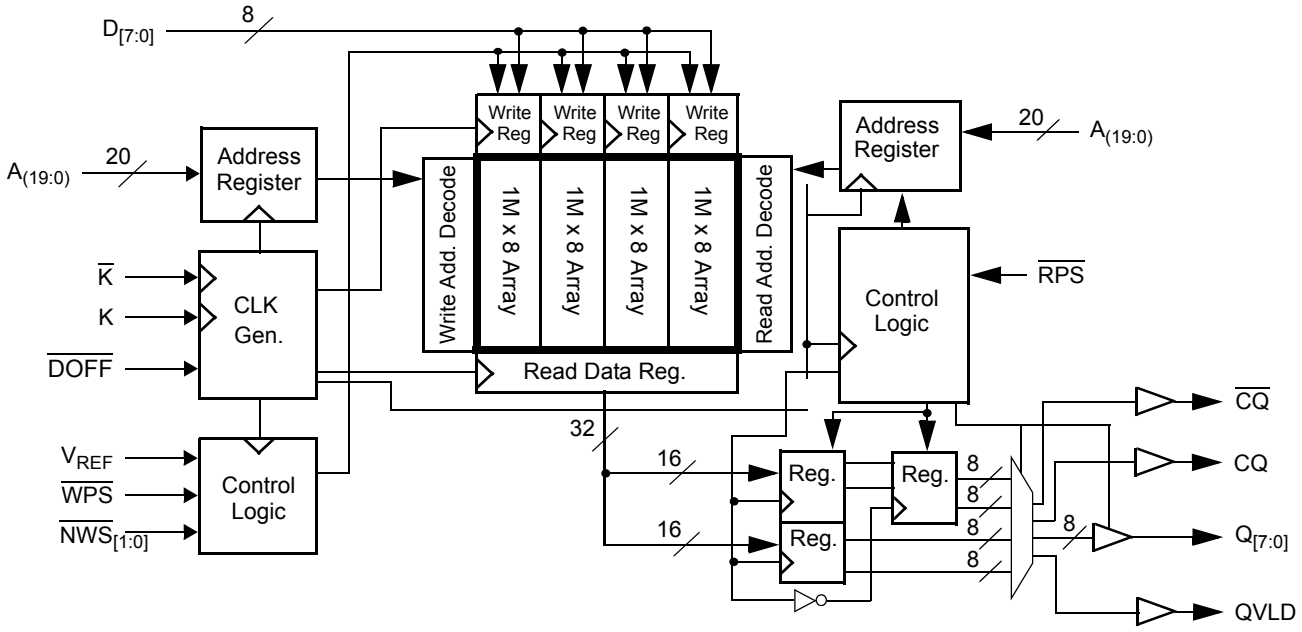
These devices are down bonded from the 65nm 72M QDRII+/DDRII+ devices and hence have the same I_{DD}/I_{SB1} values and the same JTAG ID code as the equivalent 72M device options. For details refer to the application note AN53189, *65nm Technology InterimQDRII+/DDRII+ SRAM device family description.*

Table 1. Selection Guide

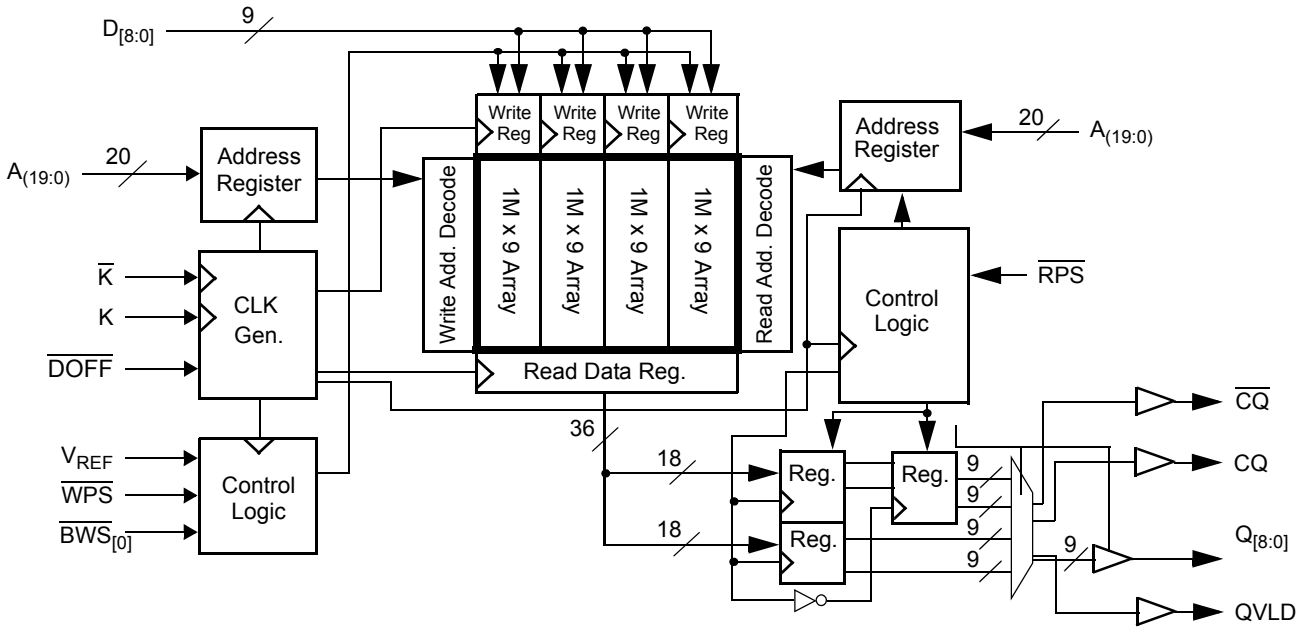
Description		450 MHz	400 MHz	375 MHz	333 MHz	Unit
Max Operating Frequency		450	400	375	333	MHz
Max Operating Current	x8	760	690	660	600	mA
	x9	760	690	660	600	
	x18	780	710	680	620	
	x36	1100	1000	950	850	

Note
1. The Cypress QDR II+ devices surpass the QDR consortium specification and can support V_{DDQ} = 1.4V to V_{DD}.

Logic Block Diagram (CY7C12411KV18)

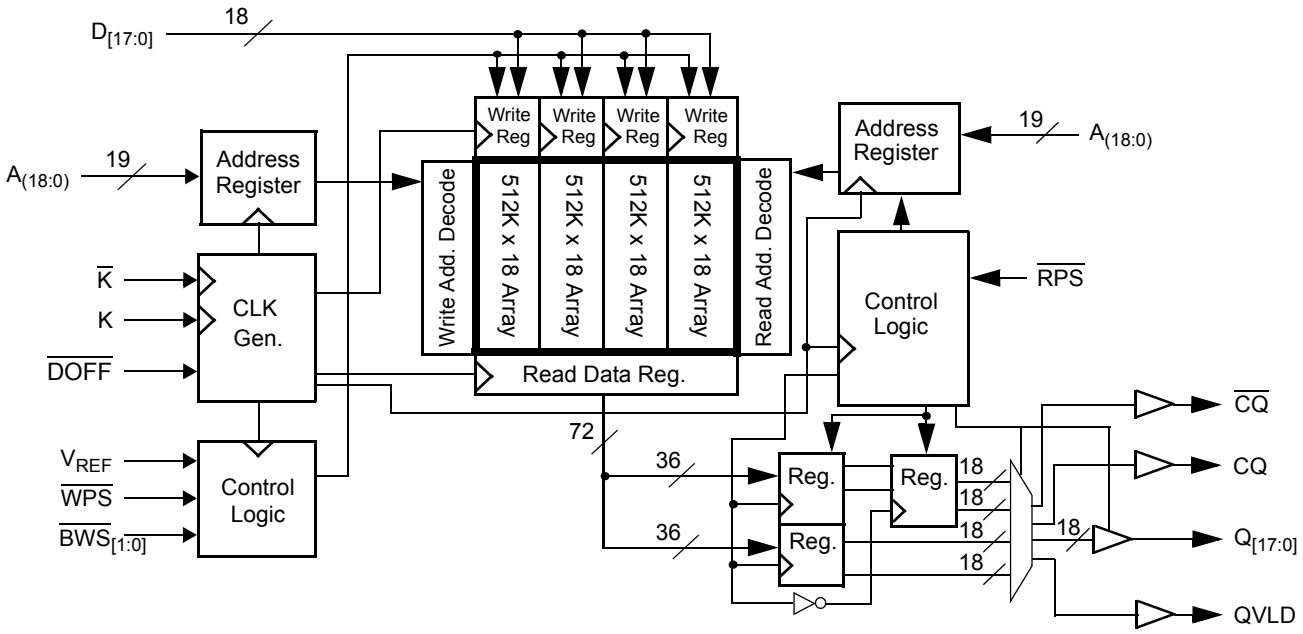


Logic Block Diagram (CY7C12561KV18)

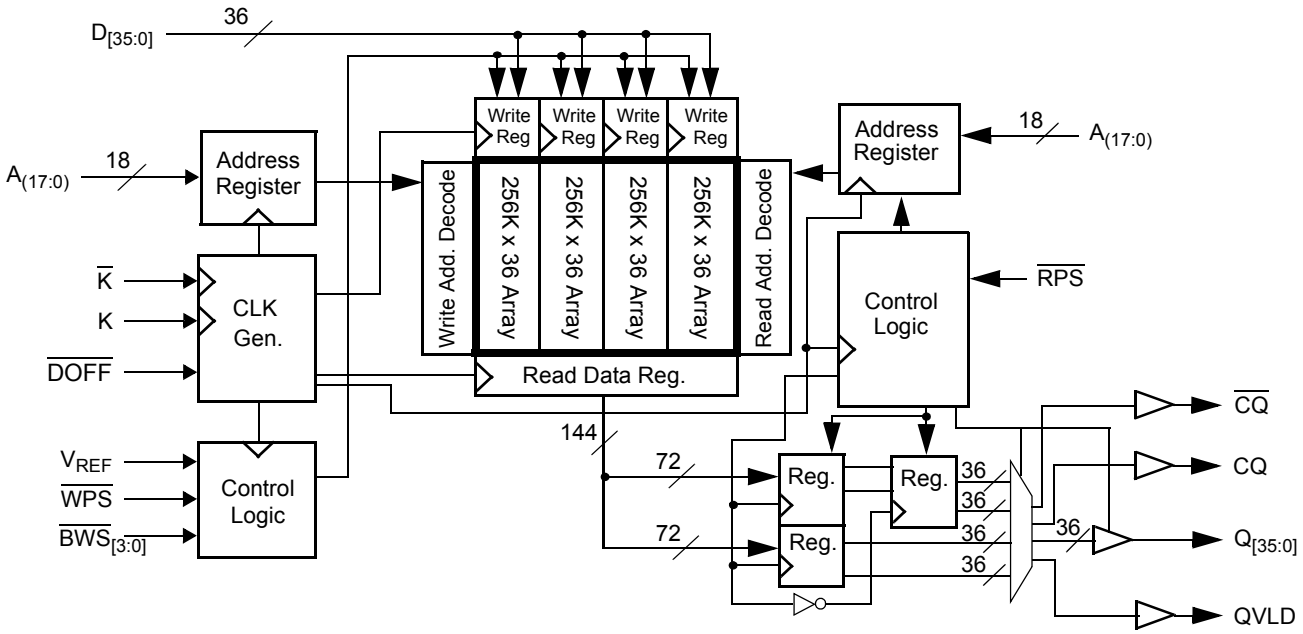


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Logic Block Diagram (CY7C12431KV18)



Logic Block Diagram (CY7C12451KV18)



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Pin Configuration

The pin configuration for CY7C12411KV18, CY7C12561KV18, CY7C12431KV18, and CY7C12451KV18 follow.[2]

165-Ball FBGA (13 x 15 x 1.4 mm) Pinout

CY7C12411KV18 (4M x 8)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/72M	A	$\overline{WPS}$	$\overline{NWS_1}$	$\overline{K}$	NC/144M	$\overline{RPS}$	A	A	CQ
B	NC	NC	NC	A	NC/288M	K	$\overline{NWS_0}$	A	NC	NC	Q3
C	NC	NC	NC	V_{SS}	A	NC	A	V_{SS}	NC	NC	D3
D	NC	D4	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	Q4	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D2	Q2
F	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
G	NC	D5	Q5	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q1	D1
K	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
L	NC	Q6	D6	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q0
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D0
N	NC	D7	NC	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
P	NC	NC	Q7	A	A	QVLD	A	A	NC	NC	NC
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

CY7C12561KV18 (4M x 9)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/72M	A	$\overline{WPS}$	NC	$\overline{K}$	NC/144M	$\overline{RPS}$	A	A	CQ
B	NC	NC	NC	A	NC/288M	K	$\overline{BWS_0}$	A	NC	NC	Q4
C	NC	NC	NC	V_{SS}	A	NC	A	V_{SS}	NC	NC	D4
D	NC	D5	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	Q5	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D3	Q3
F	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
G	NC	D6	Q6	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q2	D2
K	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
L	NC	Q7	D7	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q1
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D1
N	NC	D8	NC	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
P	NC	NC	Q8	A	A	QVLD	A	A	NC	D0	Q0
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

Note
2. NC/72M, NC/144M, and NC/288M are not connected to the die and can be tied to any voltage level.

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Pin Configuration (continued)

The pin configuration for CY7C12411KV18, CY7C12561KV18, CY7C12431KV18, and CY7C12451KV18 follow.[2]

165-Ball FBGA (13 x 15 x 1.4 mm) Pinout

CY7C12431KV18 (2M x 18)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/144M	A	$\overline{WPS}$	$\overline{BWS_1}$	$\overline{K}$	NC/288M	$\overline{RPS}$	A	NC/72M	CQ
B	NC	Q9	D9	A	NC	K	$\overline{BWS_0}$	A	NC	NC	Q8
C	NC	NC	D10	V_{SS}	A	NC	A	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	A	A	A	V_{SS}	NC	NC	D1
P	NC	NC	Q17	A	A	QVLD	A	A	NC	D0	Q0
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

CY7C12451KV18 (1M x 36)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/288M	NC/72M	$\overline{WPS}$	$\overline{BWS_2}$	$\overline{K}$	$\overline{BWS_1}$	$\overline{RPS}$	A	NC/144M	CQ
B	Q27	Q18	D18	A	$\overline{BWS_3}$	K	$\overline{BWS_0}$	A	D17	Q17	Q8
C	D27	Q28	D19	V_{SS}	A	NC	A	V_{SS}	D16	Q7	D8
D	D28	D20	Q19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q16	D15	D7
E	Q29	D29	Q20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	Q15	D6	Q6
F	Q30	Q21	D21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D14	Q14	Q5
G	D30	D22	Q22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q13	D13	D5
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	D31	Q31	D23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D12	Q4	D4
K	Q32	D32	Q23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q12	D3	Q3
L	Q33	Q24	D24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	D11	Q11	Q2
M	D33	Q34	D25	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D10	Q1	D2
N	D34	D26	Q25	V_{SS}	A	A	A	V_{SS}	Q10	D9	D1
P	Q35	D35	Q26	A	A	QVLD	A	A	Q9	D0	Q0
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

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Pin Definitions

Pin Name	I/O	Pin Description
$D_{[x:0]}$	Input-Synchronous	**Data Input Signals**. Sampled on the rising edge of K and $\overline{K}$ clocks when valid write operations are active. CY7C12411KV18 – $D_{[7:0]}$ CY7C12561KV18 – $D_{[8:0]}$ CY7C12431KV18 – $D_{[17:0]}$ CY7C12451KV18 – $D_{[35:0]}$
$\overline{WPS}$	Input-Synchronous	**Write Port Select** – **Active LOW**. Sampled on the rising edge of the K clock. When asserted active, a write operation is initiated. Deasserting deselects the write port. Deselecting the write port ignores $D_{[x:0]}$.
$\overline{NWS_0}$, $\overline{NWS_1}$,	Input-Synchronous	**Nibble Write Select 0, 1** – **Active LOW (CY7C12411KV18 Only)**. Sampled on the rising edge of the K and $\overline{K}$ clocks when write operations are active. Used to select which nibble is written into the device during the current portion of the write operations. $\overline{NWS_0}$ controls $D_{[3:0]}$ and $\overline{NWS_1}$ controls $D_{[7:4]}$. All the Nibble Write Selects are sampled on the same edge as the data. Deselecting a Nibble Write Select ignores the corresponding nibble of data and it is not written into the device.
$\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$	Input-Synchronous	**Byte Write Select 0, 1, 2 and 3** – **Active LOW**. Sampled on the rising edge of the K and $\overline{K}$ clocks when write operations are active. Used to select which byte is written into the device during the current portion of the write operations. Bytes not written remain unaltered. CY7C12561KV18 – $\overline{BWS_0}$ controls $D_{[8:0]}$ CY7C12431KV18 – $\overline{BWS_0}$ controls $D_{[8:0]}$ and $\overline{BWS_1}$ controls $D_{[17:9]}$. CY7C12451KV18 – $\overline{BWS_0}$ controls $D_{[8:0]}$, $\overline{BWS_1}$ controls $D_{[17:9]}$, $\overline{BWS_2}$ controls $D_{[26:18]}$ and $\overline{BWS_3}$ controls $D_{[35:27]}$. All the Byte Write Selects are sampled on the same edge as the data. Deselecting a Byte Write Select ignores the corresponding byte of data and it is not written into the device.
A	Input-Synchronous	**Address Inputs**. Sampled on the rising edge of the K clock during active read and write operations. These address inputs are multiplexed for both read and write operations. Internally, the device is organized as 4M x 8 (4 arrays each of 1M x 8) for CY7C12411KV18, 4M x 9 (4 arrays each of 1M x 9) for CY7C12561KV18, 2M x 18 (4 arrays each of 512K x 18) for CY7C12431KV18 and 1M x 36 (4 arrays each of 256K x 36) for CY7C12451KV18. Therefore, only 20 address inputs are needed to access the entire memory array of CY7C12411KV18 and CY7C12561KV18, 19 address inputs for CY7C12431KV18 and 18 address inputs for CY7C12451KV18. These inputs are ignored when the appropriate port is deselected.
$Q_{[x:0]}$	Outputs-Synchronous	**Data Output Signals**. These pins drive out the requested data when the read operation is active. Valid data is driven out on the rising edge of the K and $\overline{K}$ clocks during read operations. On deselecting the read port, $Q_{[x:0]}$ are automatically tristated. CY7C12411KV18 – $Q_{[7:0]}$ CY7C12561KV18 – $Q_{[8:0]}$ CY7C12431KV18 – $Q_{[17:0]}$ CY7C12451KV18 – $Q_{[35:0]}$
$\overline{RPS}$	Input-Synchronous	**Read Port Select** – **Active LOW**. Sampled on the rising edge of positive input clock (K). When active, a read operation is initiated. Deasserting deselects the read port. When deselected, the pending access is allowed to complete and the output drivers are automatically tristated following the next rising edge of the K clock. Each read access consists of a burst of four sequential transfers.
QVLD	Valid output indicator	**Valid Output Indicator**. The Q Valid indicates valid output data. QVLD is edge aligned with CQ and $\overline{CQ}$.
K	Input Clock	**Positive Input Clock Input**. The rising edge of K is used to capture synchronous inputs to the device and to drive out data through $Q_{[x:0]}$. All accesses are initiated on the rising edge of K.
$\overline{K}$	Input Clock	**Negative Input Clock Input**. $\overline{K}$ is used to capture synchronous inputs being presented to the device and to drive out data through $Q_{[x:0]}$.
CQ	Echo Clock	**Synchronous Echo Clock Outputs**. This is a free running clock and is synchronized to the input clock (K) of the QDR II+. The timings for the echo clocks are shown in the Switching Characteristics on page 24.
$\overline{CQ}$	Echo Clock	**Synchronous Echo Clock Outputs**. This is a free running clock and is synchronized to the input clock ($\overline{K}$) of the QDR II+.The timings for the echo clocks are shown in the Switching Characteristics on page 24.

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Pin Definitions (continued)

Pin Name	I/O	Pin Description
ZQ	Input	**Output Impedance Matching Input**. This input is used to tune the device outputs to the system data bus impedance. CQ, $\overline{CQ}$, and $Q_{[x:0]}$ output impedance are set to 0.2 x RQ, where RQ is a resistor connected between ZQ and ground. Alternatively, this pin can be connected directly to V_{DDQ}, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.
$\overline{DOFF}$	Input	**PLL Turn Off** – **Active LOW**. Connecting this pin to ground turns off the PLL inside the device. The timings in the PLL turned off operation differs from those listed in this data sheet. For normal operation, this pin can be connected to a pull up through a 10 KΩ or less pull up resistor. The device behaves in QDR-I mode when the PLL is turned off. In this mode, the device can be operated at a frequency of up to 167 MHz with QDR-I timing.
TDO	Output	**TDO for JTAG**.
TCK	Input	**TCK Pin for JTAG**.
TDI	Input	**TDI Pin for JTAG**.
TMS	Input	**TMS Pin for JTAG**.
NC	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/144M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
NC/288M	N/A	**Not Connected to the Die**. Can be tied to any voltage level.
V_{REF}	Input-Reference	**Reference Voltage Input**. Static input used to set the reference level for HSTL inputs, outputs, and AC measurement points.
V_{DD}	Power Supply	**Power Supply Inputs to the Core of the Device**.
V_{SS}	Ground	**Ground for the Device**.
V_{DDQ}	Power Supply	**Power Supply Inputs for the Outputs of the Device**.

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Functional Overview

The CY7C12411KV18, CY7C12561KV18, CY7C12431KV18, CY7C12451KV18 are synchronous pipelined Burst SRAMs equipped with a read port and a write port. The read port is dedicated to read operations and the write port is dedicated to write operations. Data flows into the SRAM through the write port and flows out through the read port. These devices multiplex the address inputs to minimize the number of address pins required. By having separate read and write ports, the QDR II+ eliminates the need to “turnaround” the data bus and avoids any possible data contention, thereby simplifying system design. Each access consists of four 8-bit data transfers in the case of CY7C12411KV18, four 9-bit data transfers in the case of CY7C12561KV18, four 18-bit data transfers in the case of CY7C12431KV18, and four 36-bit data transfers in the case of CY7C12451KV18, in two clock cycles.

These devices operate with a read latency of two cycles when $\overline{DOFF}$ pin is tied HIGH. When $\overline{DOFF}$ pin is set LOW or connected to V_{SS} then device behaves in QDR-I mode with a read latency of one clock cycle.

Accesses for both ports are initiated on the positive input clock (K). All synchronous input and output timing are referenced from the rising edge of the input clocks (K and $\overline{K}$).

All synchronous data inputs ($D_{[x:0]}$) pass through input registers controlled by the input clocks (K and $\overline{K}$). All synchronous data outputs ($Q_{[x:0]}$) outputs pass through output registers controlled by the rising edge of the input clocks (K and $\overline{K}$) as well.

All synchronous control ($\overline{RPS}$, $\overline{WPS}$, $\overline{NWS}_{[x:0]}$, $\overline{BWS}_{[x:0]}$) inputs pass through input registers controlled by the rising edge of the input clocks (K and $\overline{K}$).

CY7C12431KV18 is described in the following sections. The same basic descriptions apply to CY7C12411KV18, CY7C12561KV18 and CY7C12451KV18.

Read Operations

The CY7C12431KV18 is organized internally as four arrays of 512K x 18. Accesses are completed in a burst of four sequential 18-bit data words. Read operations are initiated by asserting $\overline{RPS}$ active at the rising edge of the positive input clock (K). The address presented to the address inputs is stored in the read address register. Following the next two K clock rise, the corresponding lowest order 18-bit word of data is driven onto the $Q_{[17:0]}$ using K as the output timing reference. On the subsequent rising edge of $\overline{K}$, the next 18-bit data word is driven onto the $Q_{[17:0]}$. This process continues until all four 18-bit data words have been driven out onto $Q_{[17:0]}$. The requested data is valid 0.45 ns from the rising edge of the input clock (K or $\overline{K}$). To maintain the internal logic, each read access must be allowed to complete. Each read access consists of four 18-bit data words and takes two clock cycles to complete. Therefore, read accesses to the device cannot be initiated on two consecutive K clock rises. The internal logic of the device ignores the second read request. Read accesses can be initiated on every other K clock rise. Doing so pipelines the data flow such that data is transferred out of the device on every rising edge of the input clocks (K and $\overline{K}$).

When the read port is deselected, CY7C12431KV18 first completes the pending read transactions. Synchronous internal circuitry automatically tristates the outputs following the next rising edge of the positive input clock (K). This enables a seamless transition between devices without the insertion of wait states in a depth expanded memory.

Write Operations

Write operations are initiated by asserting $\overline{WPS}$ active at the rising edge of the positive input clock (K). On the following K clock rise the data presented to $D_{[17:0]}$ is latched and stored into the lower 18-bit write data register, provided $\overline{BWS}_{[1:0]}$ are both asserted active. On the subsequent rising edge of the negative input clock ($\overline{K}$) the information presented to $D_{[17:0]}$ is also stored into the write data register, provided $\overline{BWS}_{[1:0]}$ are both asserted active. This process continues for one more cycle until four 18-bit words (a total of 72 bits) of data are stored in the SRAM. The 72 bits of data are then written into the memory array at the specified location. Therefore, write accesses to the device cannot be initiated on two consecutive K clock rises. The internal logic of the device ignores the second write request. Write accesses can be initiated on every other rising edge of the positive input clock (K). Doing so pipelines the data flow such that 18 bits of data can be transferred into the device on every rising edge of the input clocks (K and $\overline{K}$).

When deselected, the write port ignores all inputs after the pending write operations have been completed.

Byte Write Operations

Byte write operations are supported by the CY7C12431KV18. A write operation is initiated as described in the Write Operations section. The bytes that are written are determined by $\overline{BWS}_0$ and $\overline{BWS}_1$, which are sampled with each set of 18-bit data words. Asserting the appropriate Byte Write Select input during the data portion of a write latches the data being presented and writes it into the device. Deasserting the Byte Write Select input during the data portion of a write enables the data stored in the device for that byte to remain unaltered. This feature can be used to simplify read, modify, or write operations to a byte write operation.

Concurrent Transactions

The read and write ports on the CY7C12431KV18 operate independently of one another. As each port latches the address inputs on different clock edges, the user can read or write to any location, regardless of the transaction on the other port. If the ports access the same location when a read follows a write in successive clock cycles, the SRAM delivers the most recent information associated with the specified address location. This includes forwarding data from a write cycle that was initiated on the previous K clock rise.

Read access and write access must be scheduled such that one transaction is initiated on any clock cycle. If both ports are selected on the same K clock rise, the arbitration depends on the previous state of the SRAM. If both ports are deselected, the read port takes priority. If a read was initiated on the previous cycle, the write port takes priority (as read operations cannot be initiated on consecutive cycles). If a write was initiated on the previous cycle, the read port takes priority (as write operations cannot be initiated on consecutive cycles). Therefore, asserting both port selects active from a deselected state results in alternating read or write operations being initiated, with the first access being a read.

[+] Feedback

Depth Expansion

The CY7C12431KV18 has a port select input for each port. This enables easy depth expansion. Both port selects are sampled on the rising edge of the positive input clock only (K). Each port select input can deselect the specified port. Deselecting a port does not affect the other port. All pending transactions (read and write) are completed before the device is deselected.

Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to allow the SRAM to adjust its output driver impedance. The value of RQ must be 5X the value of the intended line impedance driven by the SRAM, the allowable range of RQ to guarantee impedance matching with a tolerance of ±15% is between 175Ω and 350Ω, with V_{DDQ} = 1.5V. The output impedance is adjusted every 1024 cycles upon power up to account for drifts in supply voltage and temperature.

Echo Clocks

Echo clocks are provided on the QDR II+ to simplify data capture on high speed systems. Two echo clocks are generated by the QDR II+. CQ is referenced with respect to K and $\overline{CQ}$ is referenced with respect to $\overline{K}$. These are free running clocks and are synchronized to the input clock of the QDR II+. The timing for the echo clocks is shown in the Switching Characteristics on page 24.

Valid Data Indicator (QVLD)

QVLD is provided on the QDR II+ to simplify data capture on high speed systems. The QVLD is generated by the QDR II+ device along with data output. This signal is also edge-aligned with the echo clock and follows the timing of any data pin. This signal is asserted half a cycle before valid data arrives.

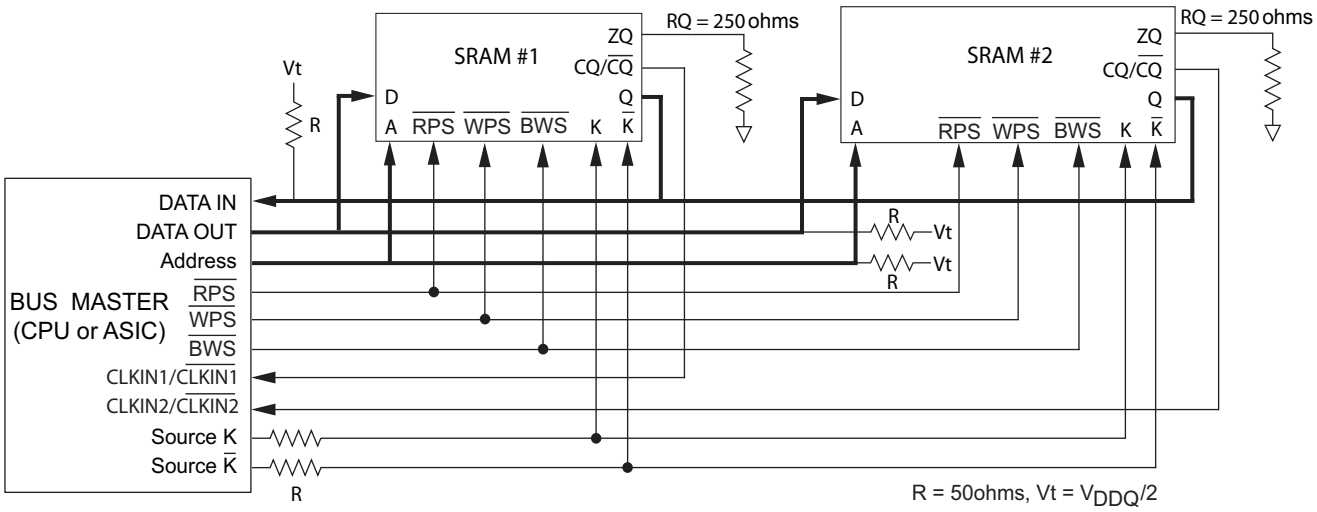
PLL

These chips use a PLL that is designed to function between 120 MHz and the specified maximum clock frequency. During power up, when the DOFF is tied HIGH, the PLL is locked after 20 µs of stable clock. The PLL can also be reset by slowing or stopping the input clocks K and $\overline{K}$ for a minimum of 30 ns. However, it is not necessary to reset the PLL to lock to the desired frequency. The PLL automatically locks 20 µs after a stable clock is presented. The PLL may be disabled by applying ground to the DOFF pin. When the PLL is turned off, the device behaves in QDR-I mode (with one cycle latency and a longer access time). For more information, refer to the application note *PLL Considerations in QDRII/DDRII/QDRII+/DDRII+*.

Application Example

Figure 1 shows two QDR II+ used in an application.

Figure 1. Application Example



[+] Feedback

Truth Table

The truth table for CY7C12411KV18, CY7C12561KV18, CY7C12431KV18, and CY7C12451KV18 follows.[3, 4, 5, 6, 7, 8]

Operation	K	$\overline{RPS}$	$\overline{WPS}$	DQ	DQ	DQ	DQ
Write Cycle: Load address on the rising edge of K; input write data on two consecutive K and $\overline{K}$ rising edges.	L-H	H [9]	L [10]	D(A) at K(t + 1)↑	D(A + 1) at $\overline{K}$(t + 1)↑	D(A + 2) at K(t + 2)↑	D(A + 3) at $\overline{K}$(t + 2)↑
Read Cycle: (2.0 cycle Latency) Load address on the rising edge of K; wait two cycles; read data on two consecutive K and $\overline{K}$ rising edges.	L-H	L [10]	X	Q(A) at K(t + 2)↑	Q(A + 1) at $\overline{K}$(t + 2)↑	Q(A + 2) at K(t + 3)↑	Q(A + 3) at $\overline{K}$(t + 3)↑
NOP: No Operation	L-H	H	H	D = X Q = High Z	D = X Q = High Z	D = X Q = High Z	D = X Q = High Z
Standby: Clock Stopped	Stopped	X	X	Previous State	Previous State	Previous State	Previous State

Write Cycle Descriptions

The write cycle description table for CY7C12411KV18 and CY7C12431KV18 follows.[3, 11]

$\overline{BWS_0}$/ $\overline{NWS_0}$	$\overline{BWS_1}$/ $\overline{NWS_1}$	K	$\overline{K}$	Comments
L	L	L–H	–	During the data portion of a write sequence: CY7C12411KV18 – both nibbles ($D_{[7:0]}$) are written into the device. CY7C12431KV18 – both bytes ($D_{[17:0]}$) are written into the device.
L	L	–	L-H	During the data portion of a write sequence: CY7C12411KV18 – both nibbles ($D_{[7:0]}$) are written into the device. CY7C12431KV18 – both bytes ($D_{[17:0]}$) are written into the device.
L	H	L–H	–	During the data portion of a write sequence: CY7C12411KV18 – only the lower nibble ($D_{[3:0]}$) is written into the device, $D_{[7:4]}$ remains unaltered. CY7C12431KV18 – only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9]}$ remains unaltered.
L	H	–	L–H	During the data portion of a write sequence: CY7C12411KV18 – only the lower nibble ($D_{[3:0]}$) is written into the device, $D_{[7:4]}$ remains unaltered. CY7C12431KV18 – only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9]}$ remains unaltered.
H	L	L–H	–	During the data portion of a write sequence: CY7C12411KV18 – only the upper nibble ($D_{[7:4]}$) is written into the device, $D_{[3:0]}$ remains unaltered. CY7C12431KV18 – only the upper byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ remains unaltered.
H	L	–	L–H	During the data portion of a write sequence: CY7C12411KV18 – only the upper nibble ($D_{[7:4]}$) is written into the device, $D_{[3:0]}$ remains unaltered. CY7C12431KV18 – only the upper byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ remains unaltered.
H	H	L–H	–	No data is written into the devices during this portion of a write operation.
H	H	–	L–H	No data is written into the devices during this portion of a write operation.

Notes

3. X = "Don't Care," H = Logic HIGH, L = Logic LOW, ↑represents rising edge.
4. Device powers up deselected with the outputs in a tri-state condition.
5. "A" represents address location latched by the devices when transaction was initiated. A + 1, A + 2, and A + 3 represents the address sequence in the burst.
6. "t" represents the cycle at which a read/write operation is started. t + 1, t + 2, and t + 3 are the first, second and third clock cycles respectively succeeding the "t" clock cycle.
7. Data inputs are registered at K and $\overline{K}$ rising edges. Data outputs are delivered on K and $\overline{K}$ rising edges as well.
8. It is recommended that K = $\overline{K}$ = HIGH when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.
9. If this signal was LOW to initiate the previous cycle, this signal becomes a "Don't Care" for this operation.
10. This signal was HIGH on previous K clock rise. Initiating consecutive read or write operations on consecutive K clock rises is not permitted. The device ignores the second read or write request.
11. Is based on a write cycle that was initiated in accordance with the Write Cycle Descriptions table. $\overline{NWS_0}$, $\overline{NWS_1}$, $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, and $\overline{BWS_3}$ can be altered on different portions of a write cycle, as long as the setup and hold requirements are achieved.

[+] Feedback

Write Cycle Descriptions

The write cycle description table for CY7C12561KV18 follows. [3, 11]

$\overline{BWS_0}$	K	$\overline{K}$	Comments
L	L–H	–	During the data portion of a write sequence, the single byte ($D_{[8:0]}$) is written into the device.
L	–	L–H	During the data portion of a write sequence, the single byte ($D_{[8:0]}$) is written into the device.
H	L–H	–	No data is written into the device during this portion of a write operation.
H	–	L–H	No data is written into the device during this portion of a write operation.

Write Cycle Descriptions

The write cycle description table for CY7C12451KV18 follows.[3, 11]

$\overline{BWS_0}$	$\overline{BWS_1}$	$\overline{BWS_2}$	$\overline{BWS_3}$	K	$\overline{K}$	Comments
L	L	L	L	L–H	–	During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	L	L	L	–	L–H	During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	H	H	H	L–H	–	During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ remains unaltered.
L	H	H	H	–	L–H	During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ remains unaltered.
H	L	H	H	L–H	–	During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	L	H	H	–	L–H	During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	H	L	H	L–H	–	During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	L	H	–	L–H	During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	H	L	L–H	–	During the data portion of a write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	L	–	L–H	During the data portion of a write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	H	L–H	–	No data is written into the device during this portion of a write operation.
H	H	H	H	–	L–H	No data is written into the device during this portion of a write operation.

[+] Feedback

IEEE 1149.1 Serial Boundary Scan (JTAG)

These SRAMs incorporate a serial boundary scan Test Access Port (TAP) in the FBGA package. This part is fully compliant with IEEE Standard #1149.1-2001. The TAP operates using JEDEC standard 1.8V I/O logic levels.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternatively be connected to V_{DD} through a pull up resistor. TDO must be left unconnected. Upon power up, the device comes up in a reset state, which does not interfere with the operation of the device.

Test Access Port—Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram on page 15. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

Test Data-Out (TDO)

The TDO output pin is used to serially clock data out from the registers. The output is active, depending upon the current state of the TAP state machine (see Instruction Codes on page 18). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This Reset does not affect the operation of the SRAM and can be performed while the SRAM is operating. At power up, the TAP is reset internally to ensure that TDO comes up in a high Z state.

TAP Registers

Registers are connected between the TDI and TDO pins to scan the data in and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins, as shown in TAP Controller Block Diagram on page 16. Upon power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state, as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to enable fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This enables shifting of data through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and output pins on the SRAM. Several No Connect (NC) pins are also included in the scan register to reserve pins for higher density devices.

The boundary scan register is loaded with the contents of the RAM input and output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the input and output ring.

The Boundary Scan Order on page 19 shows the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in Identification Register Definitions on page 18.

TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in Instruction Codes on page 18. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in this section in detail.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction after it is shifted in, the TAP controller must be moved into the Update-IR state.

[+] Feedback

IDCODE

The IDCODE instruction loads a vendor-specific, 32-bit code into the instruction register. It also places the instruction register between the TDI and TDO pins and shifts the IDCODE out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register at power up or whenever the TAP controller is supplied a Test-Logic-Reset state.

SAMPLE Z

The SAMPLE Z instruction connects the boundary scan register between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a High Z state until the next command is supplied during the Update IR state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the input and output pins is captured in the boundary scan register.

The TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and $\overline{CK}$ captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD places an initial data pattern at the latched parallel outputs of the boundary scan register cells before the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required, that is, while the data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST

The EXTEST instruction drives the preloaded data out through the system output pins. This instruction also connects the boundary scan register for serial access between the TDI and TDO in the Shift-DR controller state.

EXTEST OUTPUT BUS TRI-STATE

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tri-state mode.

The boundary scan register has a special bit located at bit #108. When this scan cell, called the “extest output bus tristate,” is latched into the preload register during the Update-DR state in the TAP controller, it directly controls the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a High Z condition.

This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the Shift-DR state. During Update-DR, the value loaded into that shift-register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is preset HIGH to enable the output when the device is powered up, and also when the TAP controller is in the Test-Logic-Reset state.

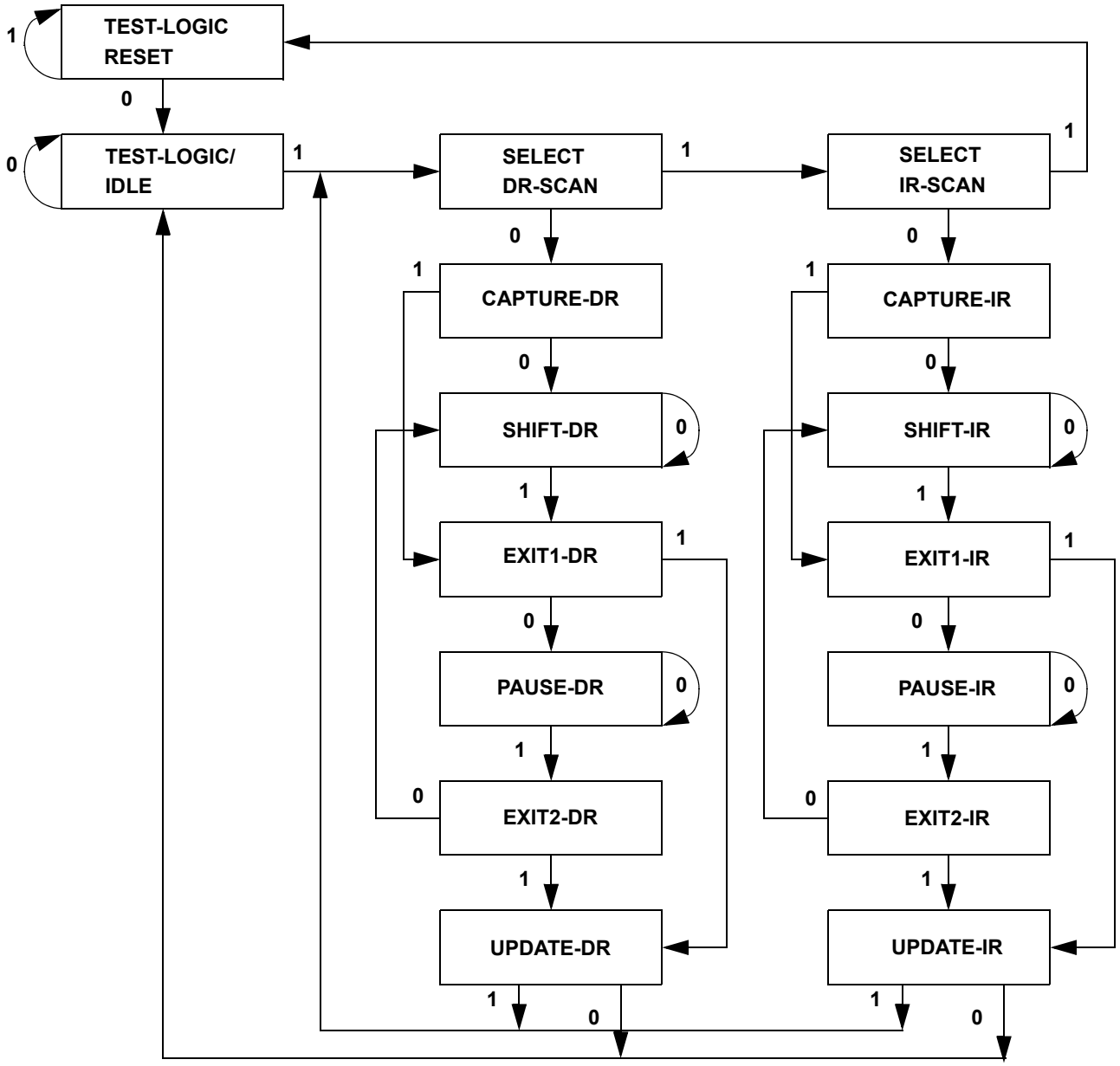
Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

[+] Feedback

TAP Controller State Diagram

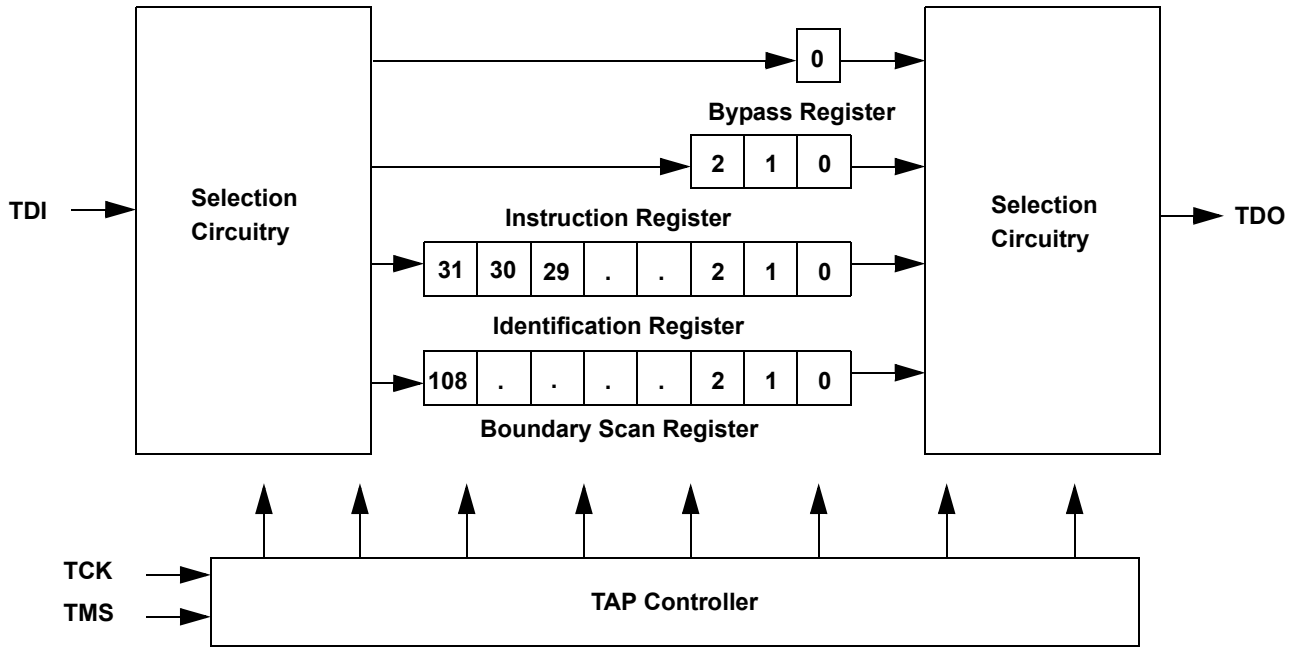
The state diagram for the TAP controller follows.[12]



Note
12. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

[+] Feedback

TAP Controller Block Diagram



TAP Electrical Characteristics

Over the Operating Range[13, 14, 15]

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –2.0 mA	1.4		V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA	1.6		V
V_{OL1}	Output LOW Voltage	I_{OL} = 2.0 mA		0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA		0.2	V
V_{IH}	Input HIGH Voltage		$0.65V_{DD}$	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	$0.35V_{DD}$	V
I_X	Input and Output Load Current	$GND \le V_I \le V_{DD}$	–5	5	µA

Notes
13. These characteristics pertain to the TAP inputs (TMS, TCK, TDI and TDO). Parallel load levels are specified in the Electrical Characteristics Table.
14. Overshoot: $V_{IH}(AC) \le V_{DDQ} + 0.35V$ (Pulse width less than $t_{CYC}/2$), Undershoot: $V_{IL}(AC) \ge -0.3V$ (Pulse width less than $t_{CYC}/2$).
15. All Voltage referenced to Ground.

[+] Feedback

TAP AC Switching Characteristics

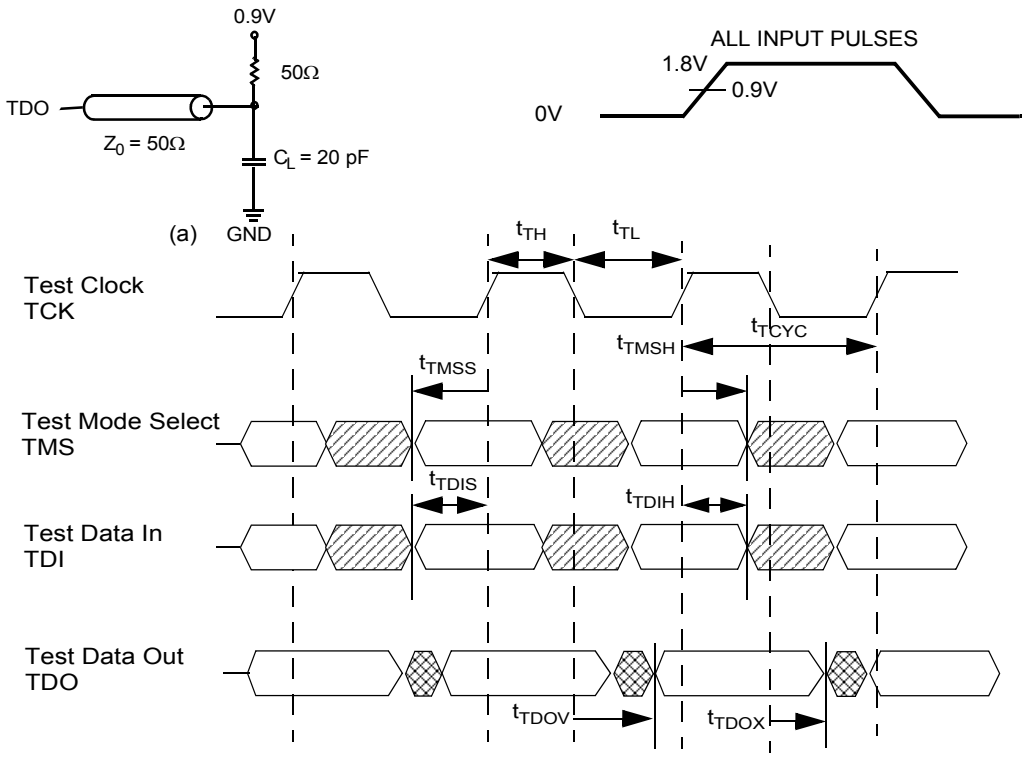
Over the Operating Range[16, 17]

Parameter	Description	Min	Max	Unit
t_{TCYC}	TCK Clock Cycle Time	50		ns
t_{TF}	TCK Clock Frequency		20	MHz
t_{TH}	TCK Clock HIGH	20		ns
t_{TL}	TCK Clock LOW	20		ns
Setup Times				
t_{TMSS}	TMS Setup to TCK Clock Rise	5		ns
t_{TDIS}	TDI Setup to TCK Clock Rise	5		ns
t_{CS}	Capture Setup to TCK Rise	5		ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	5		ns
t_{TDIH}	TDI Hold after Clock Rise	5		ns
t_{CH}	Capture Hold after Clock Rise	5		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		10	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns

TAP Timing and Test Conditions

Figure 2 shows the TAP timing and test conditions.[17]

Figure 2. TAP Timing and Test Conditions



Notes

16. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
17. Test conditions are specified using the load in TAP AC Test Conditions. t_R/t_F = 1 ns.

[+] Feedback

Identification Register Definitions

Instruction Field	Value				Description
	CY7C12411KV18	CY7C12561KV18	CY7C12431KV18	CY7C12451KV18	
Revision Number (31:29)	000	000	000	000	Version number.
Cypress Device ID (28:12)	11010010101000100	11010010101001100	11010010101010100	11010010101100100	Defines the type of SRAM.
Cypress JEDEC ID (11:1)	00000110100	00000110100	00000110100	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence (0)	1	1	1	1	Indicates the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	109

Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures the input and output ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the input and output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the input and output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

Boundary Scan Order

Bit #	Bump ID	Bit #	Bump ID	Bit #	Bump ID	Bit #	Bump ID
0	6R	28	10G	56	6A	84	1J
1	6P	29	9G	57	5B	85	2J
2	6N	30	11F	58	5A	86	3K
3	7P	31	11G	59	4A	87	3J
4	7N	32	9F	60	5C	88	2K
5	7R	33	10F	61	4B	89	1K
6	8R	34	11E	62	3A	90	2L
7	8P	35	10E	63	2A	91	3L
8	9R	36	10D	64	1A	92	1M
9	11P	37	9E	65	2B	93	1L
10	10P	38	10C	66	3B	94	3N
11	10N	39	11D	67	1C	95	3M
12	9P	40	9C	68	1B	96	1N
13	10M	41	9D	69	3D	97	2M
14	11N	42	11B	70	3C	98	3P
15	9M	43	11C	71	1D	99	2N
16	9N	44	9B	72	2C	100	2P
17	11L	45	10B	73	3E	101	1P
18	11M	46	11A	74	2D	102	3R
19	9L	47	10A	75	2E	103	4R
20	10L	48	9A	76	1E	104	4P
21	11K	49	8B	77	2F	105	5P
22	10K	50	7C	78	3F	106	5N
23	9J	51	6C	79	1G	107	5R
24	9K	52	8A	80	1F	108	Internal
25	10J	53	7A	81	3G		
26	11J	54	7B	82	2G		
27	11H	55	6B	83	1H		

Power Up Sequence in QDR II+ SRAM

QDR II+ SRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

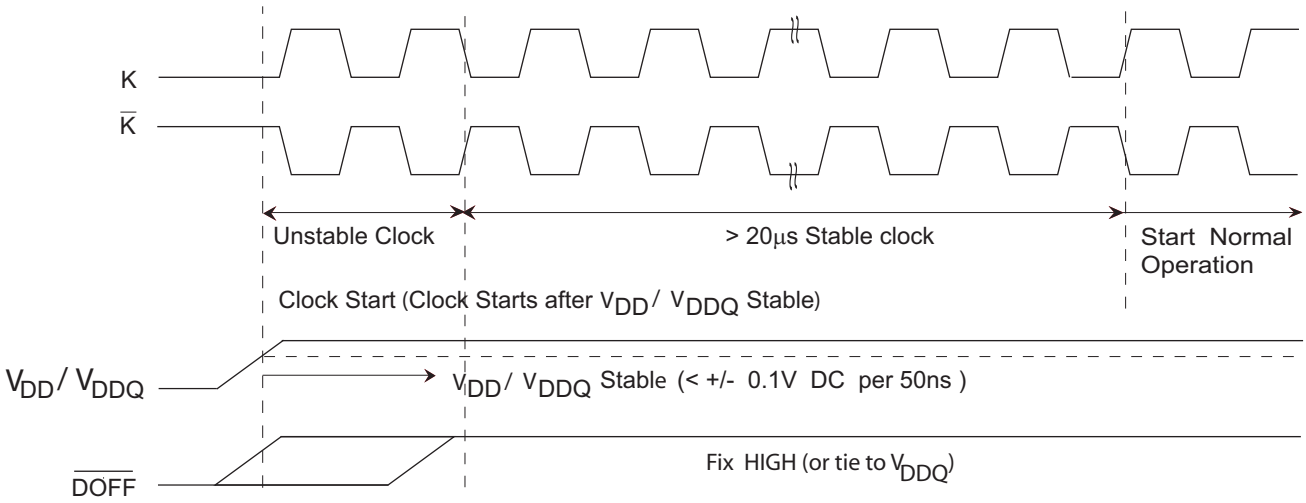
Power Up Sequence

- Apply power and drive $\overline{DOFF}$ either HIGH or LOW (All other inputs can be HIGH or LOW).
  - Apply V_{DD} before V_{DDQ}.
  - Apply V_{DDQ} before V_{REF} or at the same time as V_{REF}.
  - Drive $\overline{DOFF}$ HIGH.
- Provide stable $\overline{DOFF}$ (HIGH), power and clock (K, $\overline{K}$) for 20 µs to lock the PLL.

PLL Constraints

- PLL uses K clock as its synchronizing input. The input must have low phase jitter, which is specified as $t_{KC\ Var}$.
- The PLL functions at frequencies down to 120 MHz.
- If the input clock is unstable and the PLL is enabled, then the PLL may lock onto an incorrect frequency, causing unstable SRAM behavior. To avoid this, provide 20 µs of stable clock to relock to the desired clock frequency.

Figure 3. Power Up Waveforms



[+] Feedback

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied –55 °C to +125 °C

Supply Voltage on V_{DD} Relative to GND .....–0.5V to +2.9V

Supply Voltage on V_{DDQ} Relative to GND.....–0.5V to +V_{DD}

DC Applied to Outputs in High-Z ..... –0.5V to V_{DDQ} + 0.3V

DC Input Voltage[14]..... –0.5V to V_{DD} + 0.3V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage (MIL-STD-883, M. 3015).. > 2001V

Latch up Current..... > 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{DD}[18]	V_{DDQ}[18]
Commercial	0 °C to +70 °C	1.8 ± 0.1V	1.4V to V_{DD}
Industrial	–40 °C to +85 °C		

Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU	Logical Single-Bit Upsets	25 °C	197	216	FIT/ Mb
LMBU	Logical Multi-Bit Upsets	25 °C	0	0.01	FIT/ Mb
SEL	Single Event Latchup	85 °C	0	0.1	FIT/ Dev

** No LMBU or SEL events occurred during testing*; this column represents a statistical χ^2, 95% confidence limit calculation. For more details refer to Application Note AN 54908 "Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates"

Electrical Characteristics

DC Electrical Characteristics

Over the Operating Range[15]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{DD}	Power Supply Voltage		1.7	1.8	1.9	V
V_{DDQ}	I/O Supply Voltage		1.4	1.5	V_{DD}	V
V_{OH}	Output HIGH Voltage	Note 19	$V_{DDQ}/2 – 0.12$		$V_{DDQ}/2 + 0.12$	V
V_{OL}	Output LOW Voltage	Note 20	$V_{DDQ}/2 – 0.12$		$V_{DDQ}/2 + 0.12$	V
$V_{OH(LOW)}$	Output HIGH Voltage	I_{OH} = –0.1 mA, Nominal Impedance	$V_{DDQ} – 0.2$		V_{DDQ}	V
$V_{OL(LOW)}$	Output LOW Voltage	I_{OL} = 0.1 mA, Nominal Impedance	V_{SS}		0.2	V
V_{IH}	Input HIGH Voltage		$V_{REF} + 0.1$		$V_{DDQ} + 0.15$	V
V_{IL}	Input LOW Voltage		–0.15		$V_{REF} – 0.1$	V
I_X	Input Leakage Current	$GND \le V_I \le V_{DDQ}$	–2		2	µA
I_{OZ}	Output Leakage Current	$GND \le V_I \le V_{DDQ}$, Output Disabled	–2		2	µA
V_{REF}	Input Reference Voltage[21]	Typical Value = 0.75V	0.68	0.75	0.95	V

Notes

18. Power up: Assumes a linear ramp from 0V to V_{DD}(min) within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \le V_{DD}$.
19. Output are impedance controlled. $I_{OH} = -(V_{DDQ}/2)/(RQ/5)$ for values of 175 ohms <= RQ <= 350 ohms.
20. Output are impedance controlled. $I_{OL} = (V_{DDQ}/2)/(RQ/5)$ for values of 175 ohms <= RQ <= 350 ohms.
21. V_{REF} (min) = 0.68V or 0.46V_{DDQ}, whichever is larger, V_{REF} (max) = 0.95V or 0.54V_{DDQ}, whichever is smaller.

[+] Feedback

Electrical Characteristics (continued)

DC Electrical Characteristics

Over the Operating Range[15]

Parameter	Description	Test Conditions			Min	Typ	Max	Unit
I_{DD}[22]	V_{DD} Operating Supply	V_{DD} = Max, I_{OUT} = 0 mA, $f = f_{MAX} = 1/t_{CYC}$	450 MHz	(x8)			760	mA
				(x9)			760	
				(x18)			780	
				(x36)			1100	
			400 MHz	(x8)			690	mA
				(x9)			690	
				(x18)			710	
				(x36)			1000	
			375 MHz	(x8)			660	mA
				(x9)			660	
				(x18)			680	
				(x36)			950	
			333 MHz	(x8)			600	mA
				(x9)			600	
				(x18)			620	
				(x36)			850	
I_{SB1}	Automatic Power down Current	Max V_{DD}, Both Ports Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ $f = f_{MAX} = 1/t_{CYC}$, Inputs Static	450 MHz	(x8)			340	mA
				(x9)			340	
				(x18)			340	
				(x36)			340	
			400 MHz	(x8)			320	mA
				(x9)			320	
				(x18)			320	
				(x36)			320	
			375 MHz	(x8)			310	mA
				(x9)			310	
				(x18)			310	
				(x36)			310	
			333 MHz	(x8)			290	mA
				(x9)			290	
				(x18)			290	
				(x36)			290	

AC Electrical Characteristics

Over the Operating Range[14]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage		V_{REF} + 0.2	–	V_{DDQ} + 0.24	V
V_{IL}	Input LOW Voltage		–0.24	–	V_{REF} – 0.2	V

Note
22. The operation current is calculated with 50% read cycle and 50% write cycle.

[+] Feedback

Capacitance

Tested initially and after any design or process change that may affect these parameters.

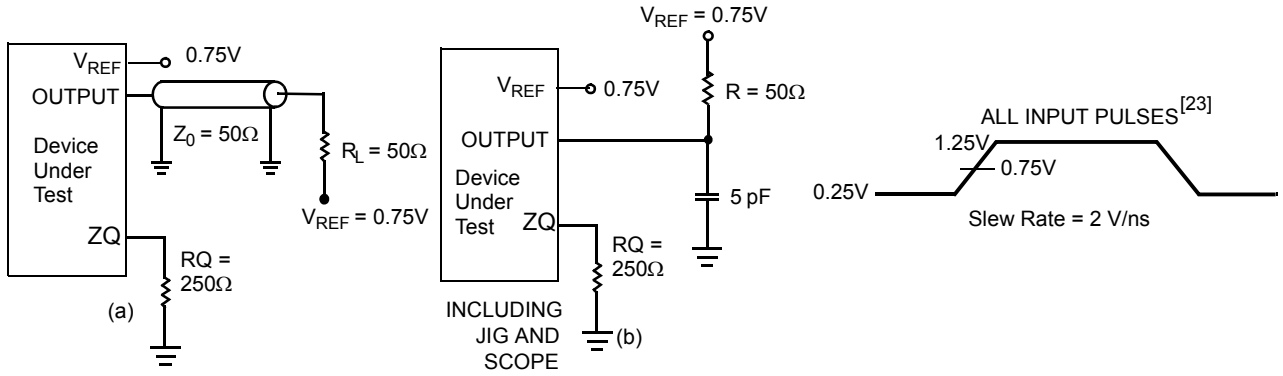
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 1.8V, V_{DDQ} = 1.5V	4	pF
C_O	Output Capacitance		4	pF

Thermal Resistance

Tested initially and after any design or process change that may affect these parameters.

Parameter	Description	Test Conditions	165 FBGA Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	13.7	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		3.73	°C/W

Figure 4. AC Test Loads and Waveforms



Note

23. Unless otherwise noted, test conditions are based on signal transition time of 2V/ns, timing reference levels of 0.75V, Vref = 0.75V, RQ = 250Ω, V_{DDQ} = 1.5V, input pulse levels of 0.25V to 1.25V, and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in (a) of AC Test Loads and Waveforms.

[+] Feedback

Switching Characteristics

Over the Operating Range[23, 24]

Cypress Parameter	Consortium Parameter	Description	450 MHz		400 MHz		375 MHz		333 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{POWER}		V_{DD}(Typical) to the First Access[25]	1		1		1		1		ms
t_{CYC}	t_{KHKH}	K Clock Cycle Time	2.2	8.4	2.5	8.4	2.66	8.4	3.0	8.4	ns
t_{KH}	t_{KHKL}	Input Clock (K/$\overline{K}$) HIGH	0.4	–	0.4	–	0.4	–	0.4	–	ns
t_{KL}	t_{KLKH}	Input Clock (K/$\overline{K}$) LOW	0.4	–	0.4	–	0.4	–	0.4	–	ns
$t_{KH\overline{K}H}$	$t_{KH\overline{K}H}$	K Clock Rise to $\overline{K}$ Clock Rise (rising edge to rising edge)	0.94	–	1.06	–	1.13	–	1.28	–	ns
Setup Times											
t_{SA}	t_{AVKH}	Address Setup to K Clock Rise	0.275	–	0.4	–	0.4	–	0.4	–	ns
t_{SC}	t_{IVKH}	Control Setup to K Clock Rise ($\overline{RPS}$, $\overline{WPS}$)	0.275	–	0.4	–	0.4	–	0.4	–	ns
t_{SCDDR}	t_{IVKH}	DDR Control Setup to Clock (K/$\overline{K}$) Rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$)	0.22	–	0.28	–	0.28	–	0.28	–	ns
t_{SD}	t_{DVKH}	$D_{[X:0]}$ Setup to Clock (K/$\overline{K}$) Rise	0.22	–	0.28	–	0.28	–	0.28	–	ns
Hold Times											
t_{HA}	t_{KHAX}	Address Hold after K Clock Rise	0.275	–	0.4	–	0.4	–	0.4	–	ns
t_{HC}	t_{KHIX}	Control Hold after K Clock Rise ($\overline{RPS}$, $\overline{WPS}$)	0.275	–	0.4	–	0.4	–	0.4	–	ns
t_{HCDDR}	t_{KHIX}	DDR Control Hold after Clock (K/$\overline{K}$) Rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$)	0.22	–	0.28	–	0.28	–	0.28	–	ns
t_{HD}	t_{KHDX}	$D_{[X:0]}$ Hold after Clock (K/$\overline{K}$) Rise	0.22	–	0.28	–	0.28	–	0.28	–	ns
Output Times											
t_{CO}	t_{CHQV}	K/$\overline{K}$ Clock Rise to Data Valid	–	0.45	–	0.45	–	0.45	–	0.45	ns
t_{DOH}	t_{CHQX}	Data Output Hold after Output K/$\overline{K}$ Clock Rise (Active to Active)	–0.45	–	–0.45	–	–0.45	–	–0.45	–	ns
t_{CCQO}	t_{CHCQV}	K/$\overline{K}$ Clock Rise to Echo Clock Valid	–	0.45	–	0.45	–	0.45	–	0.45	ns
t_{CQOH}	t_{CHCQX}	Echo Clock Hold after K/$\overline{K}$ Clock Rise	–0.45	–	–0.45	–	–0.45	–	–0.45	–	ns
t_{CQD}	t_{CQHQV}	Echo Clock High to Data Valid		0.15		0.20		0.20		0.20	ns
t_{CQDOH}	t_{CQHQX}	Echo Clock High to Data Invalid	–0.15	–	–0.20	–	–0.20	–	–0.20	–	ns
t_{CQH}	t_{CQHCQL}	Output Clock (CQ/$\overline{CQ}$) HIGH[26]	0.85	–	1.0	–	1.08	–	1.25	–	ns
$t_{CQH\overline{CQ}H}$	$t_{CQH\overline{CQ}H}$	CQ Clock Rise to $\overline{CQ}$ Clock Rise (rising edge to rising edge)[26]	0.85	–	1.0	–	1.08	–	1.25	–	ns
t_{CHZ}	t_{CHQZ}	Clock (K/$\overline{K}$) Rise to High Z (Active to High Z) [27, 28]	–	0.45	–	0.45	–	0.45	–	0.45	ns
t_{CLZ}	t_{CHQX1}	Clock (K/$\overline{K}$) Rise to Low Z[27, 28]	–0.45	–	–0.45	–	–0.45	–	–0.45	–	ns
t_{QVLD}	$t_{CQHQVLD}$	Echo Clock High to QVLD Valid[29]	–0.15	0.15	–0.20	0.20	–0.20	0.20	–0.20	0.20	ns
PLL Timing											
$t_{KC\ Var}$	$t_{KC\ Var}$	Clock Phase Jitter	–	0.15	–	0.20	–	0.20	–	0.20	ns
$t_{KC\ lock}$	$t_{KC\ lock}$	PLL Lock Time (K)	20	–	20	–	20	–	20	–	µs
$t_{KC\ Reset}$	$t_{KC\ Reset}$	K Static to PLL Reset[30]	30		30		30		30		ns

Notes

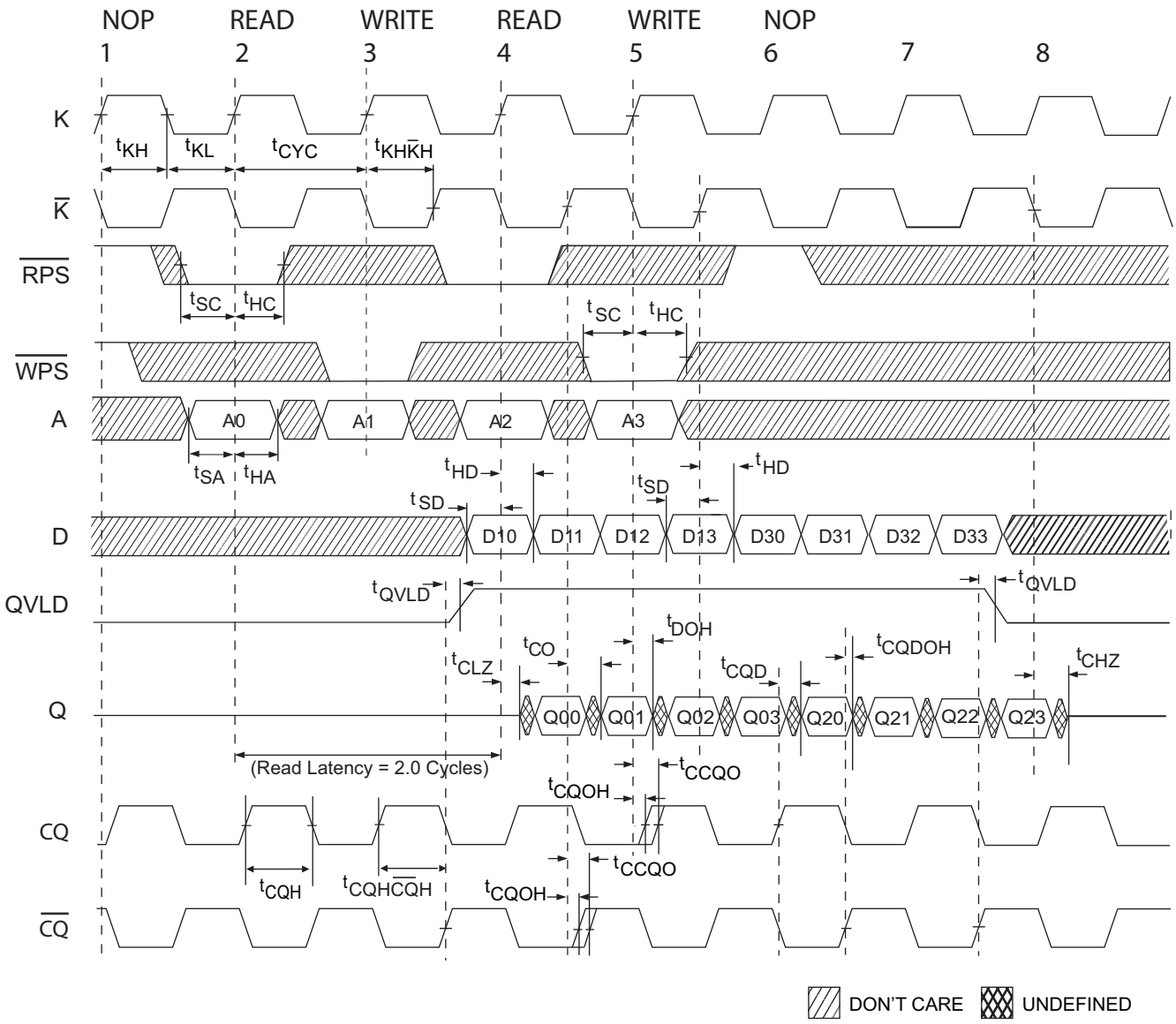
24. When a part with a maximum frequency above 333 MHz is operating at a lower clock frequency, it requires the input timings of the frequency range in which it is being operated and outputs data with the output timings of that frequency range.
25. This part has a voltage regulator internally; t_{POWER} is the time that the power must be supplied above V_{DD} minimum initially before a read or write operation can be initiated.
26. These parameters are extrapolated from the input timing parameters (t_{CYC}/2 - 250 ps, where 250 ps is the internal jitter). These parameters are only guaranteed by design and are not tested in production.
27. t_{CHZ}, t_{CLZ}, are specified with a load capacitance of 5 pF as in (b) of AC Test Loads and Waveforms on page 23. Transition is measured ± 100 mV from steady-state voltage.
28. At any voltage and temperature t_{CHZ} is less than t_{CLZ} and t_{CHZ} less than t_{CO}.
29. t_{QVLD} spec is applicable for both rising and falling edges of QVLD signal.
30. Hold to >V_{IH} or <V_{IL}.

[+] Feedback

Switching Waveforms

Read/Write/Deselect Sequence[31, 32, 33]

Figure 5. Waveform for 2.0 Cycle Read Latency



Notes
31. Q00 refers to output from address A0. Q01 refers to output from the next internal burst address following A0, that is, A0+1.
32. Outputs are disabled (High Z) one clock cycle after a NOP.
33. In this example, if address A2 = A1, then data Q20 = D10, Q21 = D11, Q22 = D12, and Q23 = D13. Write data is forwarded immediately as read results. This note applies to the whole diagram.

[+] Feedback

Ordering Information

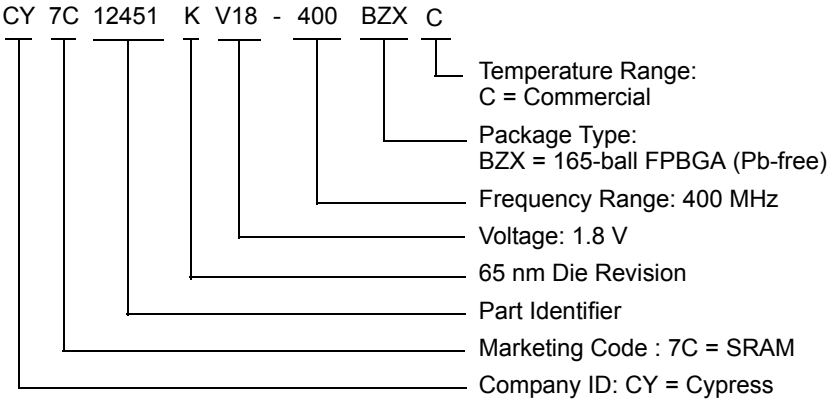
The following table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products

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Table 2. Ordering Information

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
400	CY7C12451KV18-400BZXC	51-85180	165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Pb-free	Commercial

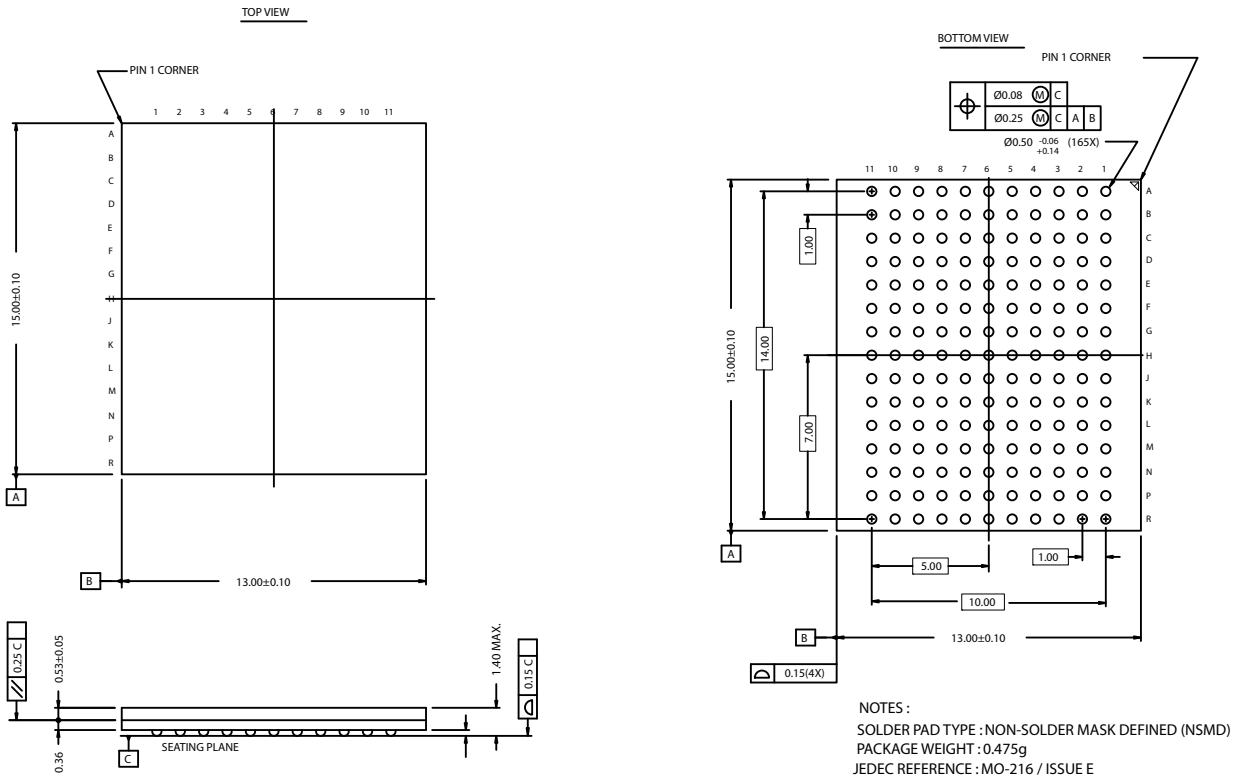
Ordering Code Definitions



[+] Feedback

Package Diagram

Figure 6. 165-ball FBGA (13 x 15 x 1.4 mm), 51-85180



[+] Feedback

Document History Page

Document Title: CY7C12411KV18/CY7C12561KV18/CY7C12431KV18/CY7C12451KV18, 36-Mbit QDR® II+ SRAM 4-Word Burst Architecture (2.0 Cycle Read Latency) Document Number: 001-53192				
REV.	**ECN NO.**	**Orig. Of Change**	**Submission Date**	**Description Of Change**
**	2702761	VKN/PYRS	05/06/2009	New data sheet
*A	2747635	VKN/AESA	08/03/2009	Converted from preliminary to final For 450 MHz speed, changed t_{CO}, t_{CCQO}, t_{CHZ} from 370ps to 450ps and t_{DOH}, t_{CQOH}, t_{CLZ} from -370ps to -450ps Included Soft Error Immunity Data Modified Ordering Information table by including parts that are available and modified the disclaimer for the Ordering information
*B	2761928	AJU	09/10/2009	Post to external web.
*C	2767155	VKN	09/23/2009	Changed Input Capacitance (C_{IN}) from 2 pF to 4 pF Changed Output Capacitance (C_O) from 3 pF to 4 pF Modified Ordering code disclaimer
*D	2855911	VKN	01/18/2010	Included “CY7C12451KV18-400BZXC” part in the Ordering information table Updated package outline diagram
*E	3158296	AJU	01/31/2011	Updated Ordering Information and added Ordering Code Definitions.

[+] Feedback

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