1-Mbit (64K x 16) Static RAM

Features

- **Temperature Ranges**
  - **— Commercial: 0°C to 70°C**
  - **— Industrial: –40°C to 85°C**
  - **— Automotive-A: –40°C to 85°C**
  - **— Automotive-E: –40°C to 125°C**
- **Pin- and function-compatible with CY7C1021BV33**
- **High speed**
  - **— t_{AA} = 8 ns (Commercial & Industrial)**
  - **— t_{AA} = 12 ns (Automotive)**
- **CMOS for optimum speed/power**
- **Low active power: 345 mW (max.)**
- **Automatic power-down when deselected**
- **Independent control of upper and lower bits**
- **Available in Pb-free and non Pb-free 44-pin 400-Mil SOJ 44-pin TSOP II and 48-ball FBGA packages**

Functional Description[1]

The CY7C1021CV33 is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

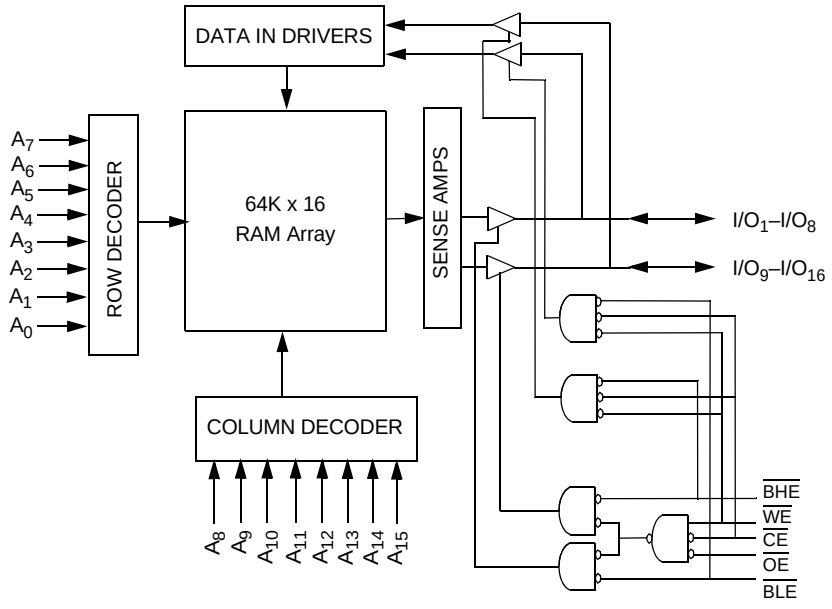
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_1 through I/O_8), is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_9 through I/O_{16}) is written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_1 to I/O_8. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_9 to I/O_{16}. See the truth table at the end of this data sheet for a complete description of Read and Write modes.

The input/output pins (I/O_1 through I/O_{16}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a Write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1021CV33 is available in 44-pin 400-Mil wide SOJ, 44-pin TSOP II and 48-ball FBGA packages.

Logic Block Diagram



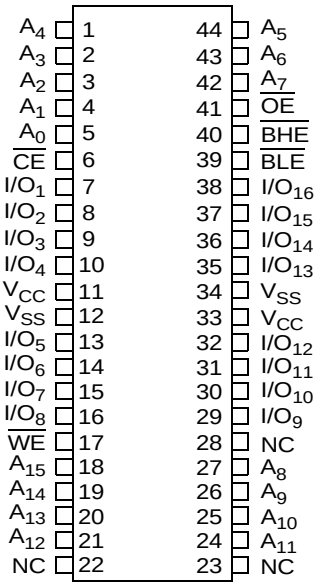
Note:
1. For best-practice recommendations, please refer to the Cypress application note “System Design Guidelines” on http://www.cypress.com.

Selection Guide

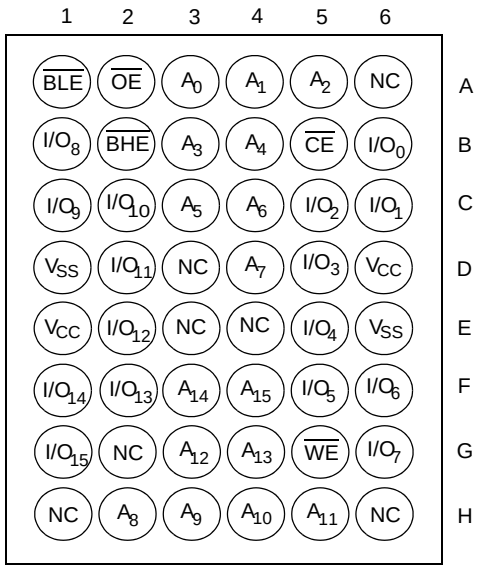
		-8	-10	-12	-15	Unit
Maximum Access Time		8	10	12	15	ns
Maximum Operating Current	Comm'l/Ind'l	95	90	85	80	mA
	Automotive-A				80	mA
	Automotive-E			90		mA
Maximum CMOS Standby Current	Comm'l/Ind'l	5	5	5	5	mA
	Automotive-A				5	mA
	Automotive-E			10		mA

Pin Configurations[2]

SOJ/TSOP II
Top View



48-ball FBGA
Top View



Note:
2. NC pins are not connected on the die.

Pin Definitions

Pin Name	SOJ, TSOP Pin Number	BGA Pin Number	I/O Type	Description
A_0–A_{15}	1–5, 18–21, 24–27, 42–44	A3, A4, A5, B3, B4, C3, C4, D4, H2, H3, H4, H5, G3, G4, F3, F4	Input	**Address Inputs used to select one of the address locations.**
I/O_0–I/O_{15}[3]	7–10, 13–16, 29–32, 35–38	B6, C6, C5, D5, E5, F5, F6, G6, B1, C1, C2, D2, E2, F2, F1, G1	Input/Output	**Bidirectional Data I/O lines**. Used as input or output lines depending on operation.
NC	22, 23, 28	A6, D3, E3, E4, G2, H1, H6	No Connect	**No Connects**. Not connected to the die.
$\overline{WE}$	17	G5	Input/Control	**Write Enable Input, active LOW**. When selected LOW, a Write is conducted. When deselected HIGH, a Read is conducted.
$\overline{CE}$	6	B5	Input/Control	**Chip Enable Input, active LOW**. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{BHE}$, $\overline{BLE}$	40, 39	B2, A1	Input/Control	**Byte Write Select Inputs, active LOW**. $\overline{BHE}$ controls I/O_{16}–I/O_9, $\overline{BLE}$ controls I/O_8–I/O_1.
$\overline{OE}$	41	A2	Input/Control	**Output Enable, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins.
V_{SS}	12,34	D1, E6	Ground	**Ground for the device**. Should be connected to ground of the system.
V_{CC}	11,33	D6, E1	Power Supply	**Power Supply inputs to the device.**

Note:
3. I/O_1–I/O_{16} for SOJ/TSOP and I/O_0–I/O_{15} for BGA packages.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[4] .... –0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State[4].....–0.5V to V_{CC}+0.5V

DC Input Voltage[4].....–0.5V to V_{CC}+0.5V

Current into Outputs (LOW).....20 mA

Static Discharge Voltage.....>2001V (per MIL-STD-883, Method 3015)

Latch-up Current.....>200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Commercial	0°C to +70°C	3.3V ± 10%
Industrial	–40°C to +85°C	
Automotive-A	–40°C to +85°C	
Automotive -E	–40°C to +125°C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		-8		-10		-12		-15		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[4]			–0.3	0.8	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	Com'l/Ind'l	–1	+1	–1	+1	–1	+1	–1	+1	µA
			Auto-A							–1	+1	
			Auto-E					–12	+12			
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	Com'l/Ind'l	–1	+1	–1	+1	–1	+1	–1	+1	µA
			Auto-A							–1	+1	
			Auto-E					–12	+12			
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l/Ind'l		95		90		85		80	mA
			Auto-A								80	mA
			Auto-E						90			
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, CE ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l/Ind'l		15		15		15		15	mA
			Auto-A								15	
			Auto-E						20			
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, CE ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0	Com'l/Ind'l		5		5		5		5	mA
			Auto-A								5	
			Auto-E						10			

Note:
4. V_{IL} (min.) = –2.0V and V_{IH}(max) = V_{CC} + 0.5V for pulse durations of less than 20 ns.

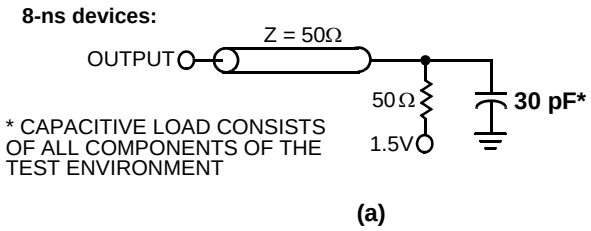
Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	8	pF
C_{OUT}	Output Capacitance		8	pF

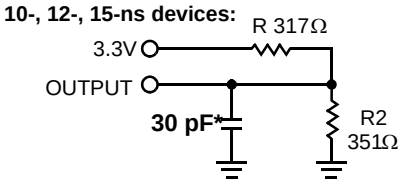
Thermal Resistance[5]

Parameter	Description	Test Conditions	SOJ	TSOP II	FBGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	65.06	76.92	95.32	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		34.21	15.86	10.68	°C/W

AC Test Loads and Waveforms[6]



(a)



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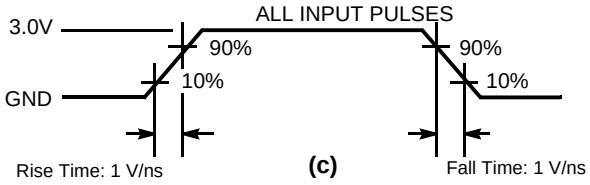

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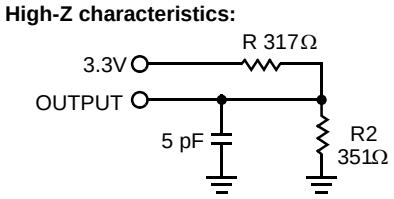


(d)

Notes:
5. Tested initially and after any design or process changes that may affect these parameters.
6. AC characteristics (except High-Z) for all 8-ns parts are tested using the load conditions shown in Figure (a). All other speeds are tested using the Thevenin load shown in Figure (b). High-Z characteristics are tested for all speeds using the test load shown in Figure (d).

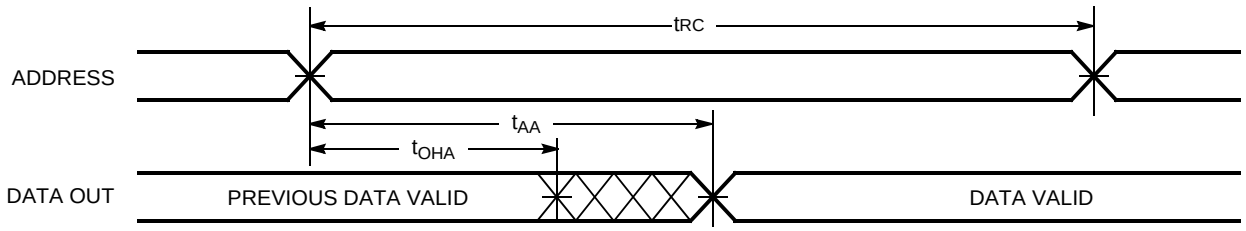
Switching Characteristics Over the Operating Range[7]

Parameter	Description	-8		-10		-12		-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{power}[8]	V_{CC}(typical) to the first access	100		100		100		100		µs
t_{RC}	Read Cycle Time	8		10		12		15		ns
t_{AA}	Address to Data Valid		8		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		8		10		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		5		6		7	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[9]	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[9, 10]		4		5		6		7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[9]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[9, 10]		4		5		6		7	ns
t_{PU}[11]	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}[11]	$\overline{CE}$ HIGH to Power-Down		8		10		12		15	ns
t_{DBE}	Byte Enable to Data Valid		5		5		6		7	ns
t_{LZBE}	Byte Enable to Low-Z	0		0		0		0		ns
t_{HZBE}	Byte Disable to High-Z		4		5		6		7	ns
Write Cycle[12]										
t_{WC}	Write Cycle Time	8		10		12		15		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	7		8		9		10		ns
t_{AW}	Address Set-up to Write End	7		8		9		10		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	6		7		8		10		ns
t_{SD}	Data Set-up to Write End	5		5		6		8		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[9]	3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[9, 10]		4		5		6		7	ns
t_{BW}	Byte Enable to End of Write	6		7		8		9		ns

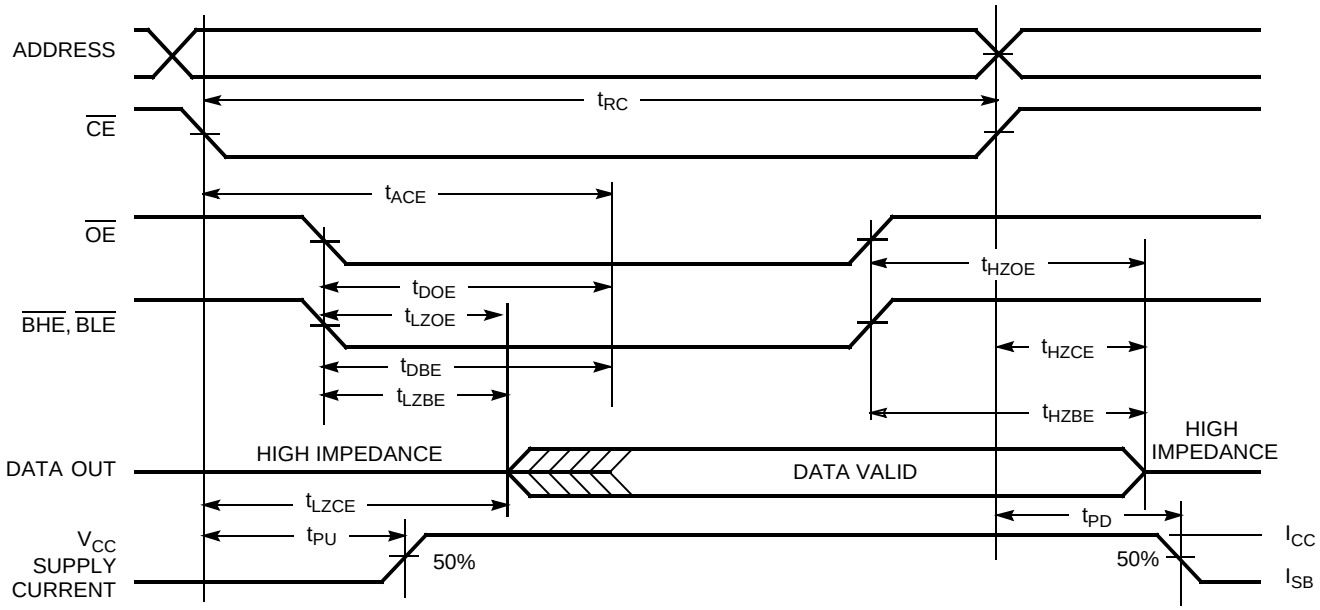
Notes:
7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
8. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access is performed.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
10. t_{HZOE}, t_{HZBE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
11. This parameter is guaranteed by design and is not tested.
12. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW and $\overline{BHE}$/$\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$ and $\overline{BHE}$/$\overline{BLE}$ must be LOW to initiate a Write, and the transition of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.

Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled)[13, 14]



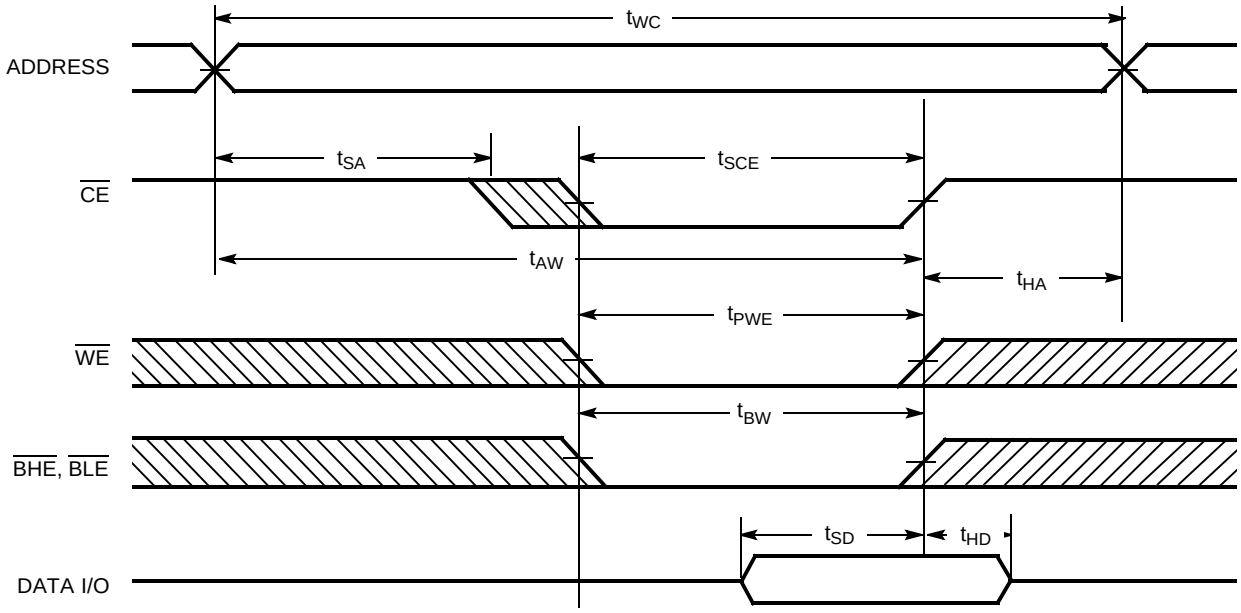
Read Cycle No. 2 ($\overline{OE}$ Controlled)[14, 15]



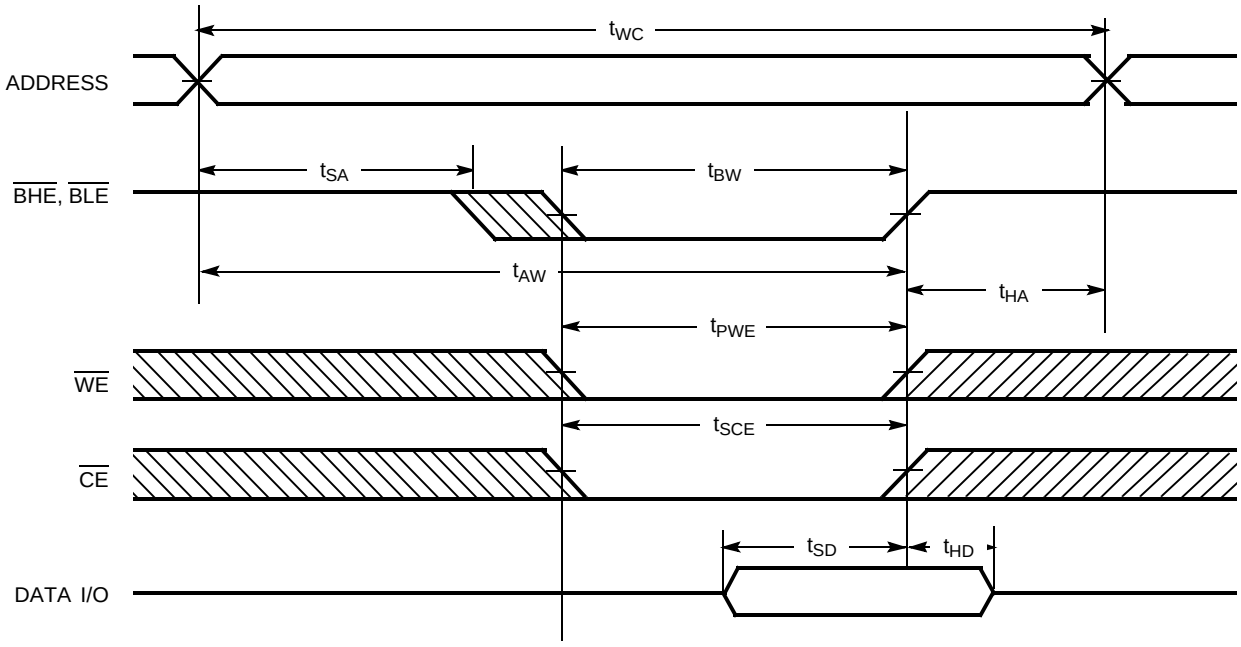
Notes:
13. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}.
14. $\overline{WE}$ is HIGH for Read cycle.
15. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)[16, 17]



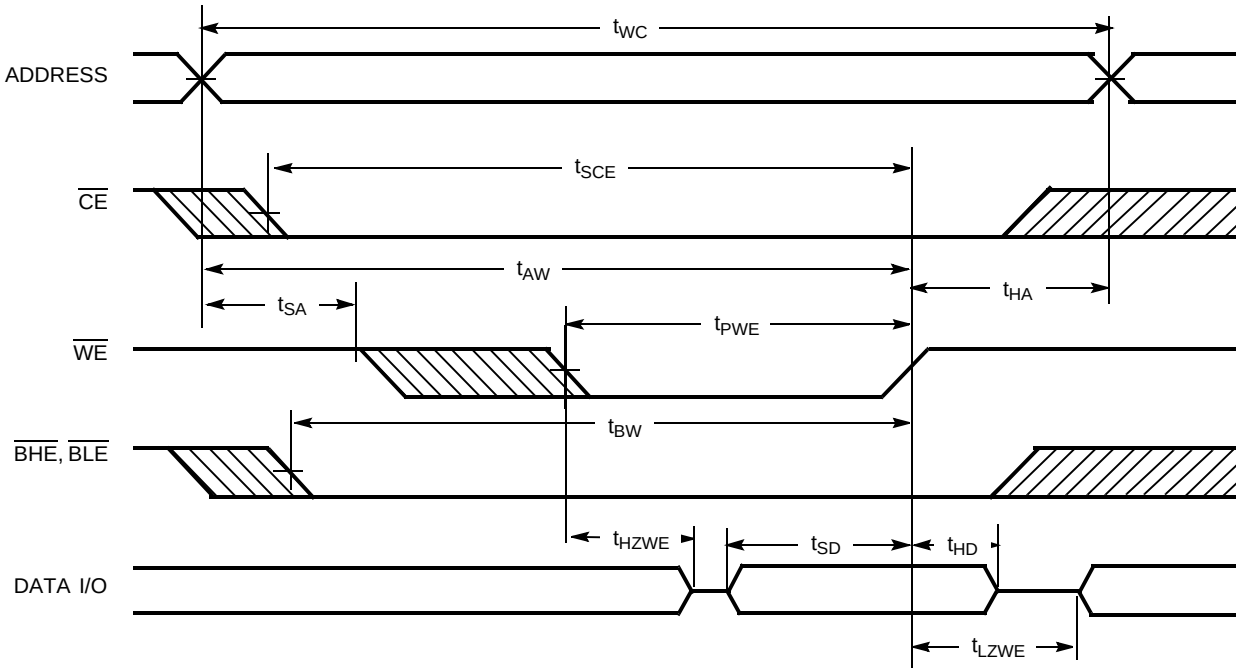
Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)



Notes:
16. Data I/O is high impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$= V_{IH}.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{WE}$ Controlled, LOW)



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_1–I/O_8[3]	I/O_9–I/O_{16}[3]	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power-down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read – All bits	Active (I_{CC})
			L	H	Data Out	High-Z	Read – Lower bits only	Active (I_{CC})
			H	L	High-Z	Data Out	Read – Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write – All bits	Active (I_{CC})
			L	H	Data In	High-Z	Write – Lower bits only	Active (I_{CC})
			H	L	High-Z	Data In	Write – Upper bits only	Active (I_{CC})
L	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})

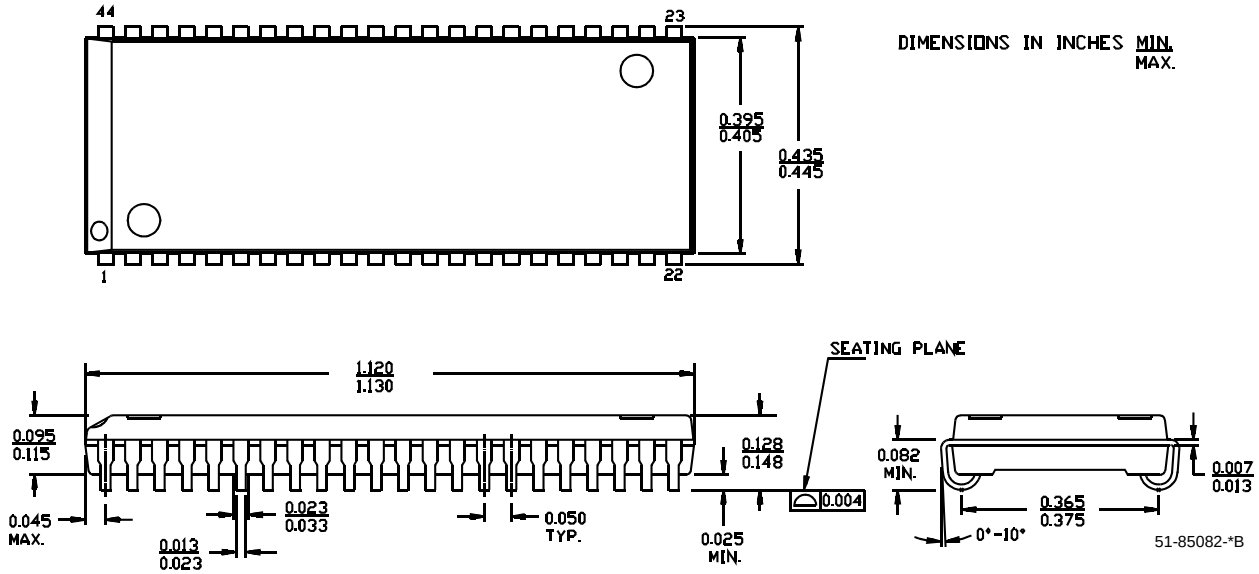
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
8	CY7C1021CV33-8VXC	51-85082	44-pin (400-Mil) Molded SOJ (Pb-free)	Commercial
	CY7C1021CV33-8ZXC		44-pin TSOP Type II (Pb-free)	
	CY7C1021CV33-8BAXC	51-85096	48-ball FBGA (Pb-free)	
10	CY7C1021CV33-10VC	51-85082	44-pin (400-Mil) Molded SOJ	Commercial
	CY7C1021CV33-10VXC		44-pin (400-Mil) Molded SOJ (Pb-free)	
	CY7C1021CV33-10ZXC	51-85087	44-pin TSOP Type II (Pb-free)	
	CY7C1021CV33-10ZI		44-pin TSOP Type II	Industrial
	CY7C1021CV33-10ZXI		44-pin TSOP Type II (Pb-free)	
	CY7C1021CV33-10BAXI	51-85096	48-ball FBGA (Pb-free)	
12	CY7C1021CV33-12VC	51-85082	44-pin (400-Mil) Molded SOJ	Commercial
	CY7C1021CV33-12VXC		44-pin (400-Mil) Molded SOJ (Pb-free)	
	CY7C1021CV33-12VI		44-pin (400-Mil) Molded SOJ	Industrial
	CY7C1021CV33-12VXI		44-pin (400-Mil) Molded SOJ (Pb-free)	
	CY7C1021CV33-12ZXC	51-85087	44-pin TSOP Type II (Pb-free)	Commercial
	CY7C1021CV33-12ZXI		44-pin TSOP Type II (Pb-free)	Industrial
	CY7C1021CV33-12BAI	51-85096	48-ball FBGA	Industrial
	CY7C1021CV33-12BAXI		48-ball FBGA (Pb-free)	
	CY7C1021CV33-12ZSE	51-85087	44-pin TSOP Type II	Automotive-E
	CY7C1021CV33-12ZSXE		44-pin TSOP Type II (Pb-free)	
	CY7C1021CV33-12VE	51-85082	44-pin (400-Mil) Molded SOJ	
	CY7C1021CV33-12VXE		44-pin (400-Mil) Molded SOJ (Pb-free)	
	CY7C1021CV33-12BAE	51-85096	48-ball FBGA	
15	CY7C1021CV33-15VXC	51-85082	44-pin (400-Mil) Molded SOJ (Pb-free)	Commercial
	CY7C1021CV33-15ZXC	51-85087	44-pin TSOP Type II (Pb-free)	Commercial
	CY7C1021CV33-15ZI		44-pin TSOP Type II	Industrial
	CY7C1021CV33-15ZXI		44-pin TSOP Type II (Pb-free)	
	CY7C1021CV33-15BAXI	51-85096	48-ball FBGA (Pb-free)	
	CY7C1021CV33-15ZSXA	51-85087	44-pin TSOP Type II (Pb-free)	Automotive-A

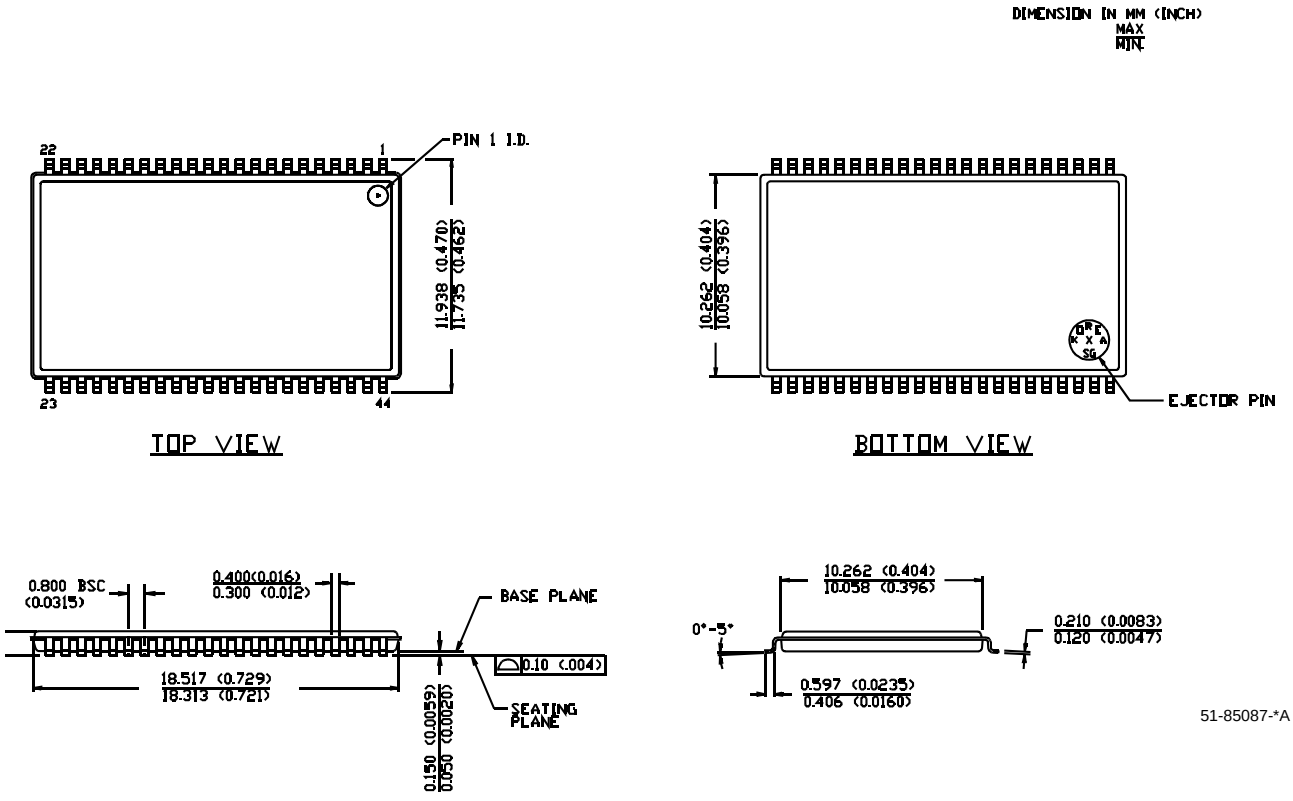
Please contact local sales representative regarding availability of these parts

Package Diagrams

44-pin (400-Mil) Molded SOJ (51-85082)

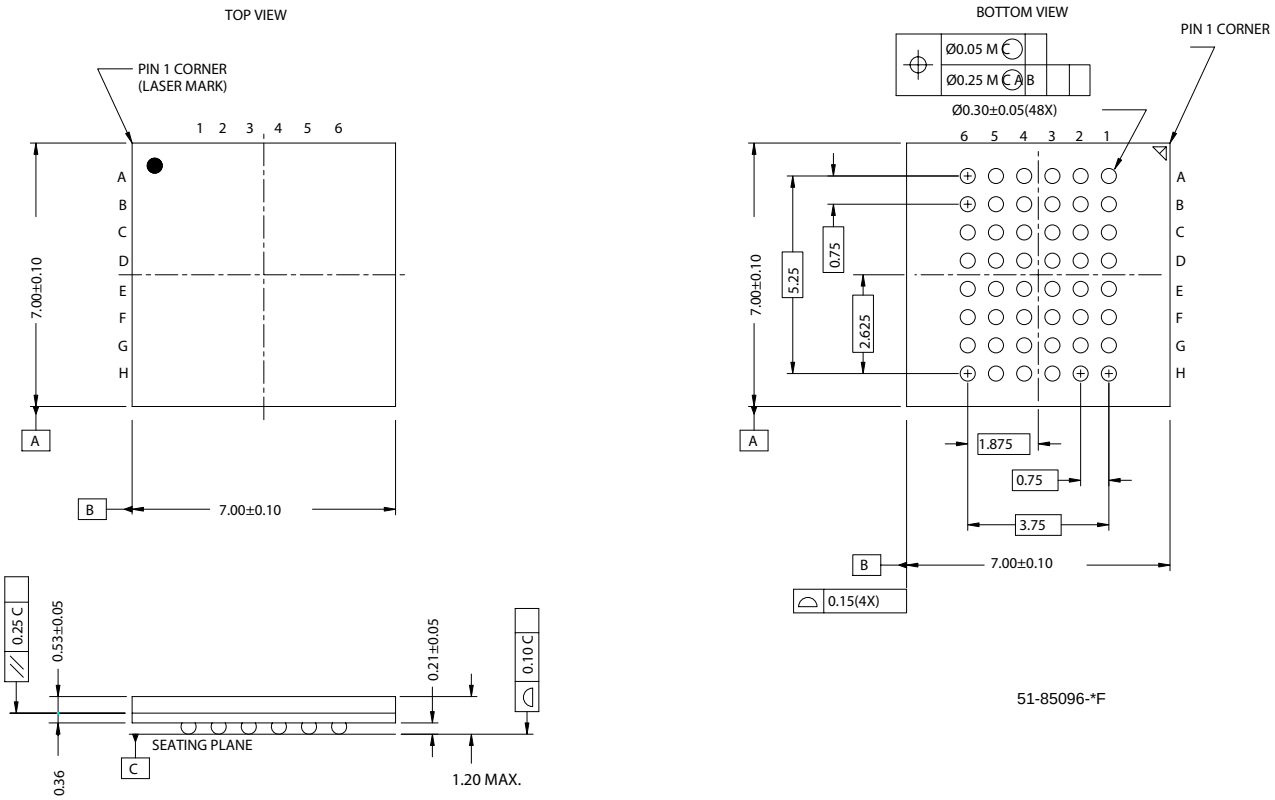


44-pin Thin Small Outline Package Type II (51-85087)



Package Diagrams (continued)

48-ball FBGA (7 x 7 x 1.2 mm) (51-85096)



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Document History Page

Document Title: CY7C1021CV33, 1-Mbit (64K x 16) Static RAM Document Number: 38-05132				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	109472	12/06/01	HGK	New Data Sheet
*A	115044	05/08/02	HGK	Ram7 version C4K x 16 Async Remove “Preliminary”
*B	115808	06/25/02	HGK	I_{SB1} and I_{CC} values changed
*C	120413	10/31/02	DFP	Updated BGA pin E4 to NC
*D	238454	See ECN	RKF	1) Added Automotive Specs to Data sheet 2) Added Pb-free devices in the Ordering Information
*E	334398	See ECN	SYT	Added Pb-free on page# 9 and 10
*F	493565	See ECN	NXR	Added Automotive-A operating range Corrected typo in the Pin Definition table Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I_{OS} parameter from DC Electrical Characteristics table Updated the ordering information table
*G	563963	See ECN	VKN	Added t_{POWER} spec in the AC Switching Characteristics table Added footnote #8