



CY7C1020V

32K x 16 Static RAM

Features

- **3.3V operation (3.0V - 3.6V)**
- **High speed**
 - $t_{AA} = 10 \text{ ns}$
- **Low active power**
 - 540 mW (max., 12 ns)
- **Very Low standby power**
 - 330 μW (max., "L" version)
- **Automatic power-down when deselected**
- **Independent Control of Upper and Lower bytes**
- **Available in 44-pin TSOP II and 400-mil SOJ**

Functional Description

The CY7C1020V is a high-performance CMOS static RAM organized as 32,768 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking chip enable ($\overline{\text{CE}}$) and write enable ($\overline{\text{WE}}$) inputs LOW. If byte low enable

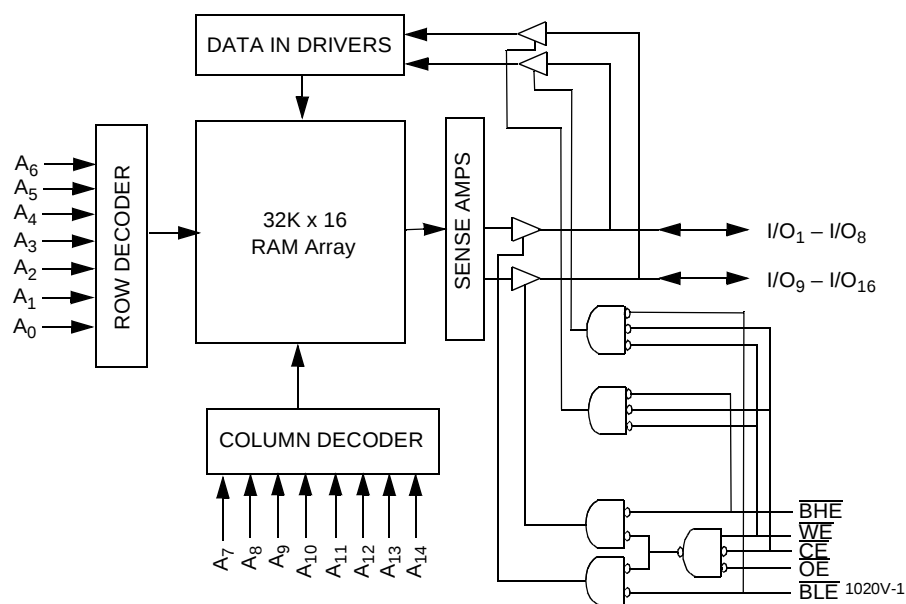
($\overline{\text{BLE}}$) is LOW, then data from I/O pins (I/O_1 through I/O_8), is written into the location specified on the address pins (A_0 through A_{14}). If byte high enable ($\overline{\text{BHE}}$) is LOW, then data from I/O pins (I/O_9 through I/O_{16}) is written into the location specified on the address pins (A_0 through A_{14}).

Reading from the device is accomplished by taking chip enable ($\overline{\text{CE}}$) and output enable ($\overline{\text{OE}}$) LOW while forcing the write enable ($\overline{\text{WE}}$) HIGH. If byte low enable ($\overline{\text{BLE}}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_1 to I/O_8 . If byte high enable ($\overline{\text{BHE}}$) is LOW, then data from memory will appear on I/O_9 to I/O_{16} . See the truth table at the back of this datasheet for a complete description of read and write modes.

The input/output pins (I/O_1 through I/O_{16}) are placed in a high-impedance state when the device is deselected ($\overline{\text{CE}}$ HIGH), the outputs are disabled ($\overline{\text{OE}}$ HIGH), the $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$ are disabled ($\overline{\text{BHE}}$, $\overline{\text{BLE}}$ HIGH), or during a write operation ($\overline{\text{CE}}$ LOW, and $\overline{\text{WE}}$ LOW).

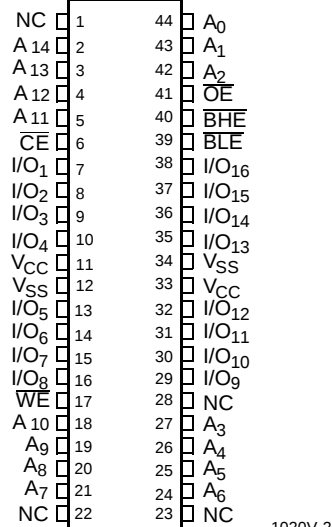
The CY7C1020V is available in standard 44-pin TSOP type II and 400-mil-wide SOJ packages.

Logic Block Diagram



Pin Configuration

SOJ / TSOP II
Top View



1020V-2

Selection Guide

		7C1020V-10	7C1020V-12	7C1020V-15	7C1020V-20
Maximum Access Time (ns)		10	12	15	20
Maximum Operating Current (mA)		130	120	110	100
	L	100	90	80	70
Maximum CMOS Standby Current (mA)		1	1	1	1
	L	0.1	0.1	0.1	0.1

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied -55°C to +125°C

Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to +4.6V

DC Voltage Applied to Outputs

in High Z State^[1] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[1] -0.5V to $V_{CC} + 0.5V$

Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature ^[2]	V_{CC}
Commercial	0°C to +70°C	3.0V - 3.6V
Industrial	-40°C to +85°C	3.0V - 3.6V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C1020V-10		7C1020V-12		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.3V$	2.0	$V_{CC} + 0.3V$	V
V_{IL}	Input LOW Voltage ^[1]		-0.5	0.8	-0.5	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{CC}$, Output Disabled	-2	+2	-2	+2	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$		130		120	mA
			L	100		90	mA
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$		15		15	mA
			L	7		7	mA
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V$, $f=0$		1		1	mA
			L	100		100	μA

Notes:

- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range (continued)

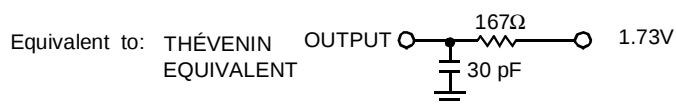
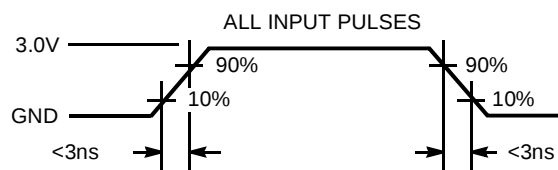
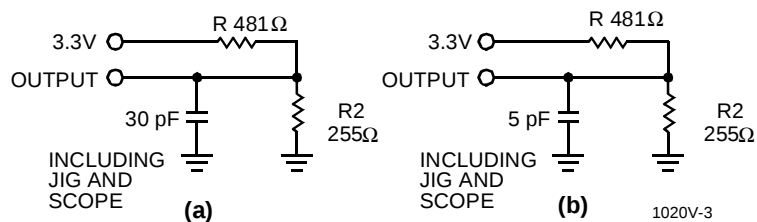
Parameter	Description	Test Conditions	7C1020V-15		7C1020V-20		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.3V$	2.0	$V_{CC} + 0.3V$	V
V_{IL}	Input LOW Voltage ^[1]		-0.5	0.8	-0.5	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{CC}$, Output Disabled	-2	+2	-2	+2	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$		110		100	mA
			L	80		70	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC} , $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$		15		15	mA
			L	7		7	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V$, $f=0$		1		1	mA
			L	100		100	μA

Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz}, V_{CC} = 3.3V$	8	pF
C_{OUT}	Output Capacitance		8	pF

Notes:

3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms


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Switching Characteristics^[4] Over the Operating Range

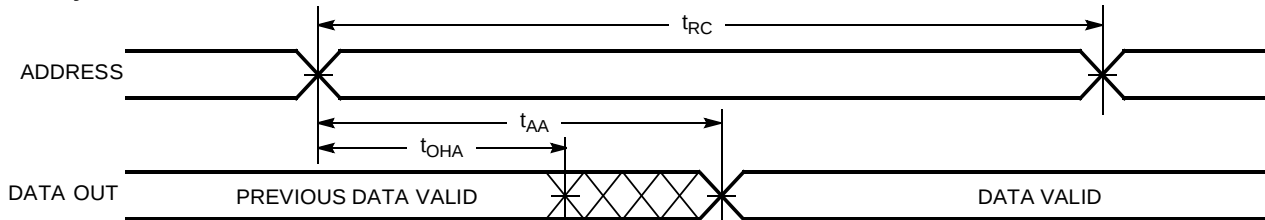
Parameter	Description	7C1020V-10		7C1020V-12		7C1020V-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	10		12		15		ns
t _{AA}	Address to Data Valid		10		12		15	ns
t _{OHA}	Data Hold from Address Change	3		3		3		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid		10		12		15	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		5		6		7	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z ^[5, 6]		5		6		7	ns
t _{LZCE}	$\overline{CE}$ LOW to Low Z ^[6]	3		3		3		ns
t _{HZCE}	$\overline{CE}$ HIGH to High Z ^[5, 6]		5		6		7	ns
t _{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t _{PD}	$\overline{CE}$ HIGH to Power-Down		12		12		15	ns
t _{DBE}	Byte enable to Data Valid		5		6		7	ns
t _{LZBE}	Byte enable to Low Z	0		0		0		ns
t _{HZBE}	Byte disable to High Z		5		6		7	ns
WRITE CYCLE ^[7]								
t _{WC}	Write Cycle Time	10		12		15		ns
t _{SCE}	$\overline{CE}$ LOW to Write End	8		9		10		ns
t _{AW}	Address Set-Up to Write End	7		8		10		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	7		8		10		ns
t _{SD}	Data Set-Up to Write End	5		6		10		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z ^[6]	3		3		3		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[5, 6]		5		6		7	ns
t _{BW}	Byte enable to end of write	7		8		9		ns

Notes:

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE} , t_{HZBE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW and BHE / BLE LOW. $\overline{CE}$, $\overline{WE}$ and BHE / BLE must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Switching Characteristics^[4] Over the Operating Range (continued)

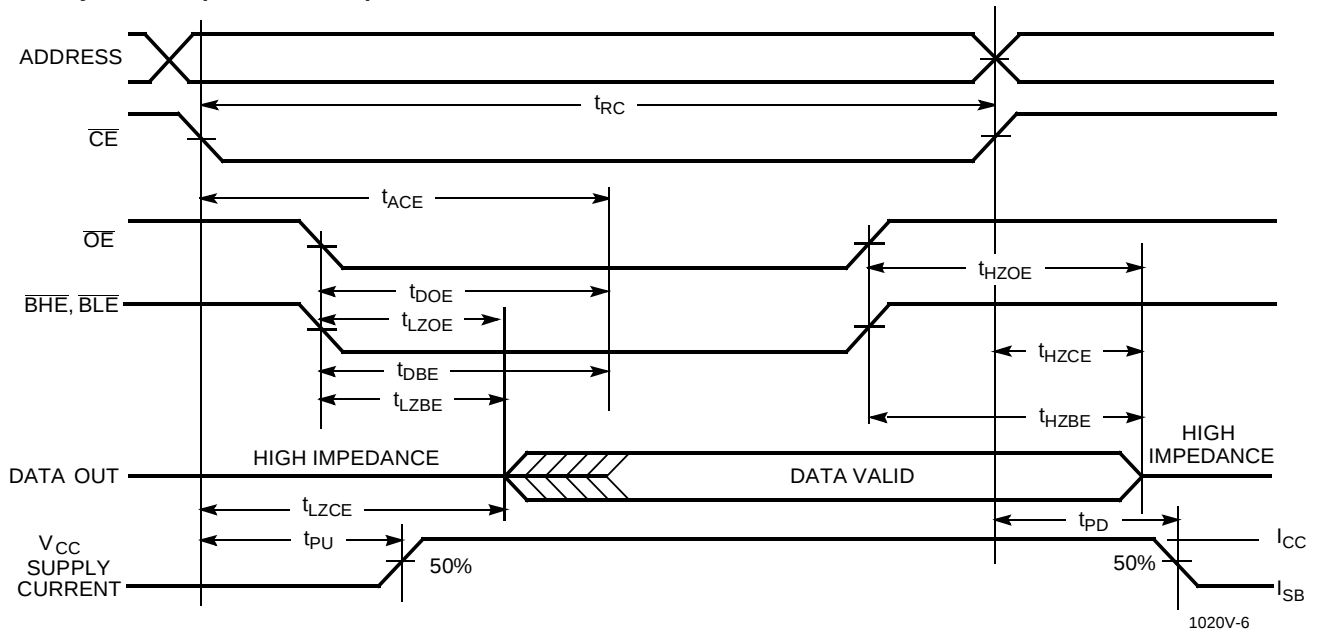
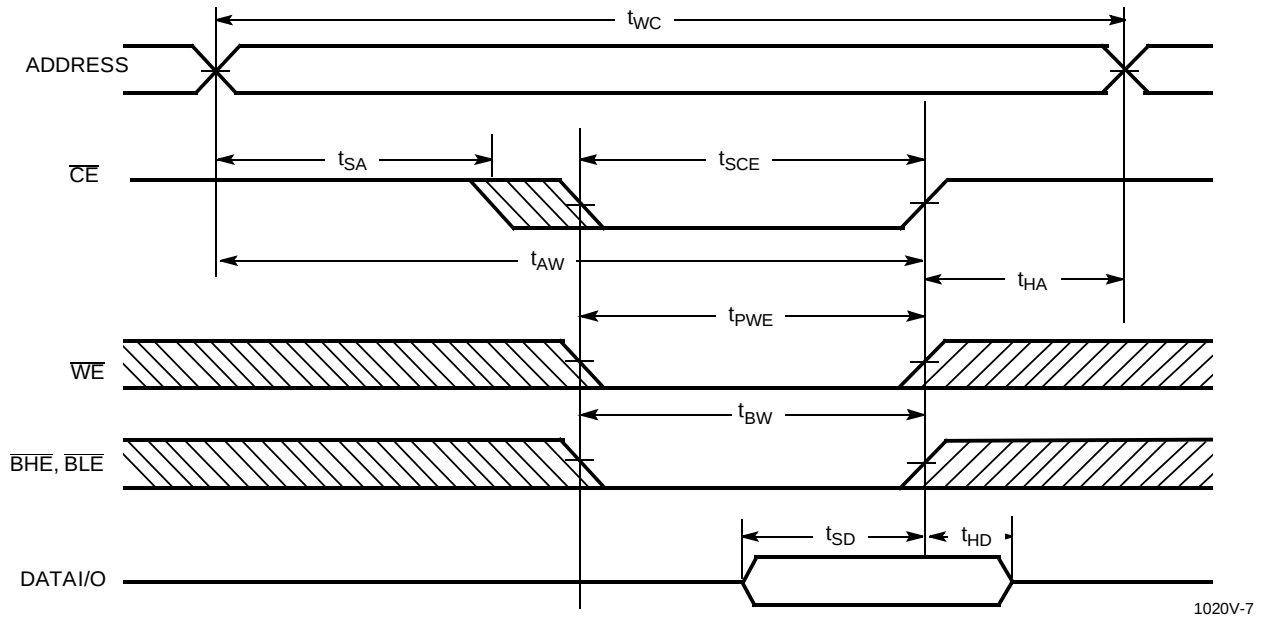
Parameter	Description	7C1020V-20		Unit
		Min.	Max.	
READ CYCLE				
t _{RC}	Read Cycle Time	20		ns
t _{AA}	Address to Data Valid		20	ns
t _{OHA}	Data Hold from Address Change	3		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid		20	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		9	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z	0		ns
t _{LZCE}	$\overline{CE}$ LOW to Low Z ^[6]	3		ns
t _{HZCE}	$\overline{CE}$ HIGH to High Z ^[5, 6]		9	ns
t _{PU}	$\overline{CE}$ LOW to Power-Up	0		ns
t _{PD}	$\overline{CE}$ HIGH to Power-Down		20	ns
t _{DBE}	Byte enable to Data Valid		9	ns
t _{LZBE}	Byte enable to Low Z	0		ns
t _{HZBE}	Byte disable to High Z		9	ns
WRITE CYCLE ^[7]				
t _{WC}	Write Cycle Time	20		ns
t _{SCE}	$\overline{CE}$ LOW to Write End	12		ns
t _{AW}	Address Set-Up to Write End	12		ns
t _{HA}	Address Hold from Write End	0		ns
t _{SA}	Address Set-Up to Write Start	0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	12		ns
t _{SD}	Data Set-Up to Write End	10		ns
t _{HD}	Data Hold from Write End	0		ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z ^[6]	3		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[5, 6]		9	ns
t _{BW}	Byte enable to end of write	12		ns

Switching Waveforms
Read Cycle No.1^[8, 9]


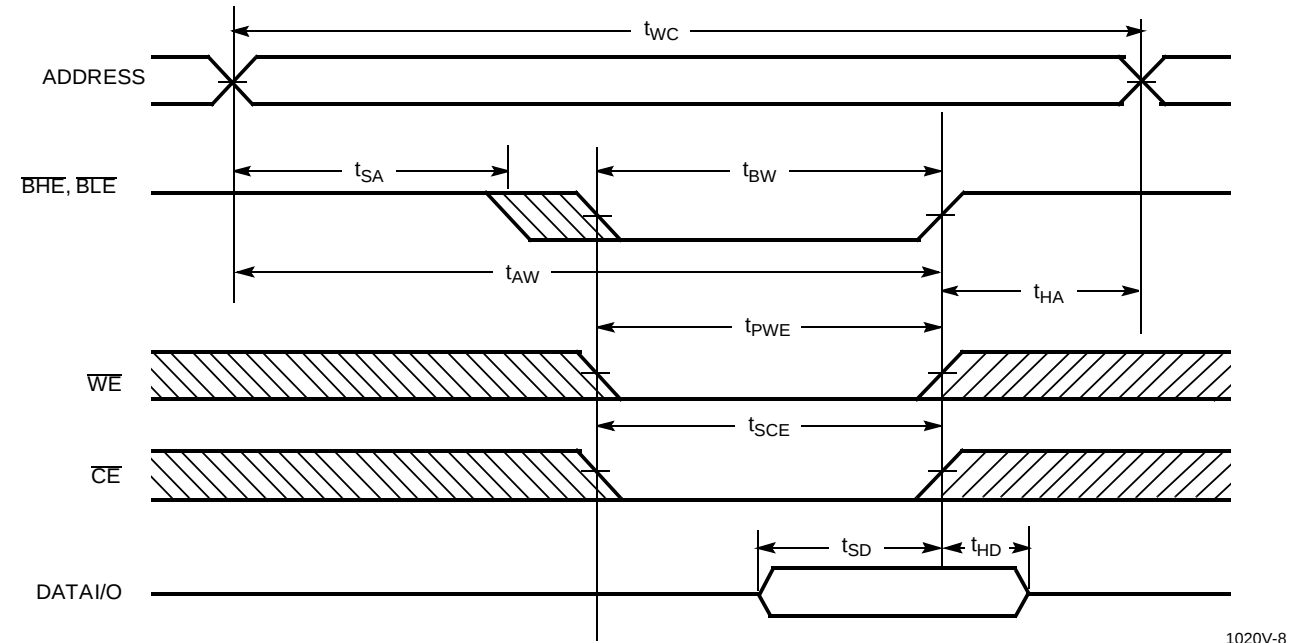
1020V-5

Notes:

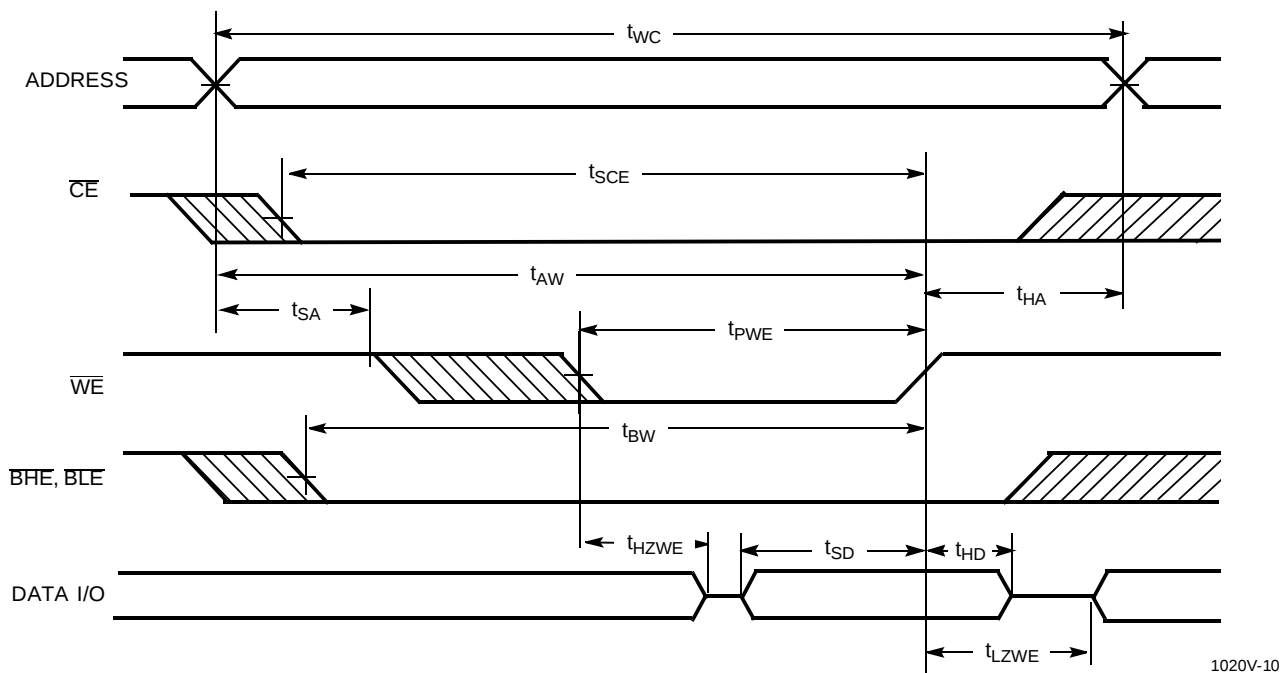
8. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$, and/or $\overline{BHE} = V_{IL}$
9. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)
Read Cycle No.2 ($\overline{OE}$ Controlled) ^[9, 10]

Write Cycle No. 1 ($\overline{CE}$ Controlled) ^[11, 12]

Notes:

10. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
11. Data I/O is high impedance if $\overline{OE}$ or BHE and/or BLE = V_{IH} .
12. If $\overline{CE}$ goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)
Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)


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Write Cycle No.3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)


1020V-10

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O ₁ - I/O ₈	I/O ₉ - I/O ₁₆	Mode	Power
H	X	X	X	X	High Z	High Z	Power-Down	Standby (I _{SB})
L	L	H	L	L	Data Out	Data Out	Read - All bits	Active (I _{CC})
			L	H	Data Out	High Z	Read - Lower bits only	Active (I _{CC})
			H	L	High Z	Data Out	Read - Upper bits only	Active (I _{CC})
L	X	L	L	L	Data In	Data In	Write - All bits	Active (I _{CC})
			L	H	Data In	High Z	Write - Lower bits only	Active (I _{CC})
			H	L	High Z	Data In	Write - Upper bits only	Active (I _{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I _{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I _{CC})

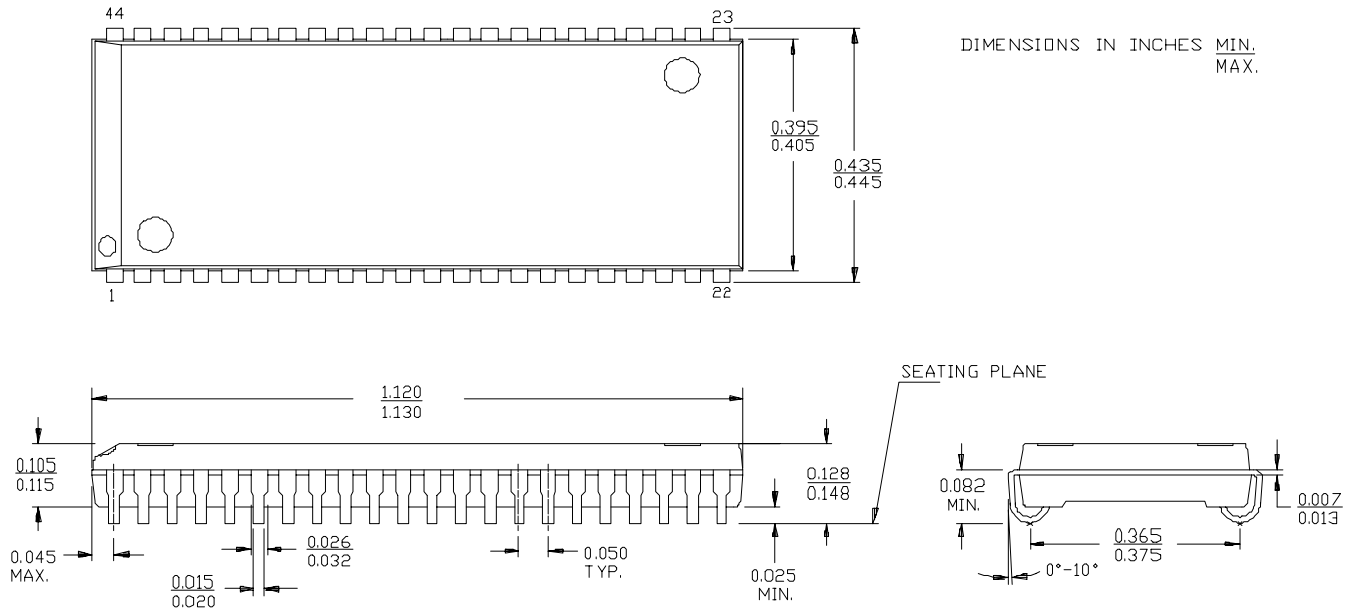
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1020V33-10VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020V33L-10VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020V33-10ZC	Z44	44-Lead TSOP Type II	Commercial
	CY7C1020V33L-10ZC	Z44	44-Lead TSOP Type II	Commercial
12	CY7C1020V33-12VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020V33L-12VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020V33-12ZC	Z44	44-Lead TSOP Type II	Commercial
	CY7C1020V33L-12ZC	Z44	44-Lead TSOP Type II	Commercial
15	CY7C1020V33-15VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020V33L-15VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020V33-15ZC	Z44	44-Lead TSOP Type II	Commercial
	CY7C1020V33L-15ZC	Z44	44-Lead TSOP Type II	Commercial
	CY7C1020V33-15ZI	Z44	44-Lead TSOP Type II	Industrial
20	CY7C1020V33L-20ZC	Z44	44-Lead TSOP Type II	Commercial

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Package Diagrams

44-Lead (400-Mil) Molded SOJ V34



44-Pin TSOP II Z44

DIMENSION IN MM (INCH)
MAX
MIN
LEAD COPLANARITY 0.004 INCHES.

