

2-Mbit (128K x 16) Static RAM

Features

- Pin equivalent to CY7C1011BV33
- High speed
 - $t_{AA} = 10 \text{ ns}$
- Low active power
 - 360 mW (max.)
- Data Retention at 2.0
- Automatic power-down when deselected
- Independent control of upper and lower bits
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Available in Pb-free and non Pb-free 44-pin TSOP II, 44-pin TQFP and non Pb-free 48-ball VFBGA packages

Functional Description

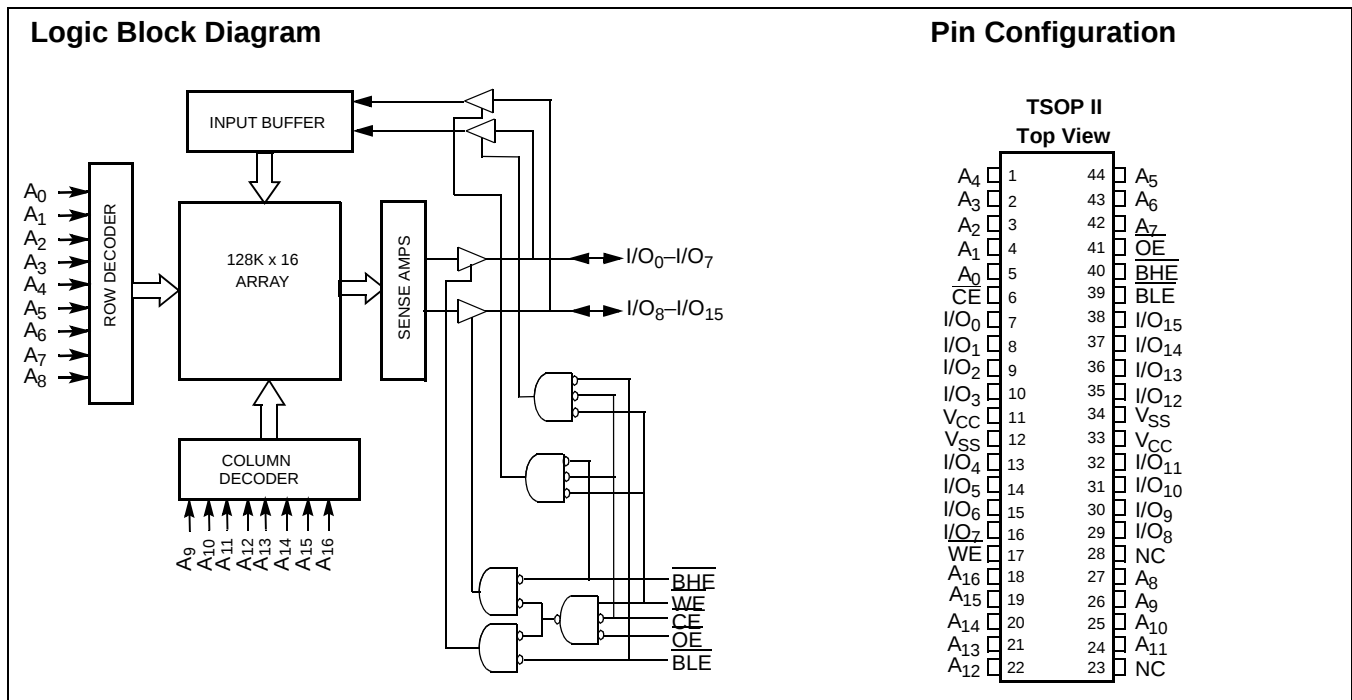
The CY7C1011CV33 is a high-performance CMOS Static RAM organized as 131,072 words by 16 bits.

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{16}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7 . If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1011CV33 is available in a standard 44-pin TSOP II package with center power and ground pinout, a 44-pin Thin Plastic Quad Flatpack (TQFP), as well as a 48-ball fine-pitch ball grid array (VFBGA) package.

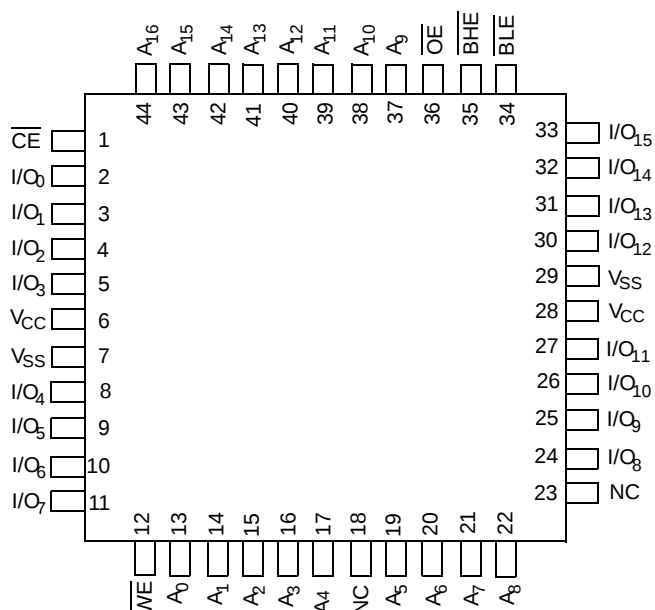


Selection Guide

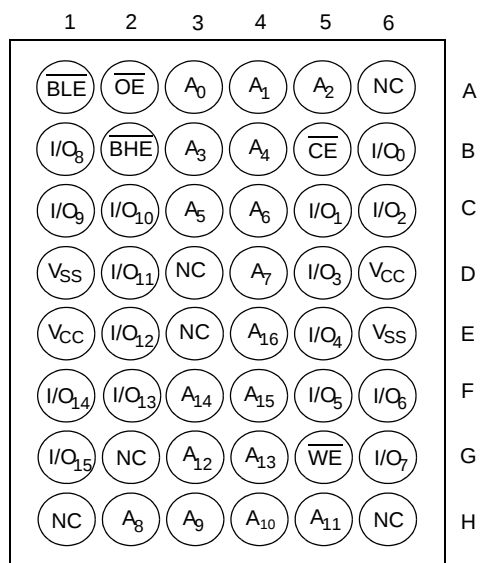
		-10	-12	-15	Unit
Maximum Access Time		10	12	15	ns
Maximum Operating Current	Com'l	90	85	80	mA
	Ind'l	100	95	90	
Maximum CMOS Standby Current	Com'l/Ind'l	10	10	10	mA

Pin Configurations

**44-pin TQFP
(Top View)**



**48-ball VFBGA
(Top View)**



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with
Power Applied -55°C to +125°C

Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to +4.6V

DC Voltage Applied to Outputs
in High-Z State^[1] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[1] -0.5V to $V_{CC} + 0.5V$

Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-up Current >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	-40°C to +85°C	

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-10		-12		-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage ^[1]		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	-1	+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$, Output Disabled	-1	+1	-1	+1	-1	+1	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.},$ $f = f_{MAX} = 1/t_{RC}$	Com'l	90		85		80	mA
			Ind'l	100		95		90	
I_{SB1}	Automatic CE Power-down Current —TTL Inputs	Max. V_{CC} , $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$		40		40		40	mA
I_{SB2}	Automatic CE Power-down Current —CMOS Inputs	Max. V_{CC} , $CE \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V$, $f = 0$	Com'l/ Ind'l	10		10		10	mA

Capacitance^[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz}, V_{CC} = 3.3V$	8	pF
C_{OUT}	I/O Capacitance		8	pF

Thermal Resistance^[2]

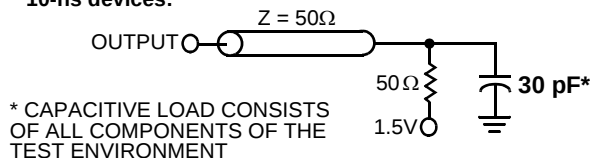
Parameter	Description	Test Conditions	TSOP II	TQFP	VFBGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	44.56	42.66	46.98	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		10.75	14.64	9.63	°C/W

Notes:

- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

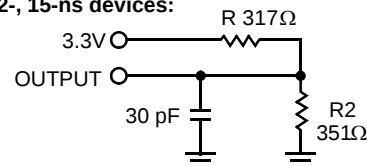
AC Test Loads and Waveforms^[3]

10-ns devices:



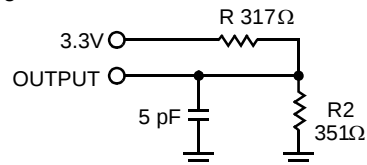
(a)

12-, 15-ns devices:

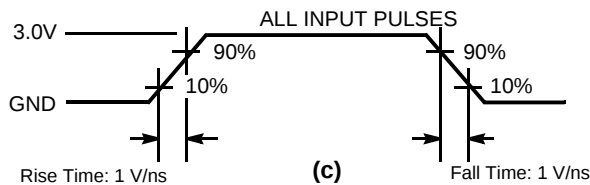


(b)

High-Z characteristics:



(d)



(c)

AC Switching Characteristics Over the Operating Range^[4]

Parameter	Description	−10		−12		−15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t _{power} ^[5]	V _{CC} (typical) to the first access	1		1		1		μs
t _{RC}	Read Cycle Time	10		12		15		ns
t _{AA}	Address to Data Valid		10		12		15	ns
t _{OHA}	Data Hold from Address Change	3		3		3		ns
t _{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		10		12		15	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		5		6		7	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low-Z	0		0		0		ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High-Z ^[6, 7]		5		6		7	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to Low-Z ^[7]	3		3		3		ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to High-Z ^[6, 7]		5		6		7	ns
t _{PU}	$\overline{\text{CE}}$ LOW to Power-up	0		0		0		ns
t _{PD}	$\overline{\text{CE}}$ HIGH to Power-down		10		12		15	ns
t _{DBE}	Byte Enable to Data Valid		5		6		7	ns
t _{LZBE}	Byte Enable to Low-Z	0		0		0		ns
t _{HZBE}	Byte Disable to High-Z		6		6		7	ns

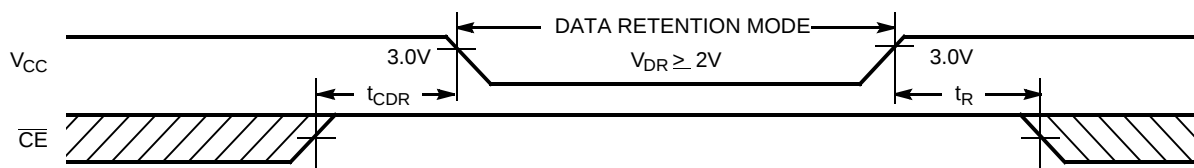
Notes:

- AC characteristics (except High-Z) for all 10-ns parts are tested using the load conditions shown in (a). All other speeds are tested using the Thevenin load shown in (b). High-Z characteristics are tested for all speeds using the test load shown in (d).
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
- t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access is performed.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.

AC Switching Characteristics Over the Operating Range^[4] (continued)

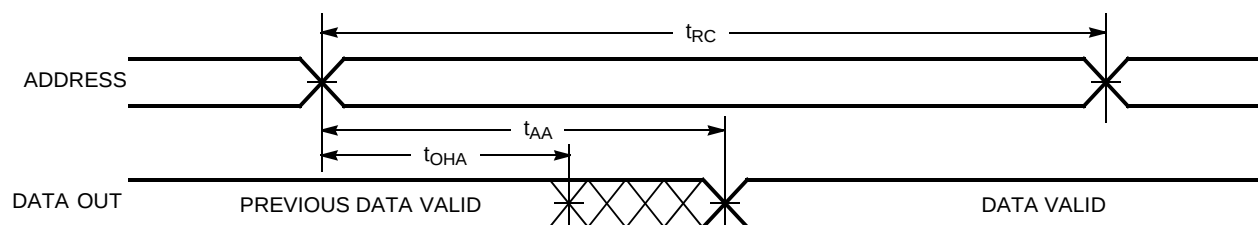
Parameter	Description	-10		-12		-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle ^[8, 9]								
t _{WC}	Write Cycle Time	10		12		15		ns
t _{SCE}	$\overline{CE}$ LOW to Write End	7		8		10		ns
t _{AW}	Address Set-up to Write End	7		8		10		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-up to Write Start	0		0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	7		8		10		ns
t _{SD}	Data Set-up to Write End	5		6		7		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{LZWE}	$\overline{WE}$ HIGH to Low-Z ^[7]	3		3		3		ns
t _{HZWE}	$\overline{WE}$ LOW to High-Z ^[6, 7]		5		6		7	ns
t _{BW}	Byte Enable to End of Write	7		8		10		ns

Data Retention Waveform



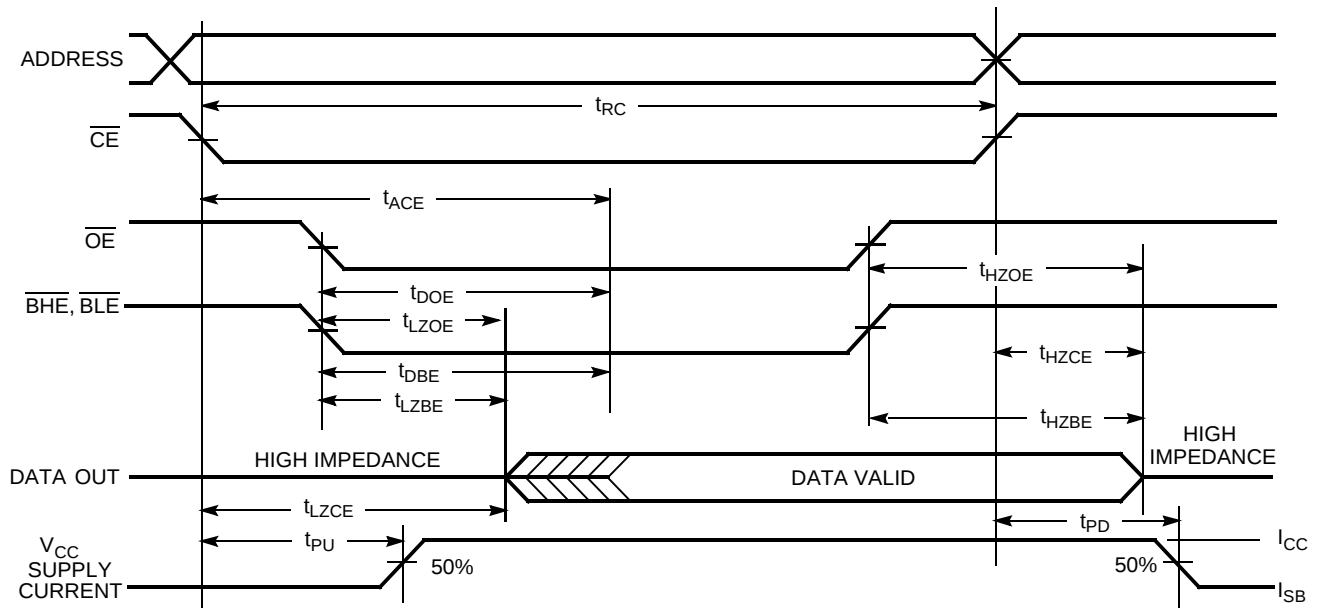
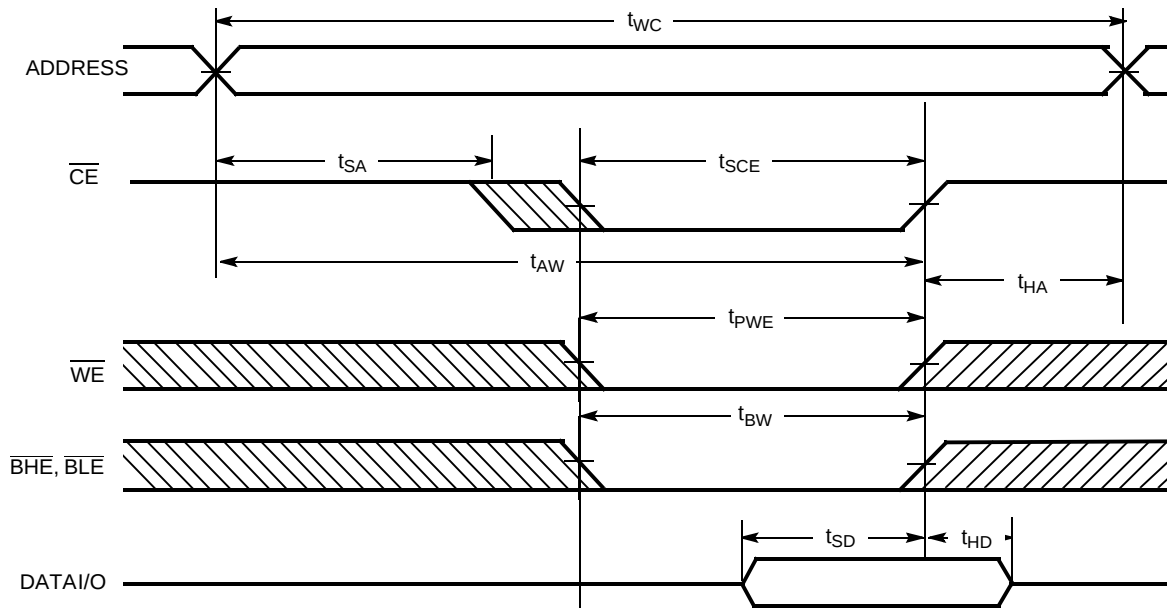
Switching Waveforms

Read Cycle No. 1^[10, 11]



Notes:

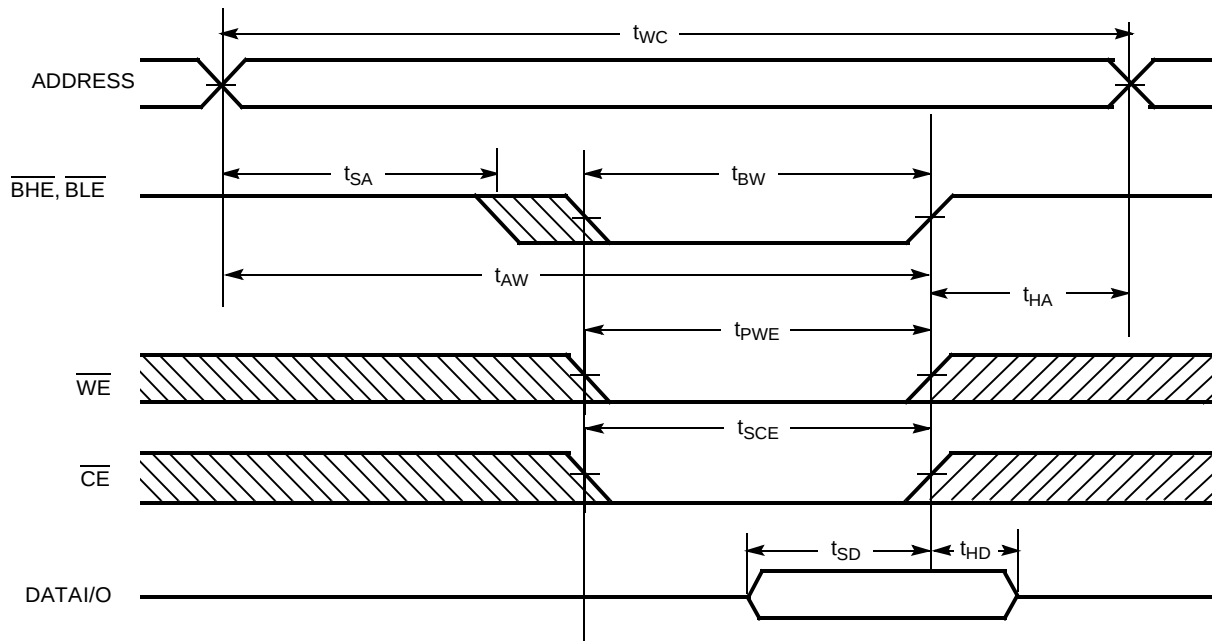
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
9. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD} .
10. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, BHE and/or $\overline{BHE} = V_{IL}$.
11. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)
Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled)^[11, 12]

Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[13, 14]

Notes:

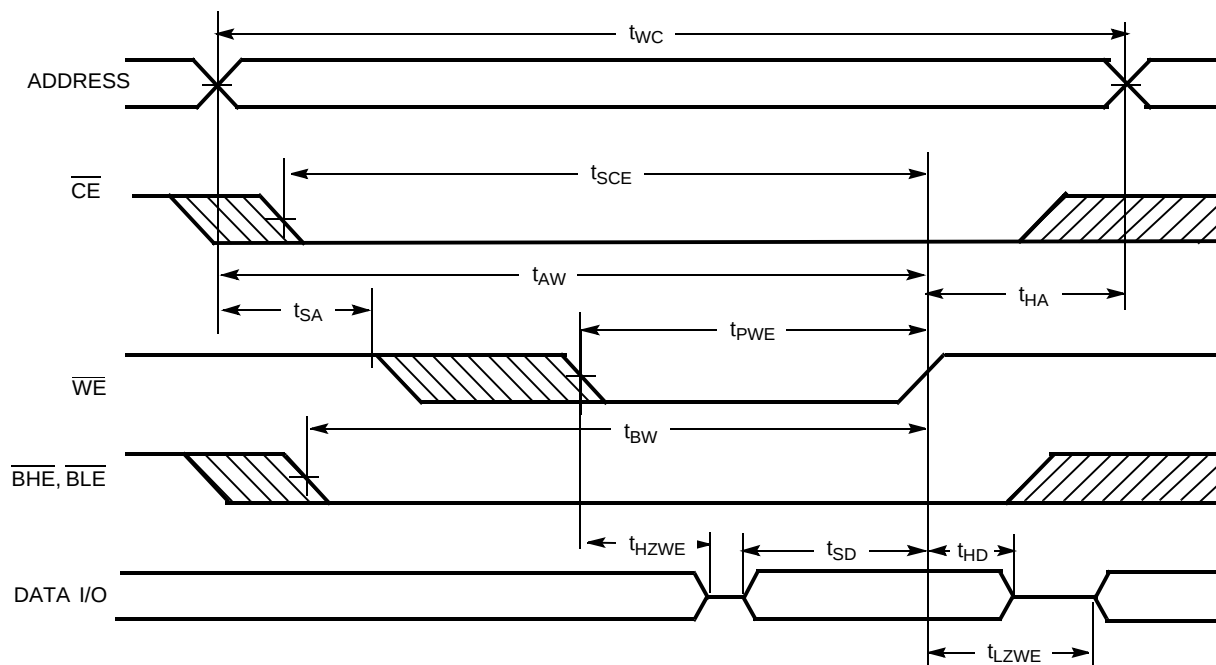
12. Address valid prior to or coincident with $\overline{\text{CE}}$ transition LOW.
13. Data I/O is high-impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{\text{IH}}$.
14. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)



Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O ₀ –I/O ₇	I/O ₈ –I/O ₁₅	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power-down	Standby (I _{SB})
L	L	H	L	L	Data Out	Data Out	Read All Bits	Active (I _{CC})
L	L	H	L	H	Data Out	High-Z	Read Lower Bits Only	Active (I _{CC})
L	L	H	H	L	High-Z	Data Out	Read Upper Bits Only	Active (I _{CC})
L	X	L	L	L	Data In	Data In	Write All Bits	Active (I _{CC})
L	X	L	L	H	Data In	High-Z	Write Lower Bits Only	Active (I _{CC})
L	X	L	H	L	High-Z	Data In	Write Upper Bits Only	Active (I _{CC})
L	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active (I _{CC})

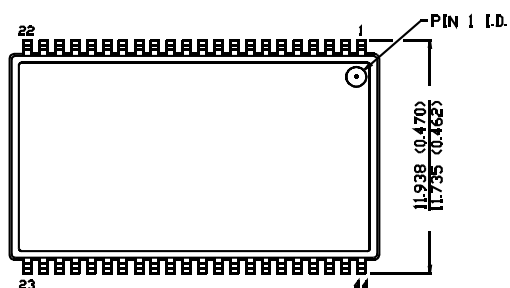
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1011CV33-10ZC	51-85087	44-pin TSOP II	Commercial
	CY7C1011CV33-10ZXC		44-pin TSOP II (Pb-Free)	
	CY7C1011CV33-10ZXI		44-pin TSOP II (Pb-Free)	Industrial
	CY7C1011CV33-10BVI	51-85150	48-ball (6 x 8 x 1 mm) VFBGA	
12	CY7C1011CV33-12ZC	51-85087	44-pin TSOP II	Commercial
	CY7C1011CV33-12ZXC		44-pin TSOP II (Pb-Free)	
	CY7C1011CV33-12ZI		44-pin TSOP II	Industrial
	CY7C1011CV33-12ZXI		44-pin TSOP II (Pb-Free)	
	CY7C1011CV33-12AXI	51-85064	44-pin TQFP (Pb-Free)	Industrial
	CY7C1011CV33-12BVI	51-85150	48-ball (6 x 8 x 1 mm) VFBGA	
15	CY7C1011CV33-15ZXC	51-85087	44-pin TSOP II (Pb-Free)	Commercial
	CY7C1011CV33-15AI	51-85064	44-pin TQFP	Industrial

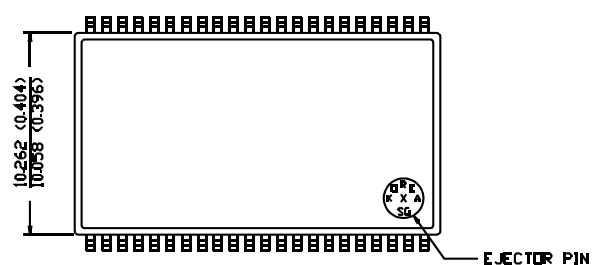
Package Diagrams

44-Pin TSOP II (51-85087)

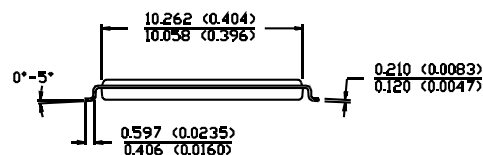
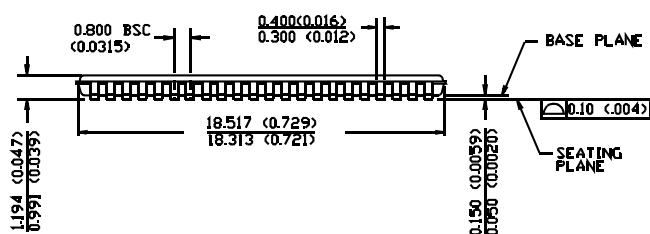
DIMENSION IN MM (INCH)



TOP VIEW

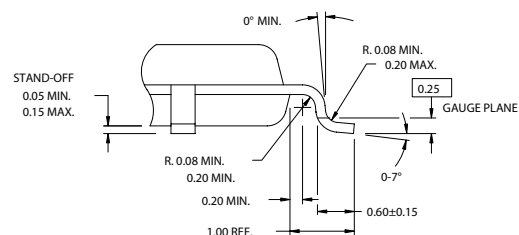
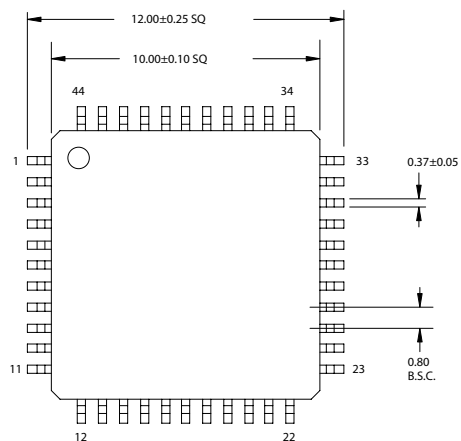


BOTTOM VIEW

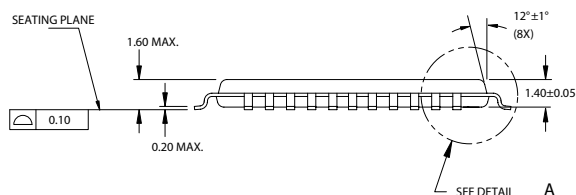


51-85087-*A

44-pin Thin Plastic Quad Flat Pack (51-85064)



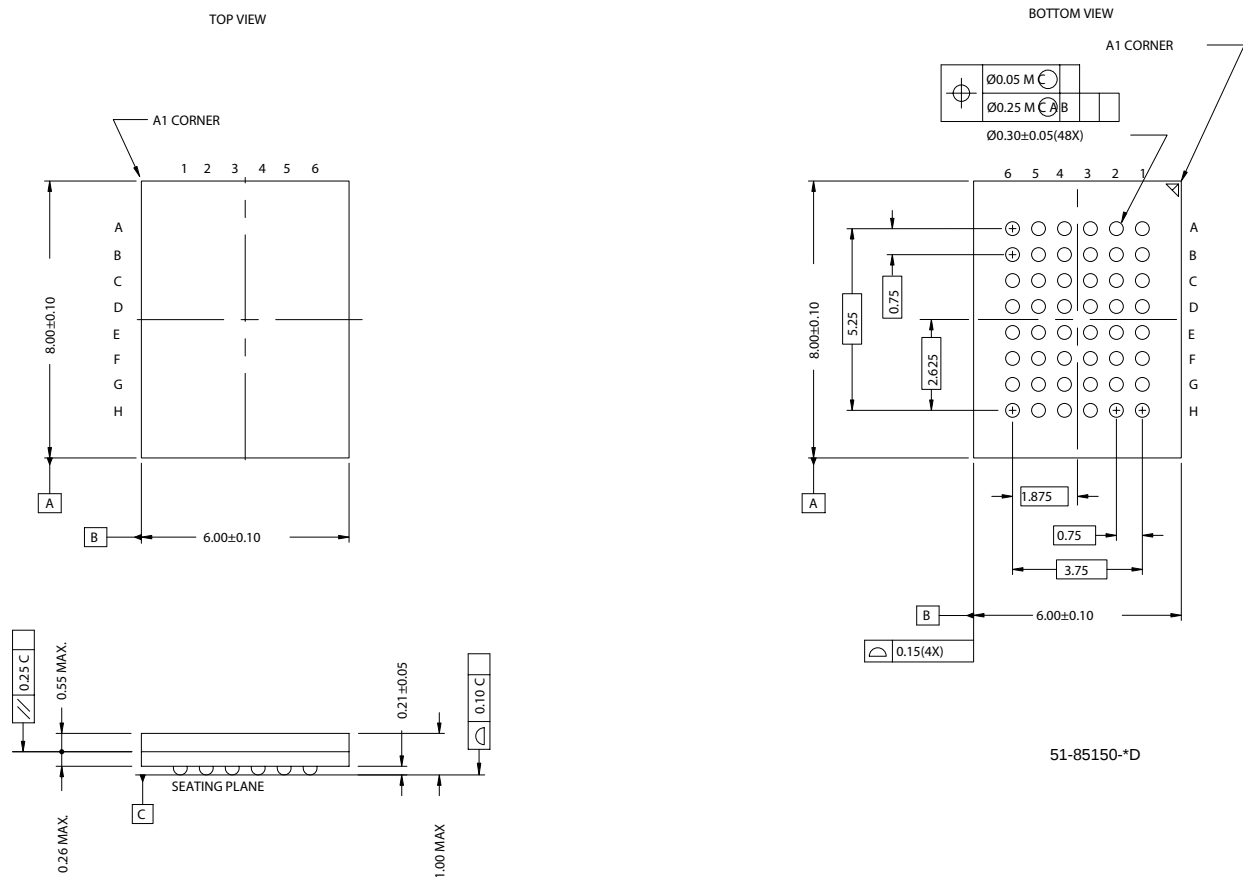
DETAIL A



NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85064-*C

Package Diagrams (continued)
48-ball VFBGA (6 x 8 x 1 mm) (51-85150)


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Document History Page

Document Title: CY7C1011CV33, 2-Mbit (128K x 16) Static RAM Document Number: 38-05232				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	117132	07/31/02	HGK	New Data Sheet
*A	118057	08/19/02	HGK	Pin configuration for 48-ball FBGA correction
*B	119702	10/11/02	DFP	Updated FBGA to VFBGA; updated package code on page 8 to BV48A. Updated address pinouts on page 1 to A0 to A16. Updated CMOS standby current on page 1 from 8 to 10 mA
*C	386106	See ECN	PCI	Added lead-free parts in Ordering Information Table
*D	498501	See ECN	NXR	Corrected typo in the Logic Block Diagram on page# 1 Included the Maximum Ratings for Static Discharge Voltage and Latch up Current on page# 3 Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Updated the Ordering Information Table
*E	522620	See ECN	VKN	Added Thermal Resistance Table