CY7C106B
CY7C1006B

256K x 4 Static RAM

Features

- **High speed**
  - **— t_{AA} = 12 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— 495 mW**
- **Low standby power**
  - **— 275 mW**
- **2.0V data retention (optional)**
  - **— 100 μW**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C106B and CY7C1006B are high-performance CMOS static RAMs organized as 262,144 words by 4 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$), an active LOW Output Enable ($\overline{OE}$), and three-state drivers. These devices have an automatic power-down feature that reduces power consumption by more than 65% when the devices are deselected.

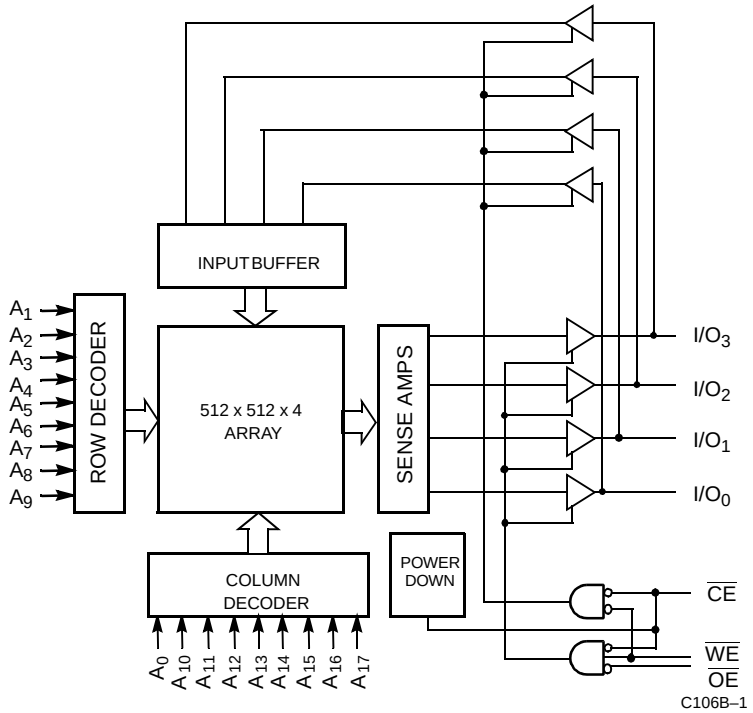
Writing to the devices is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the four I/O pins (I/O_0 through I/O_3) is then written into the location specified on the address pins (A_0 through A_{17}).

Reading from the devices is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the four I/O pins.

The four input/output pins (I/O_0 through I/O_3) are placed in a high-impedance state when the devices are deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ and $\overline{WE}$ LOW).

The CY7C106B is available in a standard 400-mil-wide SOJ; the CY7C1006B is available in a standard 300-mil-wide SOJ.

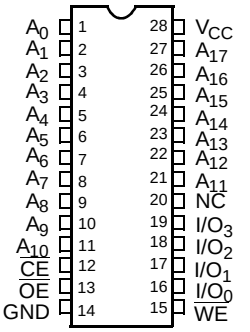
Logic Block Diagram



C106B–1

Pin Configuration

SOJ
Top View



C106B–2

Selection Guide

	7C106B-12 7C1006B-12	7C106B-15 7C1006B-15	7C106B-20 7C1006B-20	7C106B-25 7C1006B-25	7C106B-35
Maximum Access Time (ns)	12	15	20	25	35
Maximum Operating Current (mA)	90	80	75	70	60
Maximum Standby Current (mA)	50	30	30	30	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] .... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... –0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... –0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–45°C to +85°C	

Electrical Characteristics Over the Operating Range

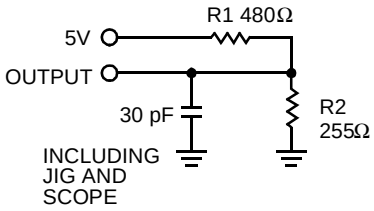
Parameter	Description	Test Conditions		7C106B-12 7C1006B-12 Min.	7C106B-12 7C1006B-12 Max.	7C106B-15 7C1006B-15 Min.	7C106B-15 7C1006B-15 Max.	7C106B-20 7C1006B-20 Min.	7C106B-20 7C1006B-20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} +0.3	2.2	V_{CC} +0.3	2.2	V_{CC} +0.3	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	$GND \le V_I \le V_{CC}$		–1	+1	–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	$GND \le V_I \le V_{CC}$, Output Disabled		–5	+5	–5	+5	–5	+5	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			–300		–300		–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $f = f_{MAX} = 1/t_{RC}$			90		80		75	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE} \ge V_{IH}$, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$, $f = f_{MAX}$			50		30		30	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE} \ge V_{CC} - 0.3V$, $V_{IN} \ge V_{CC} - 0.3V$ or $V_{IN} \le 0.3V$, f=0	Com'l		10		10		10	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		V		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V		
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V		
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	–0.3	0.8	V		
I_{IX}	Input Load Current	$GND \le V_I \le V_{CC}$		–1	+1	–1	+1	µA		
I_{OZ}	Output Leakage Current	$GND \le V_I \le V_{CC}$, Output Disabled		–5	+5	–5	+5	µA		
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			–300		–300	mA		
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $f = f_{MAX} = 1/t_{RC}$			70		60	mA		
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE} \ge V_{IH}$, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$, $f = f_{MAX}$			30		25	mA		
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE} \ge V_{CC} - 0.3V$, $V_{IN} \ge V_{CC} - 0.3V$ or $V_{IN} \le 0.3V$, f = 0	Com'l		10		10	mA		

Notes:
1. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

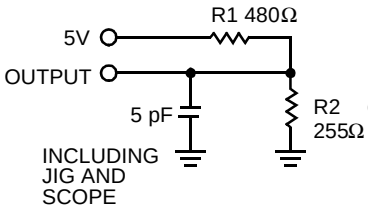
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{IN}: Controls			10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms

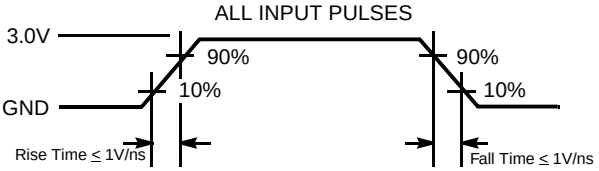


(a)



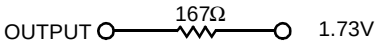
(b)

C106B–3



C106B–4

Equivalent to: THÉVENIN EQUIVALENT



Note:
4. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[5]

Parameter	Description	7C106B-12 7C1006B-12		7C106B-15 7C1006B-15		7C106B-20 7C1006B-20		7C106B-25 7C1006B-25		7C106B-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	12		15		20		25		35		ns
t_{AA}	Address to Data Valid		12		15		20		25		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		7		8		10		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		6		7		8		10		10	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		6		7		8		10		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		25		35	ns
WRITE CYCLE[8, 9]												
t_{WC}	Write Cycle Time	12		15		20		25		35		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		12		15		20		25		ns
t_{AW}	Address Set-Up to Write End	10		12		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		20		25		ns
t_{SD}	Data Set-Up to Write End	7		8		10		15		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	2		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]		6		7		8		10		10	ns

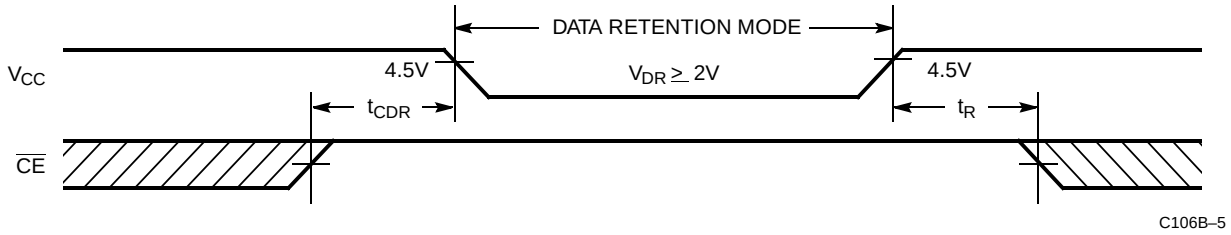
Notes:

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30–pF load capacitance.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
9. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Characteristics Over the Operating Range

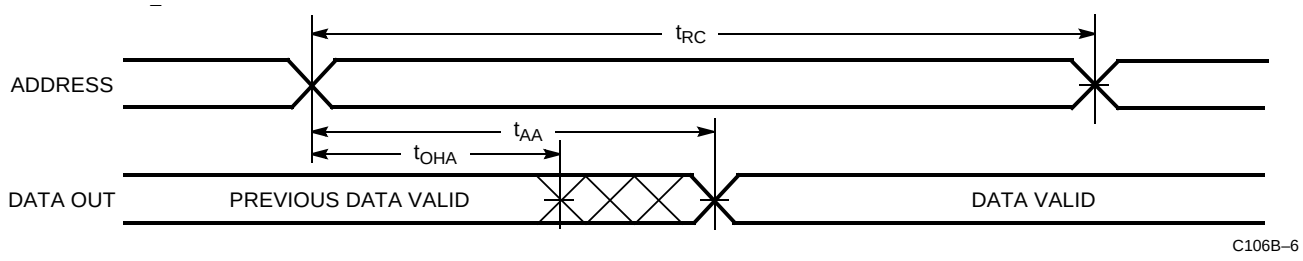
Parameter	Description	Conditions[10]	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		250	µA
t_{CDR}[4]	Chip Deselect to Data Retention Time		0		ns
t_R[4]	Operation Recovery Time		200		µs

Data Retention Waveform

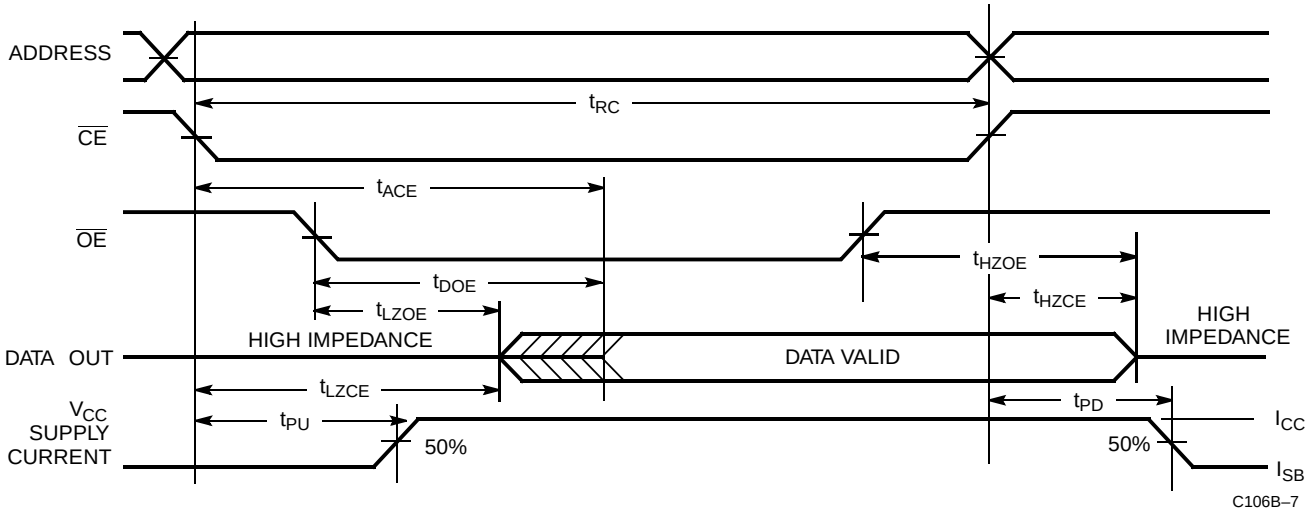


Switching Waveforms

Read Cycle No.1[11, 12]



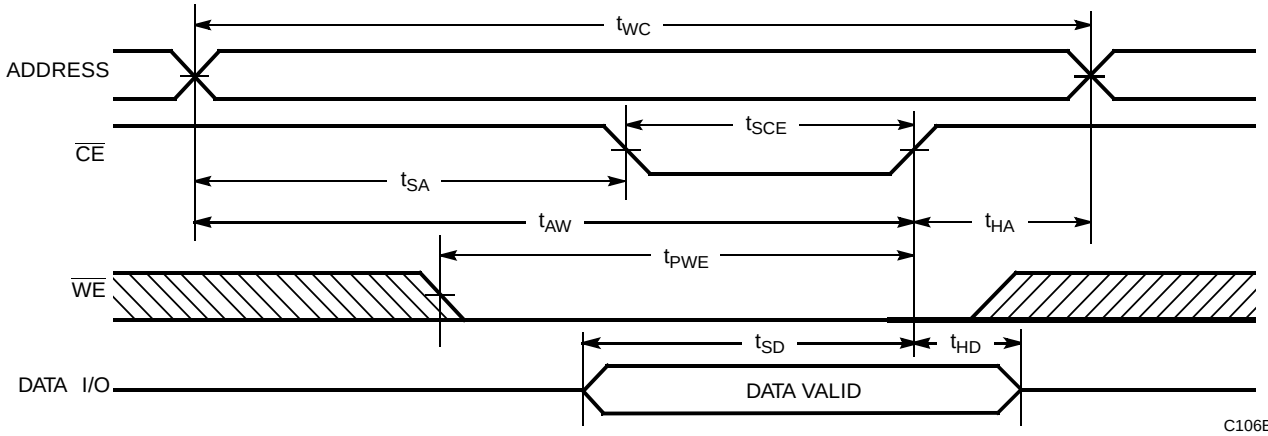
Read Cycle No. 2 ($\overline{OE}$ Controlled)[12, 13]



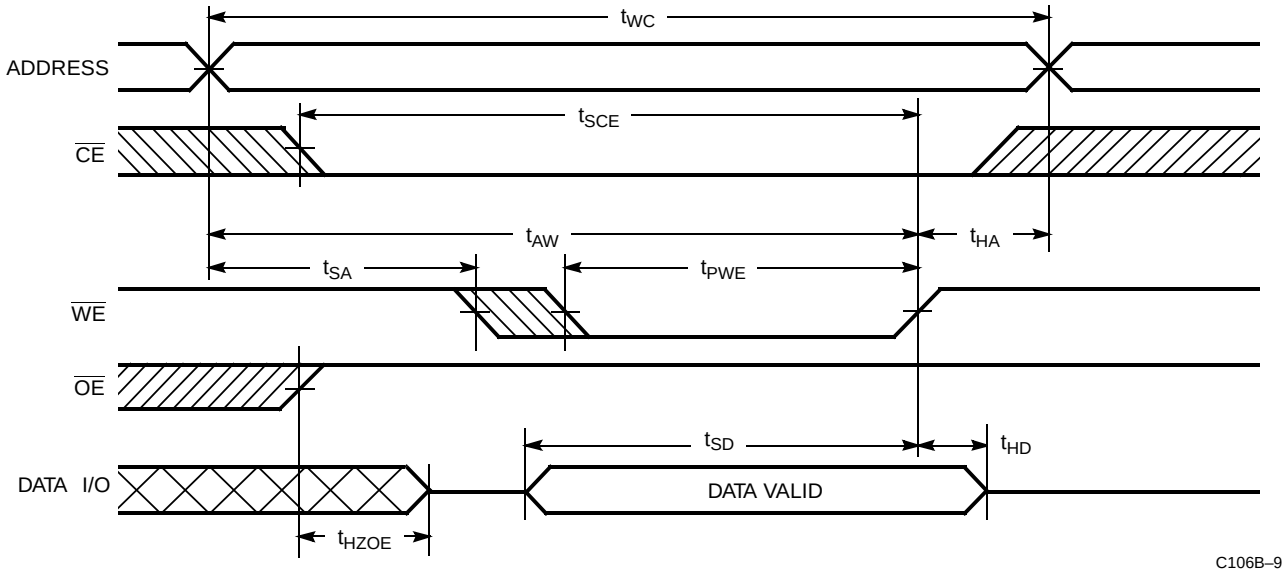
Notes:
10. No input may exceed V_{CC} +0.5V.
11. Device is continuously selected, $\overline{OE}$ and $\overline{CE} = V_{IL}$.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)[14, 15]



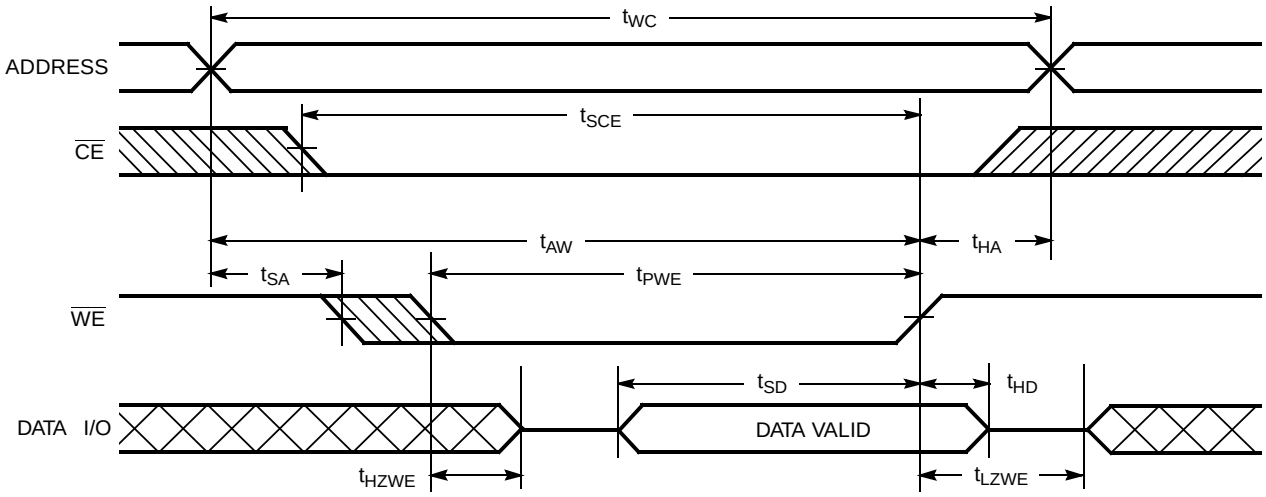
Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[14, 15]



Notes:
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
15. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[9, 15]



Truth Table

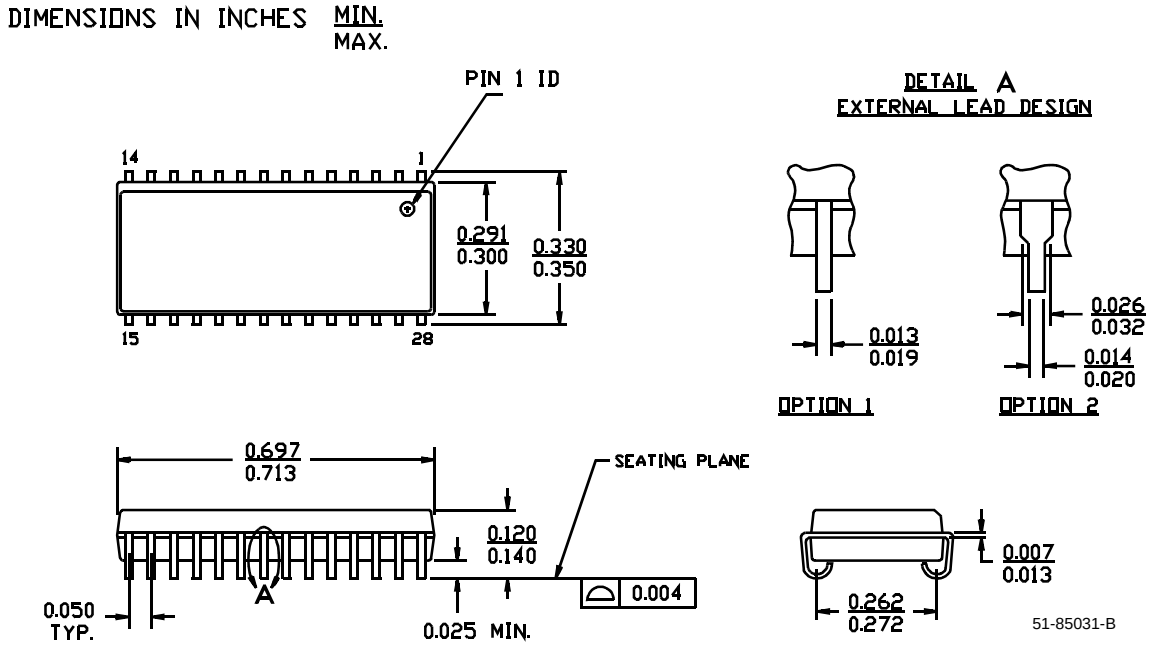
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Input/Output	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

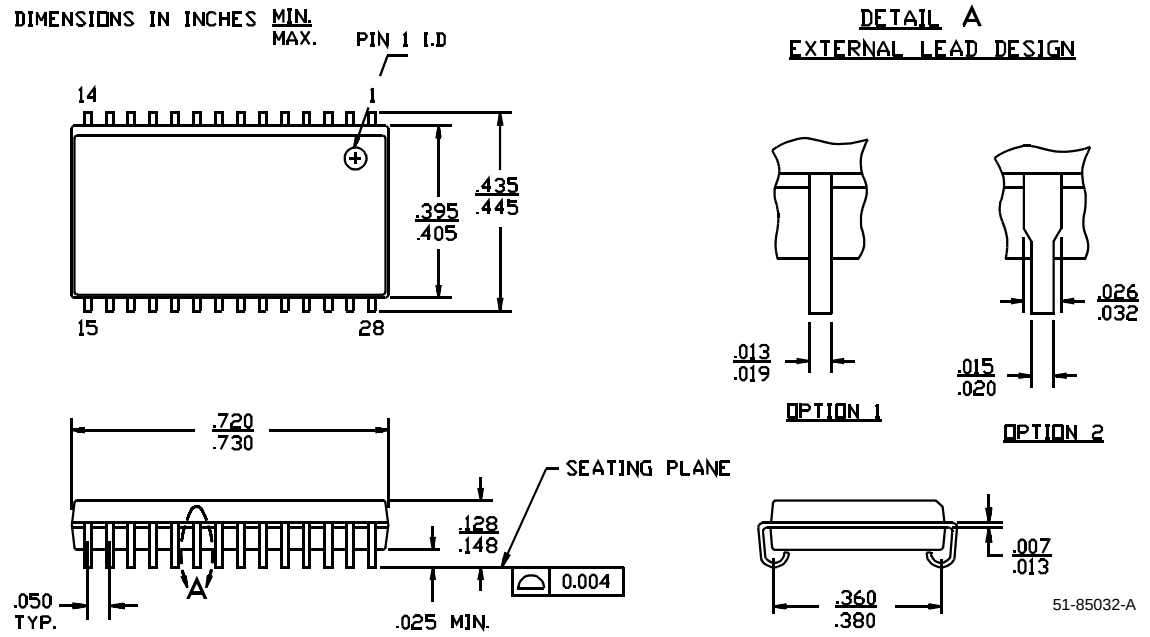
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C106B-12VC	V28	28-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1006B-12VC	V21	28-Lead (300-Mil) Molded SOJ	
15	CY7C106B-15VC	V28	28-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1006B-15VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C106B-15VI	V28	28-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1006B-15VI	V21	28-Lead (300-Mil) Molded SOJ	
20	CY7C106B-20VC	V28	28-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1006B-20VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C106B-20VI	V28	28-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1006B-20VI	V21	28-Lead (300-Mil) Molded SOJ	
25	CY7C106B-25VC	V28	28-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1006B-25VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C106B-25VI	V28	28-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1006B-25VI	V21	28-Lead (300-Mil) Molded SOJ	
35	CY7C106B-35VC	V28	28-Lead (400-Mil) Molded SOJ	Commercial
	CY7C106B-35VI	V28	28-Lead (400-Mil) Molded SOJ	Industrial

Package Diagrams

28-Lead (300-Mil) Molded SOJ V21



28-Lead (400-Mil) Molded SOJ V28



© Cypress Semiconductor Corporation, 2001. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress Semiconductor product. Nor does it convey or imply any license under patent or other rights. Cypress Semiconductor does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress Semiconductor products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress Semiconductor against all charges.

Document Title: CY7C106B, CY7C1006B 256K x 4 Static RAM Document Number: 38-05037				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106831	09/17/01	SZV	Change from Spec number: 38-00955 to 38-05037