CY7C024/0241
CY7C025/0251

# 4K x 16/18 and 8K x 16/18 Dual-Port Static RAM with SEM, INT, BUSY

## Features

- **True Dual-Ported memory cells which allow simultaneous reads of the same memory location**
- **4K x 16 organization (CY7C024)**
- **4K x 18 organization (CY7C0241)**
- **8K x 16 organization (CY7C025)**
- **8K x 18 organization (CY7C0251)**
- **0.65-micron CMOS for optimum speed/power**
- **High-speed access: 15 ns**
- **Low operating power: $I_{CC}$ = 150 mA (typ.)**
- **Fully asynchronous operation**
- **Automatic power-down**
- **Expandable data bus to 32/36 bits or more using Master/Slave chip select when using more than one device**
- **On-chip arbitration logic**
- **Semaphores included to permit software handshaking between ports**
- **$\overline{INT}$ flag for port-to-port communication**
- **Separate upper-byte and lower-byte control**
- **Pin select for Master or Slave**
- **Available in 84-pin Lead (Pb)-free PLCC, 84-pin PLCC, 100-pin Lead (Pb)-free TQFP, and 100-pin TQFP**

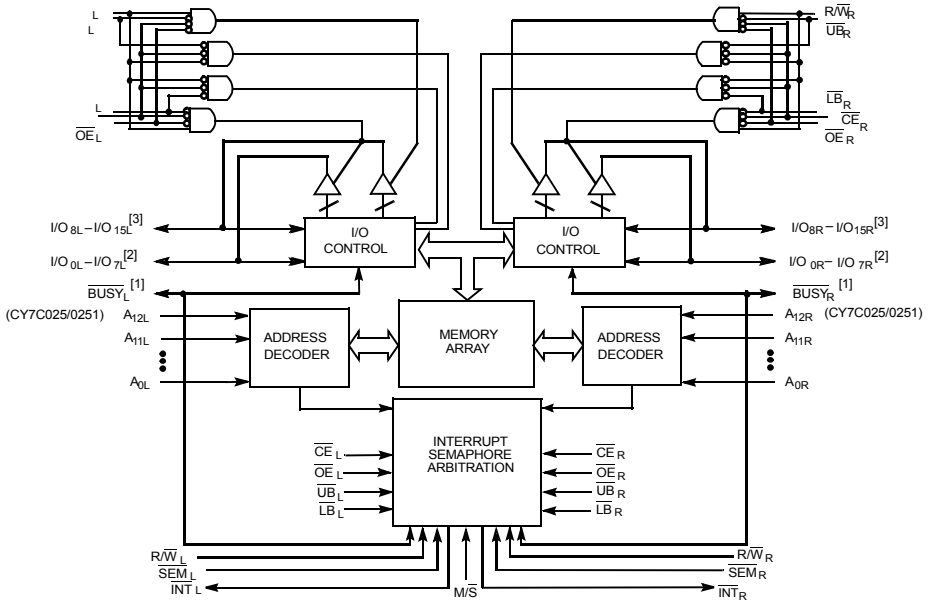
## Functional Description

The CY7C024/0241 and CY7C025/0251 are low-power CMOS 4K x 16/18 and 8K x 16/18 dual-port static RAMs. Various arbitration schemes are included on the CY7C024/0241 and CY7C025/0251 to handle situations when multiple processors access the same piece of data. Two ports are provided, permitting independent, asynchronous access for reads and writes to any location in memory. The CY7C024/0241 and CY7C025/0251 can be utilized as standalone 16-/18-bit dual-port static RAMs or multiple devices can be combined in order to function as a 32-/36-bit or wider master/slave dual-port static RAM. An M/$\overline{S}$ pin is provided for implementing 32-/36-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: Chip Enable ($\overline{CE}$), Read or Write Enable (R/$\overline{W}$), and Output Enable ($\overline{OE}$). Two flags are provided on each port ($\overline{BUSY}$ and $\overline{INT}$). $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. The Interrupt Flag ($\overline{INT}$) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a chip select ($\overline{CE}$) pin.

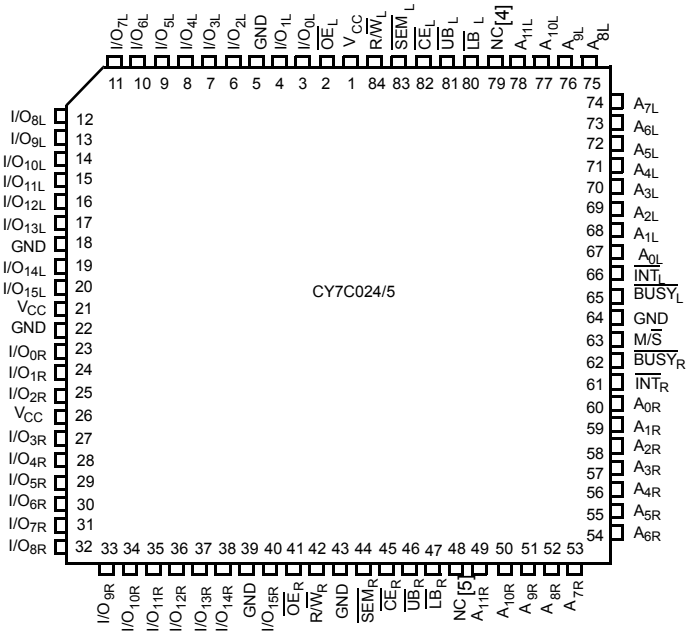
The CY7C024/0241 and CY7C025/0251 are available in 84-pin Lead (Pb)-free PLCCs, 84-pin PLCCs (CY7C024 and CY7C025 only), 100-pin Lead (Pb)-free Thin Quad Plastic Flatplack (TQFP) and 100-pin Thin Quad Plastic Flatpack.

## Logic Block Diagram




## Pin Configurations

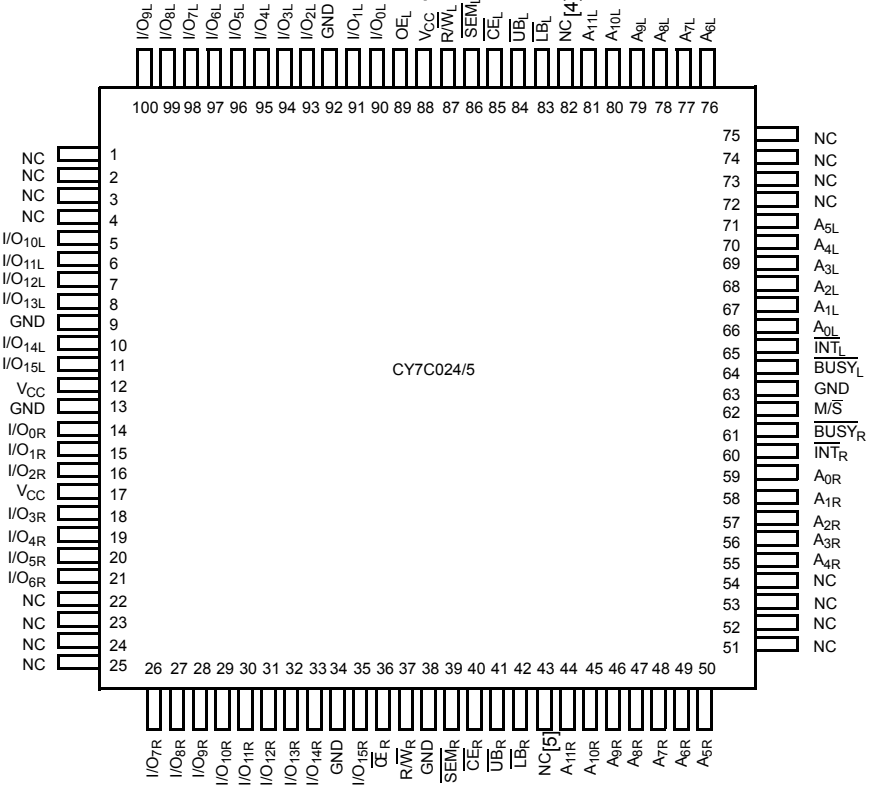
**84-Pin PLCC**
**Top View**



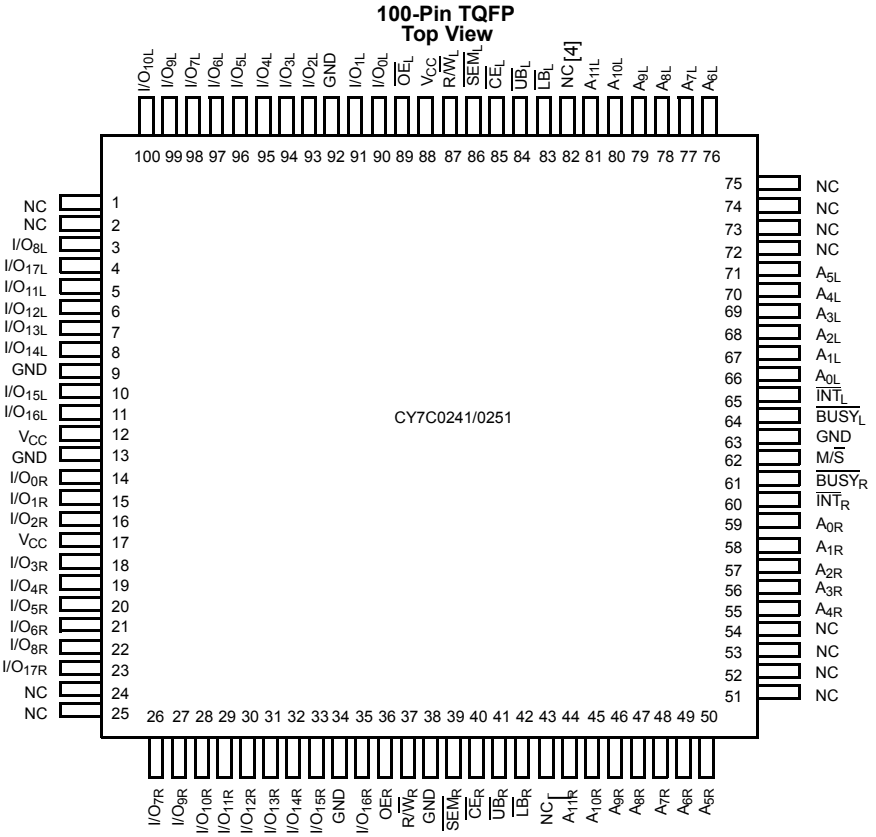

**Notes:**
1. BUSY is an output in master mode and an input in slave mode.
2. $I/O_0$ –$I/O_8$ on the CY7C0241/0251.
3. $I/O_9$ –$I/O_{17}$ on the CY7C0241/0251.
4. $A_{12L}$ on the CY7C025/0251.
5. $A_{12R}$ on the CY7C025/0251.

**Pin Configurations** (continued)

**100-Pin TQFP**
**Top View**




**100-Pin TQFP**
**Top View**



## Pin Definitions

| Left Port | Right Port | Description |
|---|---|---|
| $\overline{CE}_L$ | $\overline{CE}_R$ | Chip Enable |
| $R/\overline{W}_L$ | $R/\overline{W}_R$ | Read/Write Enable |
| $\overline{OE}_L$ | $\overline{OE}_R$ | Output Enable |
| $A_{0L}$–$A_{11/12L}$ | $A_{0R}$–$A_{11/12R}$ | Address |
| $I/O_{0L}$–$I/O_{15/17L}$ | $I/O_{0R}$–$I/O_{15/17R}$ | Data Bus Input/Output |
| $\overline{SEM}_L$ | $\overline{SEM}_R$ | Semaphore Enable |
| $\overline{UB}_L$ | $\overline{UB}_R$ | Upper Byte Select |
| $\overline{LB}_L$ | $\overline{LB}_R$ | Lower Byte Select |
| $\overline{INT}_L$ | $\overline{INT}_R$ | Interrupt Flag |
| $\overline{BUSY}_L$ | $\overline{BUSY}_R$ | Busy Flag |
| $M/\overline{S}$ | | Master or Slave Select |
| $V_{CC}$ | | Power |
| GND | | Ground |

## Selection Guide

| | 7C024/0241–15<br>7C025/0251–15 | 7C024/0241–25<br>7C025/0251–25 | 7C024/0241–35<br>7C025/0251–35 | 7C024/0241–55<br>7C025/0251–55 |
|---|---|---|---|---|
| Maximum Access Time (ns) | 15 | 25 | 35 | 55 |
| Typical Operating Current (mA) | 190 | 170 | 160 | 150 |
| Typical Standby Current for $I_{SB1}$ (mA) | 50 | 40 | 30 | 20 |

## Architecture

The CY7C024/0241 and CY7C025/0251 consist of an array of 4K words of 16/18 bits each and 8K words of 16/18 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a $\overline{BUSY}$ pin is provided on each port. Two interrupt ($\overline{INT}$) pins can be utilized for port-to-port communication. Two semaphore ($\overline{SEM}$) control pins are used for allocating shared resources. With the M/$\overline{S}$ pin, the CY7C024/0241 and CY7C025/0251 can function as a master ($\overline{BUSY}$ pins are outputs) or as a slave ($\overline{BUSY}$ pins are inputs). The CY7C024/0241 and CY7C025/0251 have an automatic power-down feature controlled by $\overline{CE}$. Each port is provided with its own output enable control ($\overline{OE}$), which allows data to be read from the device.

## Functional Description

### Write Operation

Data must be set up for a duration of $t_{SD}$ before the rising edge of R/$\overline{W}$ in order to guarantee a valid write. A write operation is controlled by either the R/$\overline{W}$ pin (see Write Cycle No. 1 waveform) or the $\overline{CE}$ pin (see Write Cycle No. 2 waveform). Required inputs for non-contention operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must occur before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port $t_{DDD}$ after the data is presented on the other port.

### Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available $t_{ACE}$ after $\overline{CE}$ or $t_{DOE}$ after $\overline{OE}$ is asserted. If the user of the CY7C024/0241 or CY7C025/0251 wishes to access a semaphore flag, then the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin, and $\overline{OE}$ must also be asserted.

### Interrupts

The upper two memory locations may be used for message passing. The highest memory location (FFF for the CY7C024/0241, 1FFF for the CY7C025/0251) is the mailbox for the right port and the second-highest memory location (FFE for the CY7C024/0241, 1FFE for the CY7C025/0251) is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner. The interrupt is reset when the owner reads the contents of the mailbox. The message is user defined.

Each port can read the other port's mailbox without resetting the interrupt. The active state of the $\overline{BUSY}$ signal (to a port) prevents the port from setting the interrupt to the winning port. Also, an active $\overline{BUSY}$ to a port prevents that port from reading its own mailbox and thus resetting the interrupt to it.

If your application does not require message passing, do not connect the interrupt pin to the processor's interrupt request input pin.

The operation of the interrupts and their interaction with Busy are summarized in *Table 2*.

### Busy

The CY7C024/0241 and CY7C025/0251 provide on-chip arbitration to resolve simultaneous memory location access (contention). If both ports' $\overline{CE}$s are asserted and an address match occurs within $t_{PS}$ of each other, the busy logic will determine which port has access. If $t_{PS}$ is violated, one port will definitely gain permission to the location, but which one is not predictable. $\overline{BUSY}$ will be asserted $t_{BLA}$ after an address match or $t_{BLC}$ after $\overline{CE}$ is taken LOW.

### Master/Slave

A M/$\overline{S}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. This will allow the device to interface to a master device with no external components. Writing to slave devices must be delayed until after the $\overline{BUSY}$ input has settled ($t_{BLC}$ or $t_{BLA}$). Otherwise, the slave chip may begin a write cycle during a contention situation.When tied HIGH, the M/$\overline{S}$ pin allows the device to be used as a master and, therefore, the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave.

### Semaphore Operation

The CY7C024/0241 and CY7C025/0251 provide eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports.The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for tSOP before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control of the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip select for the semaphore latches ($\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW). A0–2 represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only $I/O_0$ is used. If a zero is written to the left port of an available semaphore, a one will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore will be set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. Table 3 shows sample semaphore operations.

When reading a semaphore, all sixteen/eighteen data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within $t_{SPS}$ of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

**Table 1. Non-Contending Read/Write**

| Inputs | | | | | | Outputs | | |
|---|---|---|---|---|---|---|---|---|
| $\overline{CE}$ | R/$\overline{W}$ | $\overline{OE}$ | $\overline{UB}$ | $\overline{LB}$ | $\overline{SEM}$ | $I/O_0$–$I/O_7$[2] | $I/O_8$–$I/O_{15}$[3] | Operation |
| H | X | X | X | X | H | High Z | High Z | Deselected: Power-Down |
| X | X | X | H | H | H | High Z | High Z | Deselected: Power-Down |
| L | L | X | L | H | H | High Z | Data In | Write to Upper Byte Only |
| L | L | X | H | L | H | Data In | High Z | Write to Lower Byte Only |
| L | L | X | L | L | H | Data In | Data In | Write to Both Bytes |
| L | H | L | L | H | H | High Z | Data Out | Read Upper Byte Only |
| L | H | L | H | L | H | Data Out | High Z | Read Lower Byte Only |
| L | H | L | L | L | H | Data Out | Data Out | Read Both Bytes |
| X | X | H | X | X | X | High Z | High Z | Outputs Disabled |
| H | H | L | X | X | L | Data Out | Data Out | Read Data in Semaphore Flag |
| X | H | L | H | H | L | Data Out | Data Out | Read Data in Semaphore Flag |
| H | ⎍ | X | X | X | L | Data In | Data In | Write $D_{IN0}$ into Semaphore Flag |
| X | ⎍ | X | H | H | L | Data In | Data In | Write $D_{IN0}$ into Semaphore Flag |
| L | X | X | L | X | L | | | Not Allowed |
| L | X | X | X | L | L | | | Not Allowed |

**Table 2. Interrupt Operation Example (Assumes $\overline{BUSY}_L$=$\overline{BUSY}_R$=HIGH)**[6]

| Function | Left Port | | | | | Right Port | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | $R/\overline{W}_L$ | $\overline{CE}_L$ | $\overline{OE}_L$ | $A_{0L-11L}$ | $\overline{INT}_L$ | $R/\overline{W}_R$ | $\overline{CE}_R$ | $\overline{OE}_R$ | $A_{0R-11R}$ | $\overline{INT}_R$ |
| Set Right $\overline{INT}_R$ Flag | L | L | X | (1)FFF | X | X | X | X | X | L[8] |
| Reset Right $\overline{INT}_R$ Flag | X | X | X | X | X | X | L | L | (1)FFF | H[7] |
| Set Left $\overline{INT}_L$ Flag | X | X | X | X | L[7] | L | L | X | (1)FFE | X |
| Reset Left $\overline{INT}_L$ Flag | X | L | L | (1)FFE | H[8] | X | X | X | X | X |

**Table 3. Semaphore Operation Example**

| Function | $I/O_0$–$I/O_{15/17}$ Left | $I/O_0$–$I/O_{15/17}$ Right | Status |
|---|---|---|---|
| No action | 1 | 1 | Semaphore-free |
| Left port writes 0 to semaphore | 0 | 1 | Left Port has semaphore token |
| Right port writes 0 to semaphore | 0 | 1 | No change. Right side has no write access to semaphore. |
| Left port writes 1 to semaphore | 1 | 0 | Right port obtains semaphore token |
| Left port writes 0 to semaphore | 1 | 0 | No change. Left port has no write access to semaphore |
| Right port writes 1 to semaphore | 0 | 1 | Left port obtains semaphore token |
| Left port writes 1 to semaphore | 1 | 1 | Semaphore-free |
| Right port writes 0 to semaphore | 1 | 0 | Right port has semaphore token |
| Right port writes 1 to semaphore | 1 | 1 | Semaphore-free |
| Left port writes 0 to semaphore | 0 | 1 | Left port has semaphore token |
| Left port writes 1 to semaphore | 1 | 1 | Semaphore-free |

**Notes:**
6. $A_{0L-12L}$ and $A_{0R-12R}$, 1FFF/1FFE for the CY7C025.
7. If $\overline{BUSY}_R$=L, then no change.
8. If $\overline{BUSY}_L$=L, then no change.

## Maximum Ratings [9]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential .....–0.3V to +7.0V

DC Voltage Applied to Outputs in High-Z State .....–0.5V to +7.0V

DC Input Voltage[10].....–0.5V to +7.0V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 5V ± 10% |
| Industrial | –40°C to +85°C | 5V ± 10% |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | | 7C024/0241–15 7C025/0251–15 Min. | Typ. | Max. | 7C024/0241–25 7C025/0251–25 Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = –4.0 mA | | 2.4 | | | 2.4 | | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 4.0 mA | | | | 0.4 | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | | 2.2 | | | 2.2 | | | V |
| $V_{IL}$ | Input LOW Voltage | | | –0.7 | | 0.8 | –0.7 | | 0.8 | V |
| $I_{IX}$ | Input Leakage Current | $GND \le V_I \le V_{CC}$ | | –10 | | +10 | –10 | | +10 | µA |
| $I_{OZ}$ | Output Leakage Current | Output Disabled, $GND \le V_O \le V_{CC}$ | | –10 | | +10 | –10 | | +10 | µA |
| $I_{CC}$ | Operating Current | $V_{CC}$ = Max., $I_{OUT}$ = 0 mA, Outputs Disabled | Com'l | | 190 | 300 | | 170 | 250 | mA |
| | | | Ind | | 200 | 320 | | 170 | 290 | |
| $I_{SB1}$ | Standby Current (Both Ports TTL Levels) | $\overline{CE}_L$ and $\overline{CE}_R \ge V_{IH}$, f = $f_{MAX}$[11] | Com'l | | 50 | 70 | | 40 | 60 | mA |
| | | | Ind | | 50 | 70 | | | 75 | |
| $I_{SB2}$ | Standby Current (One Port TTL Level) | $\overline{CE}_L$ or $\overline{CE}_R \ge V_{IH}$, f = $f_{MAX}$[11] | Com'l | | 120 | 180 | | 100 | 150 | mA |
| | | | Ind | | 120 | 180 | | 100 | 170 | |
| $I_{SB3}$ | Standby Current (Both Ports CMOS Levels) | Both Ports $\overline{CE}$ and $\overline{CE}_R \ge$ $V_{CC}$ – 0.2V, $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le$ 0.2V, f = 0[11] | Com'l | | 3 | 15 | | 3 | 15 | mA |
| | | | Ind | | 3 | 15 | | 3 | 15 | |
| $I_{SB4}$ | Standby Current (Both Ports CMOS Levels) | One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ – 0.2V, $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le$ 0.2V, Active Port Outputs, f = $f_{MAX}$[11] | Com'l | | 110 | 160 | | 90 | 130 | mA |
| | | | Ind | | 110 | 160 | | 90 | 150 | |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | 7C024/0241–35 7C025/0251–35 Min. | Typ. | Max. | 7C024/0241–55 7C025/0251–55 Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = –4.0 mA | 2.4 | | | 2.4 | | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 4.0 mA | | | 0.4 | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.2 | | | 2.2 | | | V |
| $V_{IL}$ | Input LOW Voltage | | –0.7 | | 0.8 | –0.7 | | 0.8 | V |
| $I_{IX}$ | Input Leakage Current | $GND \le V_I \le V_{CC}$ | –10 | | +10 | –10 | | +10 | µA |
| $I_{OZ}$ | Output Leakage Current | Output Disabled, $GND \le V_O \le V_{CC}$ | –10 | | +10 | –10 | | +10 | µA |

**Notes:**

9. The voltage on any input or sI/O pin cannot exceed the power pin during power-up
10. Pulse width < 20 ns.
11. $f_{MAX} = 1/t_{RC}$ = All inputs cycling at $f = 1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby $I_{SB3}$.

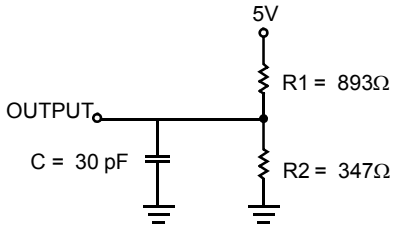
## Electrical Characteristics Over the Operating Range (continued)

| Parameter | Description | Test Conditions | | 7C024/0241–35 7C025/0251–35 | | | 7C024/0241–55 7C025/0251–55 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $I_{CC}$ | Operating Current | $V_{CC}$ = Max., $I_{OUT}$ = 0 mA, Outputs Disabled | Com'l | | 160 | 230 | | 150 | 230 | mA |
| | | | Ind | | 160 | 260 | | 150 | 260 | |
| $I_{SB1}$ | Standby Current (Both Ports TTL Levels) | $\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$, f = $f_{MAX}$[11] | Com'l | | 30 | 50 | | 20 | 50 | mA |
| | | | Ind | | 30 | 65 | | 20 | 65 | |
| $I_{SB2}$ | Standby Current (One Port TTL Level) | $\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$, f = $f_{MAX}$[11] | Com'l | | 85 | 135 | | 75 | 135 | mA |
| | | | Ind | | 85 | 150 | | 75 | 150 | |
| $I_{SB3}$ | Standby Current (Both Ports CMOS Levels) | Both Ports $\overline{CE}$ and $\overline{CE}_R \geq$ $V_{CC}$ – 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V or $V_{IN} \leq$ 0.2V, f = 0[11] | Com'l | | 3 | 15 | | 3 | 15 | mA |
| | | | Ind | | 3 | 15 | | 3 | 15 | |
| $I_{SB4}$ | Standby Current (Both Ports CMOS Levels) | One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ – 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V or $V_{IN} \leq$ 0.2V, Active Port Outputs, f = $f_{MAX}$[11] | Com'l | | 80 | 120 | | 70 | 120 | mA |
| | | | Ind | | 80 | 135 | | 70 | 135 | |

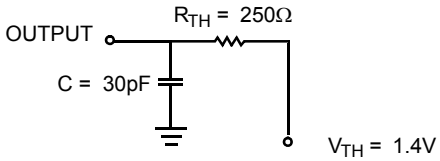
## Capacitance[12]

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25×C, f = 1 MHz, $V_{CC}$ = 5.0V | 10 | pF |
| $C_{OUT}$ | Output Capacitance | | 10 | pF |

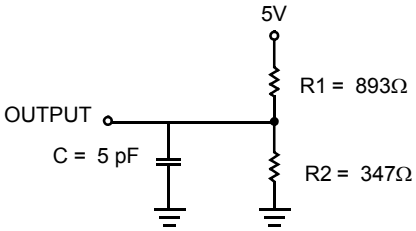
## AC Test Loads and Waveforms



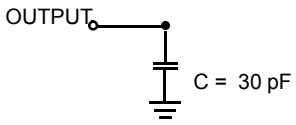

**(a) Normal Load (Load 1)**



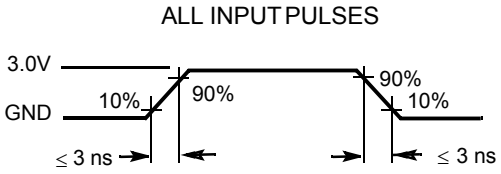

**(b) Thévenin Equivalent (Load 1)**




**(c) Three-State Delay (Load 3)**




**Load (Load 2)**




**Note:**
12. Tested initially and after any design or process changes that may affect these parameters.

## Switching Characteristics Over the Operating Range [13]

| Parameter | Description | 7C024/0241–15 7C025/0251–15 | | 7C024/0241–25 7C025/0251–25 | | 7C024/0241–35 7C025/0251–35 | | 7C024/0241–55 7C025/0251–55 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Read Cycle** | | | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 15 | | 25 | | 35 | | 55 | | ns |
| $t_{AA}$ | Address to Data Valid | | 15 | | 25 | | 35 | | 55 | ns |
| $t_{OHA}$ | Output Hold From Address Change | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{ACE}$[14] | $\overline{CE}$ LOW to Data Valid | | 15 | | 25 | | 35 | | 55 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 10 | | 13 | | 20 | | 25 | ns |
| $t_{LZOE}$[15, 16, 17] | $\overline{OE}$ Low to Low Z | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{HZOE}$[15, 16, 17] | $\overline{OE}$ HIGH to High Z | | 10 | | 15 | | 20 | | 25 | ns |
| $t_{LZCE}$[15, 16, 17] | $\overline{CE}$ LOW to Low Z | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{HZCE}$[15, 16, 17] | $\overline{CE}$ HIGH to High Z | | 10 | | 15 | | 20 | | 25 | ns |
| $t_{PU}$[17] | $\overline{CE}$ LOW to Power-Up | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{PD}$[17] | $\overline{CE}$ HIGH to Power-Down | | 15 | | 25 | | 25 | | 55 | ns |
| $t_{ABE}$[14] | Byte Enable Access Time | | 15 | | 25 | | 35 | | 55 | ns |
| **Write Cycle** | | | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 15 | | 25 | | 35 | | 55 | | ns |
| $t_{SCE}$[14] | $\overline{CE}$ LOW to Write End | 12 | | 20 | | 30 | | 35 | | ns |
| $t_{AW}$ | Address Set-Up to Write End | 12 | | 20 | | 30 | | 35 | | ns |
| $t_{HA}$ | Address Hold From Write End | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{SA}$[14] | Address Set-up to Write Start | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{PWE}$ | Write Pulse Width | 12 | | 20 | | 25 | | 35 | | ns |
| $t_{SD}$ | Data Set-Up to Write End | 10 | | 15 | | 15 | | 20 | | ns |
| $t_{HD}$ | Data Hold From Write End | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{HZWE}$[16, 17] | R/$\overline{W}$ LOW to High Z | | 10 | | 15 | | 20 | | 25 | ns |
| $t_{LZWE}$[16, 17] | R/$\overline{W}$ HIGH to Low Z | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{WDD}$[18] | Write Pulse to Data Delay | | 30 | | 50 | | 60 | | 70 | ns |
| $t_{DDD}$[18] | Write Data Valid to Read Data Valid | | 25 | | 35 | | 35 | | 45 | ns |

**Notes:**
13. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified $I_{OL}/I_{OH}$ and 30-pF load capacitance.
14. To access RAM, $\overline{CE}$=L, $\overline{UB}$=L, $\overline{SEM}$=H. To access semaphore, $\overline{CE}$=H and $\overline{SEM}$=L. Either condition must be valid for the entire $t_{SCE}$ time.
15. At any given temperature and voltage condition for any given device, $t_{HZCE}$ is less than $t_{LZCE}$ and $t_{HZOE}$ is less than $t_{LZOE}$.
16. Test conditions used are Load 3.
17. This parameter is guaranteed but not tested.
18. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform.

**Switching Characteristics** Over the Operating Range (continued)[13]

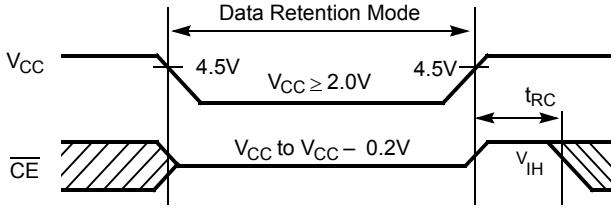
| Parameter | Description | 7C024/0241–15 7C025/0251–15 | | 7C024/0241–25 7C025/0251–25 | | 7C024/0241–35 7C025/0251–35 | | 7C024/0241–55 7C025/0251–55 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Busy Timing**[19] | | | | | | | | | | |
| $t_{BLA}$ | $\overline{BUSY}$ LOW from Address Match | | 15 | | 20 | | 20 | | 45 | ns |
| $t_{BHA}$ | $\overline{BUSY}$ HIGH from Address Mismatch | | 15 | | 20 | | 20 | | 40 | ns |
| $t_{BLC}$ | $\overline{BUSY}$ LOW from $\overline{CE}$ LOW | | 15 | | 20 | | 20 | | 40 | ns |
| $t_{BHC}$ | $\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH | | 15 | | 20 | | 20 | | 35 | ns |
| $t_{PS}$ | Port Set-up for Priority | 5 | | 5 | | 5 | | 5 | | ns |
| $t_{WB}$ | R/$\overline{W}$ HIGH after $\overline{BUSY}$ (Slave) | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{WH}$ | R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH (Slave) | 13 | | 20 | | 30 | | 40 | | ns |
| $t_{BDD}$[20] | $\overline{BUSY}$ HIGH to Data Valid | | Note 20 | | Note 20 | | Note 20 | | Note 20 | ns |
| **Interrupt Timing**[19] | | | | | | | | | | |
| $t_{INS}$ | $\overline{INT}$ Set Time | | 15 | | 20 | | 25 | | 30 | ns |
| $t_{INR}$ | $\overline{INT}$ Reset Time | | 15 | | 20 | | 25 | | 30 | ns |
| **Semaphore Timing** | | | | | | | | | | |
| $t_{SOP}$ | $\overline{SEM}$ Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$) | 10 | | 12 | | 15 | | 20 | | ns |
| $t_{SWRD}$ | SEM Flag Write to Read Time | 5 | | 10 | | 10 | | 15 | | ns |
| $t_{SPS}$ | SEM Flag Contention Window | 5 | | 10 | | 10 | | 15 | | ns |
| $t_{SAA}$ | SEM Address Access Time | | 15 | | 25 | | 35 | | 55 | ns |

## Data Retention Mode

The CY7C024/0241 is designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip enable ($\overline{CE}$) must be held HIGH during data retention, within $V_{CC}$ to $V_{CC}$ – 0.2V.
2. $\overline{CE}$ must be kept between $V_{CC}$ – 0.2V and 70% of $V_{CC}$ during the power-up and power-down transitions.
3. The RAM can begin operation >$t_{RC}$ after $V_{CC}$ reaches the minimum operating voltage (4.5V).

## Timing



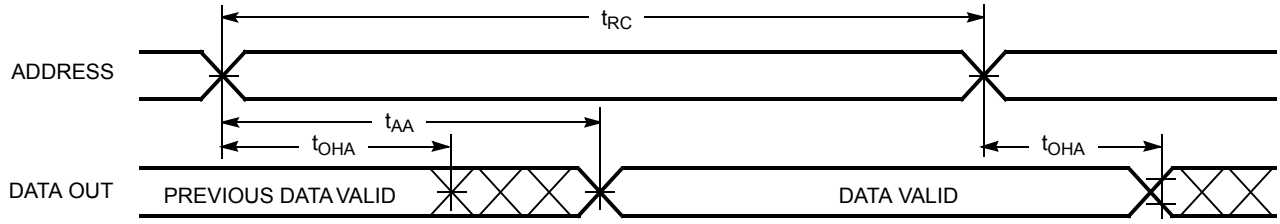

| Parameter | Test Conditions[21] | Max. | Unit |
|---|---|---|---|
| $ICC_{DR1}$ | @ $VCC_{DR}$ = 2V | 1.5 | mA |

**Notes:**

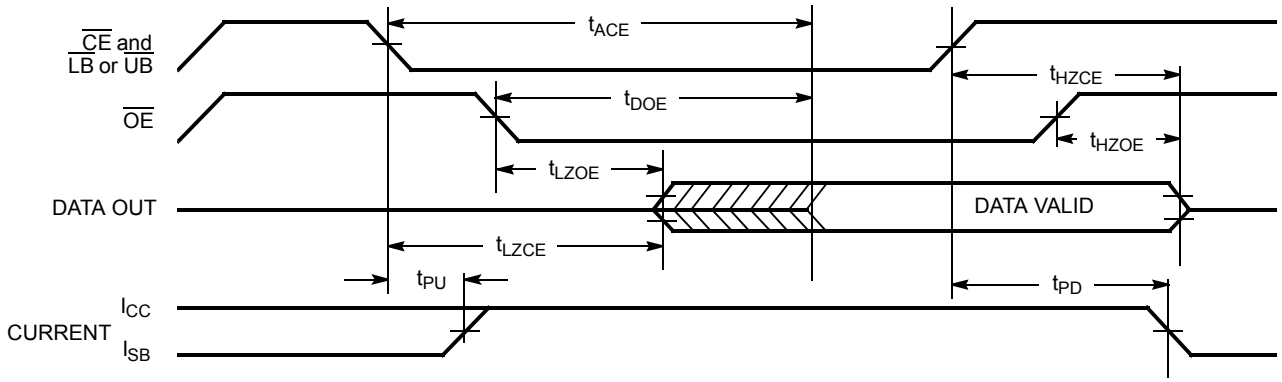
19. Test conditions used are Load 2.
20. $t_{BDD}$ is a calculated parameter and is the greater of $t_{WDD}$– $t_{PWE}$ (actual) or $t_{DDD}$– $t_{SD}$ (actual).
21. $\overline{CE}$ = $V_{CC}$, $V_{in}$ = GND to $V_{CC}$, $T_A$ = 25°C. This parameter is guaranteed but not tested.

## Switching Waveforms

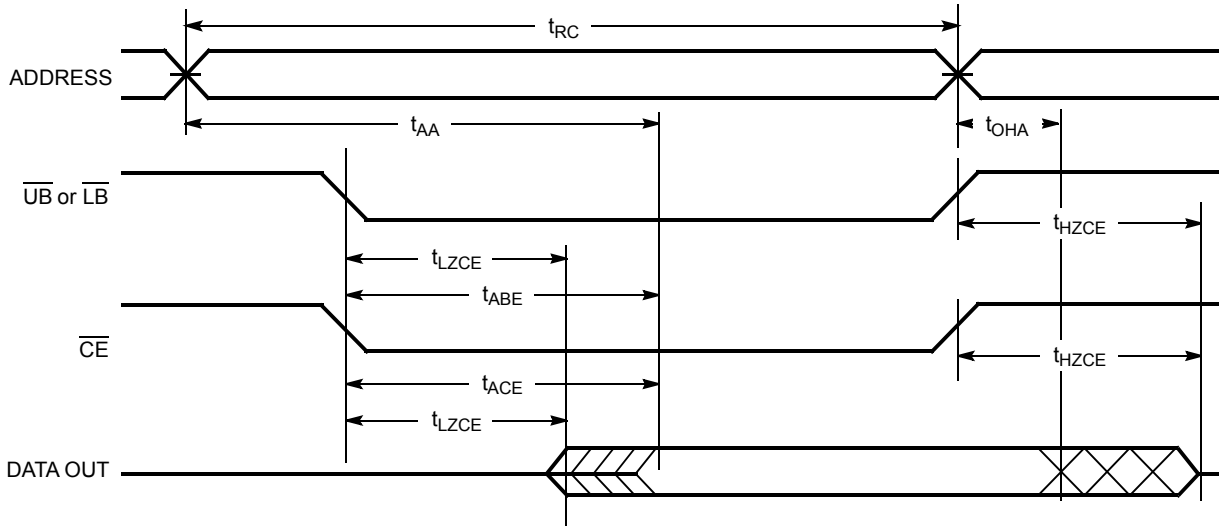
**Read Cycle No. 1 (Either Port Address Access)**[22, 23, 24]




**Read Cycle No. 2 (Either Port $\overline{CE}$/$\overline{OE}$ Access)**[22, 25, 26]



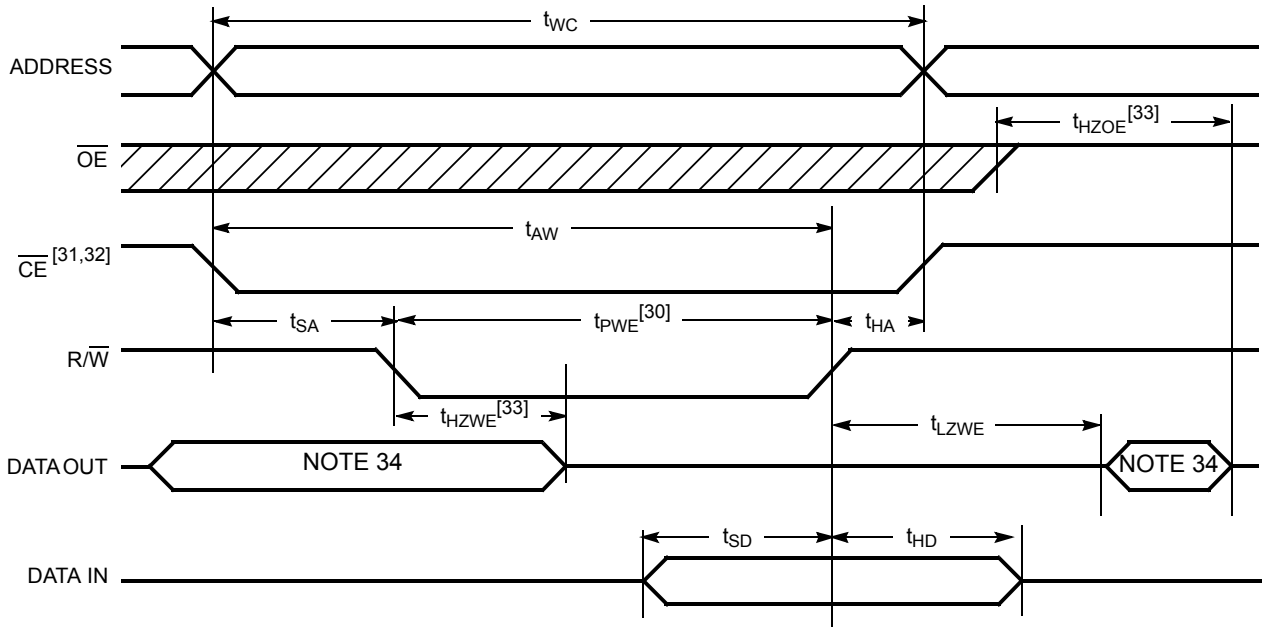

**Read Cycle No. 3 (Either Port)**[22, 24, 25, 25, 26]



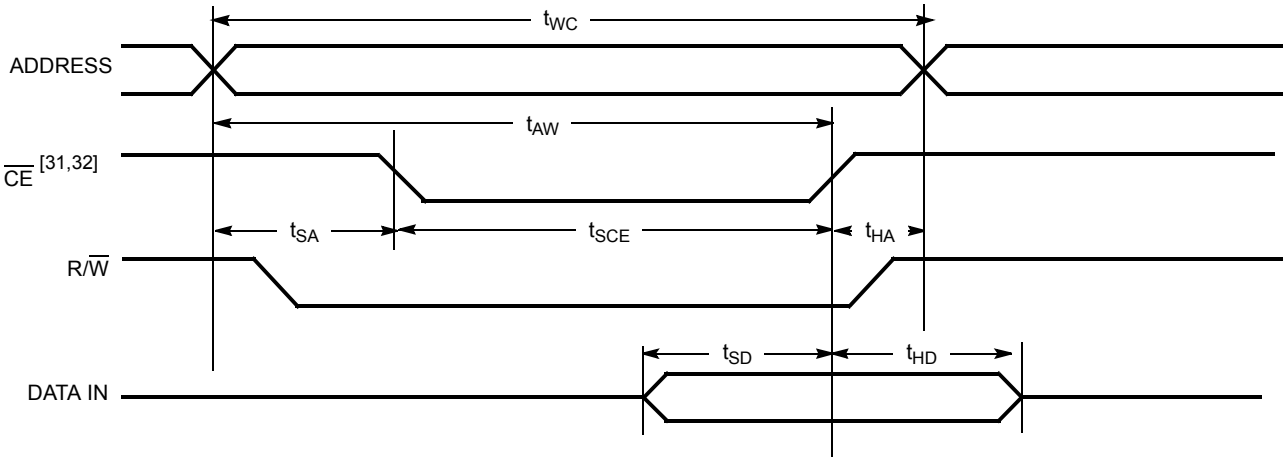

**Notes:**
22. R/$\overline{W}$ is HIGH for read cycles
23. Device is continuously selected $\overline{CE}$ = $V_{IL}$ and $\overline{UB}$ or $\overline{LB}$ = $V_{IL}$. This waveform cannot be used for semaphore reads.
24. $\overline{OE}$ = $V_{IL}$.
25. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
26. To access RAM, $\overline{CE}$ = $V_{IL}$, $\overline{UB}$ or $\overline{LB}$ = $V_{IL}$, $\overline{SEM}$ = $V_{IH}$. To access semaphore, $\overline{CE}$ = $V_{IH}$, $\overline{SEM}$ = $V_{IL}$.

## Switching Waveforms (continued)

### Write Cycle No. 1: R/$\overline{W}$ Controlled Timing[27, 28, 29, 30]



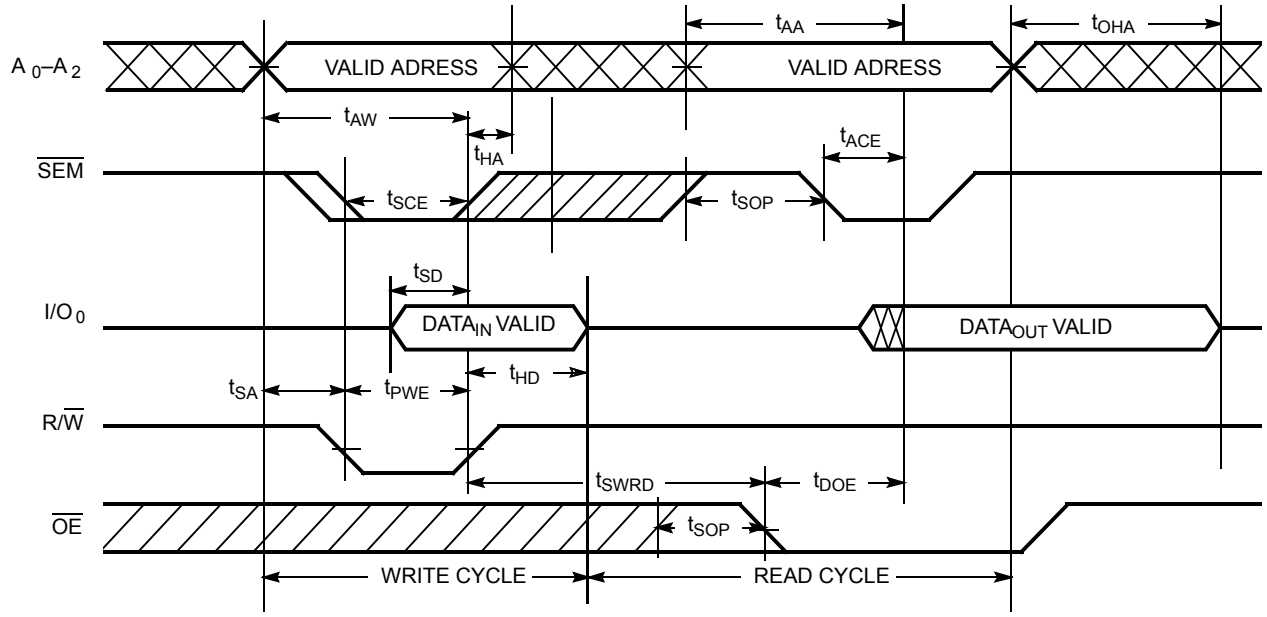

### Write Cycle No. 2: $\overline{CE}$ Controlled Timing[27, 28, 29, 35]



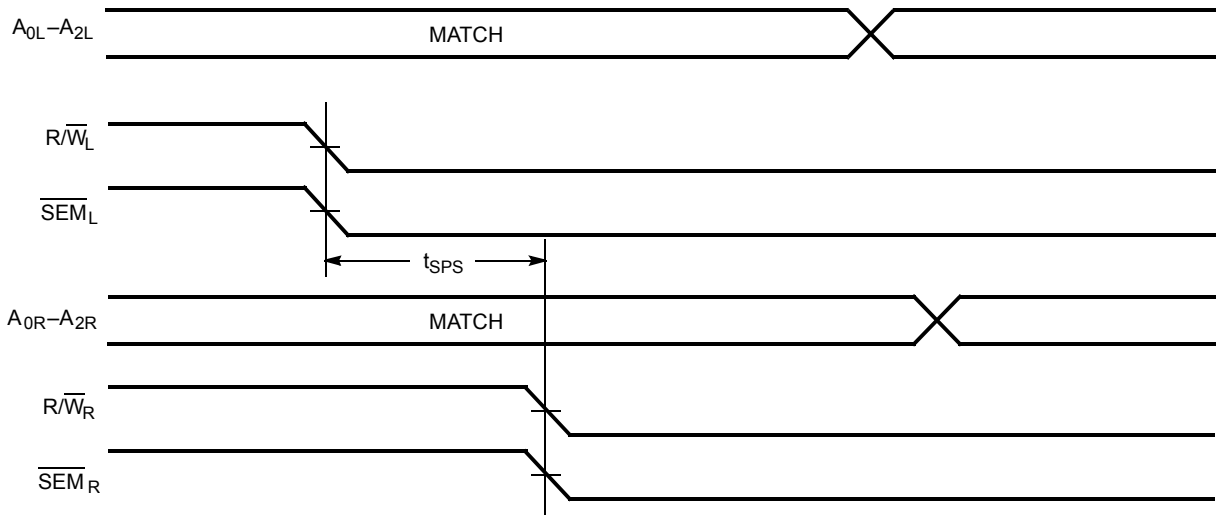

**Notes:**
27. R/$\overline{W}$ must be HIGH during all address transitions.
28. A write occurs during the overlap ($t_{SCE}$ or $t_{PWE}$) of a LOW $\overline{CE}$ or $\overline{SEM}$ and a LOW $\overline{UB}$ or $\overline{LB}$.
29. $t_{HA}$ is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ or ($\overline{SEM}$ or R/$\overline{W}$) going HIGH at the end of write cycle.
30. If $\overline{OE}$ is LOW during a R/$\overline{W}$-controlled write cycle, the write pulse width must be the larger of $t_{PWE}$ or ($t_{HZWE}$ + $t_{SD}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required $t_{SD}$. If $\overline{OE}$ is HIGH during an R/$\overline{W}$-controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified $t_{PWE}$.
31. To access RAM, $\overline{CE}$ = $V_{IL}$, $\overline{SEM}$ = $V_{IH}$.
32. To access upper byte, $\overline{CE}$ = $V_{IL}$, $\overline{UB}$ = $V_{IL}$, $\overline{SEM}$ = $V_{IH}$.
To access lower byte, $\overline{CE}$ = $V_{IL}$, $\overline{LB}$ = $V_{IL}$, $\overline{SEM}$ = $V_{IH}$.
33. Transition is measured ±500 mV from steady state with a 5-pF load (including scope and jig). This parameter is sampled and not 100% tested.
34. During this period, the I/O pins are in the output state, and input signals must not be applied.
35. If the $\overline{CE}$ or $\overline{SEM}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.

## Switching Waveforms (continued)

### Semaphore Read After Write Timing, Either Side[36]



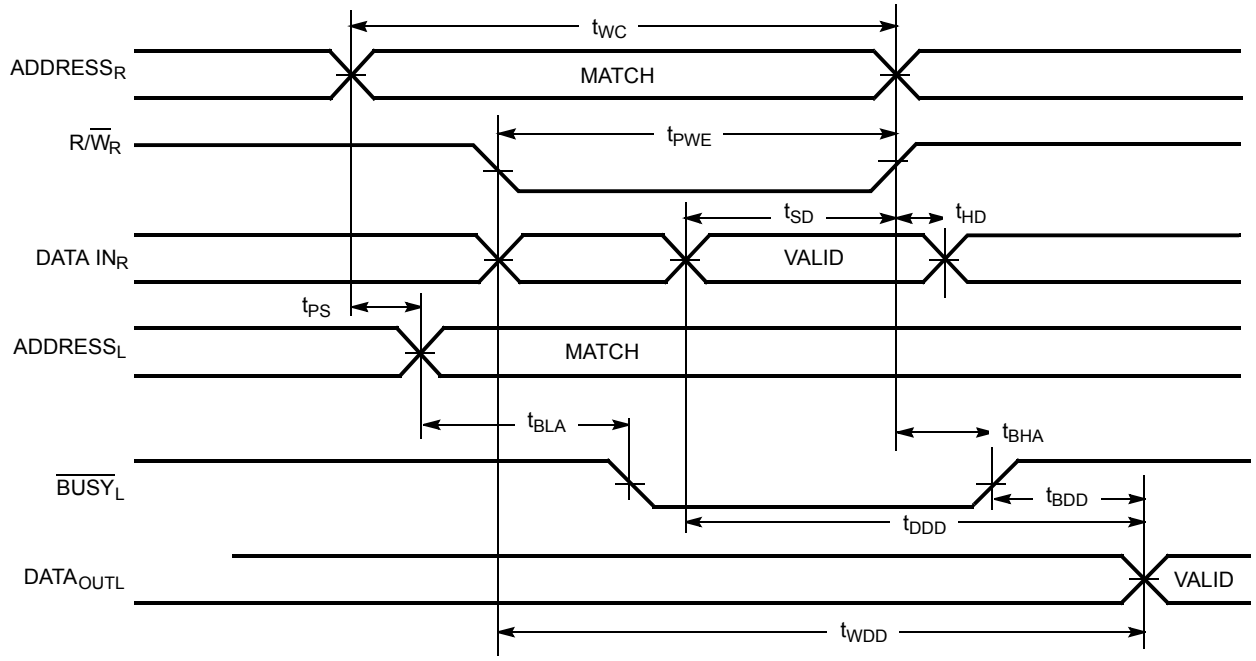

### Timing Diagram of Semaphore Contention[37, 38, 39]



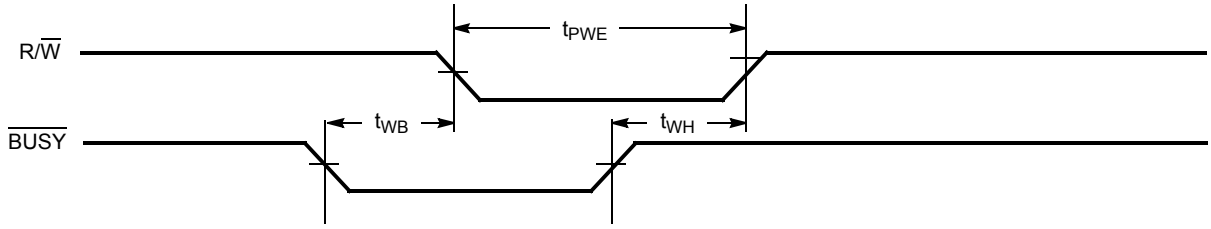

**Notes:**
36. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
37. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH.
38. Semaphores are reset (available to both ports) at cycle start.
39. If $t_{SPS}$ is violated, the semaphore will definitely be obtained by one side or the other, but which side will get the semaphore is unpredictable.

## Switching Waveforms (continued)

**Timing Diagram of Read with $\overline{BUSY}$ (M/$\overline{S}$=HIGH)**[40]



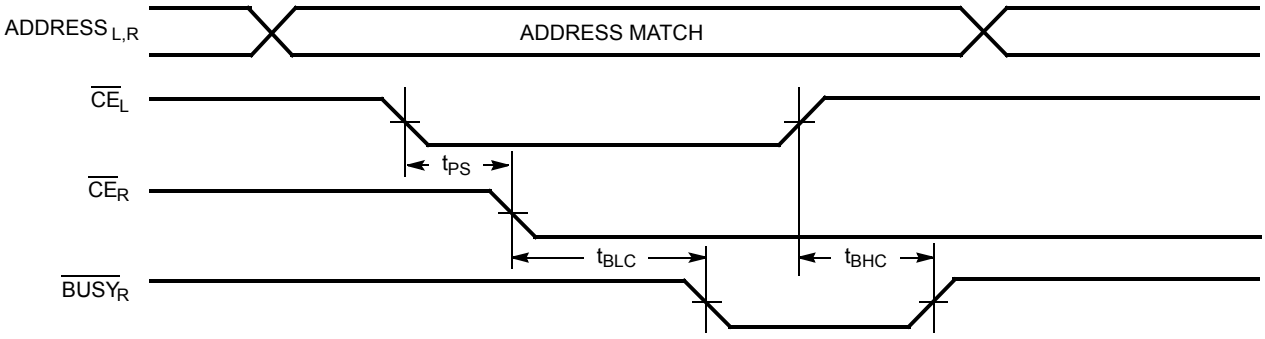

**Write Timing with Busy Input (M/$\overline{S}$=LOW)**



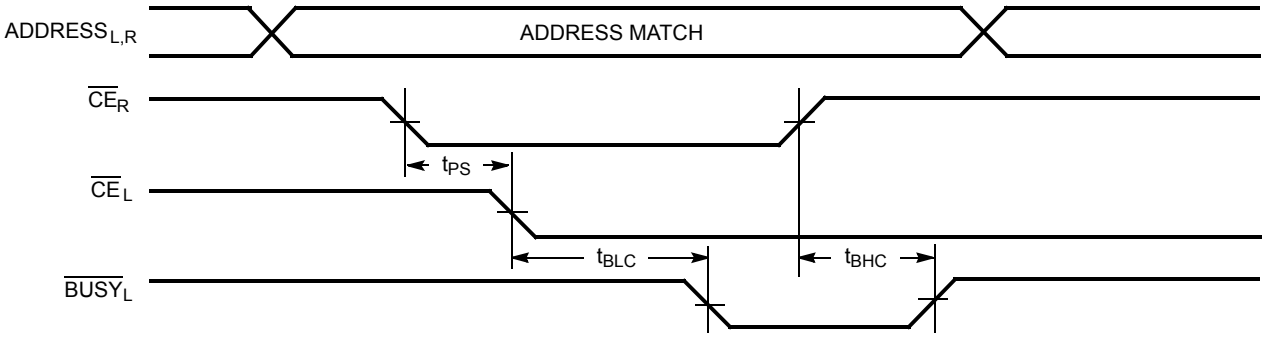

**Note:**
40. $\overline{CE}_L$ = $\overline{CE}_R$ = LOW.

## Switching Waveforms (continued)

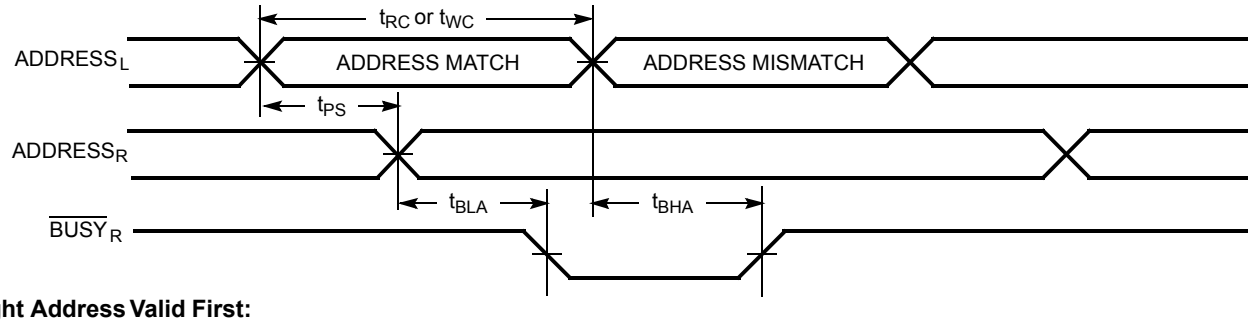
**Busy Timing Diagram No.1 ($\overline{CE}$ Arbitration)**[41]
**$CE_L$ Valid First:**



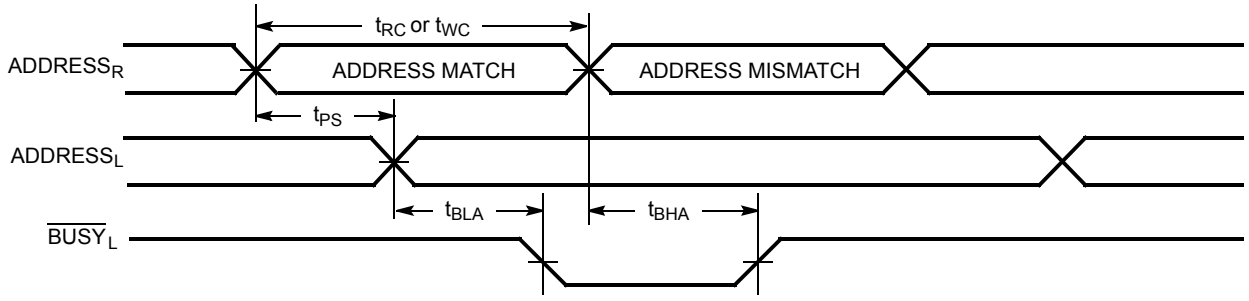

**$CE_R$ Valid First:**




**Busy Timing Diagram No.2 (Address Arbitration)**[41]
**Left Address Valid First**




**Right Address Valid First:**

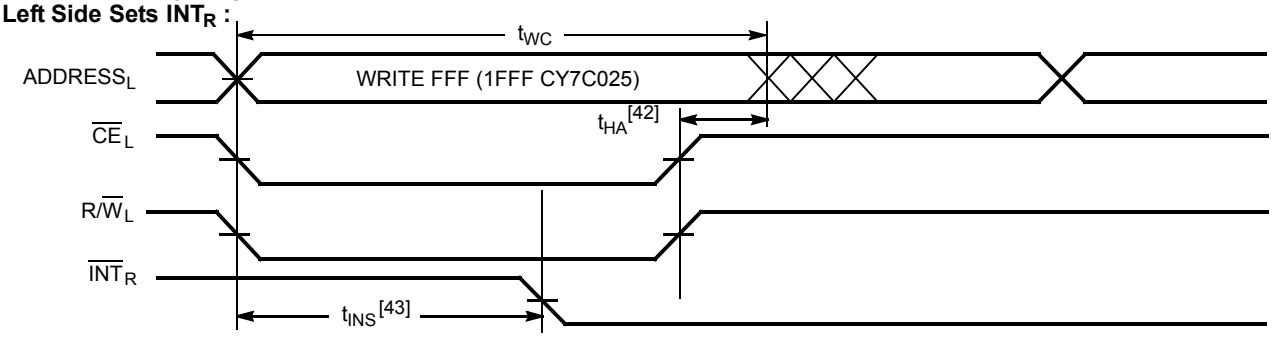



**Note:**
41. If $t_{PS}$ is violated, the busy signal will be asserted on one side or the other, but there is no guarantee to which side $\overline{BUSY}$ will be asserted.

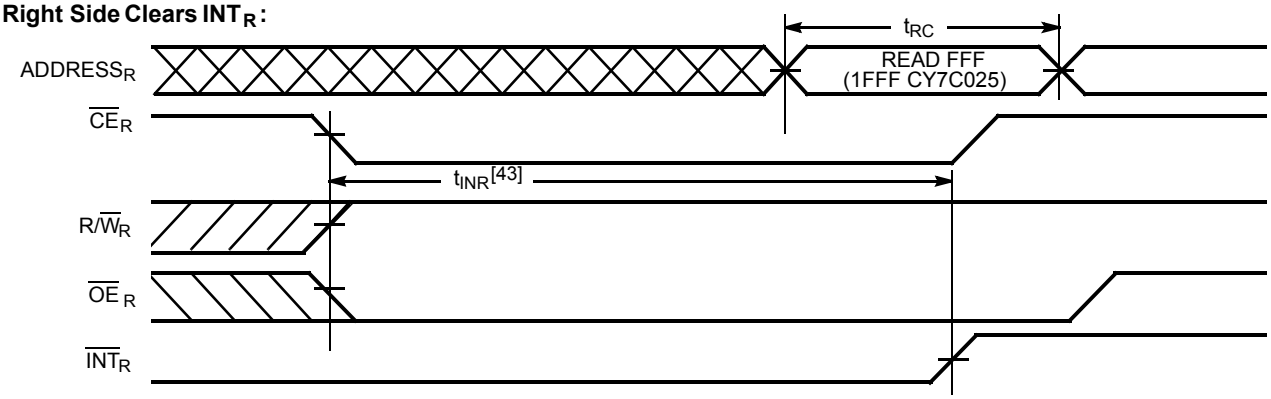
## Switching Waveforms (continued)

### Interrupt Timing Diagrams

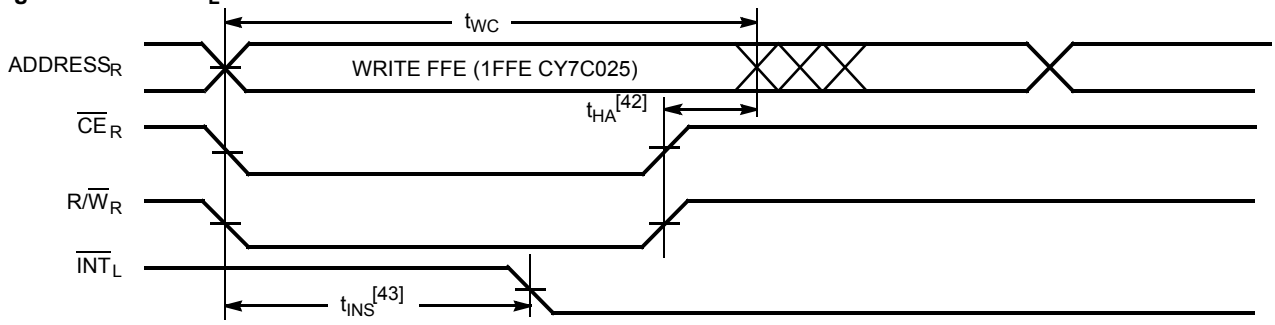
**Left Side Sets $\overline{INT}_R$ :**



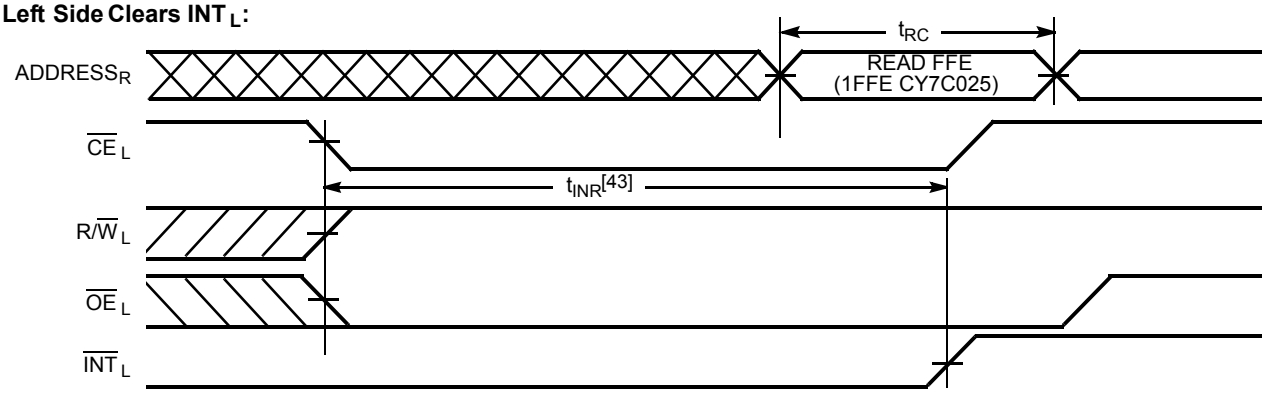

**Right Side Clears $\overline{INT}_R$:**




**Right Side Sets $\overline{INT}_L$:**




**Left Side Clears $\overline{INT}_L$:**




**Notes:**
42. $t_{HA}$ depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is deasserted first.
43. $t_{INS}$ or $t_{INR}$ depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is asserted last.

## Ordering Information (4K x16 Dual-Port SRAM)

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 15 | CY7C024–15AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| | CY7C024-15AXC | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| | CY7C024–15JC | J83 | 84-Lead Plastic Leaded Chip Carrier | |
| | CY7C024-15JXC | J83 | 84-Lead Lead Free Plastic Leaded Chip Carrier | |
| 25 | CY7C024–25AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| | CY7C024-25AXC | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| | CY7C024–25JC | J83 | 84-Lead Plastic Leaded Chip Carrier | |
| | CY7C024-25JXC | J83 | 84-Lead Lead Free Plastic Leaded Chip Carrier | |
| | CY7C024–25AI | A100 | 100-Pin Thin Quad Flat Pack | Industrial |
| | CY7C024-25AXI | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| | CY7C024–25JI | J83 | 84-Lead Plastic Leaded Chip Carrier | |
| | CY7C024-25JXI | J83 | 84-Lead Lead Free Plastic Leaded Chip Carrier | |
| 35 | CY7C024–35AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| | CY7C024-35AXC | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| | CY7C024–35JC | J83 | 84-Lead Plastic Leaded Chip Carrier | |
| | CY7C024-35JXC | J83 | 84-Lead Lead Free Plastic Leaded Chip Carrier | |
| | CY7C024–35AI | A100 | 100-Pin Thin Quad Flat Pack | Industrial |
| | CY7C024-35AXI | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| | CY7C024–35JI | J83 | 84-Lead Plastic Leaded Chip Carrier | |
| | CY7C024-35JXI | J83 | 84-Lead Lead Free Plastic Leaded Chip Carrier | |
| 55 | CY7C024–55AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| | CY7C024-55AXC | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| | CY7C024–55JC | J83 | 84-Lead Plastic Leaded Chip Carrier | |
| | CY7C024-55JXC | J83 | 84-Lead Lead Free Plastic Leaded Chip Carrier | |
| | CY7C024–55AI | A100 | 100-Pin Thin Quad Flat Pack | Industrial |
| | CY7C024-55AXI | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| | CY7C024–55JI | J83 | 84-Lead Plastic Leaded Chip Carrier | |
| | CY7C024-55JXI | J83 | 84-Lead Lead Free Plastic Leaded Chip Carrier | |

## Ordering Information (8K x 16 Dual-Port SRAM)

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 15 | CY7C025–15AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| | CY7C025-15AXC | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| | CY7C025–15JC | J83 | 84-Lead Plastic Leaded Chip Carrier | |
| | CY7C025-15JXC | J83 | 84-Lead Lead Free Plastic Leaded Chip Carrier | |
| | CY7C025–15AI | A100 | 100-Pin Thin Quad Flat Pack | Industrial |
| | CY7C025-15AXI | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |

## Ordering Information (8K x 16 Dual-Port SRAM) (continued)

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 25 | CY7C025–25AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| | CY7C025-25AXC | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| | CY7C025–25JC | J83 | 84-Lead Plastic Leaded Chip Carrier | |
| | CY7C025-25JXC | J83 | 84-Lead Lead Free Plastic Leaded Chip Carrier | |
| | CY7C025–25AI | A100 | 100-Pin Thin Quad Flat Pack | Industrial |
| | CY7C025-25AXI | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| | CY7C025–25JI | J83 | 84-Lead Plastic Leaded Chip Carrier | |
| | CY7C025-25JXI | J83 | 84-Lead Lead Free Plastic Leaded Chip Carrier | |
| 35 | CY7C025–35AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| | CY7C025-35AXC | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| | CY7C025–35JC | J83 | 84-Lead Plastic Leaded Chip Carrier | |
| | CY7C025-35JXC | J83 | 84-Lead Lead Free Plastic Leaded Chip Carrier | |
| | CY7C025–35AI | A100 | 100-Pin Thin Quad Flat Pack | Industrial |
| | CY7C025-35AXI | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| | CY7C025–35JI | J83 | 84-Lead Plastic Leaded Chip Carrier | |
| | CY7C025-35JXI | J83 | 84-Lead Lead Free Plastic Leaded Chip Carrier | |
| 55 | CY7C025–55AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| | CY7C025-55AXC | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| | CY7C025–55JC | J83 | 84-Lead Plastic Leaded Chip Carrier | |
| | CY7C025-55JXC | J83 | 84-Lead Lead Free Plastic Leaded Chip Carrier | |
| | CY7C025–55AI | A100 | 100-Pin Thin Quad Flat Pack | Industrial |
| | CY7C025-55AXI | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| | CY7C025–55JI | J83 | 84-Lead Plastic Leaded Chip Carrier | |
| | CY7C025-55JXI | J83 | 84-Lead Lead Free Plastic Leaded Chip Carrier | |

## Ordering Information (4K x 18 Dual-Port SRAM)

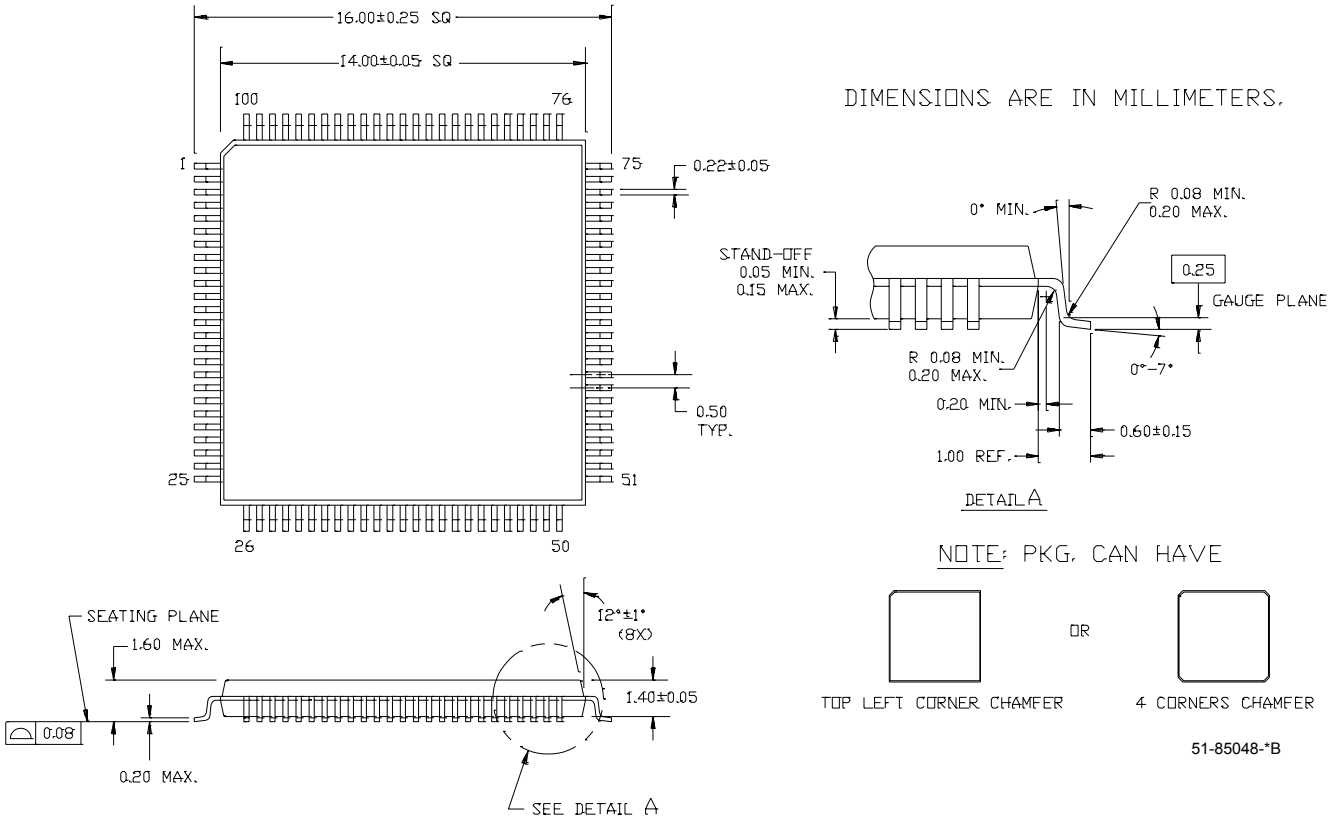
| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 15 | CY7C0241–15AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| | CY7C0241-15AXC | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| | CY7C0241–15AI | A100 | 100-Pin Thin Quad Flat Pack | Industrial |
| | CY7C0241-15AXI | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| 25 | CY7C0241–25AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| | CY7C0241-25AXC | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| | CY7C0241–25AI | A100 | 100-Pin Thin Quad Flat Pack | Industrial |
| | CY7C0241-25AXI | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| 35 | CY7C0241–35AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| | CY7C0241-35AXC | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| | CY7C0241–35AI | A100 | 100-Pin Thin Quad Flat Pack | Industrial |
| | CY7C0241-35AXI | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| 55 | CY7C0241–55AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| | CY7C0241-55AXC | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| | CY7C0241–55AI | A100 | 100-Pin Thin Quad Flat Pack | Industrial |
| | CY7C0241-55AXI | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |

## 8K x 18 Dual-Port SRAM

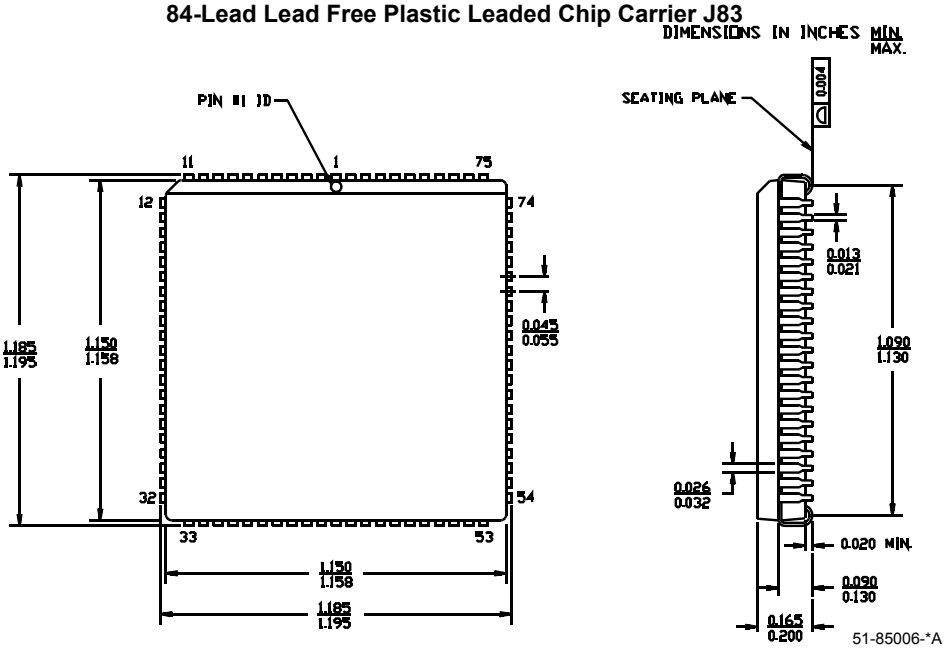
| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 15 | CY7C0251–15AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| | CY7C0251–15AXC | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| 25 | CY7C0251–25AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| | CY7C0251-25AXC | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| | CY7C0251–25AI | A100 | 100-Pin Thin Quad Flat Pack | Industrial |
| | CY7C0251–25AXI | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| 35 | CY7C0251–35AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| | CY7C0251–35AXC | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| | CY7C0251–35AI | A100 | 100-Pin Thin Quad Flat Pack | Industrial |
| | CY7C0251–35AXI | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| 55 | CY7C0251–55AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| | CY7C0251–55AXC | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |
| | CY7C0251–55AI | A100 | 100-Pin Thin Quad Flat Pack | Industrial |
| | CY7C0251–55AXI | A100 | 100-Pin Lead Free Thin Quad Flat Pack | |

## Package Diagrams

**100-Pin Lead (Pb)-Free Thin Plastic Quad Flat Pack (TQFP) A100**




**84-Lead Lead Free Plastic Leaded Chip Carrier J83**




All product and company names mentioned in this document are trademarks of their respective holders.



© Cypress Semiconductor Corporation, 2004. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

## Document History Page

| Document Title: CY7C024/0241, CY7C025/0251 4K x 16/18 and 8K x 16/18 Dual-Port Static RAM with Sem, Int, Busy<br>Document Number: 38-06035 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 110177 | 09/29/01 | SZV | Change from Spec number: 38-00255 to 38-06035 |
| *A | 122286 | 12/27/02 | RBI | Power-up requirements added to Maximum Ratings Information |
| *B | 236754 | See ECN | YDT | Removed cross information from features section |
| *C | 279132 | See ECN | RUY | Added Lead (Pb)-Free packaging information |