

128K x 8 Static RAM

Features

- 4.5V – 5.5V operation
- CMOS for optimum speed/power
- Low active power (70 ns, LL version)
— 330 mW (max.) (60 mA)
- Low standby power (70 ns, LL version)
— 110 μ W (max.) (20 μ A)
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with $\overline{CE}_1$, CE_2 , and $\overline{OE}$ options

Functional Description

The CY62128 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), an active LOW output enable ($\overline{OE}$), and three-state drivers. This device has an automatic power-down

feature that reduces power consumption by more than 75% when deselected.

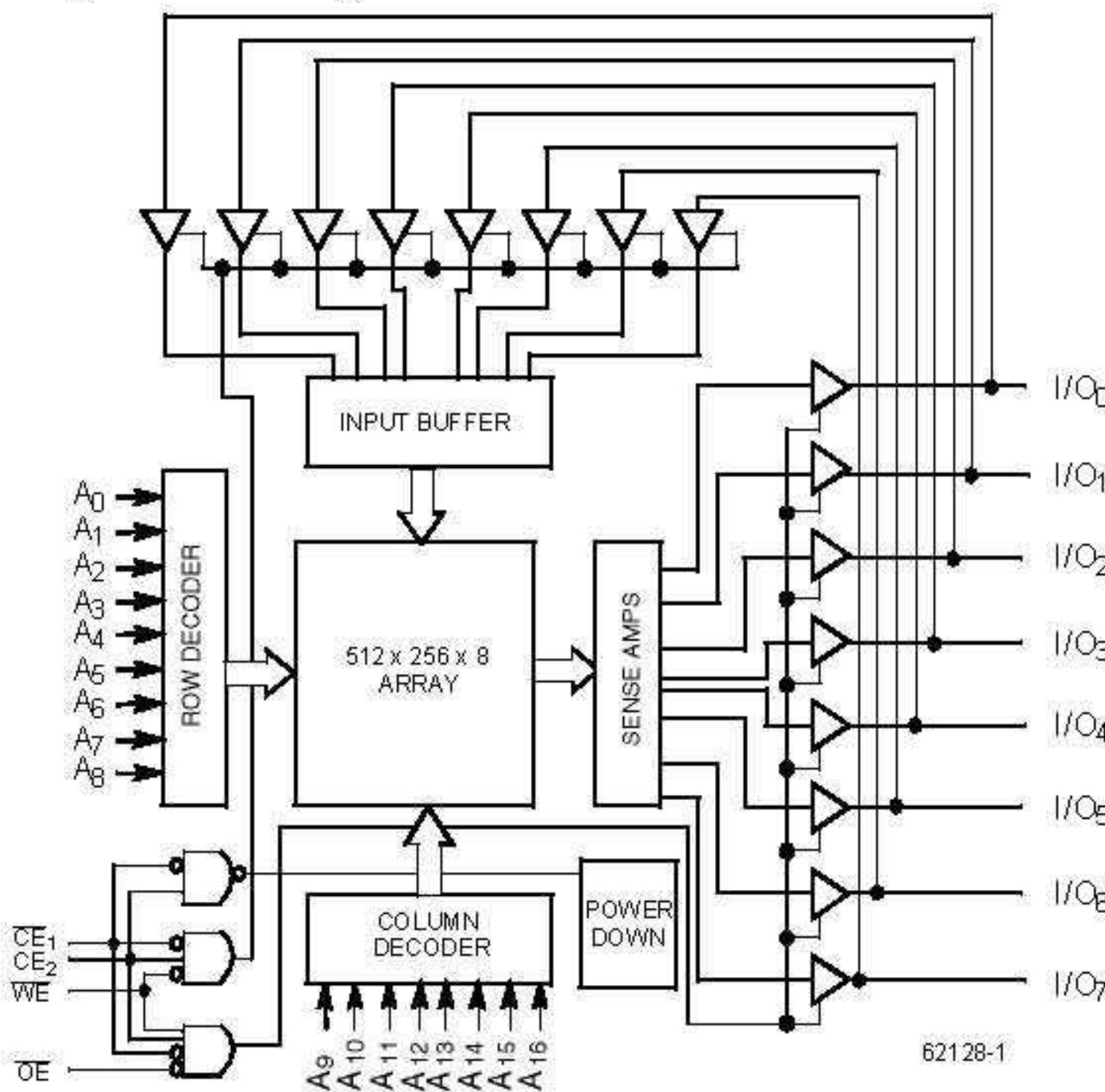
Writing to the device is accomplished by taking chip enable one ($\overline{CE}_1$) and write enable ($\overline{WE}$) inputs LOW and chip enable two (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking chip enable one ($\overline{CE}_1$) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) and chip enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

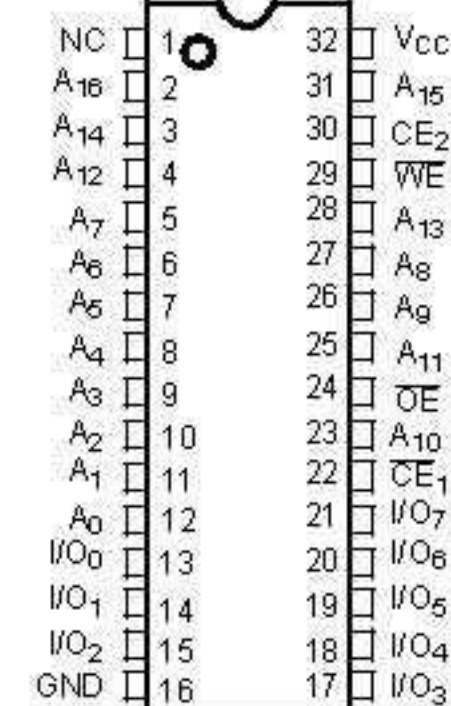
The CY62128 is available in a standard 400-mil-wide SOJ, 525-mil wide (450-mil-wide body width) SOIC and 32-pin TSOP type I.

Logic Block Diagram

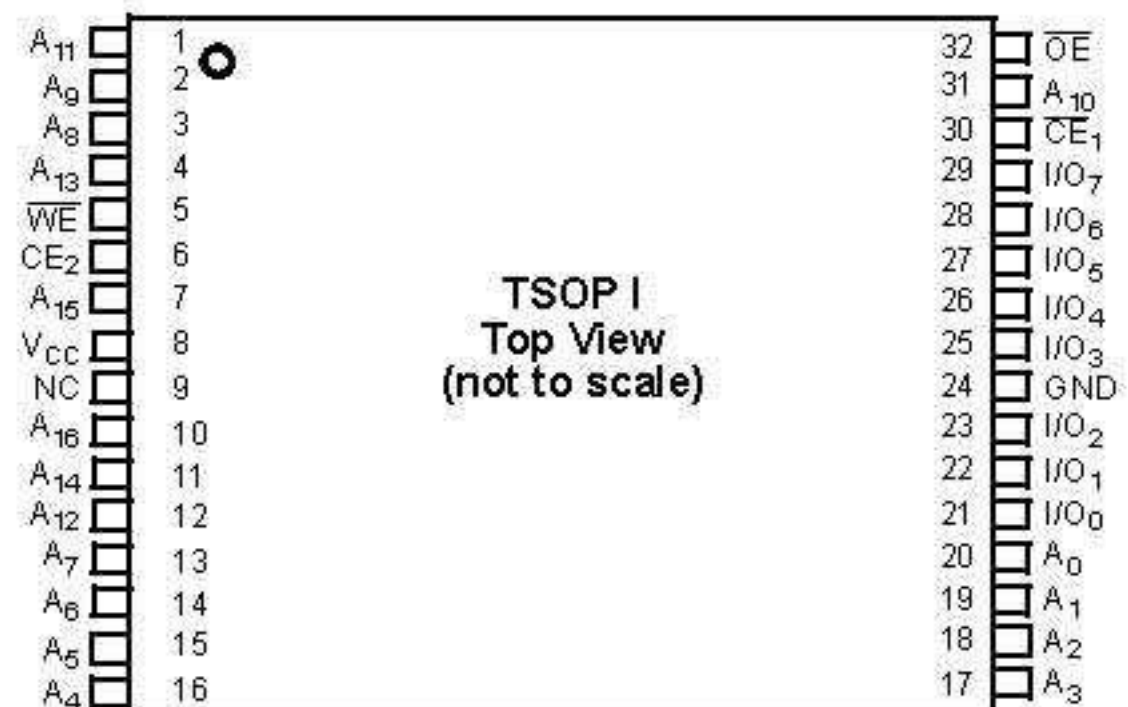


Pin Configurations

Top View SOJ / SOIC



TSOP I Top View (not to scale)



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Selection Guide

			CY62128–55	CY62128–70
Maximum Access Time (ns)			55	70
Maximum Operating Current	Commercial		115 mA	110 mA
		L	70 mA	60 mA
		LL	70 mA	60 mA
Maximum CMOS Standby Current	Commercial		10 mA	10 mA
		L	100 μ A	100 μ A
		LL	20 μ A	20 μ A

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature –65°C to +150°C

Ambient Temperature with
Power Applied –55°C to +125°C

Supply Voltage on V_{CC} to Relative GND^[1] –0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State^[1] –0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[1] –0.5V to $V_{CC} + 0.5V$

Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature ^[2]	V_{CC}
Commercial	0°C to +70°C	5V $\pm$ 10%

Electrical Characteristics Over the Operating Range^[3]

Parameter	Description	Test Conditions	62128–55		62128–70		Unit	
			Min.	Max.	Min.	Max.		
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = – 1.0 mA	2.4		2.4		V	
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 2.1mA		0.4		0.4	V	
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	V	
V _{IL}	Input LOW Voltage ^[1]		–0.3	0.8	–0.3	0.8	V	
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	–1	+1	–1	+1	μA	
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	–5	+5	–5	+5	μA	
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		–300		–300	mA	
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Com'l		115		110	mA
			L		70		60	mA
			LL		70		60	mA
I _{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V _{CC} , $\overline{CE}_1 \geq V_{IH}$ or $\overline{CE}_2 \leq V_{IL}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	Com'l		25		25	mA
			L		10		10	mA
			LL		2		2	mA
I _{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V _{CC} , $\overline{CE}_1 \geq V_{CC} - 0.3V$, or $\overline{CE}_2 \leq 0.3V$, V _{IN} ≥ V _{CC} – 0.3V, or V _{IN} ≤ 0.3V, f=0	Com'l		10		10	mA
			L		100		100	μA
			LL		20		20	μA

Shaded areas contain advance information

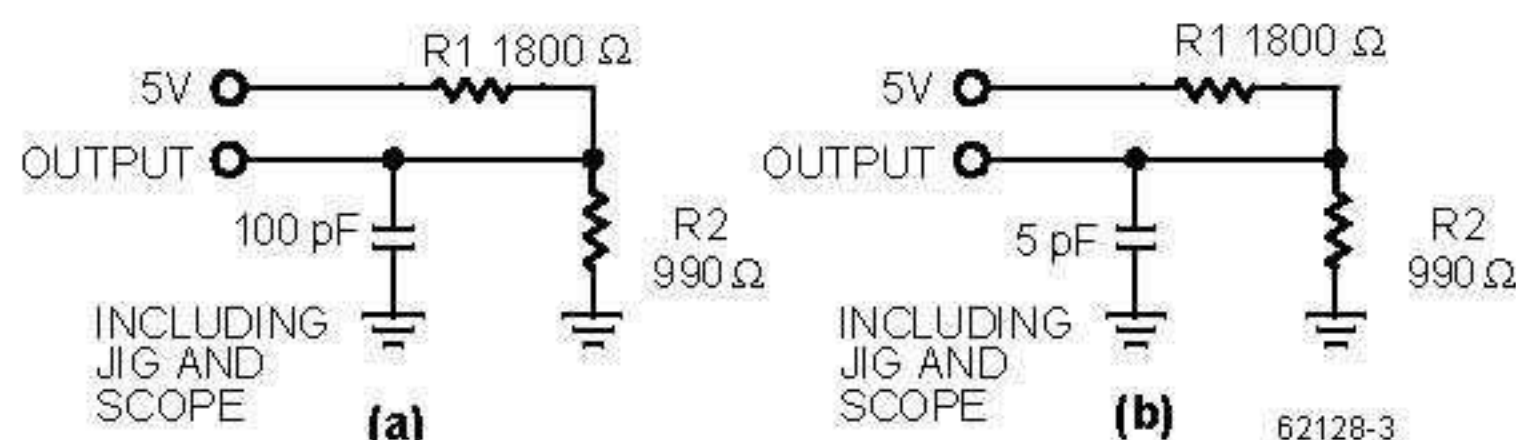
Notes:

- V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

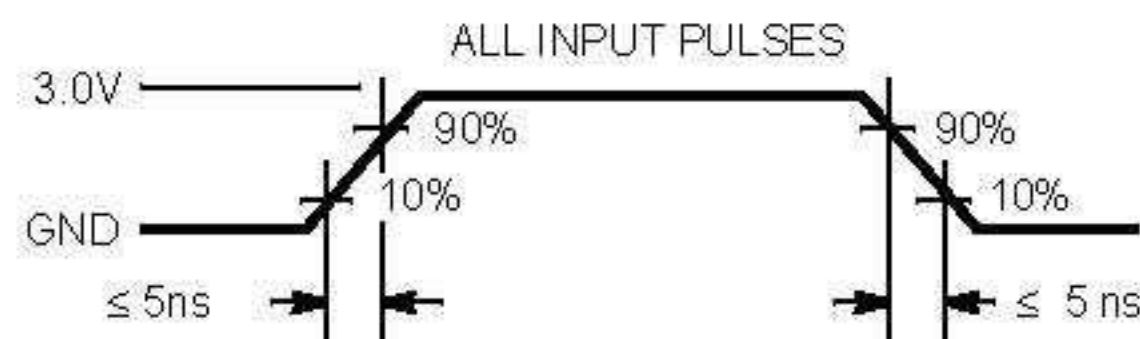
Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5.0\text{V}$	9	pF
C_{OUT}	Output Capacitance		9	pF

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT
 OUTPUT $\text{---} 639\Omega \text{---} 1.77\text{V}$



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Switching Characteristics^[3,6] Over the Operating Range

Parameter	Description	62128–55		62128–70		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	5		5		ns
t _{ACE}	CE ₁ LOW to Data Valid, CE ₂ HIGH to Data Valid		55		70	ns
t _{DOE}	OE LOW to Data Valid		20		35	ns
t _{LZOE}	OE LOW to Low Z	0		0		ns
t _{HZOE}	OE HIGH to High Z ^[7, 8]		20		25	ns
t _{LZCE}	CE ₁ LOW to Low Z, CE ₂ HIGH to Low Z ^[8]	5		5		ns
t _{HZCE}	CE ₁ HIGH to High Z, CE ₂ LOW to High Z ^[7, 8]		20		25	ns
t _{PU}	CE ₁ LOW to Power-Up, CE ₂ HIGH to Power-Up	0		0		ns
t _{PD}	CE ₁ HIGH to Power-Down, CE ₂ LOW to Power-Down		55		70	ns
WRITE CYCLE ^[9]						
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	CE ₁ LOW to Write End, CE ₂ HIGH to Write End	45		60		ns
t _{AW}	Address Set-Up to Write End	45		60		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	WE Pulse Width	45		50		ns
t _{SD}	Data Set-Up to Write End	45		55		ns

Shaded areas contain advance information

Notes:

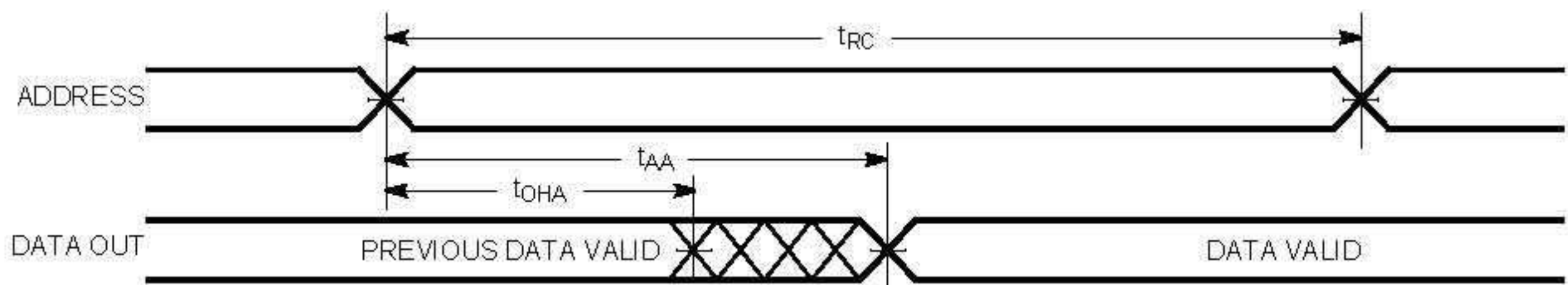
- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions assume signal transition time of 5ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100pF load capacitance.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured $\pm 500\text{ mV}$ from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} ; t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. $\overline{CE}_1$ and $\overline{WE}$ must be LOW and CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Switching Characteristics^[3,6] Over the Operating Range (continued)

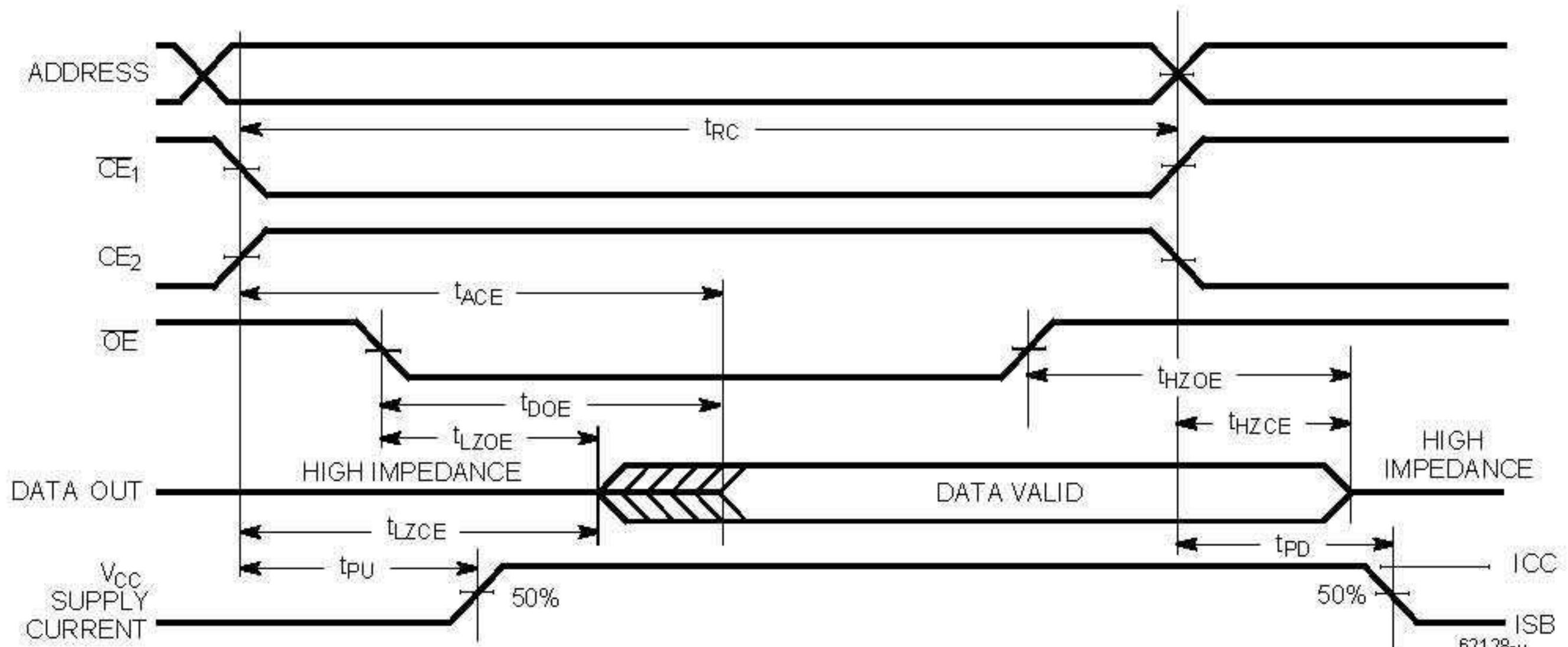
Parameter	Description	62128-55		62128-70		Unit
		Min.	Max.	Min.	Max.	
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	WE HIGH to Low Z ^[8]	5		5		ns
t_{HZWE}	WE LOW to High Z ^[7,8]		20		25	ns

Shaded area contains advanced information.

Switching Waveforms

Read Cycle No.1^[10,11]

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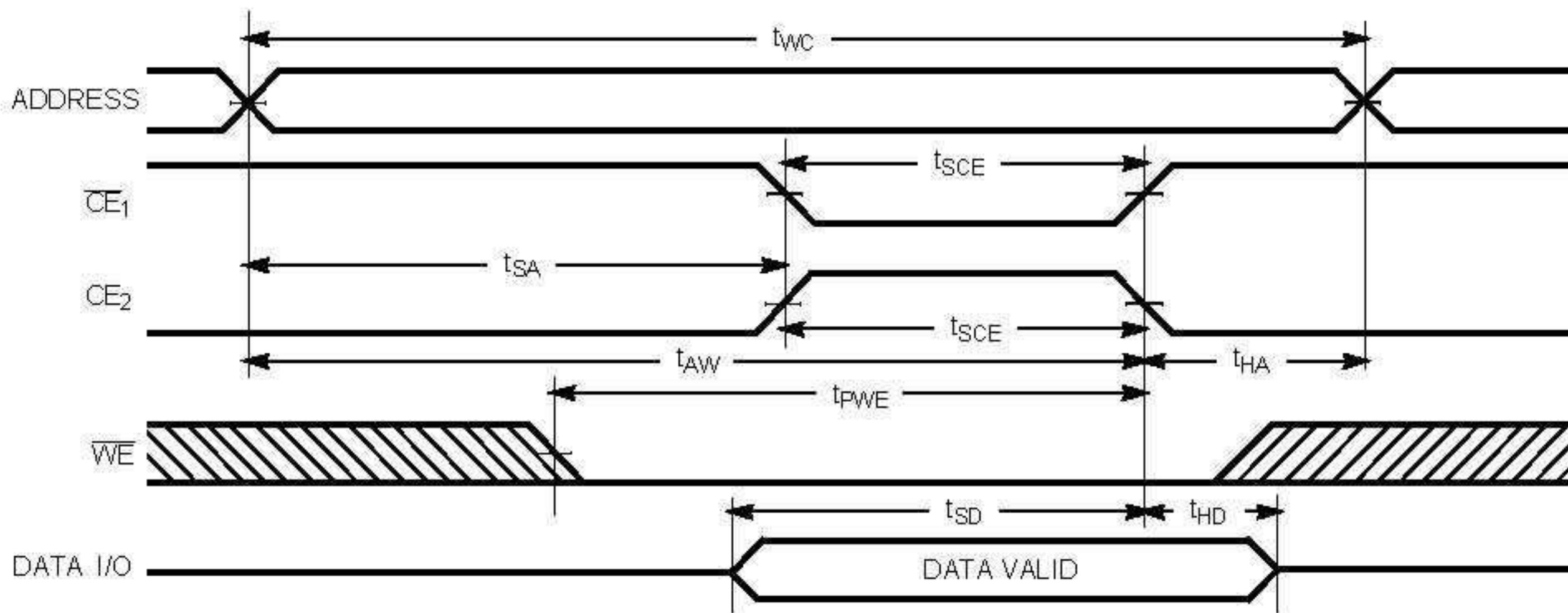
Read Cycle No. 2 (OE Controlled)^[11,12]

62128-u

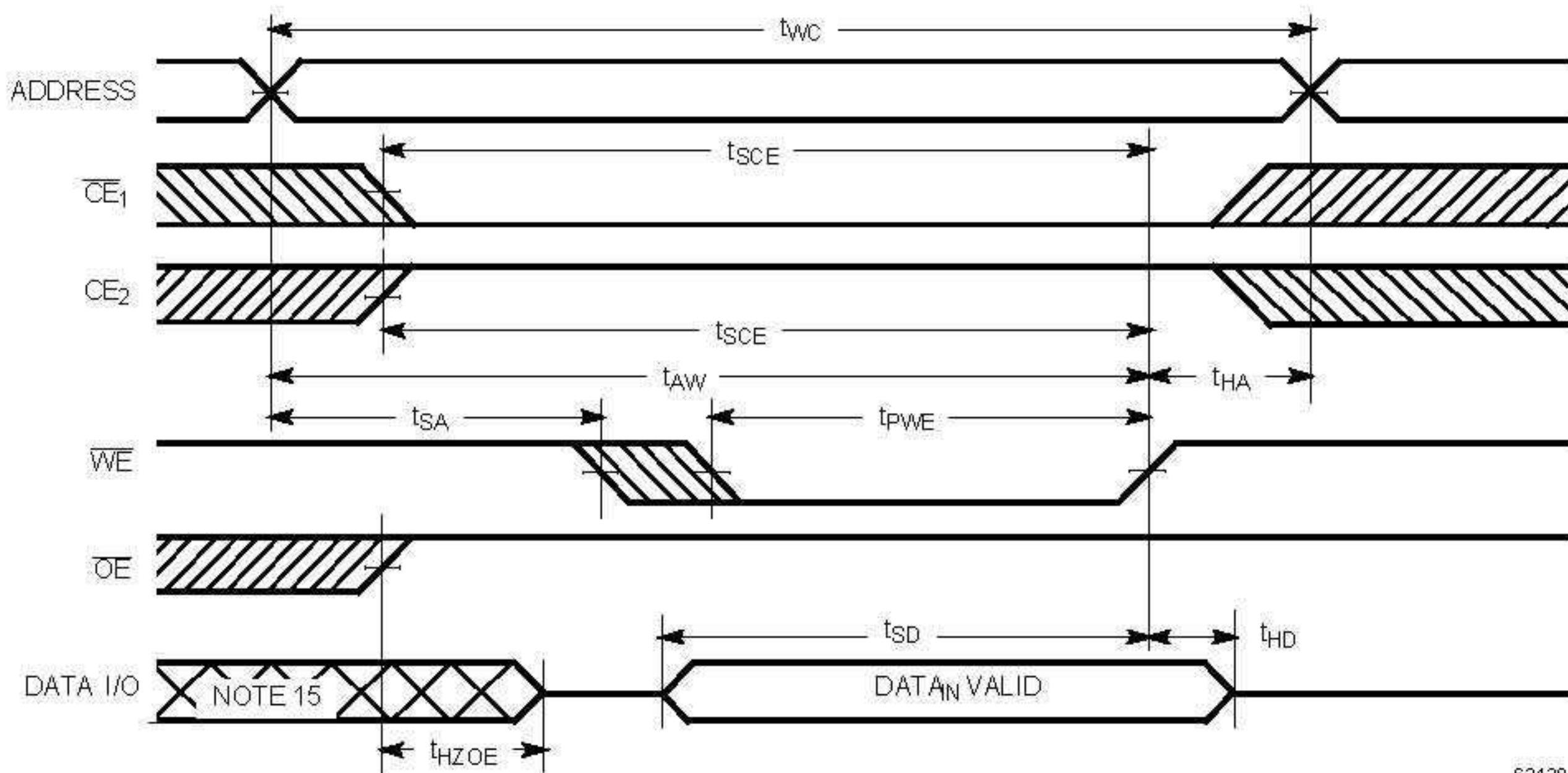
Notes:

10. Device is continuously selected. $\overline{OE}, \overline{CE}_1 = V_{IL}, CE_2 = V_{IH}$.
11. $\overline{WE}$ is HIGH for read cycle.
12. Address valid prior to or coincident with $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}_1$ or CE_2 Controlled)^[13,14]

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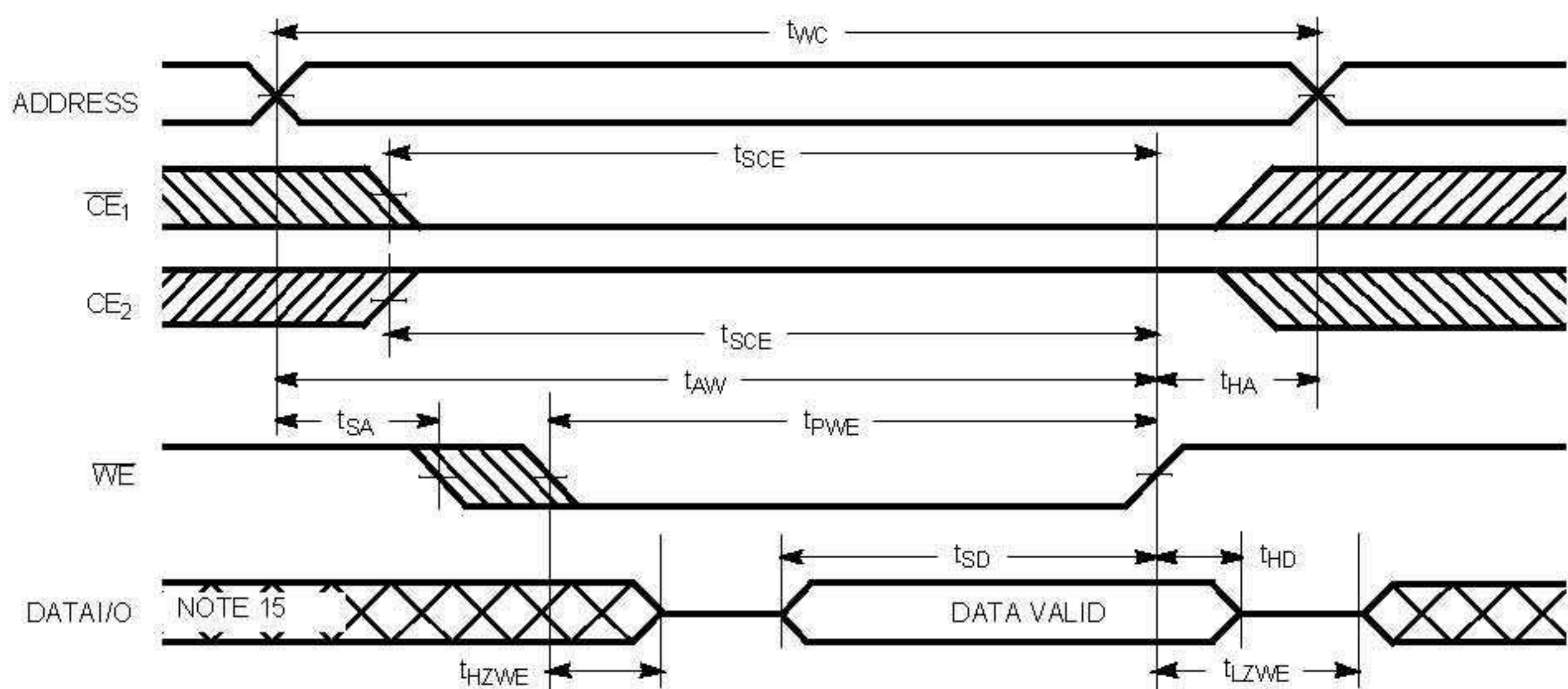
Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)^[13,14]

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Notes:

13. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
14. If $\overline{CE}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
15. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No.3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)^[13,14]

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Truth Table

CE_1	CE_2	OE	WE	$I/O_0 - I/O_7$	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	L	X	X	High Z	Power-Down	Standby (I_{SB})
L	H	L	H	Data Out	Read	Active (I_{CC})
L	H	X	L	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

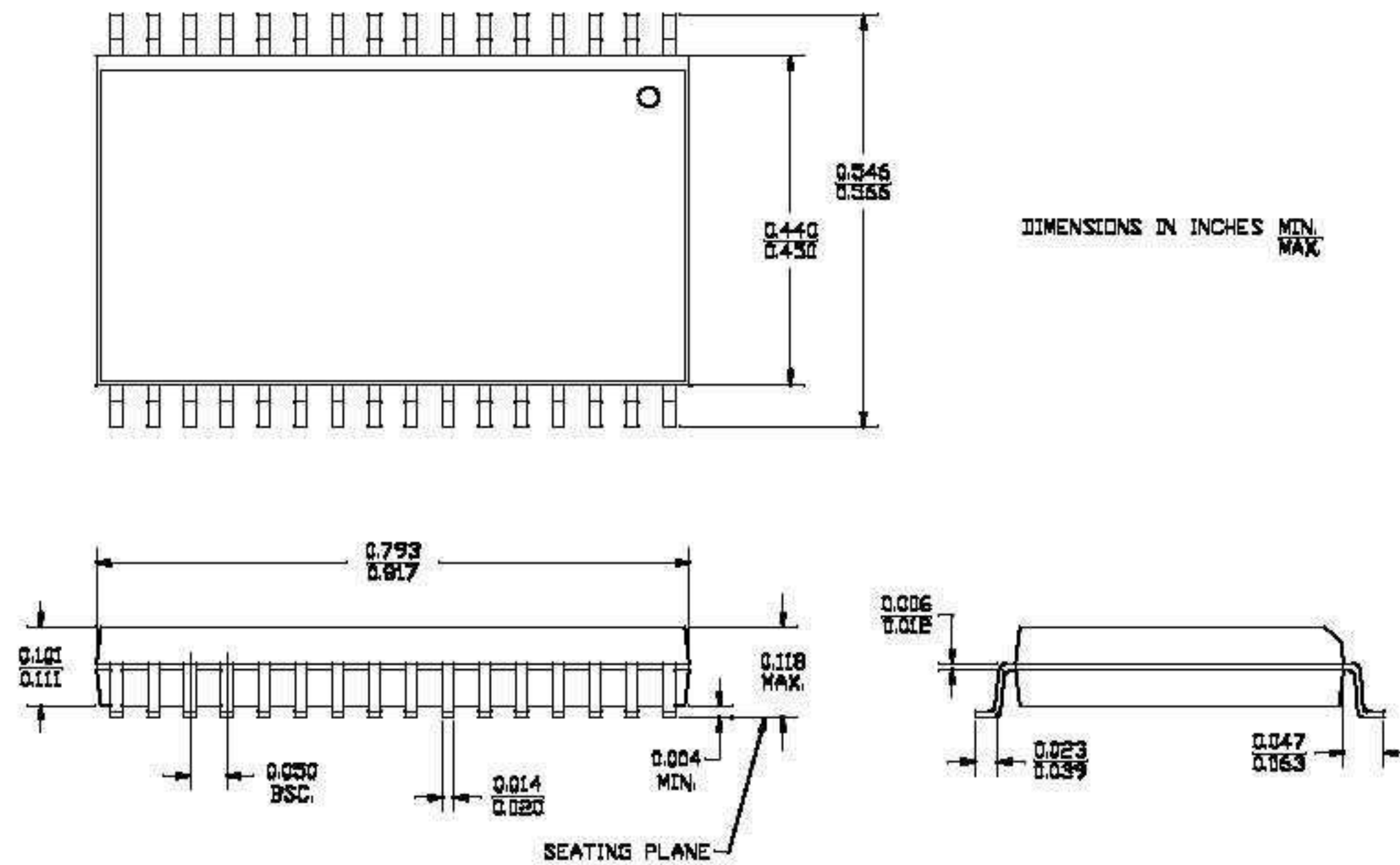
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62128-55VC	V33	32-Lead (400-Mil) Molded SOJ	Commercial
	CY62128-55SC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62128-55ZC	Z32	32-Lead TSOP Type I	
70	CY62128-70VC	V33	32-Lead (400-Mil) Molded SOJ	Commercial
	CY62128-70SC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62128-70ZC	Z32	32-Lead TSOP Type I	
	CY62128L-70SC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62128L-70ZC	Z32	32-Lead TSOP Type I	
	CY62128LL-70SC	S34	32-Lead (450-Mil) Molded SOIC	
	CY62128LL-70ZC	Z32	32-Lead TSOP Type I	

Shaded area contains advanced information.

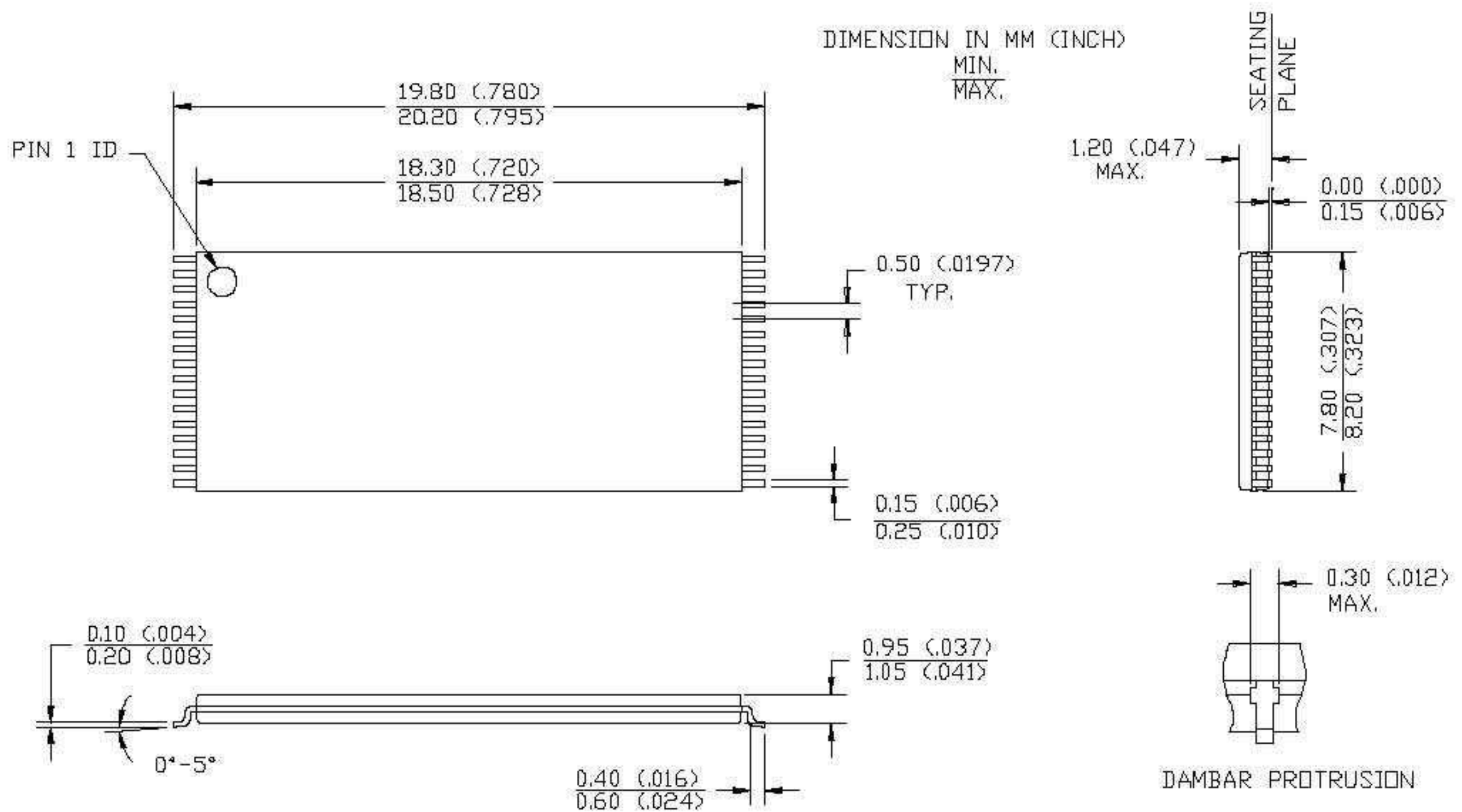
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Package Diagrams

32-Lead (450 Mil) Molded SOIC S34

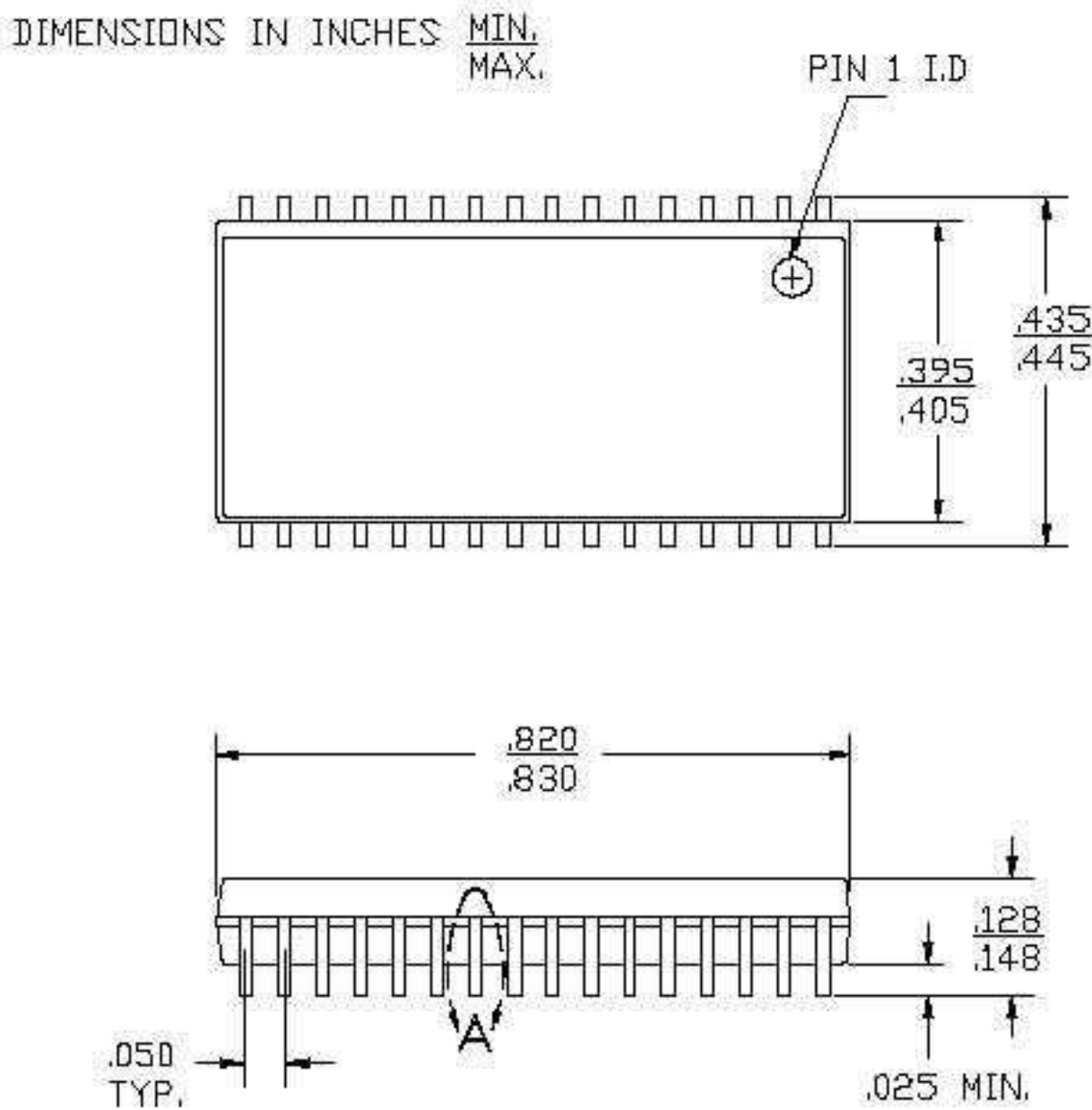


32-Lead Thin Small Outline Package Z32



Package Diagrams (continued)

32-Lead (400-Mil) Molded SOJ V33



DETAIL A
EXTERNAL LEAD DESIGN

