CY25200

Programmable Spread Spectrum Clock Generator for EMI Reduction

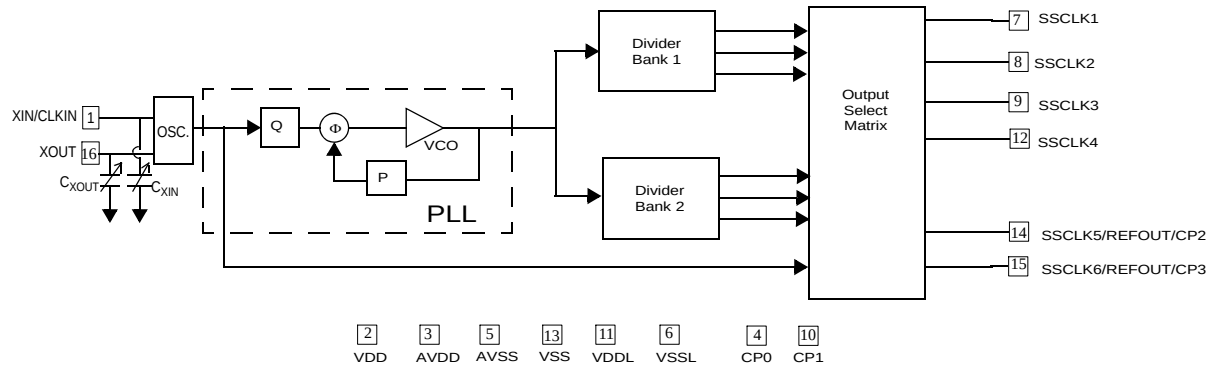
Features

- Wide operating output (SSCLK) frequency range
  - 3–200 MHz
- Programmable spread spectrum with nominal 31.5 kHz modulation frequency
- Center spread: ±0.25% to ±2.5%
- Down spread: –0.5% to –5.0%
- Input frequency range
  - External crystal: 8–30 MHz fundamental crystals
  - External reference: 8–166 MHz clock
- Integrated phase-locked loop (PLL)
- Programmable crystal load capacitor tuning array
- Low cycle-to-cycle jitter
- 3.3V operation with 2.5V output clock drive option
- Spread spectrum On and Off function
- Power down or Output Enable function
- Output frequency select option
- Field-programmable
- Package: 16 pin TSSOP

Benefits

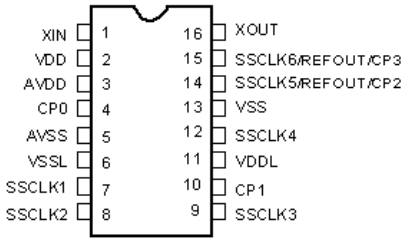
- Suitable for most PC peripherals, networking, and consumer applications.
- Provides wide range of spread percentages for maximum EMI reduction to meet regulatory agency Electro Magnetic Compliance (EMC) requirements. Reduces development and manufacturing costs and time to market.
- Eliminates the need for expensive and difficult to use higher order crystals.
- Internal PLL generates up to 200 MHz outputs; also generates custom frequencies from an external crystal or a driven source.
- Enables fine tuning of output clock frequency by adjusting C_{Load} of the crystal. Eliminates the need for external C_{Load} capacitors.
- Application compatibility in standard and low power systems.
- Provides ability to enable or disable spread spectrum with an external pin.
- Enables low power state or output clocks to High-Z state.
- Enables quick generation of sample prototype quantities.

Logic Block Diagram



Pin Configuration

Figure 1. Pin Diagram



General Description

The CY25200 is a Spread Spectrum Clock Generator (SSCG) IC used to reduce Electro Magnetic Interference (EMI) found in today's high speed digital electronic systems.

The device uses a Cypress proprietary Phase-Locked Loop (PLL) and Spread Spectrum Clock (SSC) technology to synthesize and modulate the frequency of the input clock. By frequency modulating the clock, the measured EMI at the fundamental and harmonic frequencies are greatly reduced. This reduction in radiated energy significantly reduces the cost of complying with regulatory agency requirements (EMC) and improves time to market, without degrading system performance.

The CY25200 uses a factory and field-programmable configuration memory array to synthesize output frequency, spread %, crystal load capacitor, clock control pins, PD#, and OE options.

The spread % is factory and field-programmed to either center spread or down spread with various spread percentages. The range for center spread is from ±0.25% to ±2.50%. The range for down spread is from –0.5% to –5.0%. Contact the factory for smaller or larger spread % amounts, if required.

The input to the CY25200 is either a crystal or a clock signal. The input frequency range for crystals is 8–30 MHz and for clock signals is 8–166 MHz.

The CY25200 has six clock outputs, SSCLK1 to SSCLK6. The frequency modulated SSCLK outputs are programmed from 3–200 MHz.

The CY25200 products are available in a 16-pin TSSOP package with a commercial operating temperature range of 0 to 70°C.

Table 1. Pin Summary

Name	Pin Number	Description
XIN	1	**Crystal Input or Reference Clock Input**
XOUT	16	**Crystal Output.** Leave this pin floating if external clock is used
VDD	2	3.3V power supply for digital logic and SSCLK5 and 6 clock drives
AVDD	3	3.3V analog–PLL power supply
VSS	13	Ground
AVSS	5	Analog ground
VDDL	11	2.5V or 3.3V power supply for SSCLK1/2/3/4 clock drives
VSSL	6	VDDL power supply ground
SSCLK1	7	Programmable spread spectrum clock output at VDDL level (2.5V or 3.3V)
SSCLK2	8	Programmable spread spectrum clock output at VDDL level (2.5V or 3.3V)
SSCLK3	9	Programmable spread spectrum clock output at VDDL level (2.5V or 3.3V)
SSCLK4	12	Programmable spread spectrum clock output at VDDL level (2.5V or 3.3V)
SSCLK5/REFOUT/CP2	14	Programmable spread spectrum clock or buffered reference output at VDD level (3.3V) or control pin, CP2
SSCLK6/REFOUT/CP3	15	Programmable spread spectrum clock or buffered reference output at VDD level (3.3V) or control pin, CP3
CP0[1]	4	Control pin 0
CP1[1]	10	Control pin 1

Note
1. Pins are programmed to be any of the following control signals: OE: Output Enable, OE = 1, all the SSCLK outputs are enabled; PD#: Power down, PD# = 0, all the SSCLK outputs are three-stated and the part enters a low power state; SSON: Spread Spectrum Control (SSON = 0, No Spread and SSON = 1, Spread Signal), CLKSEL: SSCLK Output Frequency Select. Please see Control Pins (CP0, CP1, CP2 and CP3) for control pins programming options.

[+] Feedback

Table 2. Fixed Function Pins

Pin Function	Output Clock Functions and Frequency				Input Frequency	C_{XIN} and C_{XOUT}	Spread Percent	Frequency Modulation
Pin Name	SSCLK1	SSCLK2	SSCLK3	SSCLK4	XIN and XOUT	XIN and XOUT	SSCLK[1:6]	SSCLK[1:6]
Pin#	7	8	9	12	1 and 16	1 and 16	7,8,9,12,14,15	7,8,9,12,14,15
Units	MHz	MHz	MHz	MHz	MHz	pF	%	kHz
Program Value CLKSEL = 0	**ENTER DATA**	**ENTER DATA**	**ENTER DATA**	**ENTER DATA**	**ENTER DATA**	**ENTER DATA**	**ENTER DATA**	**31.5**
Program Value CLKSEL = 1	**ENTER DATA**	**ENTER DATA**	**ENTER DATA**	**ENTER DATA**				

Table 3. Multi-Function Pins

Pin Function	Output Clock/REFOUT/OE/SSON/CLKSEL		OE/PD#/SSON/CLKSEL	
Pin Name	SSCLK5/REFOUT/CP2	SSCLK6/REFOUT/CP3	CP0	CP1
Pin#	14	15	4	10
Units	MHz	MHz	N/A	N/A
Program Value CLKSEL = 0	**ENTER DATA**	**ENTER DATA**	**ENTER DATA**	**ENTER DATA**
Program Value CLKSEL = 1	**ENTER DATA**	**ENTER DATA**		

Programming Description

Field-Programmable CY25200

The CY25200 is programmed at the package level, that is, in a programmer socket. The CY25200 is Flash technology based, so the parts are reprogrammed up to 100 times. This allows for fast and easy design changes and product updates, and eliminates any issues with old and out of date inventory.

Samples and small prototype quantities are programmed on the CY3672 programmer with the CY3695 socket adapter.

CyberClocks™ Online Software

CyberClocks™ Online Software is a web based software application that allows the user to custom configure the CY25200. All the parameters in given as “Enter Data” are programmed into the CY25200. CyberClocks Online outputs an industry standard JEDEC file used for programming the CY25200. CyberClocks Online is available at www.cyberclocksonline.com website through user registration. To register, fill out the registration form and make sure to check the “non-standard devices” box. For more information on the registration process refer to the CY3672 data sheet.

For information regarding Spread Spectrum software programming solutions, please contact your local Cypress Sales or Field Application Engineer (FAE), representative for details.

Factory-Programmable CY25200

Factory programming is available for volume manufacturing by Cypress. All requests must be submitted to the local Cypress Field Application Engineer (FAE) or sales representative. The sample request form provided by the representative must be completed. When the request is processed, you receive a new part number, samples, and data sheet with the programmed values. This part number is used for additional sample requests and production orders.

Additional information on the CY25200 are available on the Cypress website at www.cypress.com.

Product Functions

Control Pins (CP0, CP1, CP2 and CP3)

There are four control signals available through programming of pins 4, 10, 14, and 15.

CP0 (pin 4) and CP1 (pin10) are specifically designed to function as control pins. However pins 14 (SSCLK5/REFOUT/CP2) and 15 (SSCLK6/REFOUT/CP3) are multi-functional and are programmed to be a control signal or an output clock (SSCLK or REFOUT). All of the control pins, CP0, CP1, CP2, and CP3 are programmable and are programmed to have only one of the following functions:

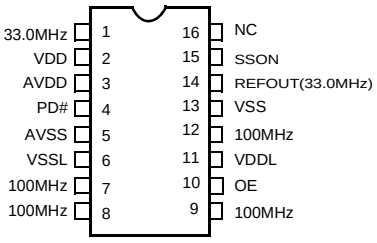
- Output Enable (OE)—if OE = 1, all the SSCLK or REFOUT outputs are enabled.
- SSON, Spread spectrum control—1 = spread on and 0 = spread off.
- CLKSEL—SSCLK output frequency select
- PD#, Active Low—if PD# = 0, all the outputs are three-stated and the part enters a low power state.

The last control signal is the power down (PD#) that is implemented only through programming CP0 or CP1 (CP2 and CP3 cannot be programmed as PD#). Here is an example with three control pins:

- CLKIN = 33 MHz
- SSCLK1/2/3/4 = 100 MHz with ±1% spread
- SSCLK 5 = REFOUT(33 MHz)
- CP0 (Pin 4) = PD#
- CP1 (Pin 10) = OE
- CP3 (pin 15) = SSON

The pinout for the above example is shown in Figure 2.

Figure 2. Pin Diagram



The CLKSEL control pin enables the user to change the output frequency from one frequency to another (for example, frequency A to frequency B). These must be related frequencies that are derived off of a common VCO frequency. For instance, 33.333 MHz and 66.666 MHz are both derived from a VCO of 400 MHz and dividing it down by 12 and 6 respectively. Table 4 shows an example of how this is implemented. The VCO frequency range is 100–400MHz. The CY25200 has two separate dividers, Divider 1 and Divider 2. These two are loaded to have any number between 2 and 130 providing two different but related frequencies as explained above.

In the above example SSCLK5 (pin 14) and SSCLK6 (pin 15) are used as output clocks. However, they can also be used as control signals. See Figure 3 for the pinout.

Input Frequency (XIN, pin 1 and XOUT, pin 16)

The input to the CY25200 is a crystal or a clock. The input frequency range for crystals is 8 to 30 MHz, and for clock signal is 8 to 166 MHz.

C_{XIN} and C_{XOUT} (pin 1 and pin 16)

The load capacitors at pin 1 (C_{XIN}) and pin 16 (C_{XOUT}) are programmed from 12 pF to 60 pF with 0.5 pF increments. The programmed value of these on-chip crystal load capacitors are the same (XIN = XOUT = 12 to 60 pF).

The required values of C_{XIN} and C_{XOUT} for matching crystal load (CL) is calculated using the following formula:

$C_{XIN} = C_{XOUT} = 2C_L – C_P$

Where C_L is the crystal load capacitor as specified by the crystal manufacturer and C_P is the parasitic PCB capacitance.

For example, if a fundamental 16 MHz crystal with C_L of 16 pF is used and C_P is 2 pF, C_{XIN} and C_{XOUT} is calculated as:

$C_{XIN} = C_{XOUT} = (2 \times 16) – 2 = 30$ pF.

If using a driven reference clock, set C_{XIN} and C_{XOUT} to the minimum value 12 pF.

Output Frequency (SSCLK1 through SSCLK6 Outputs)

All of the SSCLK outputs are produced by synthesizing the input reference frequency using a PLL and modulating the VCO frequency. SSCLK[1:4] is programmed to be only output clocks (SSCLK). SSCLK5 and SSCLK6 are also programmed to function the same as SSCLK[1:4] or a buffered copy of the input reference (REFOUT) or they are programmed to be a control pin as discussed in the control pins section. To use the 2.5V output drive option on SSCLK[1:4], VDDL must be connected to a 2.5V power supply (SSCLK[1:4] outputs are powered by VDDL). When using the 2.5V output drive option, the maximum output frequency on SSCLK[1:4] is 166 MHz.

Spread Percentage (SSCLK1 through SSCLK6 Outputs)

The SSCLK frequency is programmed at any percentage value from ±0.25% to ±2.5% for center spread and from –0.5% to –5.0% down spread.

Frequency Modulation

The frequency modulation is programmed at 31.5 kHz for all SSCLK frequencies from 3 to 200 MHz. Contact the factory if a higher modulation frequency is required.

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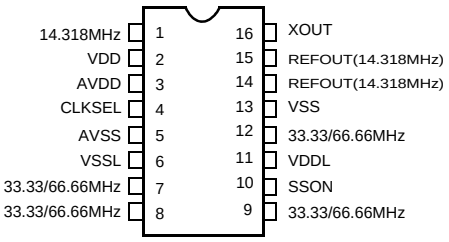
Table 4. Using Clock Select, CLKSEL Control Pin

Input Frequency (MHz)	CLKSEL (Pin 4)	SSCLK1 (Pin 7)	SSCLK2 (Pin 8)	SSCLK3 (Pin 9)	SSCLK4 (Pin 12)	REFOUT (Pin 14)	REFOUT (Pin 15)
14.318	CLKSEL = 0	33.33	33.33	33.33	33.33	14.318	14.318
	CLKSEL = 1	66.66	66.66	66.66	66.66	14.318	14.318

Figure 3. Using Clock Select, CLKSEL Control Pin Configuration Pinout



Switching Waveforms

Figure 4. Duty Cycle Timing (DC = t_{1A}/t_{1B})

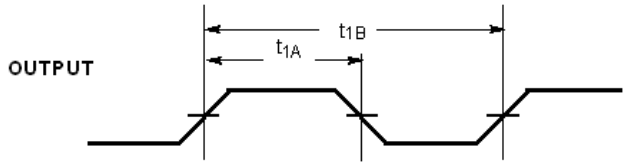
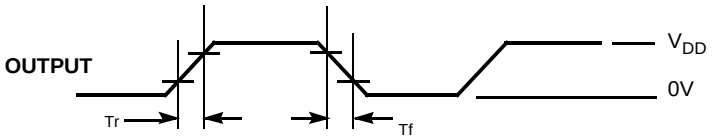


Figure 5. Output Rise and Fall Time (SSCLK and REFCLK)



Output Rise time (Tr) = (0.6 x V_{DD})/SR1 (or SR3)
Output Fall time (Tf) = (0.6 x V_{DD})/SR2 (or SR4)
Refer to AC Electrical Characteristics table for SR (Slew Rate) values.

Figure 6. Power Down and Power Up Timing

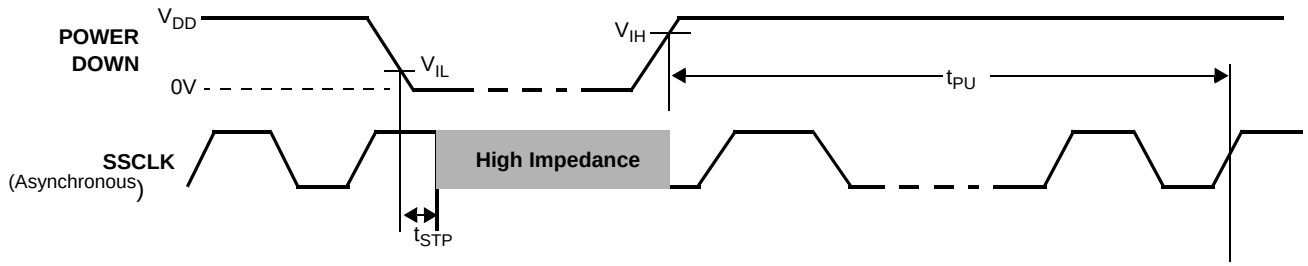
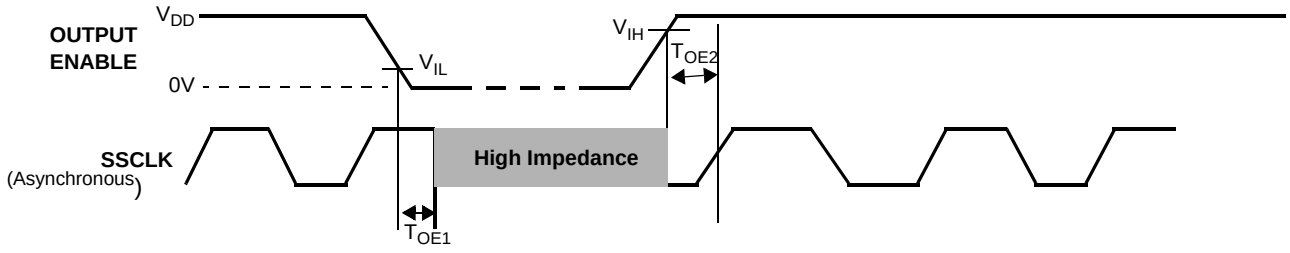


Figure 7. Output Enable and Disable Timing



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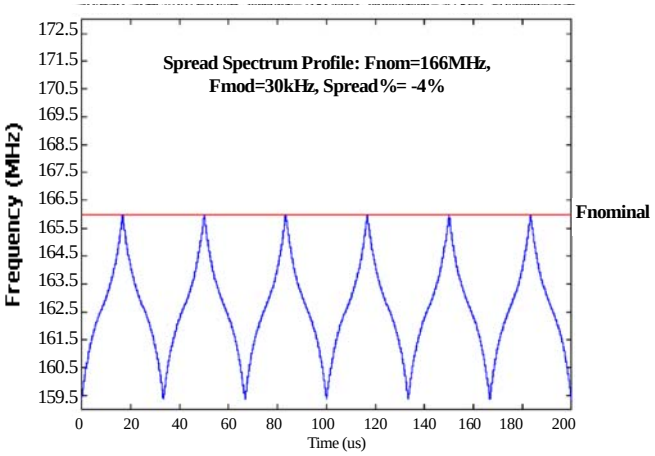
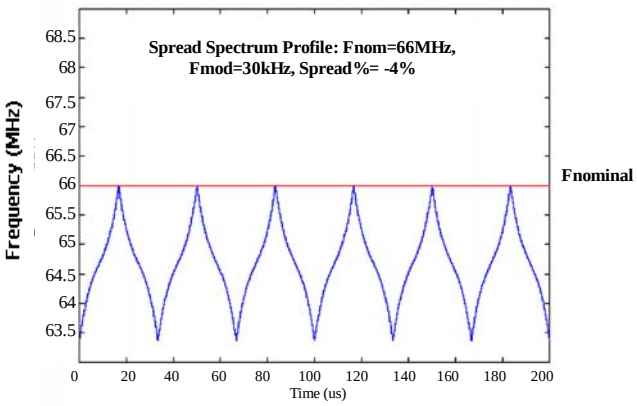
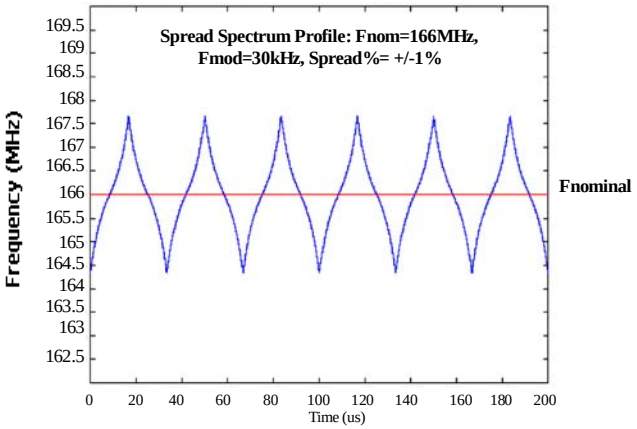
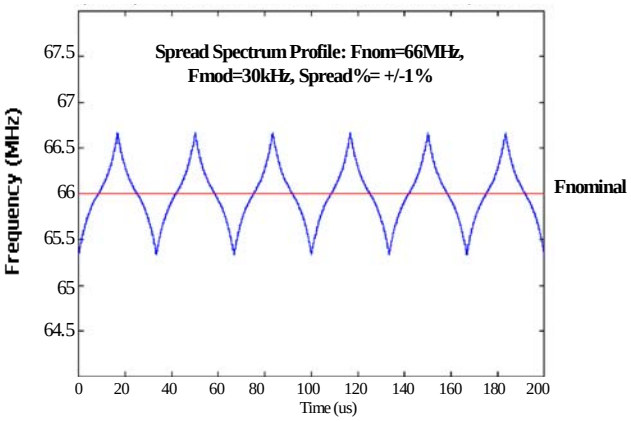
Informational Graphs

The informational graphs are meant to convey the typical performance levels. No performance specifications is implied or guaranteed. Refer to the tables on 3 and 5 for device specifications.









Absolute Maximum Rating

Supply Voltage (VDD) .....–0.5 to +7.0V
DC Input Voltage ..... –0.5V to V_{DD} + 0.5
Storage Temperature (non-condensing) .....–55°C to +125°C
Junction Temperature ..... –40°C to +125°C
Data Retention at Tj = 125°C .....> 10 years
Package Power Dissipation ..... 350 mW
Static Discharge Voltage..... ≥ 2000V (per MIL-STD-883, Method 3015)

Recommended Crystal Specifications

Parameter	Description	Comments	Min	Typ.	Max	Unit
F_{NOM}	Nominal Crystal Frequency	Parallel resonance, fundamental mode, AT cut	8		30	MHz
C_{LNOM}	Nominal Load Capacitance	Internal load caps	6		30	pF
R_1	Equivalent Series Resistance (ESR)	Fundamental mode			25	Ω
R_3/R_1	Ratio of Third Overtone Mode ESR to Fundamental Mode ESR	Ratio used because typical R_1 values are much less than the maximum specification	3			
DL	Crystal Drive Level	No external series resistor assumed		0.5	2	mW

Recommended Operating Conditions

Parameter	Description	Min	Typ.	Max	Unit
V_{DD}	Operating Voltage	3.135	3.3	3.465	V
V_{DDLHI}	Operating Voltage	3.135	3.3	3.465	V
V_{DDLLO}	Operating Voltage	2.375	2.5	2.625	V
T_{AC}	Ambient Commercial Temp	0	–	70	°C
C_{LOAD}	Maximum Load Capacitance V_{DD}/V_{DDL} = 3.3V	–	–	15	pF
C_{LOAD}	Maximum Load Capacitance V_{DDL} = 2.5V	–	–	15	pF
$F_{SSCLK\text{-}HighVoltage}$	SSCLK1/2/3/4/5/6 when $V_{DD} = A_{VDD} = V_{DDL}$ = 3.3 V	3	–	200	MHz
$F_{SSCLK\text{-}LowVoltage}$	SSCLK1/2/3/4 when $V_{DD} = A_{VDD}$ = 3.3.V and V_{DDL} = 2.5V	3	–	166	MHz
R_{EFOUT}	REFOUT when $V_{DD} = A_{VDD}$ = 3.3.V and V_{DDL} = 3.3V or 2.5V	8	–	166	MHz
f_{REF1}	Clock Input	8	–	166	MHz
f_{REF2}	Crystal Input	8	–	30	MHz
t_{PU}	Power up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

DC Electrical Specifications

Parameter[3]	Name	Description	Min	Typ.	Max	Unit
$I_{OH3.3}$	Output High Current	$V_{OH} = V_{DD} – 0.5V$, $V_{DD}/V_{DDL} = 3.3V$	10	12	–	mA
$I_{OL3.3}$	Output Low Current	$V_{OL} = 0.5V$, $V_{DD}/V_{DDL} = 3.3V$	10	12	–	mA
$I_{OH2.5}$	Output High Current	$V_{OH} = V_{DDL} – 0.5V$, $V_{DDL} = 2.5V$	8	16	–	mA
$I_{OL2.5}$	Output Low Current	$V_{OL} = 0.5V$, $V_{DDL} = 2.5V$	8	16	–	mA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	0.7	–	1.0	V_{DD}
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}	0	–	0.3	V_{DD}
I_{VDD}[4]	Supply Current	AV_{DD}/V_{DD} Current	–	–	33	mA
$I_{VDDL2.5}$[4]	Supply Current	V_{DDL} Current ($V_{DDL} = 2.625V$)	–	–	20	mA
$I_{VDDL3.3}$[4]	Supply Current	V_{DDL} Current ($V_{DDL} = 3.465V$)	–	–	26	mA
I_{DDS}	Power Down Current	$V_{DD} = V_{DDL} = AV_{DD} = 3.465V$	–	–	50	uA
I_{OHZ} I_{OLZ}	Output Leakage	$V_{DD} = V_{DDL} = AV_{DD} = 3.465V$	–	–	10	uA

Notes
2. Rated for 10 years.
3. Not 100% tested, guaranteed by design.
4. I_{VDD} currents specified for SSCLK1/2/3/4/5/6 = 33.33 MHz with CLKIN = 14.318 MHz and 15 pF on all the output clocks.

AC Electrical Specifications

Parameter	Description	Condition	Min	Typ.	Max	Unit
DC	Output Duty Cycle	SSCLK, Measured at $V_{DD}/2$	45	50	55	%
	Output Duty Cycle	REFCLK, Measured at $V_{DD}/2$ Duty Cycle of CLKIN = 50%.	40	50	60	%
SR1	Rising/Falling Edge Slew Rate	SSCLK1/2/3/4 < 100 MHz, $V_{DD} = V_{DDL} = 3.3V$	0.6	–	2.0	V/ns
SR2	Rising/Falling Edge Slew Rate	SSCLK1/2/3/4 ≥ 100 MHz, $V_{DD} = V_{DDL} = 3.3V$	0.8	–	3.5	V/ns
SR3	Rising/Falling Edge Slew Rate	SSCLK1/2/3/4 < 100 MHz, $V_{DD} = V_{DDL} = 2.5V$	0.5	–	2.2	V/ns
SR4	Rising/Falling Edge Slew Rate	SSCLK1/2/3/4 ≥ 100 MHz, $V_{DD} = V_{DDL} = 2.5V$	0.6	–	3.0	V/ns
SR5	Rising/Falling Edge Slew Rate	SSCLK5/6 < 100 MHz, $V_{DD} = V_{DDL} = 3.3V$	0.6	–	1.9	V/ns
SR6	Rising/Falling Edge Slew Rate	SSCLK5/6 ≥ 100 MHz, $V_{DD} = V_{DDL} = 3.3V$	1.0	–	2.9	V/ns
T_{CCJ1}	Cycle-to-Cycle Jitter SSCLK1/2/3/4	CLKIN = SSCLK1/2/3/4 = 166MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = V_{DDL} = 3.3V$	–	–	110	ps
		CLKIN = SSCLK1/2/3/4 = 66.66 MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = V_{DDL} = 3.3V$	–	–	170	ps
		CLKIN = SSCLK1/2/3/4 = 33.33 MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = V_{DDL} = 3.3V$	–	–	140	ps
		CLKIN = SSCLK1/2/3/4 = 14.318MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = V_{DDL} = 3.3V$	–	–	290	
T_{CCJ2}	Cycle-to-Cycle Jitter SSCLK5/6=REFOUT	CLKIN = SSCLK1/2/3/4 = 166 MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = V_{DDL} = 3.3V$	–	–	100	ps
		CLKIN = SSCLK1/2/3/4 = 66.66 MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = V_{DDL} = 3.3V$	–	–	120	ps
		CLKIN = SSCLK1/2/3/4 = 33.33 MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = V_{DDL} = 3.3V$	–	–	180	ps
		CLKIN = SSCLK1/2/3/4 = 14.318 MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = V_{DDL} = 3.3V$	–	–	180	
T_{CCJ3}	Cycle-to-Cycle Jitter SSCLK1/2/3/4	CLKIN = SSCLK1/2/3/4 = 166 MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = 3.3V$, $V_{DDL} = 2.5V$	–	–	110	ps
		CLKIN = SSCLK1/2/3/4 = 66.66MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = 3.3V$, $V_{DDL} = 2.5V$	–	–	170	ps
		CLKIN = SSCLK1/2/3/4 = 33.33 MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = 3.3V$, $V_{DDL} = 2.5V$	–	–	190	ps
		CLKIN = SSCLK1/2/3/4 = 14.318 MHz, ±2% spread and SSCLK5/6 = REFOUT, $V_{DD} = 3.3V$, $V_{DDL} = 2.5V$	–	–	330	
t_{STP}	Power Down Time (pin3 = PD#)	Time from falling edge on PD# to stopped outputs (Asynchronous)	–	150	300	ns
T_{OE1}	Output Disable Time (pin3 = OE)	Time from falling edge on OE to stopped outputs (Asynchronous)	–	150	300	ns
T_{OE2}	Output Enable Time (pin3 = OE)	Time from rising edge on OE to outputs at a valid frequency (Asynchronous)	–	150	300	ns
F_{MOD}	Spread Spectrum Modulation Frequency	SSCLK1/2/3/4/5/6	30.0	31.5	33.0	kHz
t_{PU1}	Power Up Time, Crystal is used	Time from rising edge on PD# to outputs at valid frequency (Asynchronous)	–	3	5	ms
t_{PU2}	Power Up Time, Reference clock is used	Time from rising edge on PD# to outputs at valid frequency (Asynchronous)	–	2	3	ms
t_{SKEW}[5]	Clock Skew	Output to output skew between related clock outputs. Measured at $V_{DD}/2$.	–	–	250	ps

Ordering Information

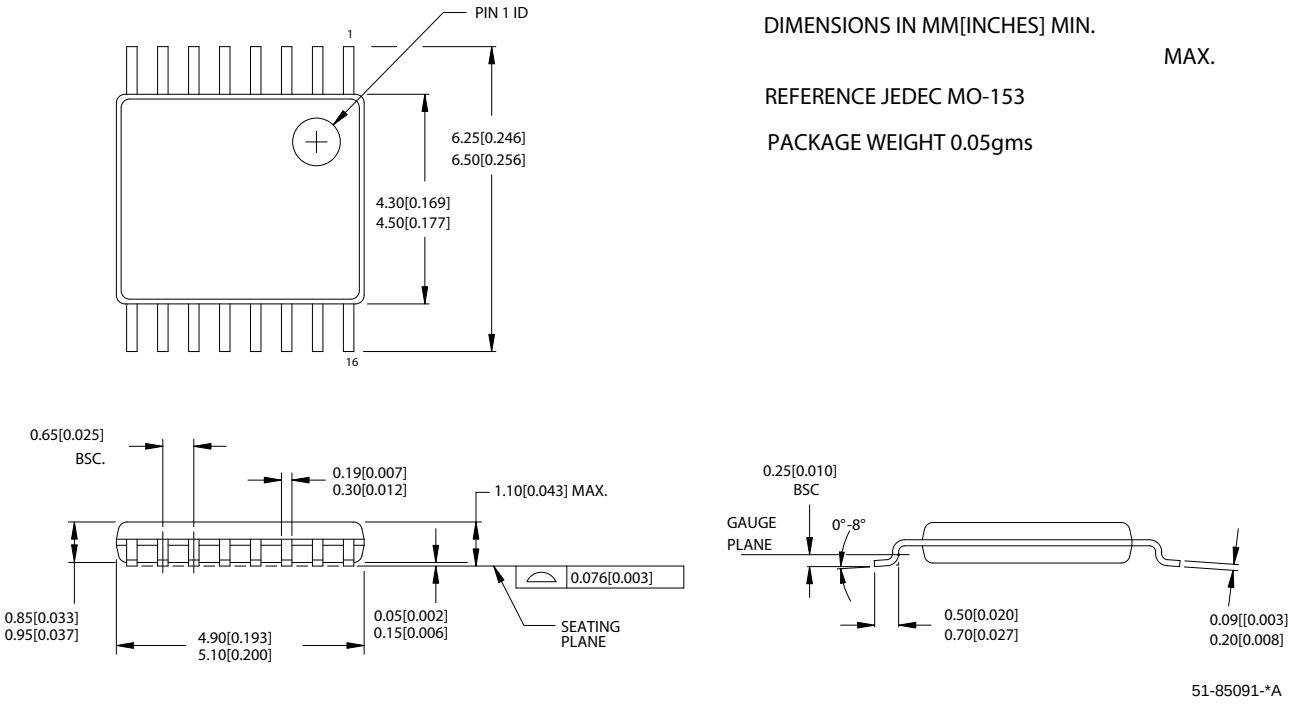
Ordering Code[6]	Package Type	Programming	Temperature Operating Range
CY25200ZXC_XXXW	16-lead TSSOP (Pb Free)	Factory	Commercial, 0 to 70°C
CY25200ZXC_XXXWT	16-lead TSSOP – Tape and Reel (Pb Free)	Factory	Commercial, 0 to 70°C
CY25200FZXC	16-lead TSSOP (Pb Free)	Field	Commercial, 0 to 70°C
CY25200FZXCT	16-lead TSSOP – Tape and Reel (Pb Free)	Field	Commercial, 0 to 70°C
CY3672	FTG Development Kit	N/A	N/A
CY3672-PRG	FTG Programmer	N/A	N/A
CY3695	CY22050F/CY22150F/CY25200F Socket Adapter	N/A	N/A

Table 5. 16-lead TSSOP Package Characteristics

Parameter	Name	Value	Unit
θ_{JA}	theta JA	115	°C/W

Package Drawing and Dimensions

Figure 8. 16-lead TSSOP 4.40 MM Body Z16.173



Notes
5. Skew and phase alignment is guaranteed within all SSCLK outputs and within both REFOUT outputs. SSCLK and REFOUT outputs are not phase aligned to each other.
6. “XXX” denotes the assigned product dash number. “W” denotes the different revisions of the product.

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Document History Page

Document Title: CY25200 Programmable Spread Spectrum Clock Generator for EMI Reduction Document Number: 38-07633				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	204243	See ECN	RGL	New data sheet
*A	220043	See ECN	RGL	Minor Change: Corrected letter assignment in the ordering info for Pb Free.
*B	267832	See ECN	RGL	Added Field Programmable Devices and Functionality
*C	291094	See ECN	RGL	Added t_{SKEW} spec. and footnote
*D	1821908	See ECN	DPF/AESA	Corrected FSSCLK-Low Voltage specification on page 7 for SSCLK5/6 to SSCLK1/2/3/4, as SSCLK5/6 output does not operate at low voltage. Deleted Tccj4 on page 8 for the same reason as above

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