SONY

CXA3003R

Baseband analog processing IC for dual-mode CDMA/FM cellular phone

For the availability of this product, please contact the sales office.

Description

The CXA3003R is a baseband analog processing IC for dual-mode CDMA/FM cellular phone. The CXA3003R interfaces between the inter-frequency section and the digital processing circuitry of the telephone. The receive circuit functions primarily convert analog IF signals to the analog baseband frequency range and to convert the analog baseband signals into digital signals. Transmit circuits convert digital data into analog baseband signals which are then up-convert to the IF frequency range.

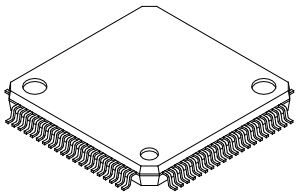
Features

- Receive signal path includes:
  - IF to baseband down conversion
  - Built-in trim-free low-pass filter for CDMA and FM
  - Built-in A/D convertor convert the RX base band signal to the digital signal
  - Analog output Receive Signal Strength Indicator (RSSI) for CDMA
  - Local Oscillator for I-Q mixer
- Transmit signal path includes:
  - Built-in D/A convertor convert the digital I-Q data to the analog baseband signal
  - Built-in trim-free low-pass filter for CDMA and FM
  - Baseband to IF up-conversion
  - Local Oscillator for I-Q mixer
  - Built-in PLL for TX IF
- Built-in House keeping A/D convertor
- Low power consumption in all modes
- Single 3.3 V power supply

Applications

- dual-mode CDMA/FM cellular telephone

80 pin LQFP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	V_{CC}	–0.3 to 5.5	V
• Operating temperature	Ta	–55 to +125	°C
• Storage temperature	Tstg	–65 to +150	°C

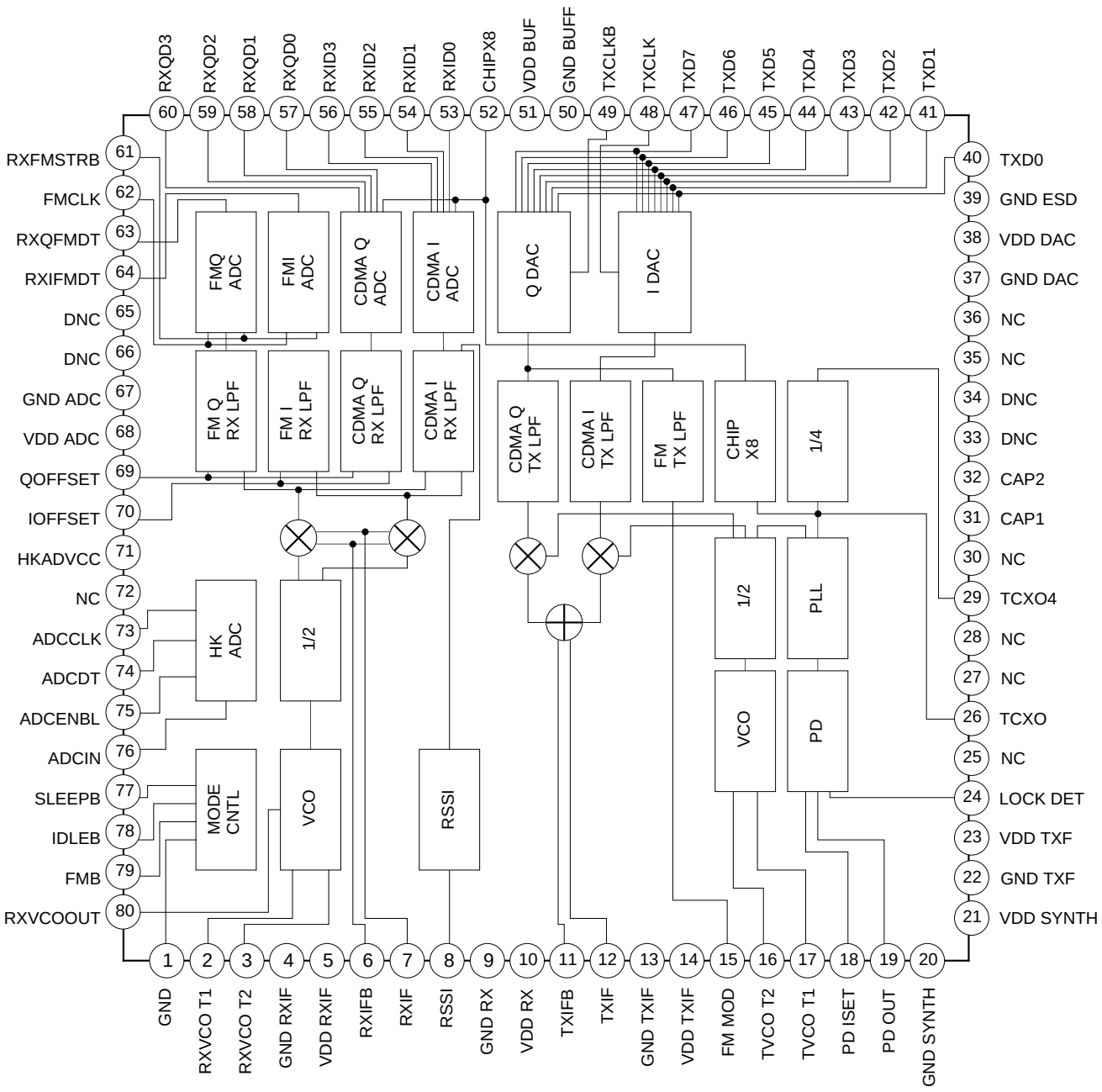
Recommended Operating Conditions

• Supply voltage	V_{CC}	3.3±0.165	V
• Operating temperature	Ta	–40 to +85	°C

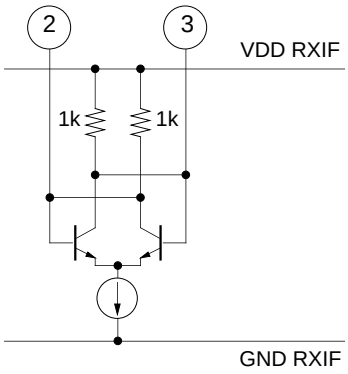
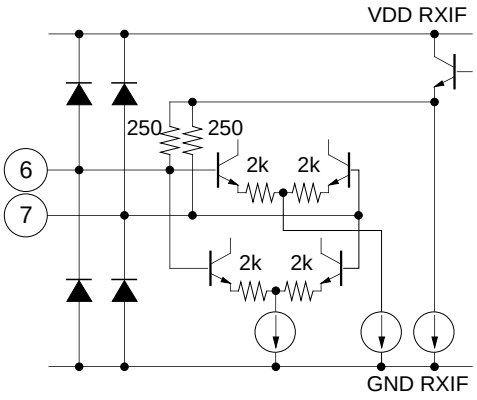
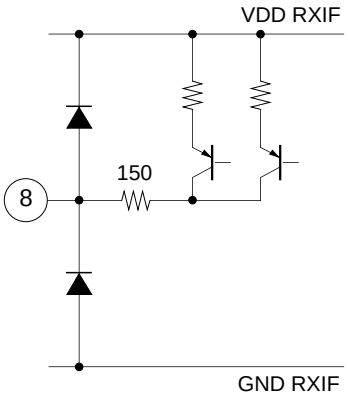
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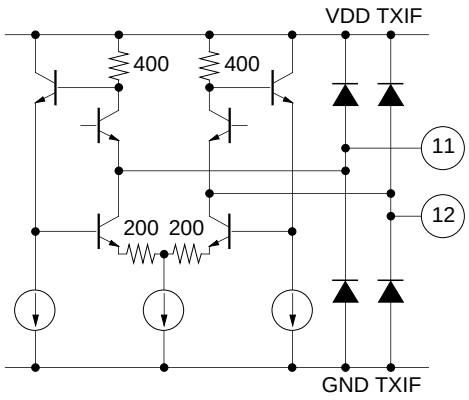
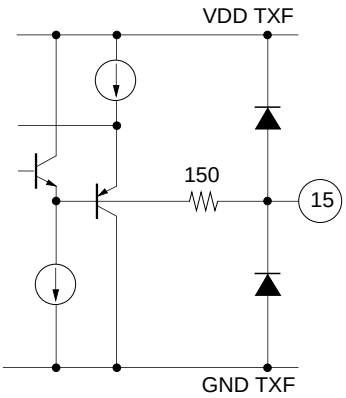
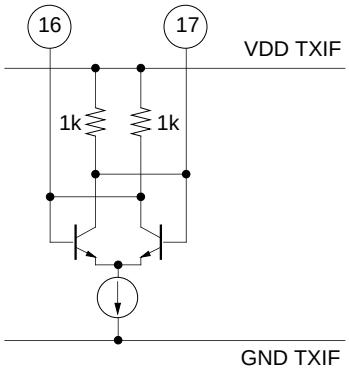
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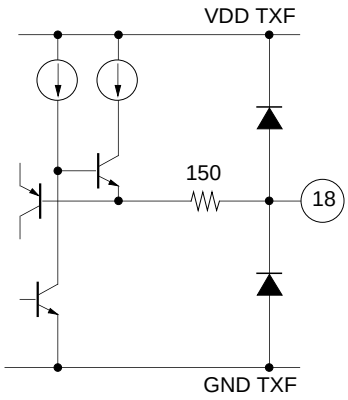
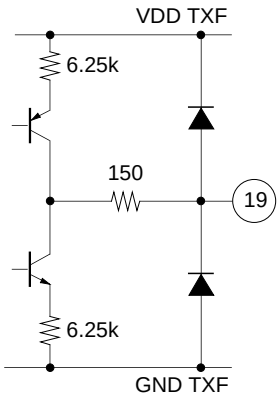
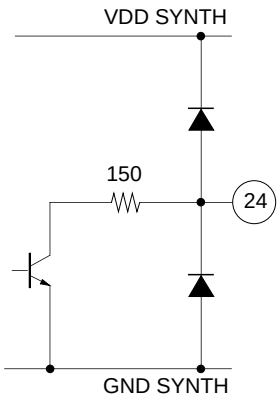
Block Diagram

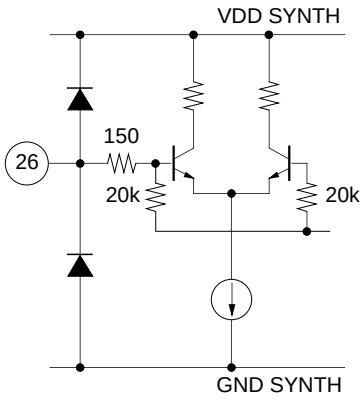
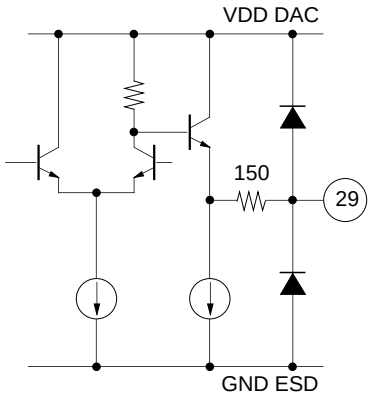
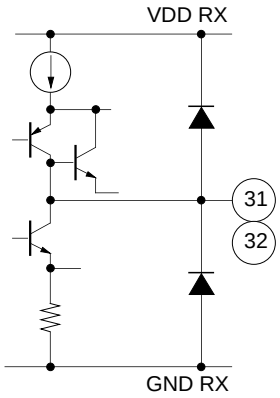


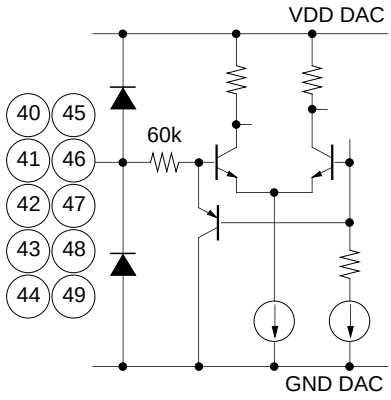
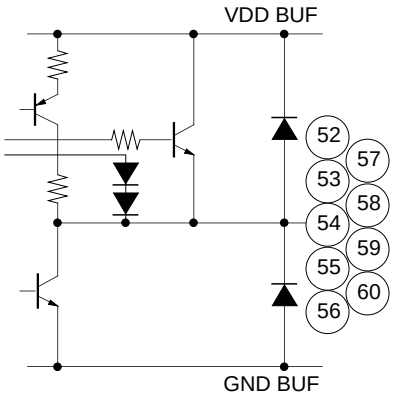
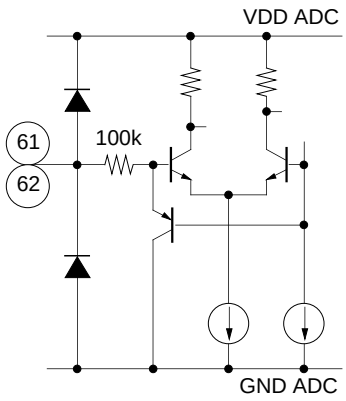
Pin Description

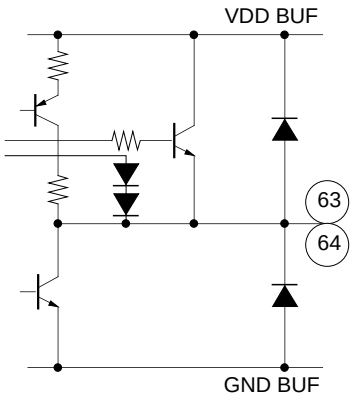
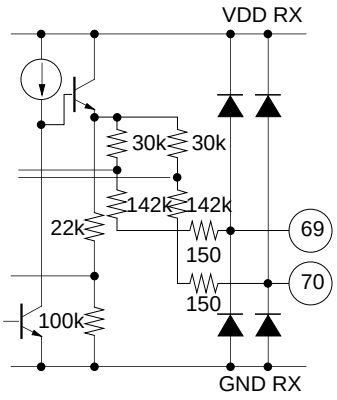
Pin No.	Symbol	Typical Voltage (V) DC	Typical Voltage (V) AC	Equivalent circuit	Description
1	GND	0 V			Negative power supply pin.
2	RXVCO TI				Receive VCO tuning pins. Connected to an external LC tank circuit for setting the receive VCO frequency.
3	RXVCO T2				
4	GND RXIF	0 V			Negative power supply pin for RXIF block.
5	VDD RXIF	3.3 V			Positive power supply pin for RXIF block.
6	RXIFB	2 V			Analog differential receive IF input pins.
7	RXIF	2 V			
8	RSSI				Analog RSSI output pin.
9	GND RX	0 V			Negative power supply pin for RX block.
10	VDD RX	3.3 V			Positive power supply pin for RX block.

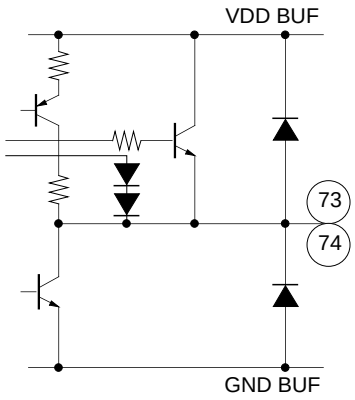
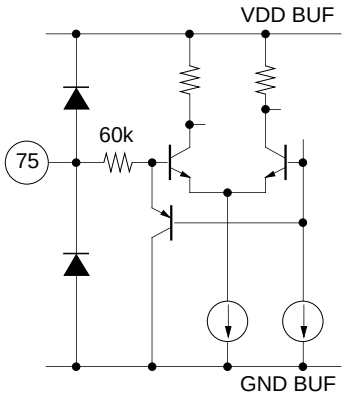
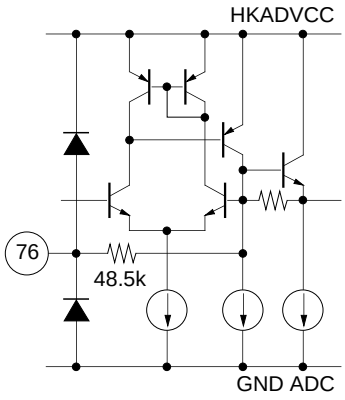
Pin No.	Symbol	Typical Voltage (V) DC	Typical Voltage (V) AC	Equivalent circuit	Description
11	TXIFB	2.1 V			Analog differential transmit IF output pins.
12	TXIF	2.1 V			
13	GND TXIF	0 V			Negative power supply pin for TXIF block.
14	VDD TXIF	3.3 V			Positive power supply pin for TXIF block.
15	FM MOD	1.5 V			Analog baseband signal output pin for FM.
16	TVCO T1				Transmit VCO tuning pins. Connected to an external LC tank circuit for setting the transmit VCO frequency.
17	TVCO T2				

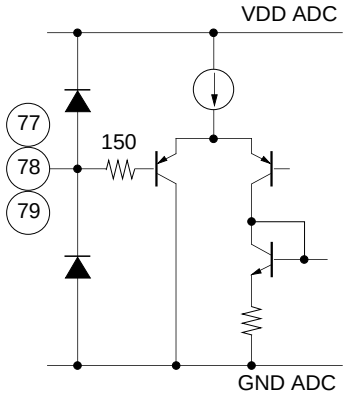
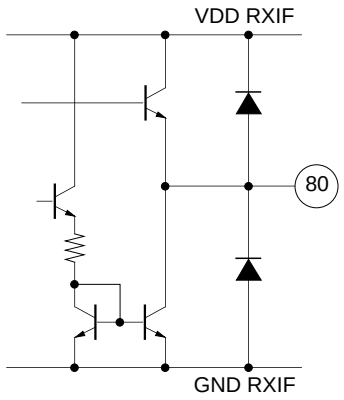
Pin No.	Symbol	Typical Voltage (V)		Equivalent circuit	Description
		DC	AC		
18	PD ISET	0.64 V			Current of PD OUT setting pin.
19	PD OUT				Transmit synthesizer charge pump output pin.
20	GND SYNTH	0 V			Negative power supply pin for PLL block.
21	VDD SYNTH	3.3 V			Positive power supply pin for PLL block.
22	GND TXF	0 V			Negative power supply pin for TX block.
23	VDD TXF	3.3 V			Positive power supply pin for TX block.
24	LOCK DET				Transmit IF synthesizer lock detect output pin.

Pin No.	Symbol	Typical Voltage (V) DC	Typical Voltage (V) AC	Equivalent circuit	Description
26	TCXO	2.2 V			Input pins for External clock 19.68 MHz (TCXO).
39	GND ESD	0 V			Negative power supply pin.
25 27 28 30 35 36	NC				Don't connect pins.
29	TCXO4				Output pin for TCXO/4 frequency.
31 32	CAP1 CAP2				The pins for External Capacitor.
33 34	DNC				Don't connect any line to this pin.
37	GND DAC	0 V			Negative power supply pin for TXDA block.

Pin No.	Symbol	Typical Voltage (V)		Equivalent circuit	Description
		DC	AC		
38	VDD DAC	3.3 V			Positive power supply pin for TXDA block.
40 to 47	TXD0 to TXD7				Transmit Data input pins for Transmit 8 bit D/A converter. TXD7 is the MSB.
48 49	TXCLK, TXCLKB				Differential transmit Clock input pins for Transmit 8 bit D/A converter.
50	GND BUF	0 V			Negative power supply pin for A/D output block.
51	VDD BUF	3.3 V			Positive power supply pin for A/D output block.
52	CHIP x 8				Output pin for CHIPx8 divider with a ratio of 512/1025xTCXO.
53 to 56	RXID0 to RXID3				Output pins for Receive CDMA 4 bit A/D converter of I signal. RXID3 is the MSB.
57 to 60	RXQD0 to RXQD3				Output pins for Receive CDMA 4 bit A/D converter of Q signal. RXQD3 is the MSB.
61	RXFMSTRB				Strobe input pin for Receive FM 8 bit A/D converter.
62	FMCLK				Clock input pin for Receive FM 8 bit A/D converter.

Pin No.	Symbol	Typical Voltage (V)		Equivalent circuit	Description
		DC	AC		
63	RXQFMDT				Q serial data output pin for Receive FM 8bit A/D converter.
64	RXIFMDT				I serial data output pin for Receive FM 8bit A/D converter.
65 66	DNC				Don't connect any line to this pins.
67	GND ADC	0 V			Negative power supply pin for A/D converter block.
68	VDD ADC	3.3 V			Positive power supply pin for A/D converter block.
69	QOFFSET	1.5 V			Receive Q channel offset adjust input pin.
70	IOFFSET	1.5 V			Receive I channel offset adjust input pin.
71	HKADVCC	3.3 V			Positive power supply pin for HKA/D converter block.
72	NC				Don't connect pin.

Pin No.	Symbol	Typical Voltage (V)		Equivalent circuit	Description
		DC	AC		
73	ADCCLK				Clock output pin for House Keeping 8 bit A/D converter.
74	ADCDT				Serial data output pin for House Keeping 8 bit A/D converter.
75	ADCENBL				Enable input pin for House Keeping 8 bit A/D converter.
76	ADCIN	1.5 V			A/D analog input pin for House Keeping 8 bit A/D converter.

Pin No.	Symbol	Typical Voltage (V)		Equivalent circuit	Description
		DC	AC		
77 78 79	SLEEPB, IDLEB, FMB	0 V			Test mode switch pins. These pins control this IC function mode (*1).
80	RXVCOOUT				Receive VCO output pin connected the external PLL IC.

*1 Function Mode

Function Mode	FMB	IDLEB	SLEEPB
CDMA RXTX	high	high	high
CDMA Idle	high	low	high
CDMA Sleep	high	low	low
FM RXTX	low	high	high
FM Idle	low	low	high
FM Idle (Transition)	low	low	low
FM RXTX (Transition)	low	high	low
CDMA Sleep (Transition)	high	high	low

Mode functions explain:

1. CDMA RXTX :
   This mode requires everything except the FM-specific circuits to be operating.
2. CDMA Idle :
   This mode powers down all transmit circuits and FM receive.
3. CDMA Sleep :
   This mode powers down everything except the TCXO divider and TCXO/4 output driver.
4. FM RXTX :
   This mode powers down all CDMA-specific circuits except the CHIPx8 synthesizer.
5. FM Idle :
   This mode powers down all transmit and CDMA Receive circuits.

Electrical Characteristics

DC Characteristics (VDD=3.3 V±5 %, Ta=40 °C to 85 °C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply current - CDMA RXTX	IDD1			40	57	mA
Power supply current - CDMA Idle	IDD2			25	35	
Power supply current - CDMA sleep	IDD3			2	3	
Power supply current - FM RXTX	IDD4			30	45	
Power supply current - FM Idle	IDD5			16	21	
Logic High level input voltage	VIH	*1	0.7xVDD			V
Logic Low level input voltage	VIL	*1			0.3xVDD	
Logic High level output voltage	VOH	*1	2.7			
Logic Low level output voltage	VOL	*1			0.4	
Logic input Leakage current	IL	*1	–100		100	µA
Input capacitance Digital input	Cin-d	*1			15	pF
Load capacitance Digital output	Cl-d	*1			15	
Load resistance Digital output	Rl-d	*1	100 k			Ω

*1 : Logic Input pins = 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 61, 62, 75, 77, 78, 79
Logic Output pins =52, 53, 54, 55, 56, 57, 58, 59, 60, 63, 64, 73, 74

AC Characteristics

TXCLK/TXCLKB vs. TXIQDATA for CDMA mode VDD=3.3 V±5 %, Ta=–40 °C to 85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Data Setup to TXCLK/TXCLKB Transition	tsua			50		ns
Data Hold after TXCLK/TXCLKB Transition	tha			50		

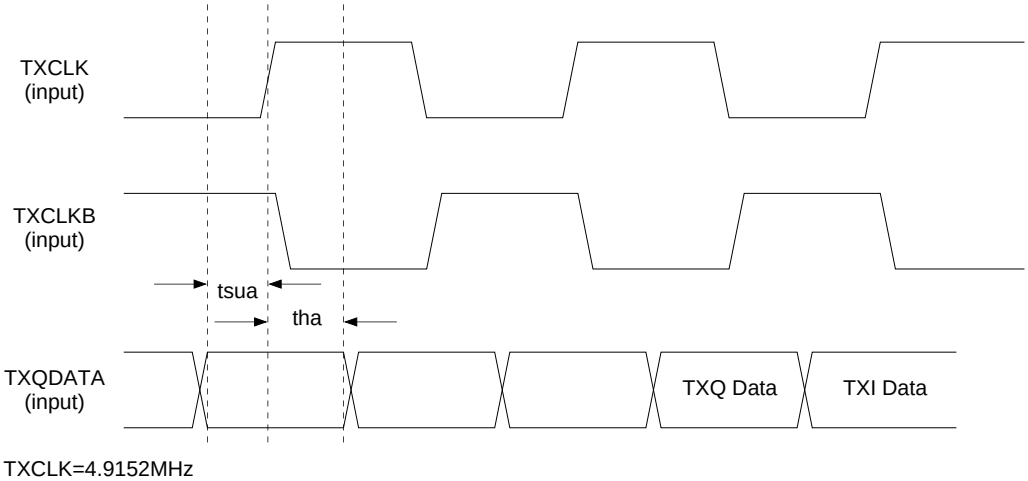


Fig. 1 TXCLK/TXCLKB vs. TXIQDATA Timing Diagram for CDMA mode

CHIPx8 vs. RXIQDATA VDD=3.3 V±5 %, Ta=–40 °C to 85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Data Output stable prior to CHIPx8 fall	tsub		20			ns
Data Hold after CHIPx8 fall	thb		15			
CHIPx8 raise time	trb	10 % to 90 %, Cload=15 pF	3	7.2		
CHIPx8 fall time	tfb		3	9.9		

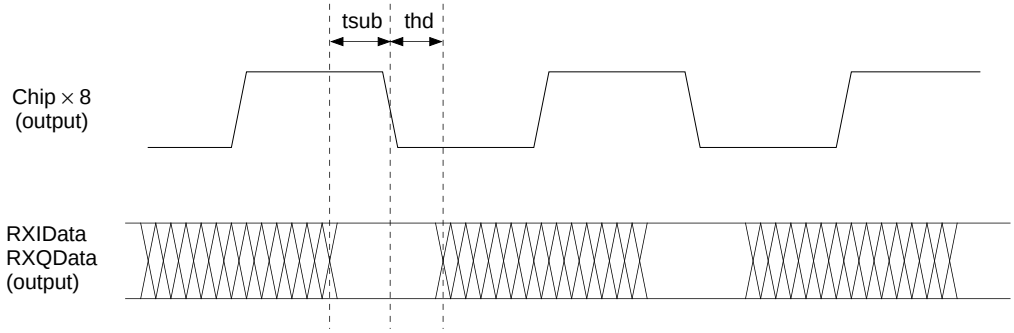


Fig. 2 CHIPx8 vs. RXIQDATA timing diagram

TXCLK vs. RXDATA for FM mode VDD=3.3 V±5 %, Ta=–40 °C to 85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Data setup to TXCLK transition	tsuc			2.08		µs
Data Hold after TXCLK transition	thc			2.08		

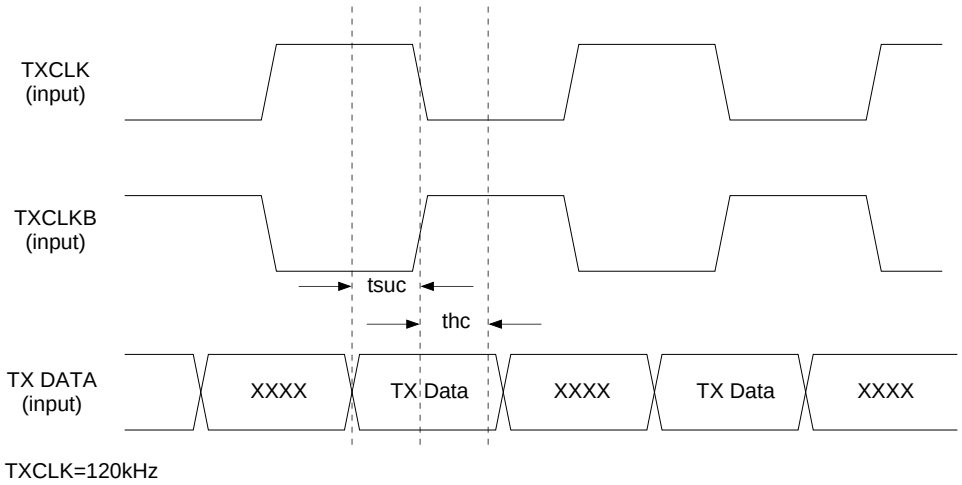


Fig. 3 TXCLK vs. RXDATA mode timing diagram for FM

FMCLK, RXFMSTROBE vs. RXFMDATA (I, Q) VDD=3.3 V±5 %, Ta=–40 °C to 85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Strobe input valid to CLK Falling Edge	tsud-s			0.69		µs
Strobe input valid after CLK Falling Edge	thd-s			2.08		
Data out valid to CLK Rising Edge	tsud-d			1.38		
Data out valid after CLK Rising Edge	thd-d			1.38		
CLK High Time	tclk-hi			1.38		
CLK Low Time	tclk-lo			1.38		
RXFMDATA (I, Q) raise time	trd	10 % to 90 %, Cload=15 pF	3	7.2		ns
RXFMDATA (I, Q) fall time	tfd		3	9.9		

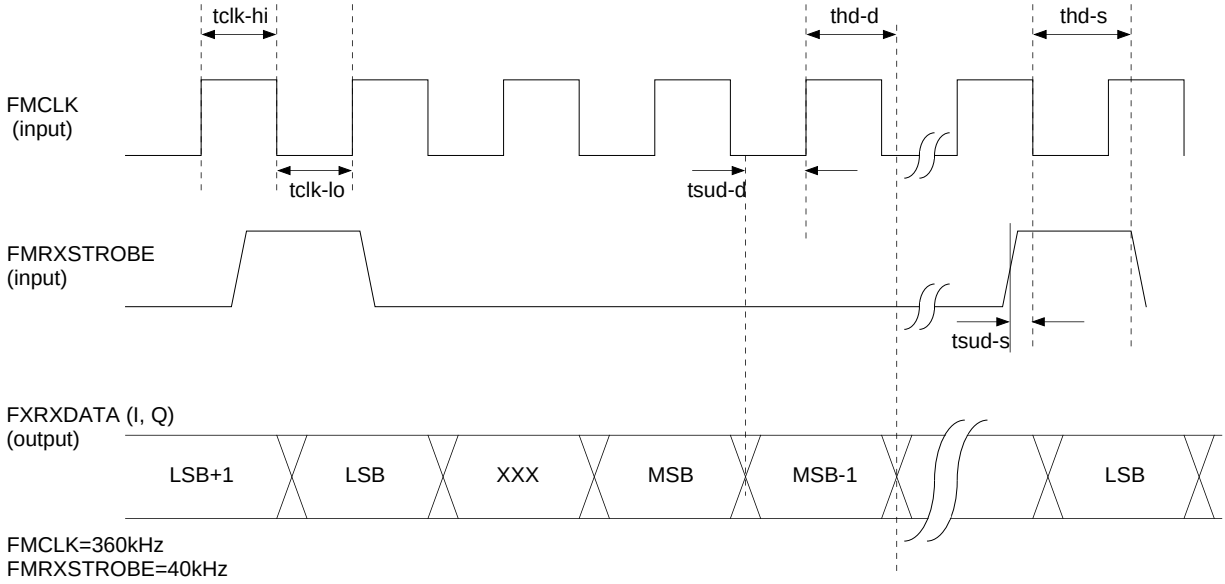
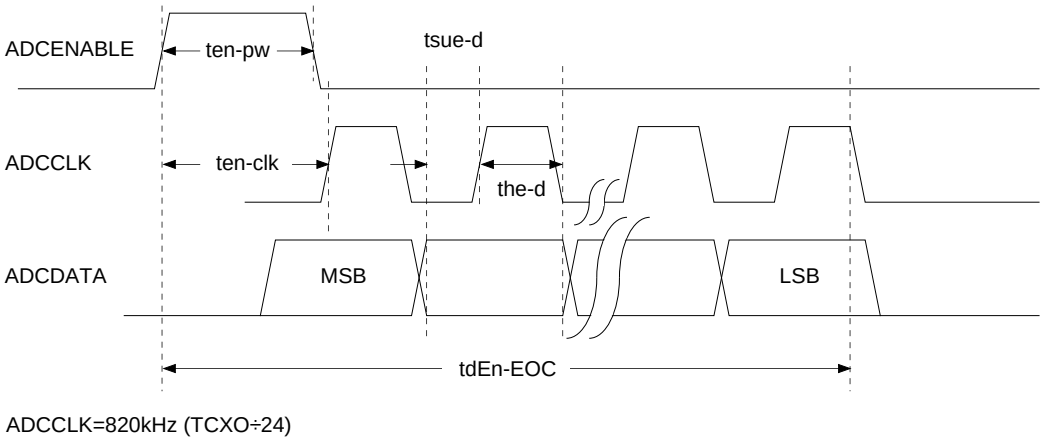


Fig. 4 FMCLK, FMRXSTROBE vs. RXFMDATA (I, Q) timing diagram

Note : FM RXSTROBE pulse width must be ≤ one FMCLK period.

ADCENABLE & ADC CLK vs. ADC DATA (VDD=3.3 V±5 %, Ta=–40 °C to 85 °C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Enable True to first Clock output	ten-clk			6		µs
Enable Pulse to end of conversion	tdEn-EOC			16.8		
Data out valid to CLK rising edge	tsue-d			600		ns
Data out valid after CLK rising edge	the-d			600		
Enable True Pulse width	ten-pw				10	µs
Output raise time	tre	10 % to 90 %, Cl=15 pF		7.2		ns
Output fall time	tfe			9.9		



ADCCLK=820kHz (TCXO÷24)

Fig. 5 ADCENABLE & ADC CLK vs. ADC DATA timing diagram

VHF Local Oscillator VDD=3.3 V±5 %, Ta=–40 °C to 85 °C

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
VCO output Frequency Range		fvcot			260.76		MHz
Lock mode charge pump Output Current		Icplt	Rset=40 kΩ	12.4	15.5	18.6	µA
Acquisition Mode charge pump Output Current		Icpat	Rset=40 kΩ	128	160	192	
Maximum Iout Adjustment Range		Icpmaxrt	Using Rset to vary nominal output current	–40		+40	%
Acquisition Mode Disable Frequency Range		∆fadt	Acquisition mode initiated only by transition to any TX active mode	–1 k		+1 k	Hz
Phase Detector Output Compliance Voltage		Vopdt		0.4		VDD–0.4	V
Phase Detector Output Impedance		Zopdt		1 M	2 M		Ω
Reference Input Frequency		freft			19.68		MHz
Phase Detector Frequency		fpdt	Ref.frequency/16		1.23		MHz
Reference Spurs		rst			–80		dBc
Lock Detect Pull Down Voltage		VLldt	Rload≥10 kΩ to VDD			0.4	V
Lock Detect Off Leakage Current		ILedt	Vo=VDD			10	µA
Phase Detect Unlock Threshold during FM	Deviation	PDfhdt	Measured at TXIF			12	kHz
	Rate	PDfhrt		300			Hz
Tank Circuit Input Impedance		Zit	Nominal Impedance into each pin	1.5 k	2 k	2.5 k	Ω
External VCO Input Levels		Vext		200	600	800	mVp-p

Receive VCO VDD=3.3 V±5 %, Ta=–40 °C to 85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
VCO output Frequency Range	fvcor			170.76		MHz
VCO Output Voltage Swing at 170 MHz	Vovr	Into 500 Ω//5 pF load, AC coupled load	100	147		mVrms
Tank Circuit Input Impedance	Zir	Nominal impedance into each pin	1.5 k	2 k	2.5 k	Ω

CDMA Receive VDD=3.3 V±5 %, Ta=–40 °C to 85 °C

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Input Signal Level	CDMA	Vincdcr			0.9		mVrms
	Sinusoid	Vinscr			5.38		mVp-p
Single Tone jammer Desense		Jdcr	≥900 kHz offset		0.13	0.5	dB
Input Center Frequency		ficcr			85.38	220.38	MHz
Input Resistance		Ricr	Differential	375	500	650	Ω
Input Capacitance		Cicr	From each pin to GND		1.5		pF
Input Referred Noise		IRNcr	Sum of I&Q,measured from 1 kHz to 630 kHz		70	135	µVrms
Spurious Content		SCcr	Total of all harmonic and non-harmonic power		–40	–25	dBc
Jammer Related Spurious Content		Jrscr	Peak in-band spurious products		–32	–18.4	dBc
Offset Adjust Gain		Gadjocr		–60	–50	–40	%Full scale/V
Offset Adjust Input Impedance		Ziocr		100 k	170 k	220 k	Ω
A/D Converter Linearity		Ladcr	Full scale				LSB
Signal Path Gain Accuracy, Part to Part		ΔGspcr	At nominal temp and VDD	–1.6		1.6	dB
Signal Path Gain Accuracy, Total		ΔGstcr	Over part to part, VDD, temp	–2.1		2.1	
CDMA RX Residual Sideband Product		RSpcr				21	dBc
Filter Attenuation		FA1cr	≥900 kHz	46	50		dB
		FA2cr	≥1.2 MHz	48	62		
Gain Flatness vs. Frequency		Gfcr	1 kHz to 630 kHz			2.0	dBp-p

CDMA Transmit VDD=3.3 V±5 %, Ta=–40 °C to 85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output Amplitude of Lower Sideband	Voct	I&Q in Quadrature Full Scale Signals.At nominal VDD and temp	267	300	337	mVp-p
Load Resistance	Rlct	Differential	495	500	505	Ω
Load Capacitance	Clct	From each pin to GND			5	pF
Output impedance	Zoct			40	50	Ω
Spurious Free Dynamic Range, In Band	Sfdr1ct		35	50		dBc
Spurious Free Dynamic Range,Bandedge	Sfdr2ct		30			
Spurious Free Dynamic Range, Out of Band	Sfdr3ct		57			
Carrier Suppression	Csct	I&Q in Quadrature, Full Scale Signals	18	32		
Spurious Free Dynamic Range :IF Harmonics	Sfdr5ct	Even Harmonics	20			
		Odd Harmonics	8	11		
Signal to Noise Ratio,Noise Band1	Snr1ct	IF±≥0.1 M to IF±<1.98 M	104	124		dBc/Hz
Signal to Noise Ratio,Noise Band2	Snr2ct	IF±≥1.98 M to IF±<44 M	117	124		
Output Center Frequency	focct			130.38		MHz
I, Q Gain Mismatch	Gerrct	In band, Measured at TX IF		0.2	0.8	dB
I, Q Phase Imbalance	Perrct	In band, Measured at TX IF		2	8	degree
Amplitude Flatness vs. Frequency, 1 kHz to 630 kHz	Afct	Including SIN(X)/X		0.6	1.0	dBp-p

CDMA CHIPX8 VDD=3.3 V±5 %, Ta=–40 °C to 85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Frequency	fic8	TCXO		19.68		MHz
Output Frequency	foc8	TCXO x 512/1025		9.8304		
Stabilization Time	tsc8	upon mode charge			10	µs

FM Receive VDD=3.3 V±5 %, Ta=–40 °C to 85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Signal Level	Vinfr			1.53		mVrms
Single Tone jammer Desense	Jdfr	60 kHz offset		0.07	0.35	dB
Input Center Frequency	ficfr			85.38		MHz
Input Resistance	Rifr	Differential	375	500	650	Ω
Input Capacitance	IRNfr	From each pin to GND		1.5		pF
Input Referred Noise	SCfr	Sum of I&Q,measured from 100 Hz to 15 kHz			38	µVrms
Spurious Content	Jrfr	At nominal temp		–56	–42	dBc
Jammer Related Spurious Content	Gadjfr	Peak in-band spurious product		–32	–18.4	
Offset Adjust Gain	ΔGspfr		–60	–50	–40	%Full scale/V
Signal Path Gain Accuracy, Part to Part	ΔGspfr	At nominal VDD and temp	–1.3		1.3	dB
Signal Path Gain Accuracy,Total	ΔGstfr	Over part to part ,VDD, temp	–2.1		2.1	
FM RX Residual Sideband Products	RSpfr		27			dBc
Gain Flatness vs. Frequency	Gffr	From 100 Hz to 12.2 kHz		0.4	1	dBp-p
Filter Attenuation	FA1fr	>45 kHz	48	68		dB
	FA2fr	>60 kHz	60	69		

FM Transmit VDD=3.3 V±5 %, Ta=–40 °C to 85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
IF Output Amplitude	Voifft	At nominal VDD and temp	124	140	161	mVp-p
IF Load Resistance	Rlifft	Differential	495	500	505	Ω
IF Load Capacitance	Clifft	From each pin to GND			5	pF
IF Output impedance	Zoft			40	50	Ω
IF Signal to Noise Ratio, Noise Band1	Snr1ft	IF±≥0.1 M to IF±<44 M	110	117		dBc/Hz
IF Output Amplitude Variation	Voifvft	Over part to part , VDD and temp	–1.6		1.6	dB
IF Output Amplitude Drift	ΔVoifdft	Over full VDD and temp ranges	–1		1	
Maximum Spurious Content : TX IF Harmonics	Sceft	Even Harmonics			–20	dBc
	Scoft	Odd Harmonics		–10.5	–8	
FM Mod Output Voltage	Vmodft	Full scale, nominal VDD and temp	490	575	610	mVp-p
FM Mod load Resistance	Rmodft		10 k			Ω
FM Mod Amplitude Variation	ΔVmodvft	Over part to part , VDD and temp	–1.2		1.2	dB
FM Mod Spurious Free Dynamic Range, to 120 kHz	Sfdrft	Two tone inputs	40	44		
FM Mod Signal to Noise Ratio, 1 kHz to 15 kHz	Shrfmodft	Single tone, full scale	87	100		dBc/Hz
Amplitude Flatness vs. Frequency, DC to 10 kHz	Afft	Including SIN (X) / X			0.6	dBp-p

TCXO VDD=3.3 V±5 %, Ta=–40 °C to 85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Frequency	fitc	From TCXO		19.68		MHz
Input Amplitude	Vitc	AC Coupled	0.5		2	Vp-p
Input Impedance	Zitc		5 k			Ω
TCXO Divide Ratio	Rtdtc			4		
TCXO / 4 Output Amplitude	Vo-tc	Into 10 kΩ // 10 pF AC coupled Load	1			Vp-p

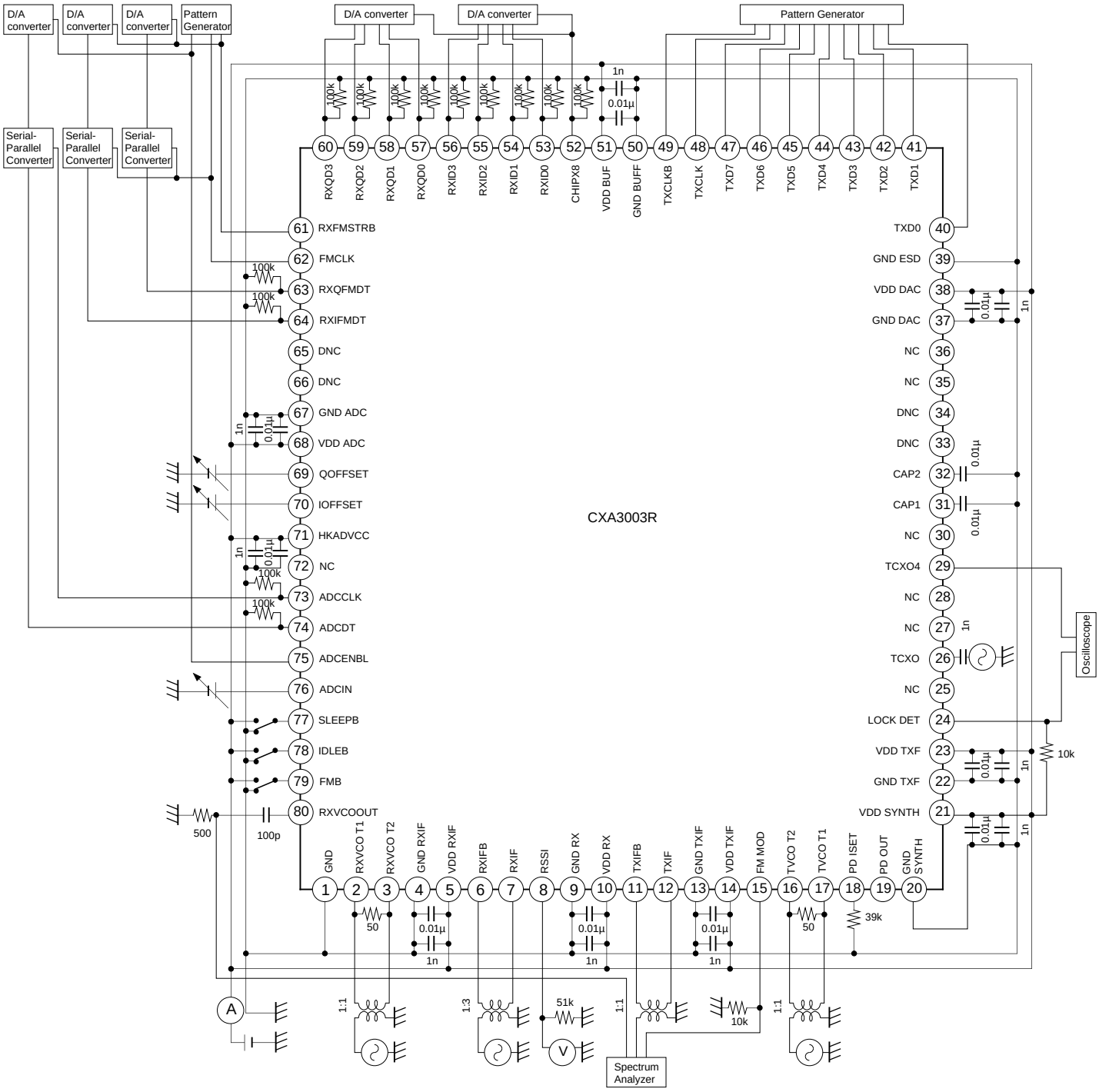
RSSI VDD=3.3 V±5 %, Ta=–40 °C to 85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Dynamic Range	DRrs		25			dB
Gain	Grs	At nominal temp and VDD	32		75	mV/dB
Gain Drift	ΔGdrs	Over VDD and Temp	–1.6		1.6	dB
Output Signal Level	Vors		0.5		2.5	V
Output Load Resistance	Rlrs		50 k			Ω
Full Scale Rise/Fall Time	trrs/tfrs				30	µs
Nominal Setpoint	Nsprs	At nominal temp and VDD	0.8		2.0	V

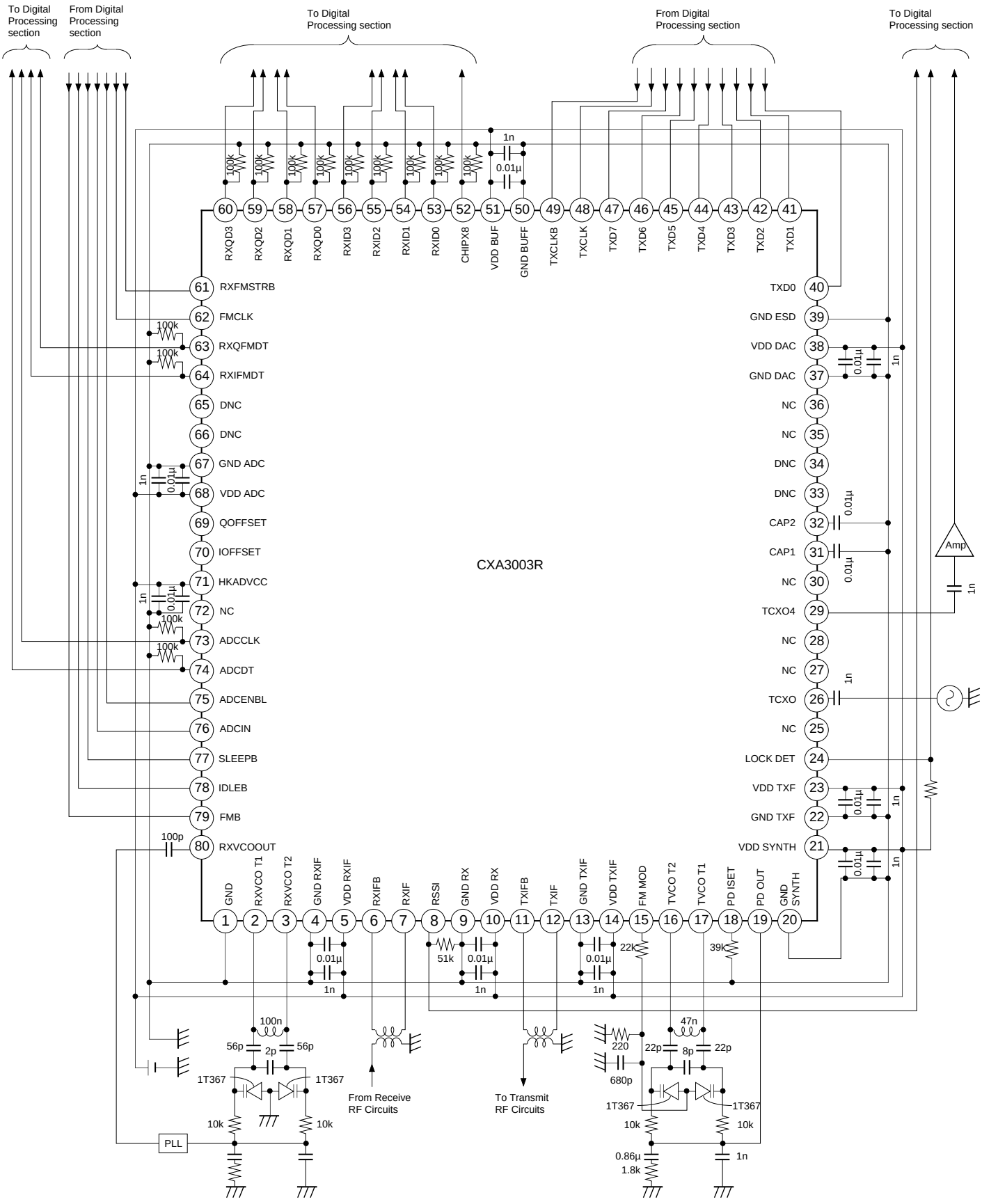
HK ADC VDD=3.3 V±5 %, Ta=–40 °C to 85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	Reshk		8			Bits
Input Voltage Range	Vihk	Internal Voltage referenced	1.79	2	2.24	V
Midscale Output Code Error	Emidhk	V (ADCIN)=1.5 V	–16		16	code
DLE	Dlehk		–1		1	LSB
ILE	Ilehk	At nominal temp and VDD	–1.25		1.25	
Conversion Time	tchk				40	µs
Input Impedance	Zihk		20 k			Ω

Electrical Characteristics Measurement Circuit



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

1. Overall operations

This IC bridges the gap between the analog RF processing and digital processing sections of the cellular telephone. Figure 6 illustrates the general circuit blocks in the portable cellular telephone employing this IC. The analog inputs and outputs of this IC interface directly with the IF (intermediate frequency) transmit/receive circuitry of the telephone. The digital inputs and outputs of this IC interface directly with the digital processing section.

The RF receive circuitry acquires the low-level forward link signal from the base station (cell site) and down-converts to the IF frequency band. The RF transmit circuitry takes CDMA or FM modulated analog IF from this IC, up-converts to the channel frequency, and outputs controlled reverse link power levels to the antenna.

The digital processing section includes CDMA modulation/demodulation , digital FM modulation/demodulation, voice processing, and a keypad interface. The CODEC (coder-decoder) block interfaces the telephone microphone and earpiece to the digital processing section.

This IC receive signal path down-converts the acquired IF signal to baseband where it is then converted to digital data. The digital baseband signals are sent to the digital processing section for demodulation. When transmitting, the digital processing section sends modulated digital baseband signals to this IC for up-conversion to the analog IF frequency.

This IC consists of a receive signal path, a transmit signal path, clock synthesis and buffering circuits, mode control logic, and a House Keeping analog-to-digital converter (ADC).

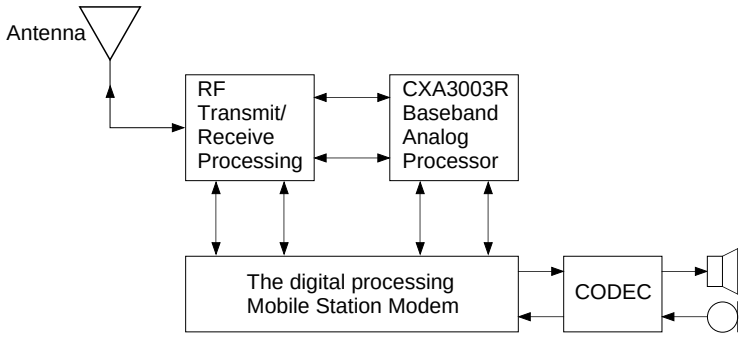


Fig. 6 Dual-mode CDMA/FM cellular Telephone Block

2. CDMA Receive Signal Path

This IC receive signal path (see Fig.7) is designed to accept a differential IF signal with CDMA spread spectrum modulation extending ±630 kHz from the IF center frequency of 85.38 MHz. The incoming IF is reduced to I and Q baseband components by mixing with 85.38 MHz local oscillator (LO) signals in quadrature followed by low-pass filtering.

The 85.38 MHz I and Q LO signals are generated on this IC. The receive VCO is set 170.76 MHz by an external varactor-tuned resonant tank circuit (inductor L and capacitor C connected in parallel). An external phase-lock loop and loop filter network provide the feedback to the varactors which tune the VCO to 170.76 MHz. A master-slave divide-by-two circuit generates I and Q signals in precise quadrature for the mixers.

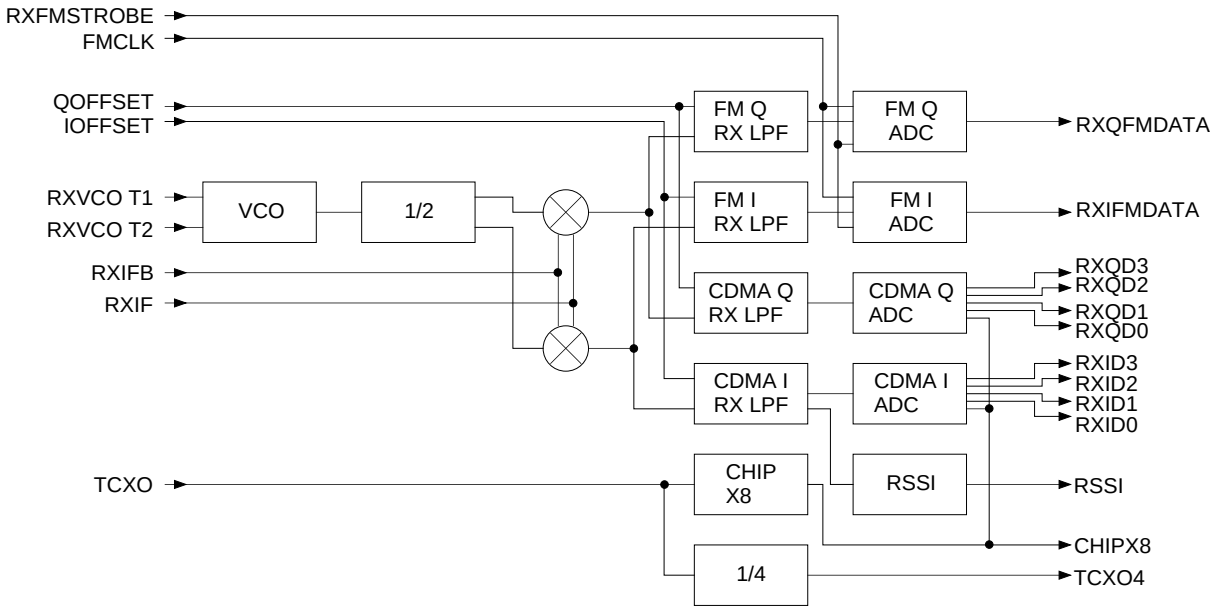


Fig. 7 Receive Section Block Diagram of CXA3003R

3. CDMA Low-Pass Filtering

After mixing, the receive signal path splits into CDMA and FM sections. For CDMA, the baseband signal extends from 1 kHz to 630 kHz. Frequency components above 750 kHz are out-of-band for CDMA operation. The mixers and the subsequent CDMA low-pass filters combine to form the down-converter which outputs the CDMA baseband signals. The passband, transition band, and rejection band characteristics of these low-pass filters, in conjunction with external IF bandpass filtering, contribute to the ability of the receiver to select the desired baseband signals from the jamming effects of unwanted signals.

The need to control the offset at the inputs of the ADCs is critical to the receive signal path and the digital processing section. The offset control inputs : IOFFSET and QOFFSET, are provided for this purpose.

4. CDMA Analog-to-Digital Conversion

Analog I and Q baseband components are converted to digital signals by the two identical 4-bit flash (parallel) ADCs. The CDMA ADCs output a new digital value on each falling edge of the ADC clock signal, CHIPx8.

The CHIPx8 ADC clock frequency of 9.8304 MHz is synthesized from the system crystal oscillator frequency of 19.68 MHz. The system crystal oscillator frequency is applied to the TCXO input of this IC.

5. FM Receive Signal Path

The receive signal path for FM operation is similar to that for CDMA operation. Differences lie in the characteristics of the I and Q low-pass filters and the ADCs. The IF frequency is the same as in CDMA (85.38 MHz), but the modulation can only extend ±15 kHz from the IF center frequency, forming a 30 kHz wide channel. The low-pass filters for FM operation have a much lower bandwidth than those used in CDMA. The offset of the FM low-pass filters is controlled just like the CDMA low-pass filters by the IOFFSET and QOFFSET input pins.

The lower bandwidth of the FM baseband signal gives rise to the use of very low power 8-bit successive-approximation ADCs. The FM I and Q analog baseband signals are sampled and held during the analog to digital (A/D) conversion process. The A/D conversion is initiated with a external strobe signal. A serial data stream is output beginning with the most significant bit (MSB) of the result.

6. CDMA Transmit Signal Path

This IC transmit signal path (see Fig.8) accepts digital I and Q baseband data from the digital processing section and outputs modulated IF centered at 130.38 MHz to the RF transmitter.

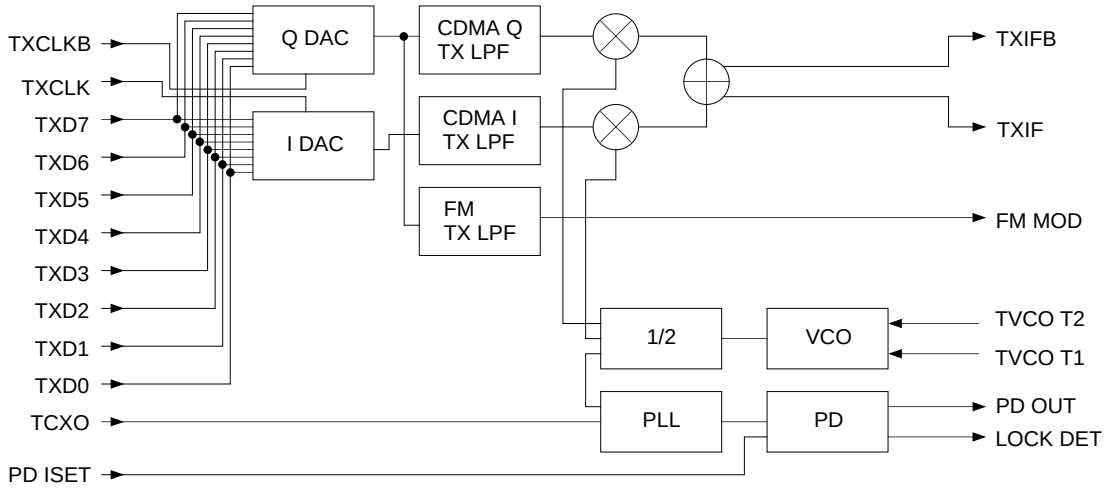


Fig. 8 Transmit Section Block Diagram of CXA3003R

7. CDMA Digital to Analog Conversion and Filters

Eight bits of I and Q transmit data are input to the CDMA digital to analog converters (DACs) by multiplexing over an 8-bit input port on the this IC. The transmit data rate is twice as fast as the differential transmit clock, TXCLK and TXCLKB. Incoming data that is valid during the rising edge of the transmit clock is registered into the I DAC. Incoming data that is valid during the falling edge of the transmit clock is registered into the Q DAC. I and Q transmit data values have been compensated in the digital processing section to account for their 1/2 clock cycle time difference.

The frequency spectrum at the output of the CDMA DACs contains unwanted frequency components due to DAC output transition edges and transients. The transmit clock frequency and harmonics are found in the spectrum and are also undesirable. Each CDMA DAC is followed by an anti-aliasing low-pass filter with a bandwidth of 630 kHz that reduces unwanted frequency components. Unlike the low-pass filters in the receive signal path, these do not require offset controls.

8. Up-Converting to IF

This IC transmit path outputs a differential IF signal with CDMA spread spectrum modulation extending ±630 kHz from the transmit IF center frequency of 130.38 MHz. The analog I and Q baseband components from the CDMA low-pass filters are mixed in quadrature with I and Q LO signals at 130.38 MHz. After mixing, the I and Q IF components are summed and output differentially.

The 130.38 MHz I and Q LO signals are generated on this IC. The transmit VCO is set to 260.76 MHz by an external varactor-tuned resonant tank circuit. An internal phase-lock loop and external loop filter network provides the feedback to the varactors which tune the VCO precisely to 260.76 MHz. A master-slave divide-by-two circuit generates I and Q signals in precise quadrature for the mixers.

9. FM Transmit Signal Path

An analog FM modulation signal is constructed from 8-bit digital data supplied by the digital processing section. Only the Q-channel DAC is used in this IC in FM mode, all other CDMA circuits are disabled. The DAC output is filtered by a low-pass anti-aliasing filter. The filtered DAC output is the analog FM modulation signal, FM MOD. This signal modulates the frequency of this IC transmit VCO using external components when in FM RXTX Mode.

10. Operating Modes

This IC has several modes of operation. The CDMA RXTX or FM RXTX modes are in effect when the telephone is making a call. IDLE mode is in effect when no call is in progress but the telephone receiver is active (ready to answer a call). SLEEP mode is a low-power mode in which the telephone cannot receive a call.

This IC operating modes are defined by the states of three digital inputs: FMB, IDLEB, and SLEEPB. The power consumed by this IC is minimized by controlling these logic signals and disabling unused circuits. The selected circuits in this IC become active after the states of the operating mode controls are changed.

11. House Keeping ADC

The House Keeping ADC provides DC measurement capability to the telephone. It is a low speed, 8-bit resolution, successive approximation analog-to-digital converter. It is designed to digitize DC voltages applied to the ADCIN pin from battery level, temperature, and other low frequency control or monitoring sensors.

This ADC is in a power-down state during normal operation. It is activated by a positive-going pulse on ADCENBL. When this input is driven high, the House Keeping ADC powers up, samples and holds the voltage applied to ADCIN, and begins a conversion. The ADC output is available from a serial digital interface. Each of the eight data bits is valid (MSB first) during the rising edge of the ADCCLK output. A rising edge of ADCENBL during a conversion will be ignored. ADCENBL must be low and a conversion completed before a new conversion can be started.

Notes of Operation

1. Signal operation

   The CXA3003R needs the master system clock “TCXO” that comes from a crystal oscillator at 19.68 MHz. A divide-by-4 derivative of TCXO called TCXO/4 operates as long as TCXO is active and power is applied to CXA3003R. Transmit and receive IF frequencies are generated by varactor-tuned TX and RX local oscillators on CXA3003R. CHIPx8, a derivative of TCXO is active for all operating modes except CDMA SLEEP and FM IDLE.

2. Receive IF Inputs

   The receive IF inputs, RXIF and RXIFB, differentially drive a input stage within the CXA3003R. The differential input impedance is nominally 500 Ω. The IF signals receive by AC coupling. AC coupling capacitor values (0.001 µF) are chosen to maximize the power transfer from receive IF circuitry.

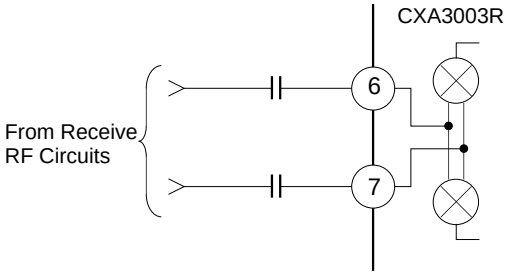


Fig. 9 Receive IF Inputs

3. Transmit IF Outputs

   The transmit IF outputs, TXIF and TXIFB, are differential outputs. The output impedance is low, 40 Ω, nominally. These signals transfer to the subsequent transmit IF circuitry by using AC coupling. AC coupling capacitor values (0.001 µF) are chosen to maximize the power transfer from the CXA3003R to the subsequent transmit IF circuitry.

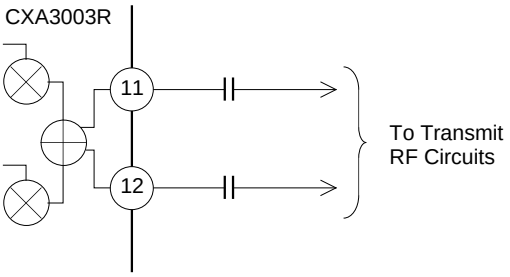


Fig. 10 Transmit IF Outputs

4. VCOs

In general terms, the frequency of oscillation, fo, for the VCOs is determined by:

$$fo = \frac{1}{2\pi\sqrt{LC}}$$

Where L and C are the net inductance and Capacitance of the external resonant tank circuit. The resonant tank circuit comprises inductor L connected in parallel with capacitance C. The tank circuit is connected between RXVCO T1 and RXVCO T2 (shown in Fig.11). Another tank circuit is connected between TXVCO T1 and TXVCO T2 (shown in Fig.12).

The net capacitance of the tank circuit comprises a varactor diode (CV), an optional scaling capacitor connected (CV2) in parallel with the varactors, two DC blocking capacitors (CB) isolating the DC bias of the varactors from the CXA3003R, and pin-to-pin and pin-to-ground parasitic capacitors (CPP, CPG) (shown in Fig.13). The net tank capacitance is found from

$$C = \frac{(C_{V2} + 1/2 \cdot C_V) \times C_B}{(C_{V2} + 1/2 \cdot C_V) \times 2 + C_B} + (C_{PP} + \frac{C_{PG}}{2})$$

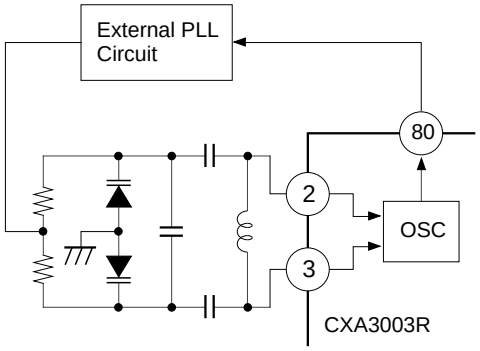


Fig. 11 Receive VCO

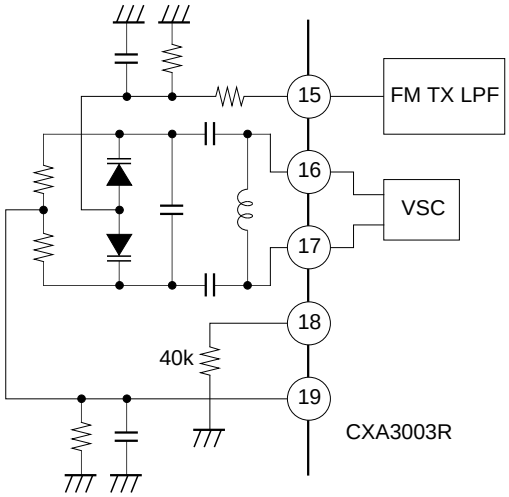


Fig. 12 Transmit VCO

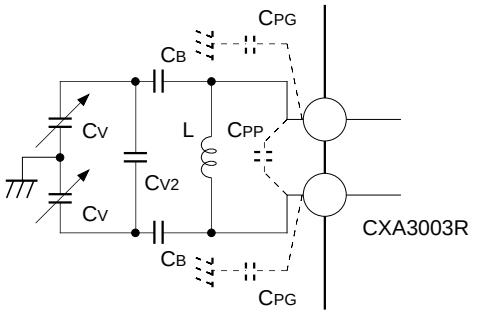


Fig. 13 VCO capacitors

5. Transmit VCO Synthesizer

The transmit synthesizer consists of a VCO, a divide-by-two phase splitter, divide by R and N counters, and a phase detector. The VCO and divide-by-two generate the I and Q IF signals used to up-convert analog baseband to IF. The loop filter and tuning components are external to the CXA3003R.

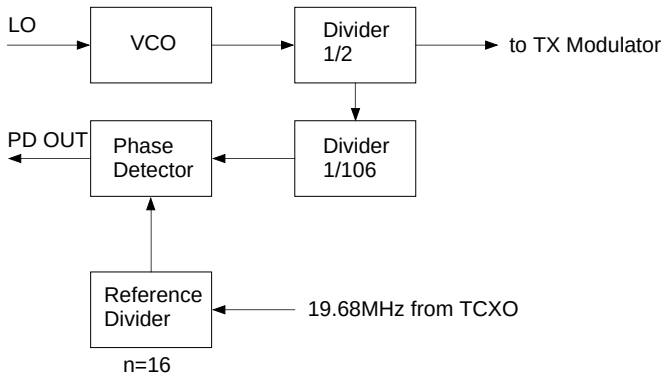


Fig. 14 Transmit VCO synthesizer

6. Transmit VCO Phase Detector

The phase detector output, PD OUT, is the output of a dual mode bi-directional charge pump. It provides two levels of output current for frequency acquisition (±175 µA) and phase lock maintenance (±16 µA) after the VCO frequency is at or near its final frequency. The phase detector also provides a lock detect output, LOCK. This signal is low when unlocked, and high (high-impedance) when unused or in IDLE or SLEEP Modes. LOCK will indicate the unlocked condition until the VCO frequency is at its final value. LOCK will then toggle until phase lock has been established.

The current available from PD OUT is set by an external resistor connected between PD ISET and ground (shown in Fig. 12). The value of the PD ISET resistor is determined by

$$R_{PD} = 0.64/I_O$$

Where Io is the current available for maintaining the transmit VCO frequency. During acquisition of the IF frequency, the current limit from PD OUT increases to 11 times that set by the resistor on PD ISET. A recommended Io of 16.3 µA results in R_{PD}=39 kΩ ±1 %.

7. FM Modulation Scaling

The FMMOD output is used to frequency modulate the transmit VCO. The output voltage swing on FM MOD is normally 550 mVp-p. This modulating voltage must be scaled to achieve the required frequency deviation of the transmit VCO frequency when the CXA3003R is operating in FM mode. A ±30 kHz deviation of the transmit VCO frequency translates into a ±15 kHz deviation of the transmit IF frequency. A simple resistive voltage divider may be used as long as the total load on FM MOD is greater than 10 kΩ. The output of the voltage divider drives the anode side of the varactor diodes (shown in Fig. 12).

8. TCXO

The temperature-compensated crystal oscillator (TCXO) used in the telephone must provide a stable and accurate 19.68 MHz signal to the TCXO input of the CXA3003R.

The specifications for this oscillator are outlined in table 1.

Power Supply Voltage	3.3 V	fout vs. load	±0.2 ppm
Output level	0.8 Vp-p min	fout phase noise	–120 dBc/Hz min (100 Hz offset)
Output load	10 kΩ min 10 pF max	Frequency control range	235±60 Hz
fout nominal frequency	19.68 MHz	Control voltage range	+0.5 tp +2.5 V
fout vs. temperature	±2 ppm/°C	Control voltage input impedance	100 kΩ min
fout vs. power supply	±0.3 ppm/V		

Table 1 TCXO Oscillator requirements

9. ADC and DAC Ranges

All ADCs and DACs on the CXA3003R have internally-generated references which eliminate the need for additional adjustment or calibration of the ADCs and DACs. All ADCs and DACs employ offset-binary coding (Tables 2 and 3). The application of the House Keeping ADC is left up to the user. However, it can be useful for monitoring parameters such as battery voltage and temperature. The midpoint of the input voltage range of the House Keeping ADC is set to 1.5 V by an internal voltage reference. The input voltage range of the ADC is 2.0 V. The gain of the ADC approximately 7.8 µ V/step.

Table 2 ADC Output Coding

Input Voltage		Output Data	Input Voltage	Output Data
FM Receive ADC	House Keeping ADC	MSB……LSB	CDMA Receive ADC	MSB…LSB
Greater than positive full-scale	>2.500	1111 1111	Greater than positive full-scale	1111
Positive full-scale	2.500	1111 1111	Positive full-scale	1111
99.6 % of full-scale	2.492	1111 1110	93.7 % of full-scale	1110
… …	… …	… …	… …	…
50.2 % of full-scale	1.504	1000 0000	53.3 % of full-scale	1000
49.8 % of full-scale	1.496	0111 1111	46.7 % of full-scale	0111
… …	… …	… …	… …	…
0.4 % of full-scale	0.508	0000 0001	6.7 % of full-scale	0001
Negative full-scale	0.500	0000 0000	Negative full-scale	0000
Less than negative full-scale	<0.500	0000 0000	Less than negative full-scale	0000

Table 3 DAC Input Coding

Input Data	Output Voltage
MSB… …LSB	FM Transmit DAC
1111 1111	Positive full-scale
1111 1110	99.6 % of full-scale
… …	… …
1000 0000	50.2 % of full-scale
0111 1111	49.8 % of full-scale
… …	… …
0000 0001	0.4 % of full-scale
0000 0000	Negative full-scale

10. ADC Offset Control

The external DC voltages connected to IOFFSET and QOFFSET pins control the output of the CDMA and FM low-pass filters to the center of the CDMA and FM ADC input range, reducing the offset to zero.

11. Receive Low Pass Filters

In CXA3003R, the receive low-pass filters remove residual IF frequency components and present baseband I and Q components to the ADCs. The CDMA baseband signal extends from 1 kHz to 630 kHz. The FM baseband signal extends from 100 Hz to 14 kHz. The low-pass filters reject frequency components above the passband while exhibiting a specific rate of attenuation in the transition band.

For FM Receive Filters two external bypass capacitors are required between pin 31 and GND,and between pin 32 and GND as is shown in Fig.15.

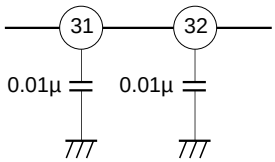


Fig. 15 FM Receive Filter

12. Transmit Signal Path Low-Pass Filters

Low-pass filters in the transmit signal path located after the transmit DACs attenuate much of the out-of-band frequency components created by digital-to-analog conversion process. These filters are relatively simple compared to the CDMA and FM low-pass filters found in the receive signal path. Since the gain of the transmit signal path is low, the offset at the filter outputs are less critical. Transmit filter offsets are not controlled as offsets are in the CDMA and FM receive paths.

13. Power Supply Considerations, Grounding, and Decoupling

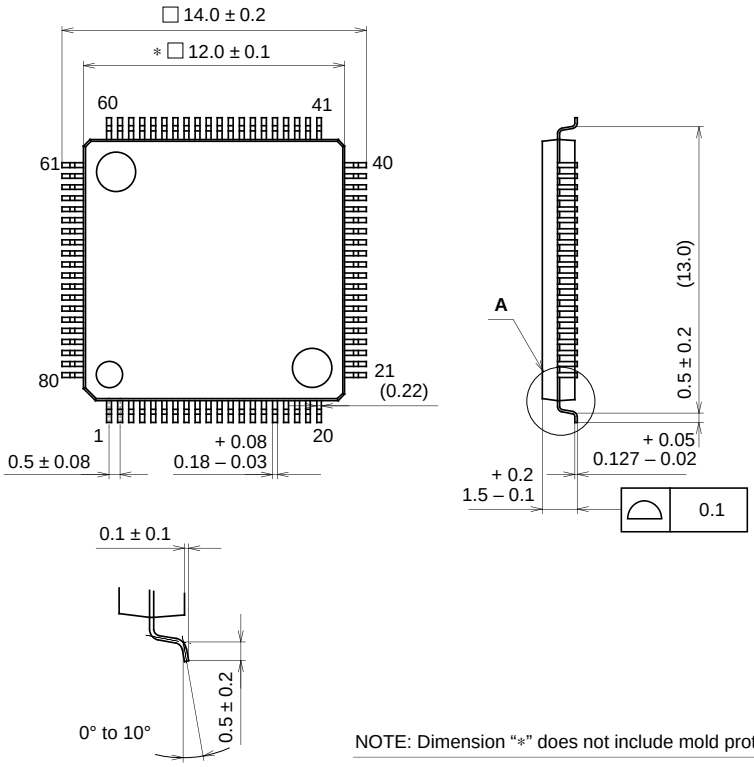
The CXA3003R is targeted for use in battery operated CDMA/FM portable cellular telephones. As such, the device has been designed to operate from a regulated 3.3 V power supply. The use of multiple voltage regulators is recommended throughout the telephone, but the CXA3003R should be powered from only one dedicated voltage regulator. Individual voltage regulators are usually assigned to the major circuit subsections within the (i.e. receive RF, transmit RF, power amplifier, CXA3003R, etc.) to reduce the possibility of signals from one subsection interfering with or distorting signals from another subsection. The voltage regulator used in telephone for the CXA3003R should be a linear voltage regulator, not a switching regulator. This is to keep power supply noise on the CXA3003R power inputs as low as possible. The recommended power supply voltage range of the CXA3003R is from 3.13 to 3.47 V (3.3±5 %). It is recommended that a ±2 % accurate regulator be used so that the proper output voltage can be maintained over the temperature range of the telephone and over the power supply current range of the CXA3003R.

Power supply decoupling around the CXA3003R is done with 0.01 µF ceramic chip capacitors on each VDD pin. The capacitors are located as close to the pins as possible to minimize series inductance in the connection to the pin. The use of additional 0.001 µF decoupling capacitors in parallel with the 0.01 µF capacitors is recommended to further reduce high frequency noise on the power supply inputs to the CXA3003R.

Although the CXA3003R has both analog and digital circuits and separate digital power and ground pins a single ground plane is recommended. The ground plane must overlap the footprint of the CXA3003R as much as possible. ALL CXA3003R ground pins must be connected to the same analog ground plane.

Package Outline Unit : mm

80PIN LQFP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

DETAIL **A**

SONY CODE	LQFP-80P-L01
EIAJ CODE	∗QFP080-P-1212-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.5g