SONY

CXA1481AQ/AR

8 mm VCR ATF

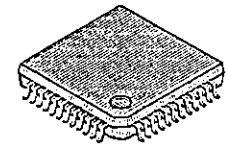
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Description

The CXA1481AQ/AR is an IC developed for the ATF* in 8mm VCRs. Combined with the microcomputer (CXP80620/CXP80624), complete ATF processing is enabled.

* ATF: Automatic Track Finding

CXA1481AQ
48pin QFP (Plastic)



CXA1481AR
48pin VQFP (Plastic)



Features

- Dramatic reduction of peripheral components due to the adoption of new functions
  - —On-chip SP/LP discrimination circuit for special playback mode
  - —On-chip clog detection circuit
- Optimum function allotment of the microcomputer (CXP80620/CXP80624)
  - —Microcomputer creates recording pilots (f_1 to f_4) input into CXA1481AQ/AR
- On-chip playback pilot LPF and recording pilot LPF
- f_H and $3f_H$ subtracter enables minimum DC offset (±30mV)
- PCM post-recording compatible
  Enables pilot recording during playback
- Low current consumption (Reference value: 7.5mA during REC, 16mA during PB)

Applications

8mm VCR

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings

• Supply voltage	V_{CC}	7	V
• Operating temperature	T_{opr}	−10 to +75	°C
• Storage temperature	T_{stg}	−55 to +125	°C
• Allowable power dissipation	P_D	CXA1481AQ 700	mW
		CXA1481AR 540	mW

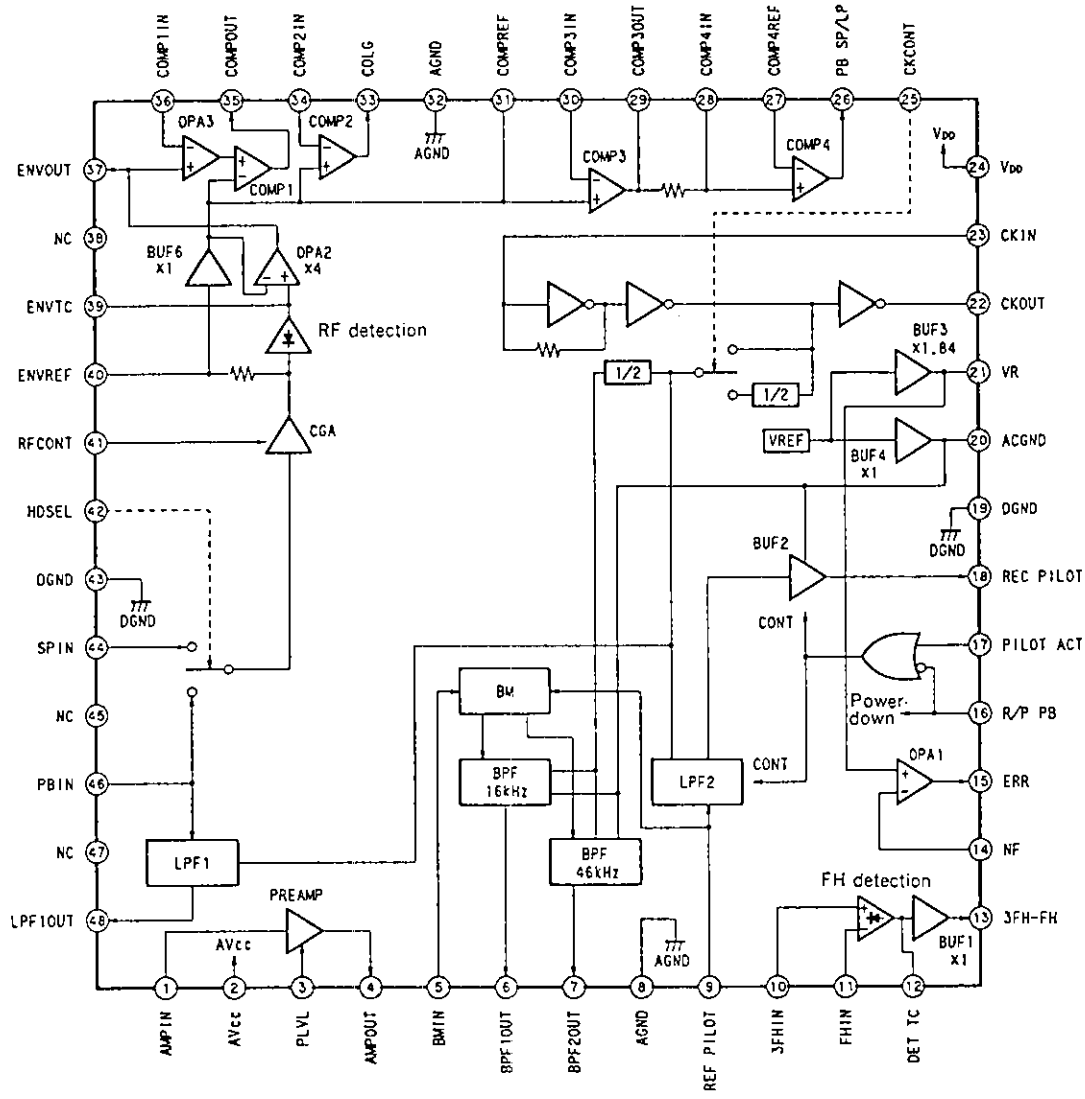
Operating Condition

Supply voltage	V_{CC}	$4.75^{+0.75}_{-0.25}$	V

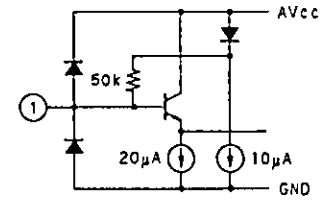
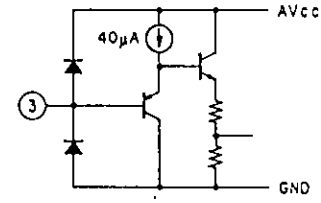
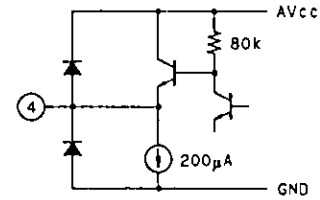
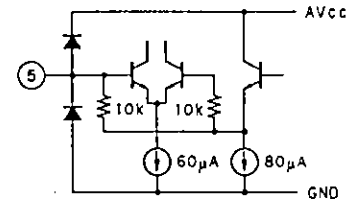
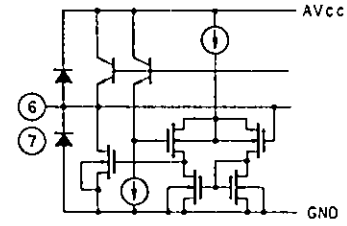
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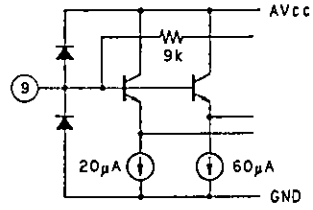
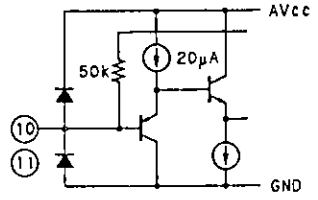
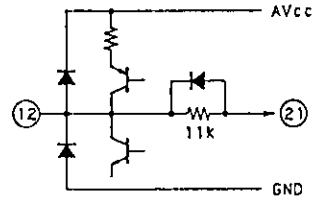
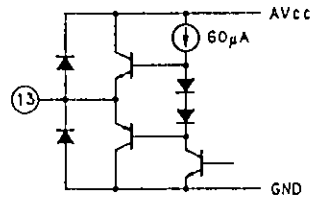
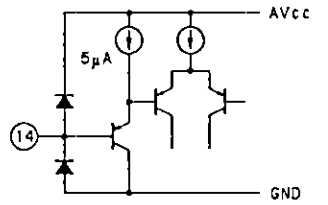
E92Y18A33-HP

Block Diagram and Pin Configuration

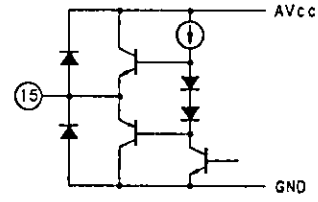
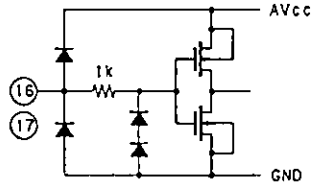
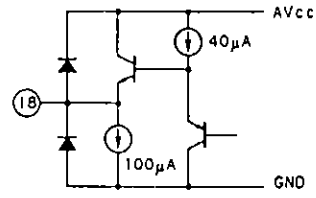
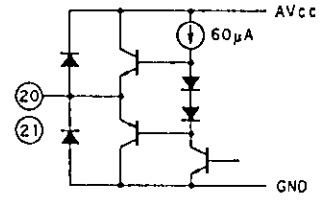
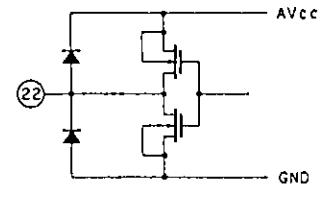


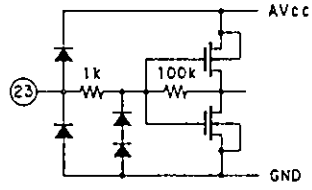
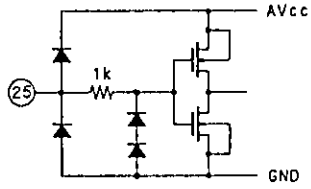
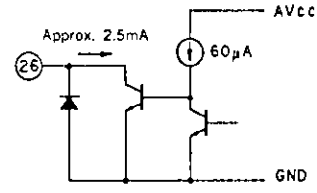
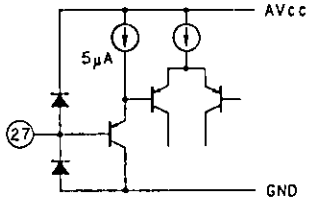
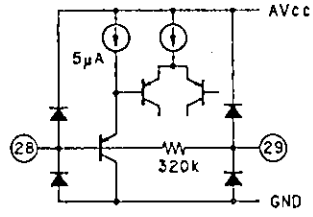
Pin Description (AV_{CC} · V_{DD} = 4.75V, Ta=25°C, * externally applied voltage)

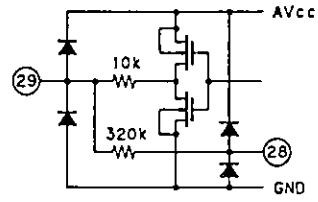
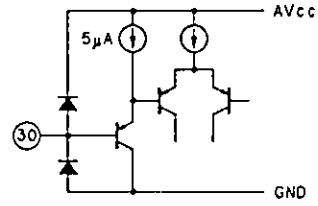
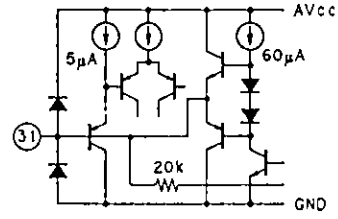
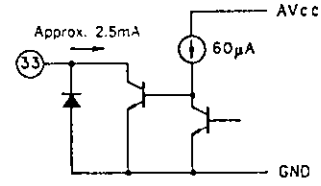
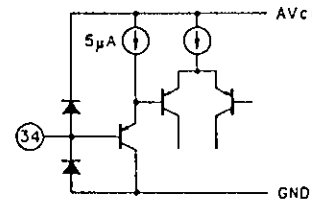
Pin No.	Symbol	Pin voltage DC	Pin voltage AC	Equivalent circuit	I/O impedance	Description
1	AMPIN	4.0V Typ.	3 to 25mV_{P-P}		50kΩ	Preamplifier input
2	AV_{CC}	* 4.75V	—		—	Analog system power supply
3	PLVL	* 0.8 to 3.3V	—		—	Gain control for pre-amplifier. Gain of pre-amplifier will change with the application of DC voltage.
4	AMPOUT	3.0V Typ.	—		650Ω	Preamplifier output
5	BM IN	1.6V Typ.	Approx. 30m V_{P-P}		10kΩ	Balance modulator input
6	BPF1 OUT	1.25V Typ	$2V_{P-P}$ and below		≃0Ω	BPF16k output
7	BPF2 OUT					BPF46k output
8	AGND	0V	—		—	Filter circuit GND

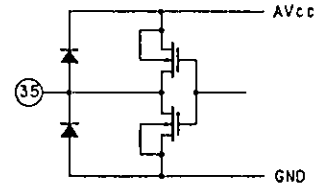
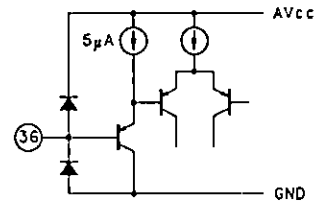
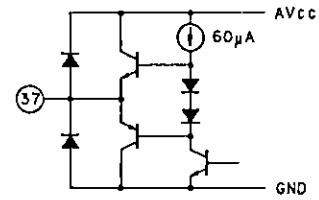
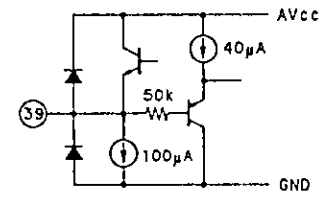
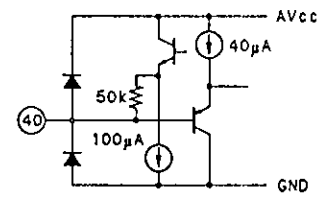
Pin No.	Symbol	Pin voltage DC	Pin voltage AC	Equivalent circuit	I/O impedance	Description
9	REF PILOT	2.3V Typ.	Approx. $0.8V_{P-P}$		9kΩ	Input for reference pilot signal. Maximum input level is $1VP_{P-P}$
10	3FHIN	2.3V Typ.	2.0V and below		50kΩ	3FH signal input. Connect by capacitance coupling with Pin 7.
11	FHIN					FH signal input. Connect by capacitance coupling with Pin 6.
12	DET TC	2.3V Typ.	—		11kΩ	Capacitance connection for FH detection circuit. Do not obtain output from this pin as impedance is high.
13	3FH·FH	2.3V Typ.	—		S.E.P.P.	FH detection circuit output
14	NF	* ≒2.3V	—		—	Inverted input for operational amplifier of FH detective circuit output

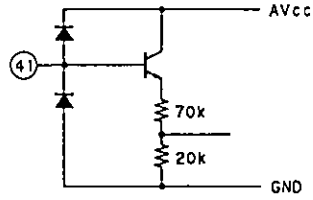
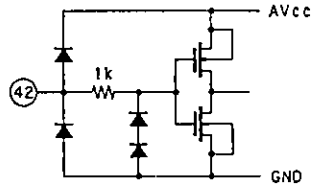
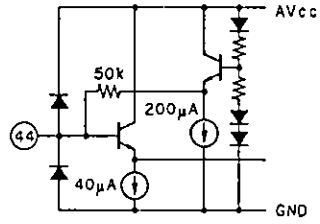
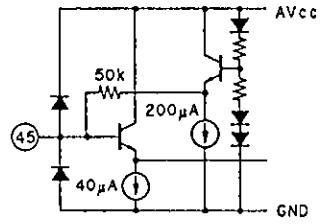
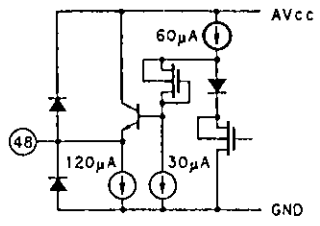
S.E.P.P. (SINGLE ENDED push — pull)

Pin No.	Symbol	Pin voltage DC	Pin voltage AC	Equivalent circuit	I/O impedance	Description
15	ERR	2.3V Typ.	—		S.E.P.P.	Operational amplifier output for the FH detection circuit output
16	R/P PB	High ≧ 2.0V Low ≦ 0.8V	—		—	Mode control. High (≧2.0V) : playback Low (≦0.8V) : recording
17	PILOT ACT	High≧2.0V Low≦0.8V				Pilot signal output control. High (≧2.0V) : pilot signal is output Low (≦0.8V) : pilot signal is not output
18	REC PILOT	Pins 16, 17, 18 Pin voltage L L 1.25V L H 1.25V H L 0.8V H H 1.25V	Approx. $0.5V_{P-P}$		260Ω	Pilot signal output
19	DGND	0V				Digital system GND
20	ACGND	1.25V Typ.	—		S.E.P.P.	Electric potential for BPF operating point
21	VR	2.3V Typ.				Electric potential for FH detection operating point
22	CKOUT	—	High≧ $V_{CC}-0.5V$ Low≦0.5V		100Ω	Crystal oscillator connection (output)

Pin No.	Symbol	Pin voltage DC	Pin voltage AC	Equivalent circuit	I/O impedance	Description
23	CKIN	2.0V Typ.	* $0.2V_{P-P}$ and above		95kΩ	Crystal oscillator connection (input). External clock input.
24	V_{DD}	* 4.75V	—	—	—	Power supply for digital system
25	CKCONT	High≧2.0V Low≦0.8V	—		—	Clock frequency demultiplication ratio switch. High (≧2.0V) : 5.94755MHz Low (≦0.8V) : 11.8951MHz
26	PB SP /LP	High≧4.25V Low≦0.5V When 100kΩ is connected between V_{CC} and Pin 26	—		—	This pin is as follows during variable speed playback : SP mode → High LP mode → Low "Low" during normal playback.
27	COMP4 REF	* 0.0V to V_{CC}-1.6V	—		—	Threshold level setting for LP/SP discrimination during special playback
28	COMP4 IN	* 0.0V to V_{CC}-1.6V	—		330kΩ	Integral capacitance connection

Pin No.	Symbol	Pin voltage DC	Pin voltage AC	Equivalent circuit	I/O impedance	Description
29	COMP3 OUT	High≧ V_{CC}−0.5V Low≦0.5V	—		10kΩ	COMP3 output
30	COMP3 IN	* 0.0V to V_{CC}-1.6V	—		—	Input for DC shifted envelope signal
31	COMP REF	1.3V Typ.	—		S.E.P.P.	Reference voltage output for comparator. (COMP1, 2, 3)
32	AGND	0V	—		—	Analog circuit GND
33	CLOG	High≧4.25V Low≦0.5V When 100kΩ is connected between V_{CC} and Pin 33	—		—	Analog detection circuit Clog detection output. ⎧Clogged state: High ⎩Normal state: Low
34	COMP2 IN	* 0.0V to V_{CC}-1.6V	—		—	Comparator 2 input

Pin No.	Symbol	Pin voltage DC	Pin voltage AC	Equivalent circuit	I/O impedance	Description
35	COMP1 OUT	High≧ V_{CC}−0.5V Low≦0.5V	—		100Ω	COMP1 output
36	COMP1 IN	* 0.0V to 1.2V	—		—	Threshold level setting for clog detection
37	ENVOUT	1.3V Typ.	—		S.E.P.P.	Envelope detector output
38	NC		—		—	Unconnected
39	ENVTC	1.3V Typ.	—		260Ω	Capacitance connection for envelope detection
40	ENVREF	1.3V Typ.	—		45kΩ	Capacitance connection for center DC ejection of the GCA output

Pin No.	Symbol	Pin voltage DC	Pin voltage AC	Equivalent circuit	I/O impedance	Description
41	RFCONT	* 0.7V to 4.5V	—		—	GCA gain control. GCA gain will change with the application of DC voltage.
42	HDSEL	* High≧ 2.0V Low≦ 0.8V	—		—	GCA input switch control. High (≧2.0V) : PBIN selection Low (≦0.8V) : SPIN selection
43	DGND	0V	—		—	Digital circuit GND
44	SPIN	2.3V Typ.	0.2 to 0.8V_{P-P}		50kΩ	Playback RF signal input
45	NC		—		—	Unconnected
46	PBIN	2.3V Typ.	0.2 to 0.8V_{P-P}		50kΩ	Playback RF signal input
47	NC		—		—	Unconnected
48	LPF1 OUT	0.8V Typ.	—		220Ω	LPFI output

Electrical Characteristics (DC)

Ta=25°C V_{CC}=4.75V

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Playback mode power supply current	I_{CC1}	ON for SW13, SW15, SW23A. OFF for other SWs. VS17=0V Test the current with ammeter A.	—	16	24	mA
Recording mode power supply current	I_{CC2}	ON for SW13, SW15, SW23A. OFF for other SWs. VS16=0V, VS17=0V Test the current with ammeter A.	—	7.5	12.0	mA
REF PILOT input resistance	R_{ERR1}	ON for SW13, SW15, SW23A. OFF for other SWs. VS9 = OPEN ± 0.3V Equation R_{ERR1} = $\frac{0.6}{(I9(VS9 = OPEN + 0.3V) - I9(VS9 = OPEN - 0.3V))}$	6.5	9.0	11.5	kΩ
FH detection offset voltage	V_{ERR1}	ON for SW13, SW15, SW23B. OFF for other SWs. VS23=0V Test the voltage difference V13 – V21.	−30	0	30	mV
Error output voltage	V_{ERR2}	ON for SW13, SW15, SW23B. OFF for other SWs. VS23=0V Test the voltage difference V15 - V21.	−100	0	100	mV
Subtracter output voltage	V_{SUB1}	ON for SW13, SW15, SW23B. OFF for other SWs. V11 = OPEN + 15mV, VS23=0V Subtract V_{ERR1} from the voltage difference V13 - V21.	−60	−45	−15	mV
	V_{SUB2}	ON for SW13, SW15, SW23B. OFF for other SWs. V10 = OPEN + 15mV, VS23=0V Subtract V_{ERR1} from the voltage difference V13 - V21.	15	45	60	mV
	V_{SUB3}	ON for SW13, SW15, SW23B. OFF for other SWs. V11 = OPEN + 200mV, VS23=0V Subtract V_{ERR1} from the voltage difference V13 - V21.	−650	−580	−480	mV
	V_{SUB4}	ON for SW13, SW15, SW23B. OFF for other SWs. V10 = OPEN + 200mV, VS23=0V Subtract V_{ERR1} from the voltage difference V13 - V21.	480	580	650	mV
	V_{SUB5}	ON for SW13, SW15, SW23B. OFF for other SWs. V10 = OPEN + 400mV, V11 = OPEN + 410mV, VS23=0V Subtract V_{ERR1} from the voltage difference V13 - V21.	−45	−30	−15	mV
	V_{SUB6}	ON for SW13, SW15, SW23B. OFF for other SWs. V10 = OPEN + 400mV, V11 = OPEN + 410mV, VS23=0V Subtract V_{ERR1} from the voltage difference V13 - V21.	15	30	45	mV
FH detection output resistance	R_{SUB}	ON for SW13, SW15, SW23A. OFF for other SWs. V12 = OPEN ± 0.5V Equation R_{SUB} = $\frac{1.0}{(I12(VS12 = OPEN + 0.5V) - I12(VS12 = OPEN - 0.5V))}$	8	11	14	kΩ

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
ERR "High" level output voltage	V_{OHERR1}	ON for SW13, SW15, SW23A. OFF for other SWs. VS14 = V_R − 20mV Test the voltage of V15.	3.45	4.0	—	V
	V_{OLERR2}	ON for SW13, SW15, SW23A. OFF for other SWs. VS14 = V_R − 20mV, V_{CC}=4.5V Test the voltage of V15.	3.2	3.8	—	V
ERR "Low" level output voltage	V_{OLERR}	ON for SW13, SW15, SW23A. OFF for other SWs. VS14 = V_R + 20mV Test the voltage of V15.	—	0.72	0.9	V
Reference voltage	V_R	ON for SW13, SW15, SW23B. OFF for other SWs. VS23=0V Test the voltage of V21.	2.18	2.30	2.42	V
Reference voltage input fluctuation	ΔV_{RIN}	ON for SW13, SW15, SW23B. OFF for other SWs. V_{CC} = 4.5/5.5V, VS23=0V Test the voltage fluctuation of V21.	−10	0	10	mV
LPF2 linearity	R_{LPF2}	ON for SW13, SW15, SW23A. OFF for other SWs. VS9 = OPEN±0.2V /±0.5V Equation R_{LPF2} = $\frac{0.4 \div (V18(VS9 = OPEN + 0.2V) - V18(VS9 = OPEN - 0.2V))}{1.0 \div (VS18(VS9 = OPEN + 0.5V) - V18(VS9 = OPEN - 0.5V))}$	0.95	0.99	1.05	
Clock input resistance	R_{CKIN}	ON for SW13, SW15, SW23B. OFF for other SWs. VS23 = OPEN±1.0V Equation R_{CKIN} = $\frac{6.75}{(I23(VS23 = OPEN + 1.0V) - I23(VS23 = OPEN - 1.0V))}$	60	95	140	kΩ
RFCONT input current	I_{RFC}	ON for SW13, SW15, SW23A. OFF for other SWs. VS41=4.0V Test the current of VS41.	—	0.4	3	μA
ENVREF output resistance	R_{EREF}	ON for SW13, SW15, SW23A. OFF for other SWs. VS40 = OPEN±0.3V Equation R_{EREF} = $\frac{0.6}{(I40(VS40 = OPEN + 0.3V) - I40(VS40 = OPEN - 0.3V))}$	30	45	60	kΩ
ENVTC sync current	I_{ENV}	ON for SW13, SW15, SW23A. OFF for other SWs. VS39=4.75V Test the current of VS39.	65	100	150	μA

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
RF detection offset voltage	ΔV_{ENV}	ON for SW13, SW15, SW23B. OFF for other SWs. VS23=0V Test the voltage of V37 - V31.	−100	0	100	mV
RF detection output voltage	V_{ENV1}	ON for SW13, SW15, SW23B. OFF for other SWs. VS23=0V Test V39.	0.9	1.3	1.7	V
	V_{ENV21}	ON for SW13, SW15, SW23B. OFF for other SWs. VS23=0V, SG44=5MHz, $0.5V_{P-P}$/0V Test the variation of V37. Equation V_{ENV21} = V37(SG44=$0.5V_{P-P}$) − V37(SG44=0V)	2.05	2.7	—	V
	V_{ENV22}	ON for SW13, SW15, SW23B. OFF for other SWs. V_{CC}=4.5V, VS23=0V, SG44=5MHz, $0.5V_{P-P}$/0V Test the variation of V37. Equation V_{ENV22} = V37(SG44=$0.5V_{P-P}$) − V37(SG44=0V)	2.05	2.45	—	V
COMP1 input current	I_{CMP1IH}	ON for SW13, SW15, SW23A. OFF for other SWs. VS36=4.75V Test the current of VS36.	—	0	1	μA
	V_{CMP1IL}	ON for SW13, SW15, SW23A. OFF for other SWs. VS36=0V Test the current of VS36.	−1	0	—	μA
COMP1 output voltage	V_{CMP1OH}	ON for SW13, SW15, SW23A. OFF for other SWs. IS35=-1mA, VS36=0.2V, VS39 = OPEN + 0.1V Test V35.	4.25	4.6	—	V
	V_{CMP1OL}	ON for SW13, SW15, SW23A. OFF for other SWs. IS35=1mA, VS36=0.6V, VS39 = OPEN + 0.1V Test V35.	—	0.1	0.5	V
COMP2 input current	I_{CMP2IH}	ON for SW13, SW15, SW23A. OFF for other SWs. VS34=4.75V Test the current of VS34.	—	0	1	μA
	I_{CMP2IL}	ON for SW13, SW15, SW23A. OFF for other SWs. VS34=0V Test the current of VS34.	−1	0	—	μA
CLOG output voltage	V_{CLOGH}	ON for SW13, SW15, SW23A. OFF for other SWs. VS34 = OPEN at Pin 31 - 20mV Test V33.	4.25	4.6	—	V

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
CLOG output voltage	V_{CLOGL}	ON for SW13, SW15, SW23A. OFF for other SWs. VS34 = OPEN at Pin 31 + 20mV Test V33.	—	0.1	0.5	V
COMP3 input current	I_{CMP3IH}	ON for SW13, SW15, SW23A. OFF for other SWs. VS30=4.75V Test the current of V30.	—	0	1	μA
	I_{CMP3IL}	ON for SW13, SW15, SW23A. OFF for other SWs. VS30=0V. Test the current of V30.	−1	0	—	μA
COMP3 output resistance	R_{CMP31}	ON for SW13, SW15, SW23A. OFF for other SWs. VS29=0V, VS30 = voltage of OPEN at Pin 31 - 20mV Equation R_{CMP31} = current of 4.75/VS29	7	10	13	kΩ
	R_{CMP32}	ON for SW13, SW15, SW23A. OFF for other SWs. VS28=0V, VS30 = voltage of OPEN at Pin 31 - 20mV Equation R_{CMP32} = current of 4.75/VS28	230	330	430	kΩ
COMP4 input current	I_{CMP4IH}	ON for SW13, SW15, SW23A. OFF for other SWs. VS27=4.75V Test the current of VS27.	—	0	1	μA
	I_{CMP4IL}	ON for SW13, SW15, SW23A. OFF for other SWs. VS27=0V Test the current of V27.	−1	0	—	μA
PB SP/LP output voltage	V_{PBSPH}	ON for SW13, SW15, SW23A. OFF for other SWs. VS27=2.28V, VS28=2.3V Test V26.	4.25	4.6	—	V
	V_{PBSPL}	ON for SW13, SW15, SW23A. OFF for other SWs. VS28=2.28V Test V26.	—	0.1	0.5	V
"High" level input voltage	V_{IH}	V_{CC} = 4.5 to 5.5V; Pins 16, 17, 25, and 42	2.0	—	—	V
"Low" level input voltage	V_{IL}	V_{CC} = 4.5 to 5.5V; Pins 16, 17, 25, and 42	—	—	0.8	V
"High" level input current	I_{IH}	V_{CC} = 4.5 to 5.5V; Pins 16, 17, 25, and 42 Applied voltage = 4.75V	—	0	1	μA
"Low" level input current	I_{IL}	V_{CC} = 4.5 to 5.5V; Pins 16, 17, 25, and 42 Applied voltage = 0V	−1	0	—	μA

Electrical Characteristics (AC)

Ta = 25°C V_{CC} = 4.75 V

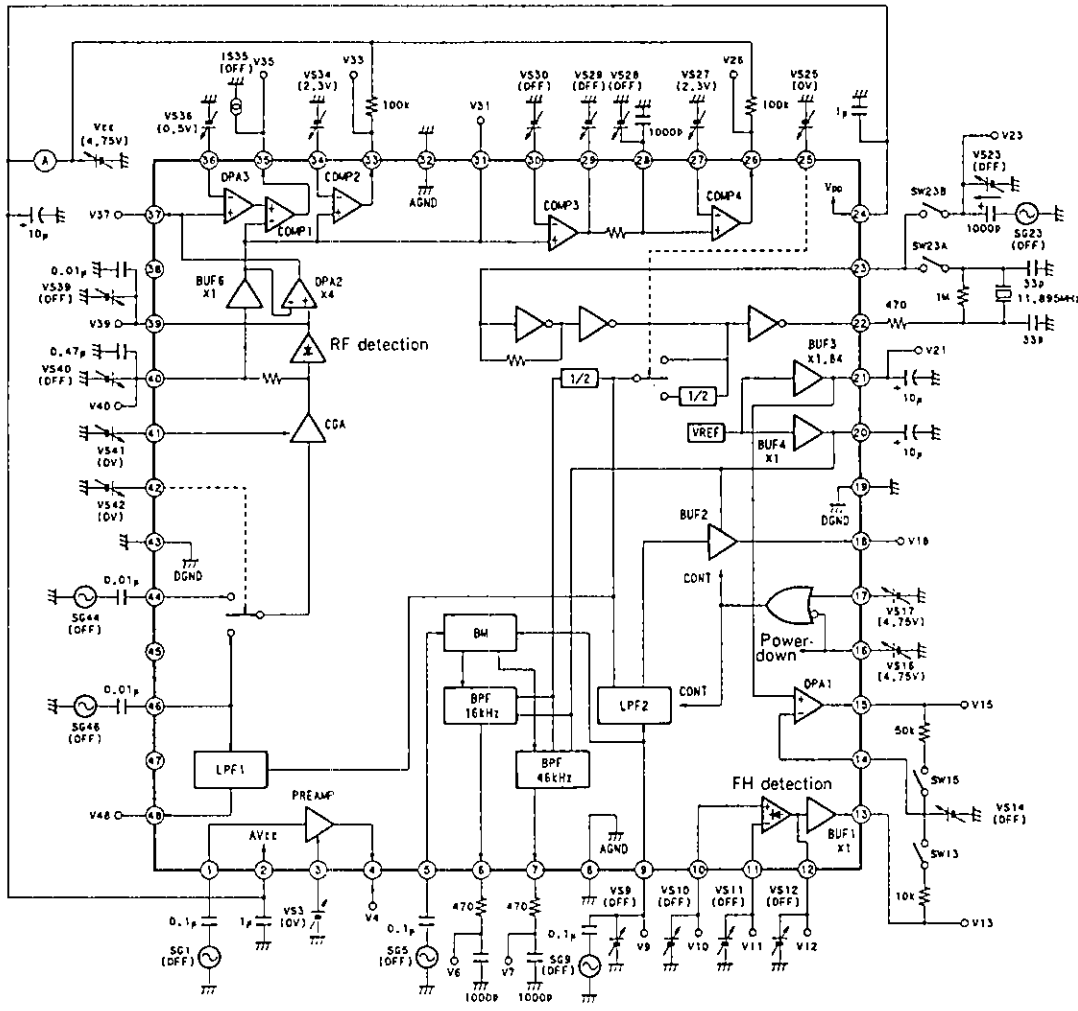
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
LPF1 reference gain	G_{LP1M}	ON for SW13, SW15, SW23A. OFF for other SWs. SG46=100kHz, 30mV$_{P-P}$ Equation G_{LP1M} = 20 * LOG (V48/V46) [dB]	−7.5	−2.5	−1.0	dB
LPF1 gain	G_{LP11}	ON for SW13, SW15, SW23A. OFF for other SWs. SG46=120kHz, 30mV$_{P-P}$ Equation G_{LP11} = 20 * LOG (V48/V46) −G_{LP1M} [dB]	−1.5	0.3	1.5	dB
	G_{LP12}	ON for SW13, SW15, SW23A. OFF for other SWs. SG46=150kHz, 30mV$_{P-P}$ Equation G_{LP12} = 20 * LOG (V48/V46)−G_{LP1M} [dB]	−1.5	0.4	1.5	dB
	G_{LP13}	ON for SW13, SW15, SW23A. OFF for other SWs. SG46=170kHz, 30mV$_{P-P}$ Equation G_{LP13} = 20 * LOG (V48/V46)−G_{LP1M} [dB]	−1.5	0.0	1.5	dB
	G_{LP14}	ON for SW13, SW15, SW23A. OFF for other SWs. SG46=250kHz, 100mV$_{P-P}$ Equation G_{LP14} = 20 * LOG (V48/V46)−G_{LP1M} [dB]	—	−5.8	−5.0	dB
	G_{LP15}	ON for SW13, SW15, SW23A. OFF for other SWs. SG46=400kHz, 800mV$_{P-P}$ Equation G_{LP15} = 20 * LOG (V48/V46)−G_{LP1M} [dB]	—	−18	−16	dB
	G_{LP16}	ON for SW13, SW15, SW23A. OFF for other SWs. SG46=750kHz, 800mV$_{P-P}$ Equation G_{LP16} = 20 * LOG (V48/V46)−G_{LP1M} [dB]	—	−37	−33	dB
	G_{LP17}	ON for SW13, SW15, SW23A. OFF for other SWs. SG46=3MHz, 800mV$_{P-P}$ Equation G_{LP17} = 20 * LOG (V48/V46)−G_{LP1M} [dB]	—	−62	−50	dB
Preamplifier gain	G_{PR1}	ON for SW13, SW15, SW23A. OFF for other SWs. VS3=0.8V, SG1=200kHz, 30mV$_{P-P}$ Equation G_{PR1} = 20 * LOG (V4/V1) [dB]	4	6	8	dB
	G_{PR2}	ON for SW13, SW15, SW23A. OFF for other SWs. VS3=2.6V, SG1=200kHz, 30mV$_{P-P}$ Equation G_{PR1} = 20 * LOG (V4/V1) [dB]	12	15	18	dB

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Preamplifier gain	G_{PR3}	ON for SW13, SW15, SW23A. OFF for other SWs. VS3=3.3V, SG1=200kHz, $5mV_{P-P}$ Equation G_{PR2} = 20 * LOG (V4/V1) [dB]	19	22	25	dB
BPF16k reference gain	G_{BP1M}	ON for SW13, SW15, SW23A. OFF for other SWs. VS9=1.25V, SG5=16.46kHz, $10mV_{P-P}$ Equation G_{BP1M} = 20 * LOG (V6/V5) [dB]	30	33	36	dB
BPF16k attenuation level	G_{BP11}	ON for SW13, SW15, SW23A. OFF for other SWs. VS9=1.25V, SG5=9kHZ, $10mV_{P-P}$ Equation G_{BP11} = 20 * LOG (V6/V5) $-G_{BP1M}$ [dB]	—	−24	−20	dB
	G_{BP12}	ON for SW13, SW15, SW23A. OFF for other SWs. VS9=1.25V, SG5=28kHz, $10mV_{P-P}$ Equation G_{BP12} = 20 * LOG (V6/V5) $-G_{BP1M}$ [dB]	—	−22	−20	dB
	G_{BP13}	ON for SW13, SW15, SW23A. OFF for other SWs. VS9=1.25V, SG5=150kHz, $10mV_{P-P}$ Equation G_{BP13} = 20 * LOG (V6/V5) $-G_{BP1M}$ [dB]	—	−35	−26	dB
BPF46k reference gain	G_{BP2M}	ON for SW13, SW15, SW23A. OFF for other SWs. VS9=1.25V, SG5=46.2kHz, $10mV_{P-P}$ Equation G_{BP2M} = 20 * LOG (V7/V5) [dB]	30	33	36	dB
BPF46k attenuation level	G_{BP21}	ON for SW13, SW15, SW23A. OFF for other SWs. VS9=1.25V, SG5=16kHz, $10mV_{P-P}$ Equation G_{BP21} = 20 * LOG (V7/V5) $-G_{BP2M}$ [dB]	—	−31	−26	dB
	G_{BP22}	ON for SW13, SW15, SW23A. OFF for other SWs. VS9=1.25V, SG5=33kHz, $10mV_{P-P}$ Equation G_{BP22} = 20 * LOG (V7/V5) $-G_{BP2M}$ [dB]	—	−26	−20	dB
	G_{BP23}	ON for SW13, SW15, SW23A. OFF for other SWs. VS9=1.25V, SG5=60kHz, $10mV_{P-P}$ Equation G_{BP23} = 20 * LOG (V7/V5) $-G_{BP2M}$ [dB]	—	−24	−20	dB
	G_{BP24}	ON for SW13, SW15, SW23A. OFF for other SWs. VS9=1.25V, SG5=150kHz, $10mV_{P-P}$ Equation G_{BP24} = 20 * LOG (V7/V5) $-G_{BP2M}$ [dB]	—	−36	−26	dB
Fo gain difference	ΔG_{BP}	Difference of G_{BP1M} and G_{BP2M}	−2	0	2	dB

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
LPF2 reference gain	G_{LP2M}	ON for SW13, SW15, SW23A. OFF for other SWs. SG9=100kHz, 100mV$_{P-P}$ Equation G_{LP2M} = 20 * LOG (V18/V9) [dB]	−6	−4	−1.5	dB
LPF2 gain	G_{LP21}	ON for SW13, SW15, SW23A. OFF for other SWs. SG9=120kHz, 100mV$_{P-P}$ Equation G_{LP21} = 20 * LOG (V18/V9) −G_{LP2M} [dB]	−1.5	0.2	1.5	dB
	G_{LP22}	ON for SW13, SW15, SW23A. OFF for other SWs. SG9=150kHz, 100mV$_{P-P}$ Equation G_{LP22} = 20 * LOG (V18/V9) −G_{LP2M} [dB]	−1.5	−0.2	1.5	dB
	G_{LP23}	ON for SW13, SW15, SW23A. OFF for other SWs. SG9=170kHz, 100mV$_{P-P}$ Equation G_{LP23} = 20 * LOG (V18/V9) −G_{LP2M} [dB]	−1.5	−0.7	1.5	dB
	G_{LP24}	ON for SW13, SW15, SW23A. OFF for other SWs. SG9=300kHz, 100mV$_{P-P}$ Equation G_{LP24} = 20 * LOG (V18/V9) −G_{LP2M} [dB]	—	−14	−12	dB
	G_{LP25}	ON for SW13, SW15, SW23A. OFF for other SWs. SG9=500kHz, 100mV$_{P-P}$ Equation G_{LP25} = 20 * LOG (V18/V9) −G_{LP2M} [dB]	—	−35	−33	dB
	G_{LP26}	ON for SW13, SW15, SW23A. OFF for other SWs. SG9=1.5kHz, 100mV$_{P-P}$ Equation G_{LP26} = 20 * LOG (V18/V9) −G_{LP2M} [dB]	—	−58	−40	dB
Crosstalk	G_{CAP}	ON for SW13, SW15, SW23A. OFF for other SWs. SG9=200kHz, 500mV$_{P-P}$ Equation G_{CAP} = 20 * LOG (V4/V9) [dB]	—	−60	−46	dB
Minimum CK input	V_{CK}	ON for SW13, SW15, SW23B. OFF for other SWs. SG9=100kHz, 100mV$_{P-P}$, SG23=12MHz Test value is attained by changing the amplitude of SG23 to the minimum level within G_{LP2M} specifications.	0.2	—	—	V_{P-P}
GCA gain	G_{RF1}	ON for SW13, SW15, SW23B. OFF for other SWs. VS23=0V, VS41=1.7V, SG44=5MHz, 500mV$_{P-P}$ Equation G_{RF1}=20 * LOG ((V37(SG44=500m V_{P-P})− V37 (SG44 = 0V))/250mV) [dB] Note: The voltage of V37 is DC.	14	17	20	dB

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
GCA gain	G_{RF2}	ON for SW13, SW15, SW23B. OFF for other SWs. VS23=0V, VS41=2.5V, SG44=5MHz, 200mV$_{P-P}$ Equation G_{RF2}=20 * LOG ((V37(SG44=200mV$_{P-P}$) − V37 (SG44 = 0V))/ 100mV) [dB] Note: The voltage of V37 is DC.	19	22	25	dB
	G_{RF3}	ON for SW13, SW15, SW23B. OFF for other SWs. VS23=0V, VS41=4.5V, SG44=5MHz, 100mV$_{P-P}$ Equation G_{RF3}=20 * LOG ((V37(SG44=100mV$_{P-P}$) − V37 (SG44 = 0V))/ 50mV) [dB] Note: The voltage of V37 is DC.	24	27	30	dB
GCA frequency response characteristics	f_W	ON for SW13, SW15, SW23B. OFF for other SWs. VS23=0V, VS41=2.5V, SG44=5MHz, 200mV$_{P-P}$ The test value is attained by changing the frequency of SG44 to a value 3dB lower than the test value for G_{RF2}.	7	14	—	MHz
ENVOUT output voltage	V_{ENVB}	ON for SW13, SW15, SW23A. OFF for other SW. VS39 = OPEN / OPEN + 0.4V Test the voltage variation of V37. Equation V_{ENVB} = V37(VS39 = OPEN + 0.4V) − V37(VS39 = OPEN)	1.5	1.6	1.7	V
LPF1 noise (white noise)	V_{ENVB}	ON for SW13, SW15, SW23A. OFF for other SWs. SG46=100kHz, 10mV$_{P-P}$. Test the S/N of V48 with spectrum analyzer. Resolution band = 300Hz Video band = 100Hz	—	53	—	dB
LPF1 noise (aliasing noise)	V_{ENVB}	ON for SW13, SW15, SW23A. OFF for other SWs. SG46=6MHz, 600mV$_{P-P}$ Test the maximum value of V48 within the range of 50kHz to 250kHz with spectrum analyzer. Resolution band = 300Hz Video band = 100Hz	—	3	—	mV$_{P-P}$

Electrical Characteristics Test Circuit



Note)

1. VSXX is the Pin XX voltage source, which includes an ammeter.
2. IS35 is the current source for Pin 35. OFF under normal operation.
3. Unless otherwise specified in the Electrical Characteristics (under Conditions), circuit will be as shown in the figure above. ("OFF" is in OPEN state; "2.3V" refers to 2.3V application)
4. When SG is OFF, connect to GND under low resistance. (<100Ω)

Control Logic Signals

1)Mode description

P/P PB	PILOT ACT	REC PILOT	Operation Mode
High	High	Output	Playback
High	Low	No output	Playback
Low	High	Output	Recording
Low	Low	Output	Recording

Playback mode: All circuits are active except for REC PILOT, which will depend on the state of PILOT ACT.
Recording mode: Reference voltage, crystal oscillator, REC PILOT, and circuits from FH detection to ERR output are active.

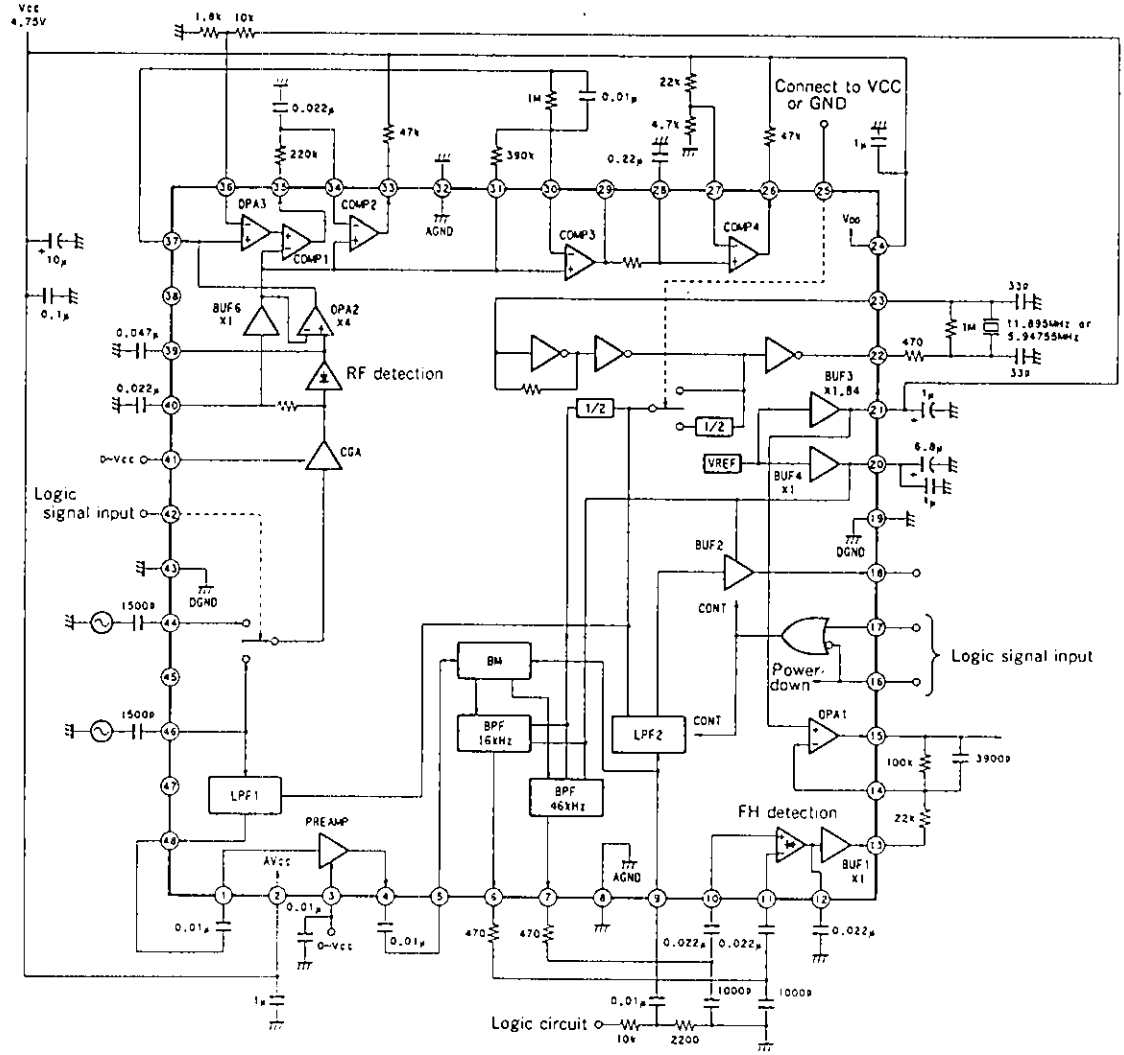
2)Clock

CKCONT = "High" : 6MHz oscillation compatible
CKCONT = "Low" : 12MHz oscillation compatible

3)RF input

HDSEL = "High" : PBIN selection
HDSEL = "Low" : SPIN selection

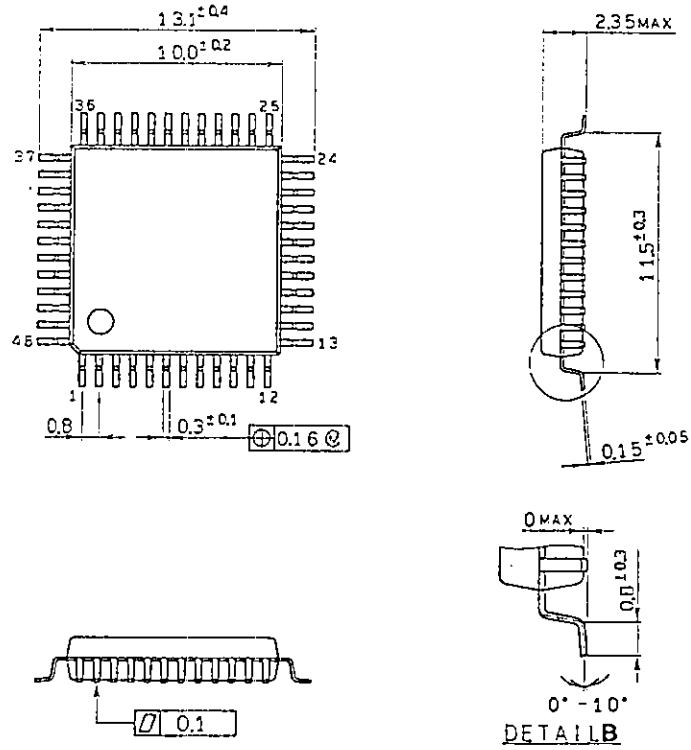
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

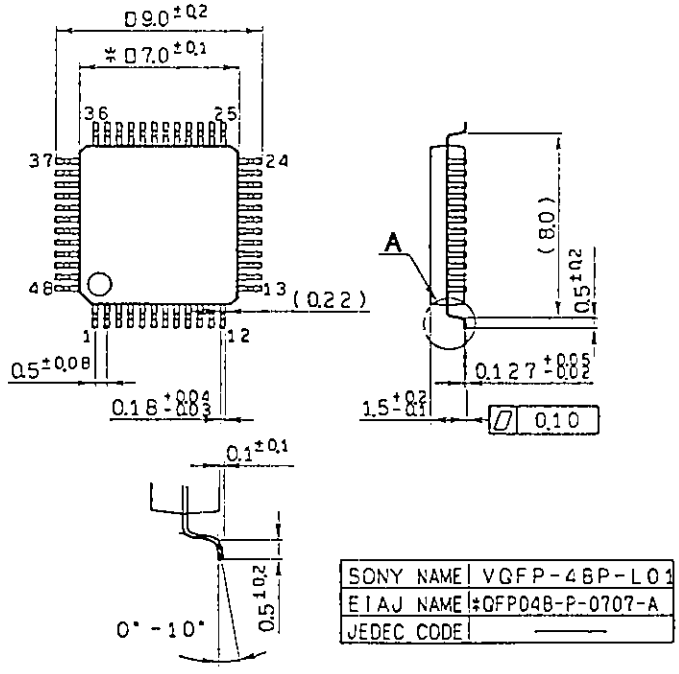
Package Outline Unit: mm

CXA1481AQ 48pin QFP (Plastic)



SONY NAME	QFP-48P-L023
EIAJ NAME	*QFP048-P-1010-AF
JEDEC CODE	———

CXA1481AR 48pin VQFP (Plastic) 0.2g



SONY NAME	VQFP-48P-L01
EIAJ NAME	*QFP048-P-0707-A
JEDEC CODE	———

Detailed diagram of A

Note) Dimensions marked with * do not include resin residue.