CVE3

Driving the Digital Lifestyle

NTSC/PAL/SECAM Video Encoder

DVD | Digital Camera | Digital TV | Imaging | IP Cores

Product Brief

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Description

Zoran's CVE3 NTSC/PAL/SECAM Video Encoder is a silicon-efficient, high-quality Intellectual Property Core for video IC designs requiring the TV output function. The CVE3 encodes YCrCb, 4:2:2 digital video into all NTSC, PAL, or SECAM TV standards. The CVE3 supports vertical blanking interval (VBI) encoding, including closed caption, teletext, WSS and CGMS-A encoding. CVE3 also includes support for Macrovision 7.1.L1, the copy protection scheme used in DVD players and set-top boxes. Six separate output busses for Y, Composite, Chroma, and RGB provide for flexibility in connection and multiplexing to DACs.

Proven in silicon and shipping in the millions, the CVE3 video encoder greatly reduces the risk and time involved when integrating the video encoding function into an IC. Zoran's video encoder technology is incorporated into its own Vaddis DVD playback and COACH digital camera ICs.

VIP-II Demonstration System

The VIP-II is an FPGA demonstration system for Zoran's IP Core products. The VIP-II accepts composite video, S-video and component video inputs and with its user friendly GUI enables customers to thoroughly evaluate the performance of Zoran's IP Core products.

Features

- Encodes 4:2:2 YCrCb into all variations of NTSC, PAL or SECAM TV standards
- Simultaneous output of composite video, S-video and component video supported
- Dual chroma paths for optimal output of both composite video and S-Video component video
- CCIR 601, 604 and 656 and SMTPE 253 standards supported
- Macrovision 7.1.L1 copy protection
- 33-tap luma filter
- Programmable Notch Filter
- Outputs 10-bit data to DACs
- Vertical Blanking Interval (VBI) encoding support including closed caption, teletext, WSS & CGMS Encoding
- Fully synchronous design
- Process technology independent "softcore"

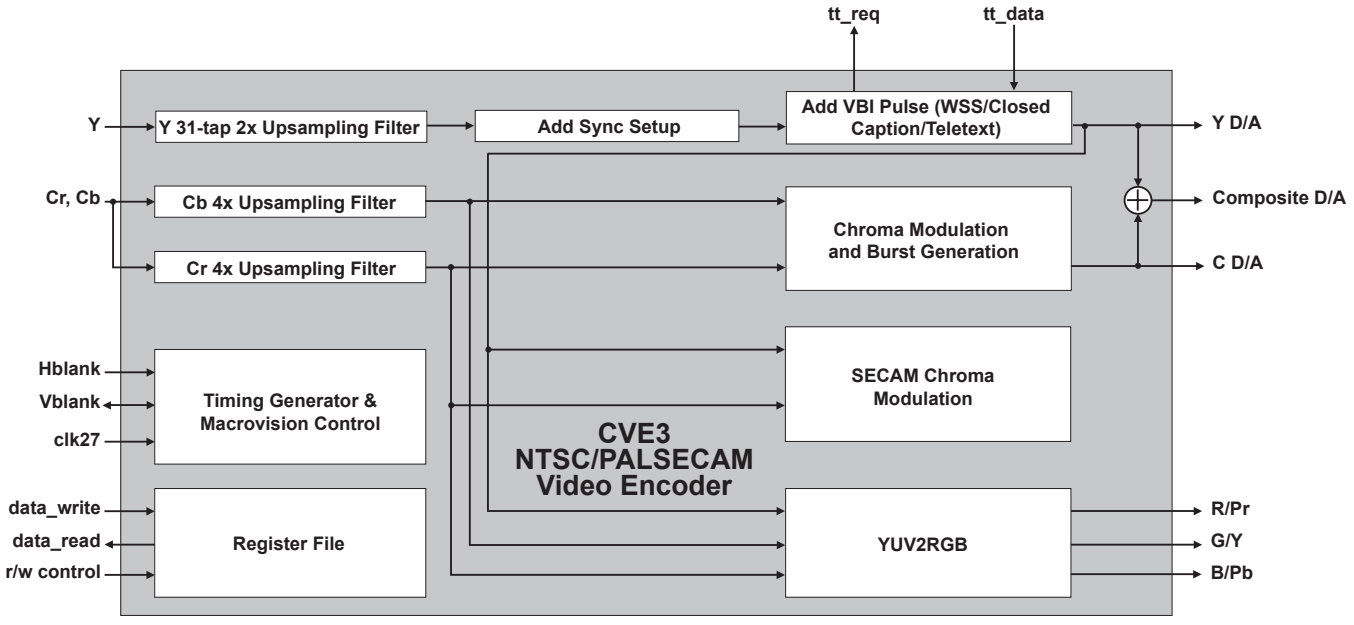
Integrated Circuit Applications

- PC video
- Digital camera processors
- PC graphics
- Set top box decoders
- Gaming systems
- Any system requiring TV output

Deliverables

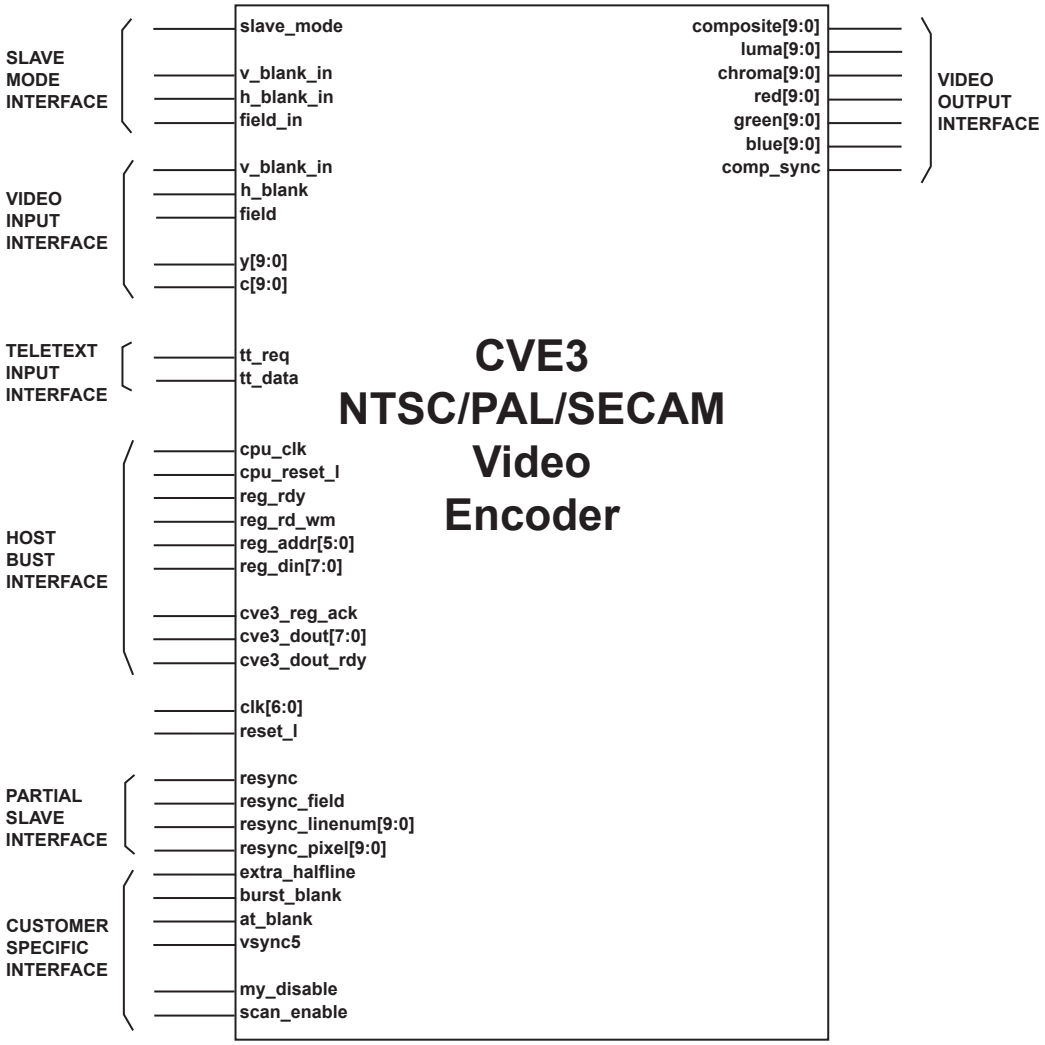
- Compilable Verilog source code
- Bit accurate, cycle accurate C model
- Synopsis synthesis scripts
- Test input files
- Documentation
- VIP-II FPGA demonstration system available

Figure 1. CVE3 Video Encoder Block Diagram



Product Brief

Figure 2. CVE3 Video Encoder Pinout Diagram



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