CSD87355Q5D Synchronous Buck NexFET™ Power Block

1 Features

- Half-Bridge Power Block
- 92.5% System Efficiency at 25 A
- Up to 45-A Operation
- High-Frequency Operation (Up to 1.5 MHz)
- High-Density SON 5-mm × 6-mm Footprint
- Optimized for 5-V Gate Drive
- Low Switching Losses
- Ultralow Inductance Package
- RoHS Compliant
- Halogen Free
- Pb-Free Terminal Plating

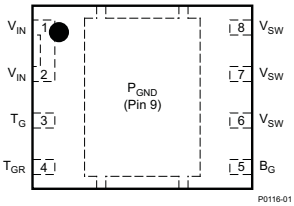
2 Applications

- Synchronous Buck Converters
  - High-Frequency Applications
  - High-Current, Low Duty Cycle Applications
- Multiphase Synchronous Buck Converters
- POL DC-DC Converters
- IMVP, VRM, and VRD Applications

3 Description

The CSD87355Q5D NexFET™ power block is an optimized design for synchronous buck applications offering high-current, high-efficiency, and high-frequency capability in a small 5-mm × 6-mm outline. Optimized for 5-V gate drive applications, this product offers a flexible solution capable of offering a high-density power supply when paired with any 5-V gate drive from an external controller/driver.

Top View

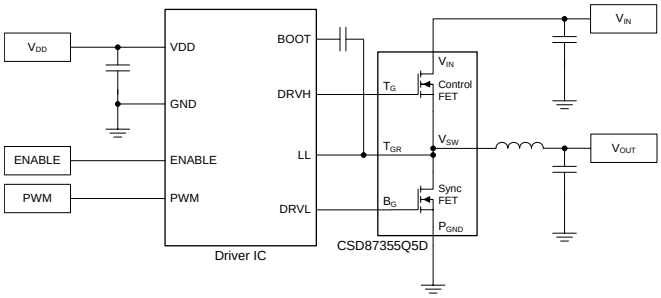


Ordering Information(1)

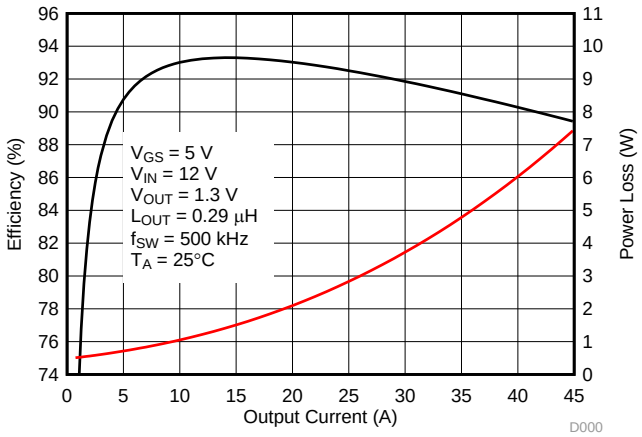
Device	Media	Qty	Package	Ship
CSD87355Q5D	13-Inch Reel	2500	SON 5 mm × 6 mm Plastic Package	Tape and Reel
CSD87355Q5DT	7-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Circuit



Typical Power Block Efficiency and Power Loss



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Original (March 2016) to Revision A **Page**

- Added footnote for $Z_{DS(ON)}$ in the *Electrical Characteristics* table. ... 4
- Deleted the *Q5D Tape and Reel Information* section ... 19

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5 Specifications

5.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	V_{IN} to P_{GND}	–0.8	30	V
	T_G to T_{GR}	–8	10	V
	B_G to P_{GND}	–8	10	V
Pulsed current rating, I_{DM}(2)			120	A
Power dissipation, P_D			12	W
Avalanche energy E_{AS}	Sync FET, I_D = 89 A, L = 0.1 mH		396	mJ
	Control FET, I_D = 50 A, L = 0.1 mH		125	mJ
Operating junction temperature, T_J		–55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Pulse duration ≤ 50 µS. Duty cycle ≤ 0.01.

5.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature range	–55	150	°C

5.3 Recommended Operating Conditions

T_A = 25° (unless otherwise noted)

		MIN	MAX	UNIT
V_{GS}	Gate drive voltage	4.5	10	V
V_{IN}	Input supply voltage		27	V
f_{SW}	Switching frequency C_{BST} = 0.1 µF (min)	200	1500	kHz
	Operating current		45	A
T_J	Operating temperature		125	°C

5.4 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (min Cu)(1)(2)			102	°C/W
	Junction-to-ambient thermal resistance (max Cu)(1)(2)			50	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance (top of package)(2)			20	°C/W
	Junction-to-case thermal resistance (P_{GND} pin)(2)			2	°C/W

(1) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2) Cu.
(2) $R_{\theta JC}$ is determined with the device mounted on a 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inches × 1.5 inches (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.

5.5 Power Block Performance

T_A = 25° (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power loss, P_{LOSS}(1)	V_{IN} = 12 V, V_{GS} = 5 V, V_{OUT} = 1.3 V, I_{OUT} = 25 A, f_{SW} = 500 kHz, L_{OUT} = 0.29 µH, T_J = 25ºC		2.8		W
V_{IN} quiescent current, I_{QVIN}	T_G to T_{GR} = 0 V ,B_G to P_{GND} = 0 V		10		µA

(1) Measurement made with six 10 µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins and using a high current 5 V driver IC.

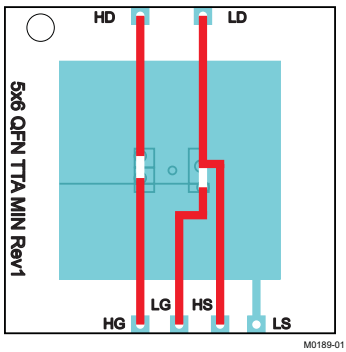
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5.6 Electrical Characteristics

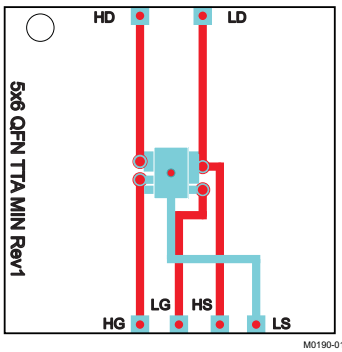
T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	Q1 CONTROL FET			Q2 SYNC FET			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC CHARACTERISTICS									
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = 250 µA	30			30			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 24 V			1			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = +10 / –8 V			100			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 250 µA	1.00		1.90	0.75		1.20	V
$Z_{DS(ON)}$ (1)	Drain-to-source ON impedance	V_{IN} = 12 V, V_{GS} = 5 V, V_{OUT} = 1.3 V, I_{OUT} = 25 A, f_{SW} = 500 kHz, L_{OUT} = 0.29 µH		3.9			0.9		mΩ
g_{fs}	Transconductance	V_{DS} = 3 V, I_{DS} = 20 A		90			151		S
DYNAMIC CHARACTERISTICS									
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		1430	1860		3570	4640	pF
C_{OSS}	Output capacitance			716	930		1730	2240	pF
C_{RSS}	Reverse transfer capacitance			25	32		52	67	pF
R_G	Series gate resistance			0.6	1.2		0.7	1.4	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 15 V, I_{DS} = 20 A		10.5	13.7		24.3	31.5	nC
Q_{gd}	Gate charge – gate-to-drain			2.3			4.1		nC
Q_{gs}	Gate charge – gate-to-source			3.2			5.6		nC
$Q_{g(th)}$	Gate charge at V_{th}			1.7			2.8		nC
Q_{OSS}	Output charge	V_{DS} = 15 V, V_{GS} = 0 V		18			40		nC
$t_{d(on)}$	Turn on delay time	V_{DS} = 15 V, V_{GS} = 4.5 V, I_{DS} = 20 A, R_G = 2 Ω		8			10		ns
t_r	Rise time			18			14		ns
$t_{d(off)}$	Turn off delay time			13			27		ns
t_f	Fall time			3			6		ns
DIODE CHARACTERISTICS									
V_{SD}	Diode forward voltage	I_{DS} = 20 A, V_{GS} = 0 V		0.8	1.0		0.8	1.0	V
Q_{rr}	Reverse recovery charge	V_{dd} = 17 V, I_F = 20 A, di/dt = 300 A/µs		43			82		nC
t_{rr}	Reverse recovery time			23.8			32.3		ns

(1) Equivalent based on application testing. See *Application and Implementation* section for details.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2 oz. (0.071-mm thick) Cu.

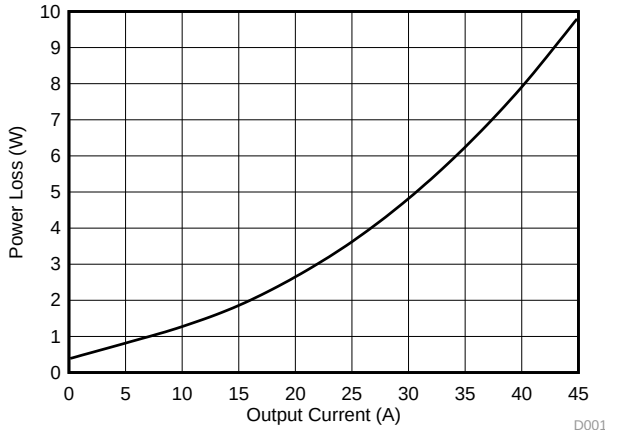


Max $R_{\theta JA}$ = 102°C/W when mounted on minimum pad area of 2 oz. (0.071-mm thick) Cu.

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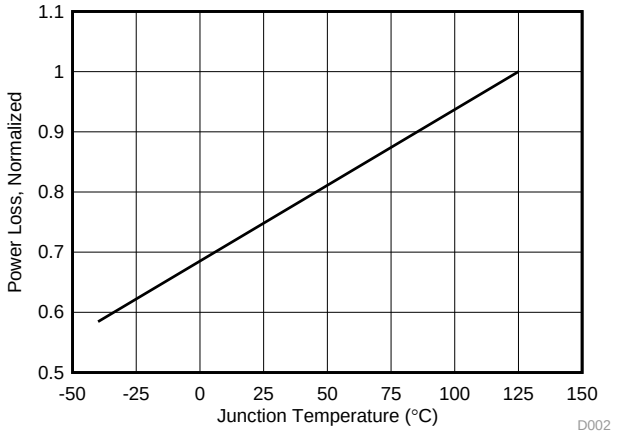
5.7 Typical Power Block Device Characteristics

T_J = 125°C, unless stated otherwise. The Typical Power Block System Characteristic curves Figure 3, , and Figure 4 are based on measurements made on a PCB design with dimensions of 4” (W) × 3.5” (L) × 0.062” (H) and 6 copper layers of 1-oz. copper thickness. See *Application and Implementation* for detailed explanation.



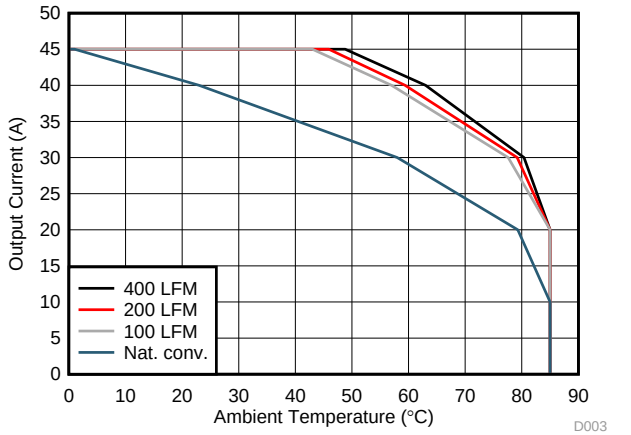
V_{IN} = 12 V V_{GS} = 5 V V_{OUT} = 1.3 V
f_{SW} = 500 kHz L_{OUT} = 0.29 µH

Figure 1. Power Loss vs Output Current



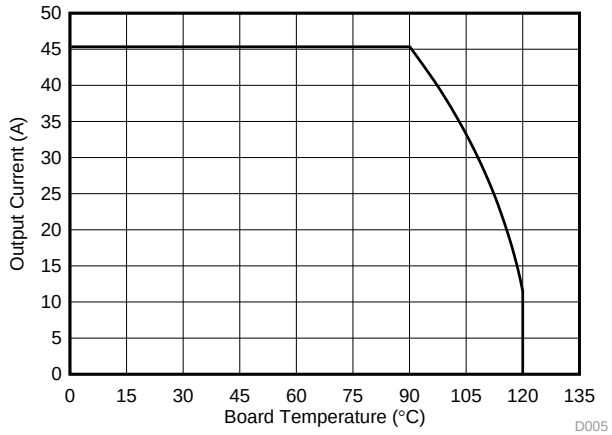
V_{IN} = 12 V V_{GS} = 5 V V_{OUT} = 1.3 V
f_{SW} = 500 kHz L_{OUT} = 0.29 µH

Figure 2. Normalized Power Loss vs Temperature



V_{IN} = 12 V V_{GS} = 5 V V_{OUT} = 1.3 V
f_{SW} = 500 kHz L_{OUT} = 0.29 µH

Figure 3. Safe Operating Area (SOA) – Thermal Airflow Measurement PCB Vertical Mount



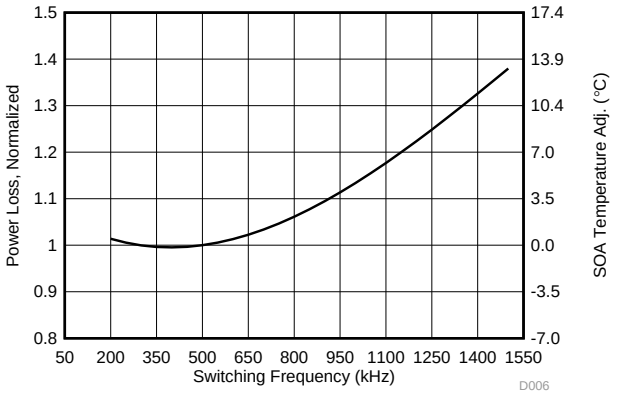
V_{IN} = 12 V V_{GS} = 5 V V_{OUT} = 1.3 V
f_{SW} = 500 kHz L_{OUT} = 0.29 µH

Figure 4. Typical Safe Operating Area (SOA)

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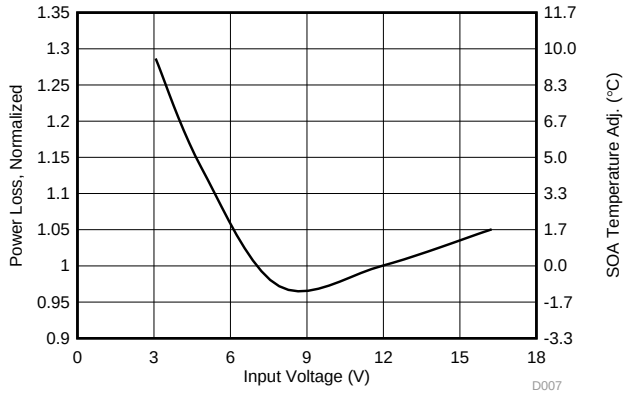
Typical Power Block Device Characteristics (continued)

T_J = 125°C, unless stated otherwise. The Typical Power Block System Characteristic curves Figure 3, , and Figure 4 are based on measurements made on a PCB design with dimensions of 4” (W) × 3.5” (L) × 0.062” (H) and 6 copper layers of 1-oz. copper thickness. See *Application and Implementation* for detailed explanation.



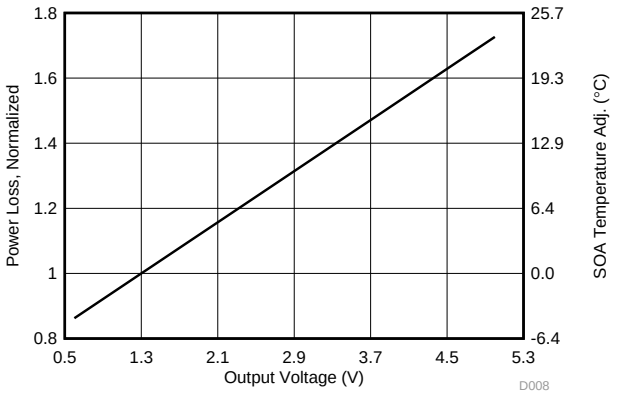
V_{IN} = 12 V V_{GS} = 5 V V_{OUT} = 1.3 V
L_{OUT} = 0.29 µH I_{OUT} = 45 A

Figure 5. Normalized Power Loss vs Switching Frequency



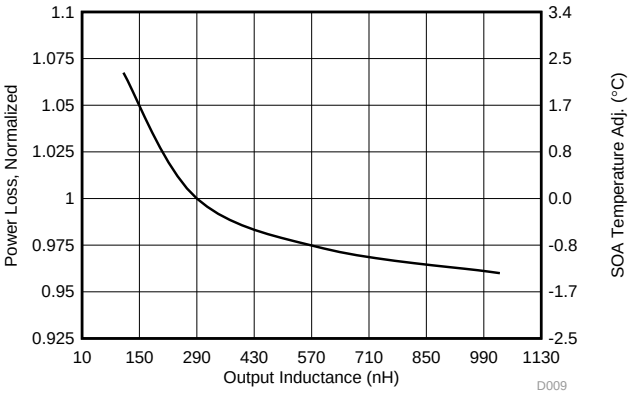
V_{IN} = 12 V V_{OUT} = 1.3 V L_{OUT} = 0.29 µH
f_{SW} = 500 kHz I_{OUT} = 45 A

Figure 6. Normalized Power Loss vs Input Voltage



V_{IN} = 12 V V_{GS} = 5 V f_{SW} = 500 kHz
L_{OUT} = 0.29 µH I_{OUT} = 45 A

Figure 7. Normalized Power Loss vs. Output Voltage



V_{IN} = 12 V V_{GS} = 5 V V_{OUT} = 1.3 V
f_{SW} = 500 kHz I_{OUT} = 45 A

Figure 8. Normalized Power Loss vs Output Inductance

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5.8 Typical Power Block MOSFET Characteristics

T_A = 25°C, unless stated otherwise.

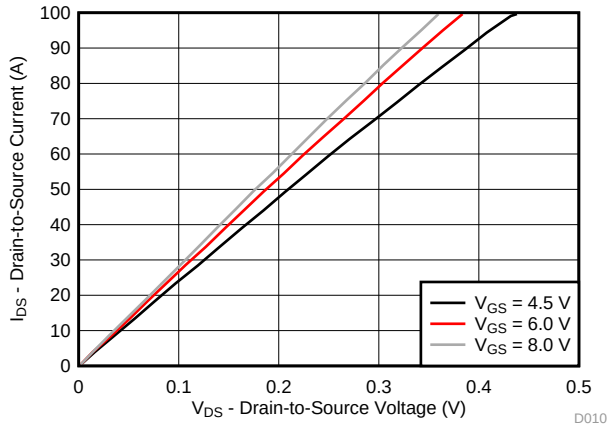


Figure 9. Control MOSFET Saturation

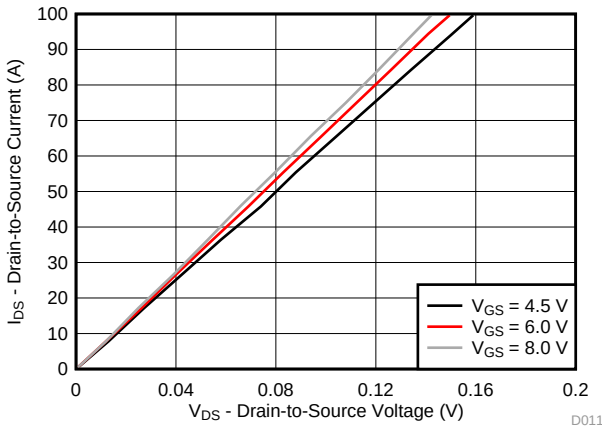


Figure 10. Sync MOSFET Saturation

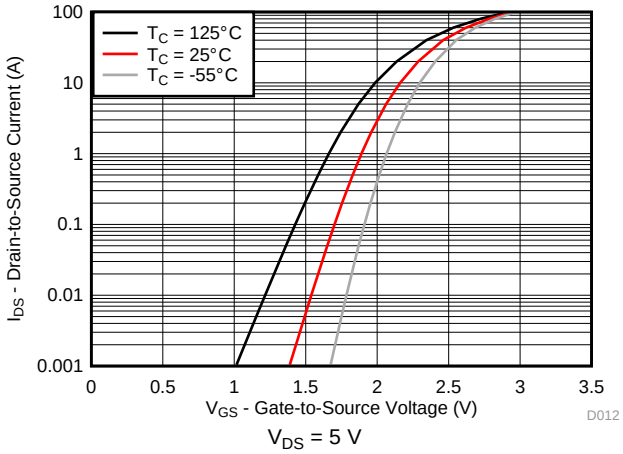


Figure 11. Control MOSFET Transfer

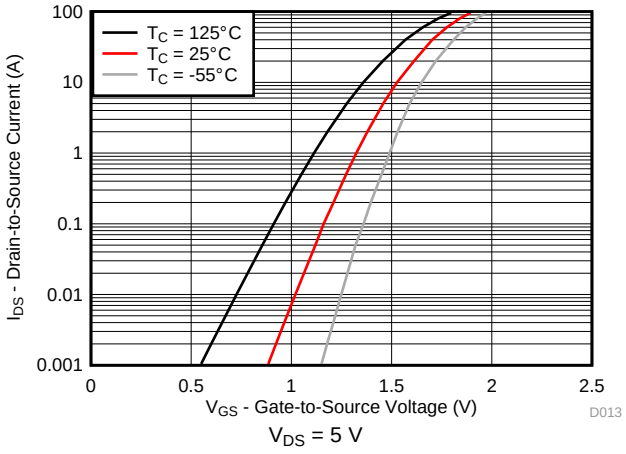


Figure 12. Sync MOSFET Transfer

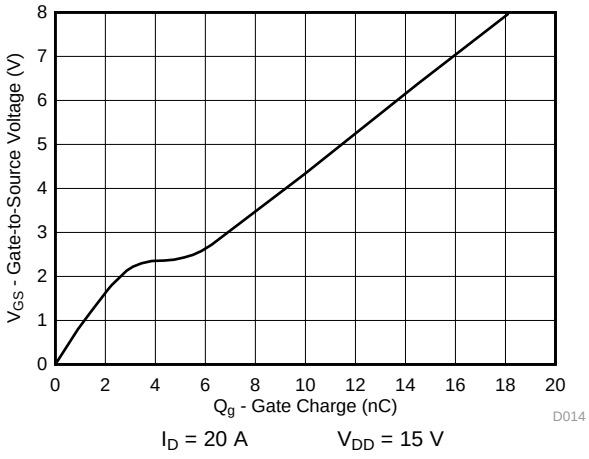


Figure 13. Control MOSFET Gate Charge

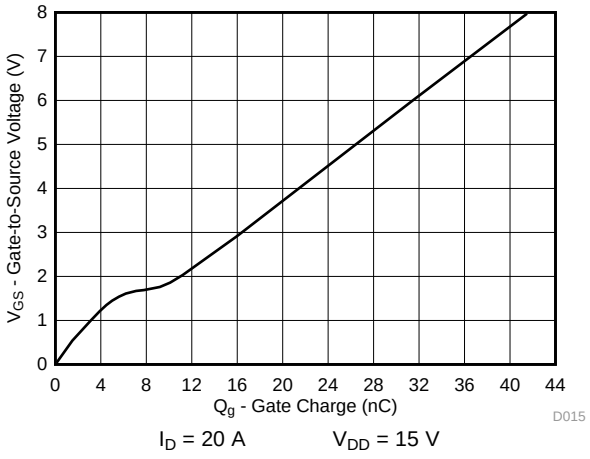


Figure 14. Sync MOSFET Gate Charge

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Typical Power Block MOSFET Characteristics (continued)

T_A = 25°C, unless stated otherwise.

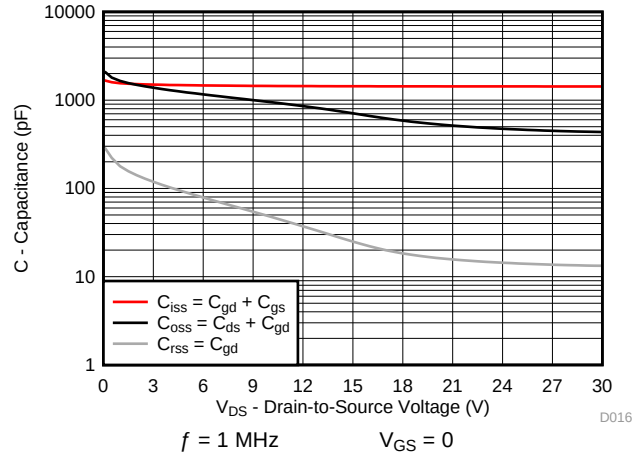


Figure 15. Control MOSFET Capacitance

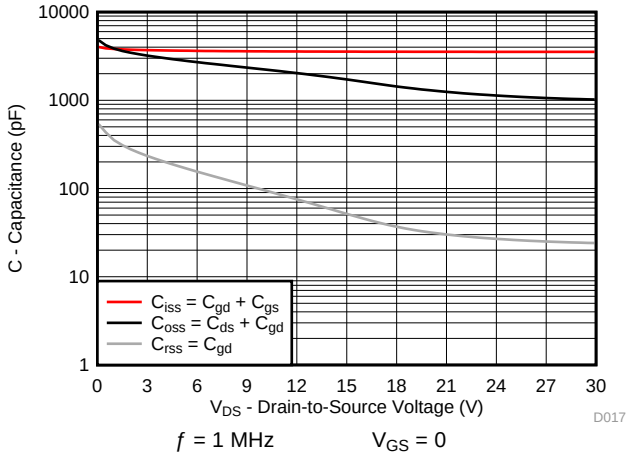


Figure 16. Sync MOSFET Capacitance

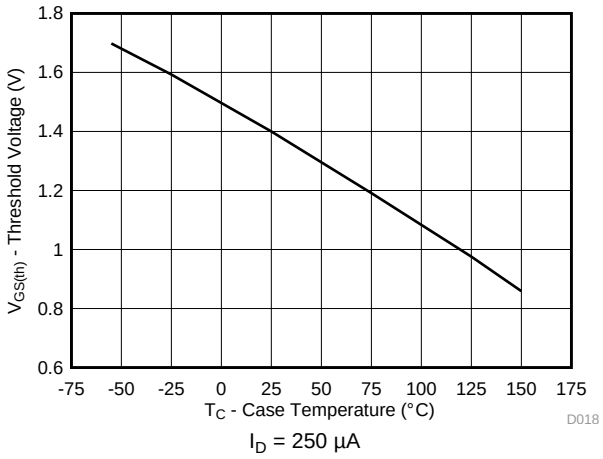


Figure 17. Control MOSFET $V_{GS(th)}$

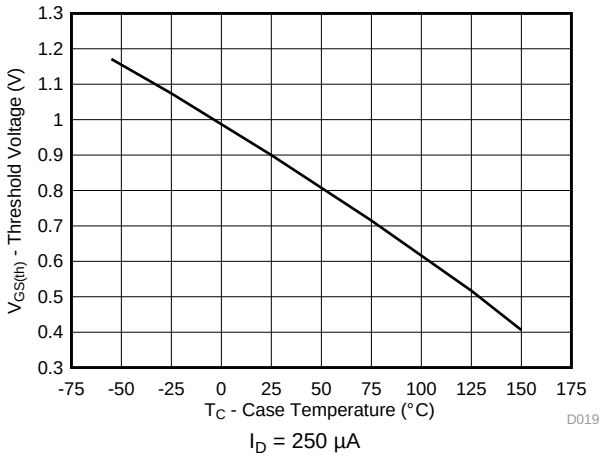


Figure 18. Sync MOSFET $V_{GS(th)}$

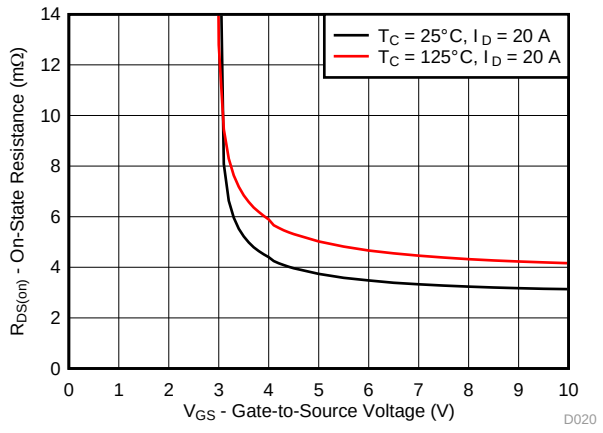


Figure 19. Control MOSFET $R_{DS(ON)}$ vs V_{GS}

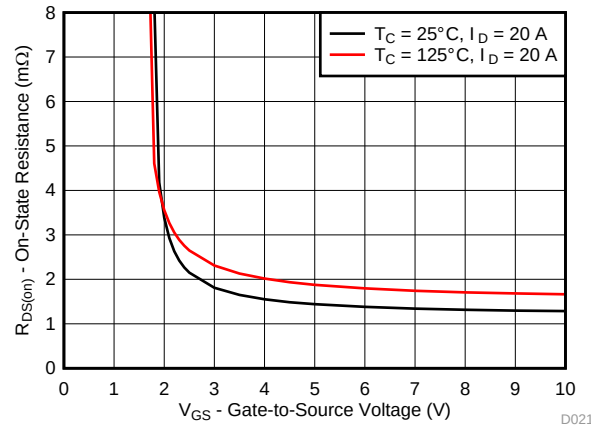


Figure 20. Sync MOSFET $R_{DS(ON)}$ vs V_{GS}

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Typical Power Block MOSFET Characteristics (continued)

T_A = 25°C, unless stated otherwise.

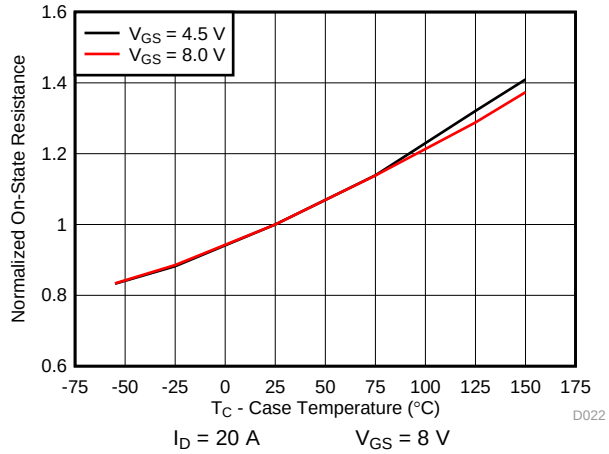


Figure 21. Control MOSFET Normalized $R_{DS(ON)}$

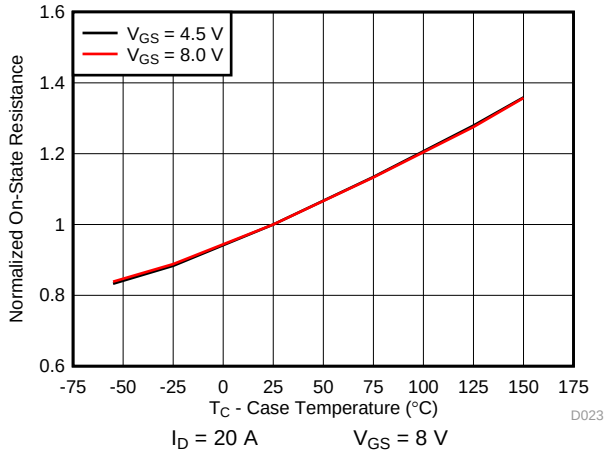


Figure 22. Sync MOSFET Normalized $R_{DS(ON)}$

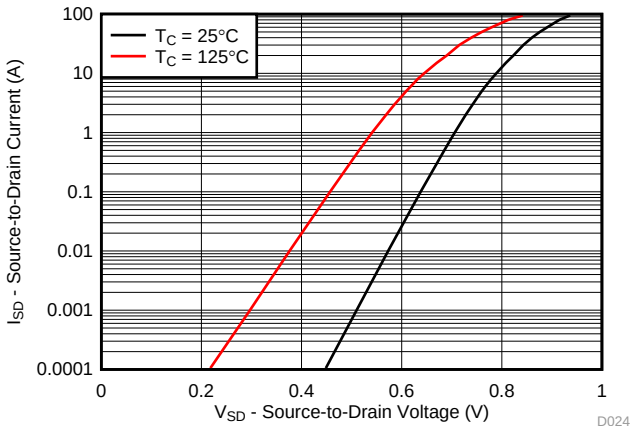


Figure 23. Control MOSFET Body Diode

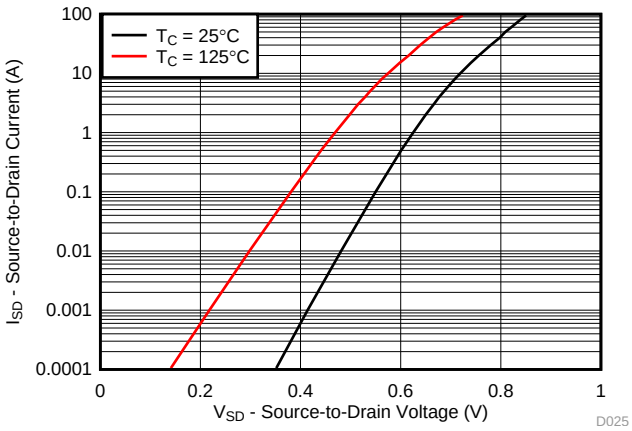


Figure 24. Sync MOSFET Body Diode

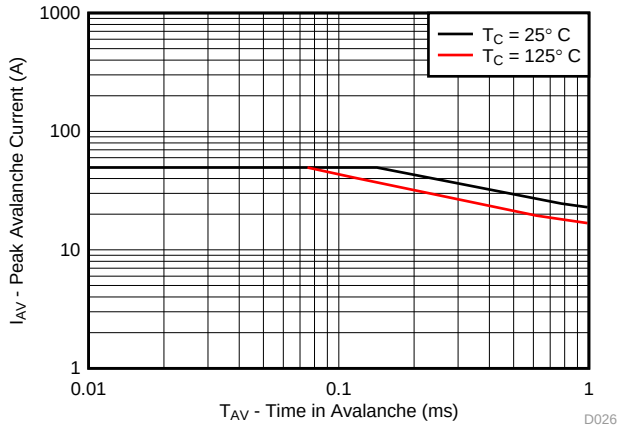


Figure 25. Control MOSFET Unclamped Inductive Switching

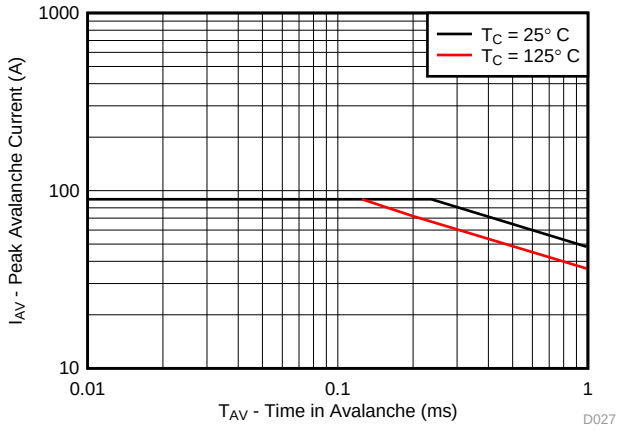


Figure 26. Sync MOSFET Unclamped Inductive Switching

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6 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

The CSD87355Q5D NexFET power block is an optimized design for synchronous buck applications using 5-V gate drive. The Control FET and Sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a new rating method is needed which is tailored towards a more systems centric environment. System level performance curves such as Power Loss, Safe Operating Area, and normalized graphs allow engineers to predict the product performance in the actual application.

6.1.1 Equivalent System Performance

Many of today's high performance computing systems require low power consumption in an effort to reduce system operating temperatures and improve overall system efficiency. This has created a major emphasis on improving the conversion efficiency of today's Synchronous Buck Topology. In particular, there has been an emphasis in improving the performance of the critical Power Semiconductor in the Power Stage of this application (see Figure 27). As such, optimization of the power semiconductors in these applications, needs to go beyond simply reducing $R_{DS(ON)}$.

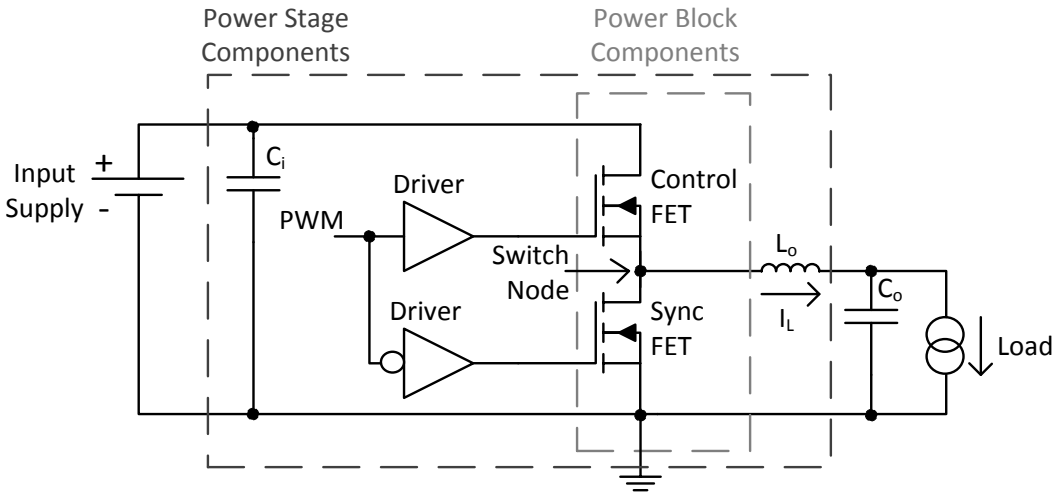


Figure 27.

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Application Information (continued)

The CSD87355Q5D is part of TI's Power Block product family which is a highly optimized product for use in a synchronous buck topology requiring high current, high efficiency, and high frequency. It incorporates TI's latest generation silicon which has been optimized for switching performance, as well as minimizing losses associated with Q_{GD}, Q_{GS}, and Q_{RR}. Furthermore, TI's patented packaging technology has minimized losses by nearly eliminating parasitic elements between the Control FET and Sync FET connections (see Figure 28). A key challenge solved by TI's patented packaging technology is the system level impact of Common Source Inductance (CSI). CSI greatly impedes the switching characteristics of any MOSFET which in turn increases switching losses and reduces system efficiency. As a result, the effects of CSI need to be considered during the MOSFET selection process. In addition, standard MOSFET switching loss equations used to predict system efficiency need to be modified in order to account for the effects of CSI. Further details behind the effects of CSI and modification of switching loss equations are outlined in TI's Application Note SLPA009.

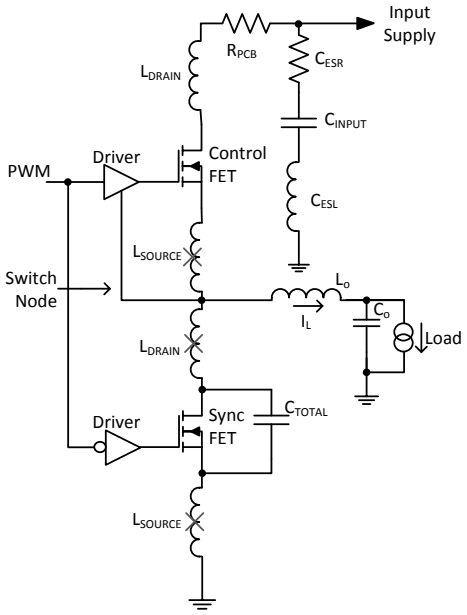
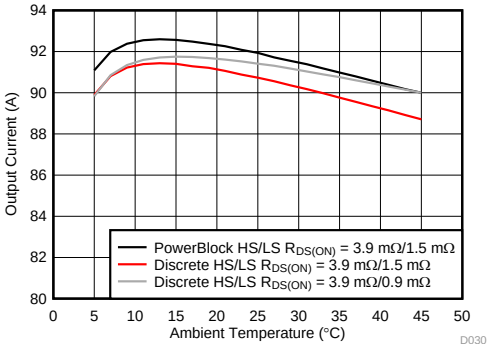


Figure 28.

The combination of TI's latest generation silicon and optimized packaging technology has created a benchmarking solution that outperforms industry standard MOSFET chipsets of similar $R_{DS(ON)}$ and MOSFET chipsets with lower $R_{DS(ON)}$. Figure 29 and Figure 30 compare the efficiency and power loss performance of the CSD87355Q5D versus industry standard MOSFET chipsets commonly used in this type of application. This comparison purely focuses on the efficiency and generated loss of the power semiconductors only. The performance of CSD87355Q5D clearly highlights the importance of considering the Effective AC On-Impedance ($Z_{DS(ON)}$) during the MOSFET selection process of any new design. Simply normalizing to traditional MOSFET $R_{DS(ON)}$ specifications is not an indicator of the actual in-circuit performance when using TI's Power Block technology.

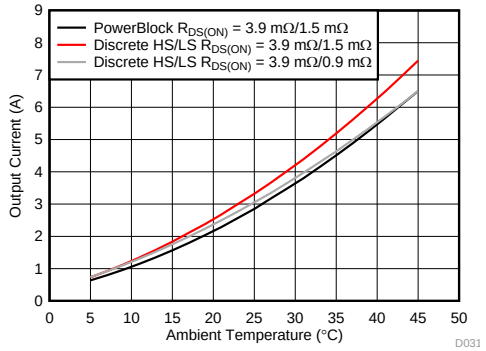
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Application Information (continued)



V_{IN} = 12 V V_{OUT} = 1.3 V L_{OUT} = 0.3 µH
f_{SW} = 500 kHz V_{DD}= 5 V T_A = 25°C

Figure 29. Efficiency



V_{IN} = 12 V V_{OUT} = 1.3 V L_{OUT} = 0.3 µH
f_{SW} = 500 kHz V_{DD} = 5 V T_A = 25°C

Figure 30. Power Loss

Table 1 compares the traditional DC measured $R_{DS(ON)}$ of CSD87355Q5D versus its $Z_{DS(ON)}$. This comparison takes into account the improved efficiency associated with TI's patented packaging technology. As such, when comparing TI's Power Block products to individually packaged discrete MOSFETs or dual MOSFETs in a standard package, the in-circuit switching performance of the solution must be considered. In this example, individually packaged discrete MOSFETs or dual MOSFETs in a standard package would need to have DC measured $R_{DS(ON)}$ values that are equivalent to CSD87355Q5D's $Z_{DS(ON)}$ value in order to have the same efficiency performance at full load. Mid to light-load efficiency will still be lower with individually packaged discrete MOSFETs or dual MOSFETs in a standard package.

Table 1. Comparison of $R_{DS(ON)}$ vs $Z_{DS(ON)}$

PARAMETER	HS		LS		UNIT
	TYP	MAX	TYP	MAX	
Effective AC On-Impedance $Z_{DS(ON)}$ (V_{GS} = 5 V)	3.9	-	0.9	-	mΩ
DC Measured $R_{DS(ON)}$ (V_{GS} = 4.5 V)	3.9	4.7	1.5	1.8	mΩ

6.1.2 Power Loss Curves

MOSFET centric parameters such as $R_{DS(ON)}$ and Q_{gd} are needed to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. Figure 1 plots the power loss of the CSD87355Q5D as a function of load current. This curve is measured by configuring and running the CSD87355Q5D as it would be in the final application (see Figure 31).The measured power loss is the CSD87355Q5D loss and consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$(V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW_AVG} \times I_{OUT}) = \text{Power Loss} \quad (1)$$

The power loss curve in Figure 1 is measured at the maximum recommended junction temperatures of 125°C under isothermal test conditions.

6.1.3 Safe Operating Curves (SOA)

The SOA curves in the CSD87355Q5D data sheet provides guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. Figure 3 to Figure 4 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4" (W) × 3.5" (L) × 0.062" (T) and 6 copper layers of 1-oz. copper thickness.

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6.1.4 Normalized Curves

The normalized curves in the CSD87355Q5D data sheet provides guidance on the Power Loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries will adjust for a given set of system conditions. The primary Y-axis is the normalized change in power loss and the secondary Y-axis is the change is system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the Power Loss curve and the change in temperature is subtracted from the SOA curve.

6.2 Typical Application

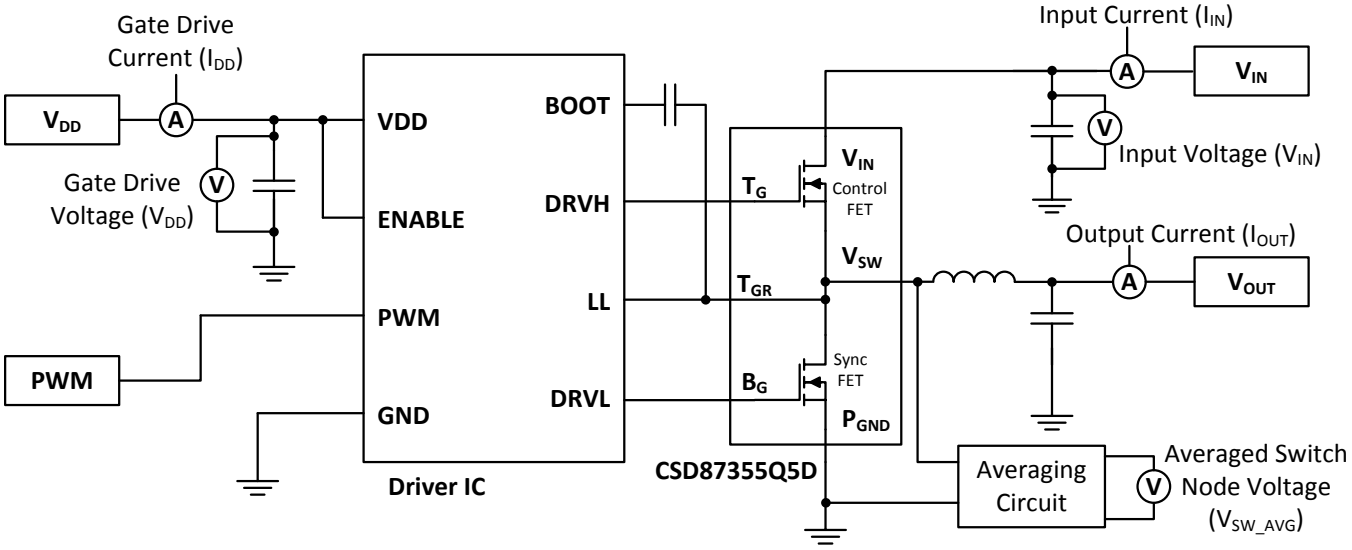


Figure 31.

Typical Application (continued)

6.2.1 Design Example: Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see *Operating Conditions*). Though the Power Loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure will outline the steps the user should take to predict product performance for any set of system conditions.

6.2.2 Operating Conditions

- Output Current = 25 A
- Input Voltage = 7 V
- Output Voltage = 1.4 V
- Switching Frequency = 800 kHz
- Inductor = 0.2 µH

6.2.2.1 Calculating Power Loss

- Power Loss at 25 A = 3.62 W (Figure 1)
- Normalized Power Loss for input voltage ≈ 0.99 (Figure 6)
- Normalized Power Loss for output voltage ≈ 1.02 (Figure 7)
- Normalized Power Loss for switching frequency ≈ 1.06 (Figure 5)
- Normalized Power Loss for output inductor ≈ 1.03 (Figure 8)
- **Final calculated Power Loss = 3.62 W × 0.99 × 1.02 × 1.06 × 1.03 ≈ 3.99 W**

6.2.2.2 Calculating SOA Adjustments

- SOA adjustment for input voltage ≈ –0.24ºC (Figure 6)
- SOA adjustment for output voltage ≈ 0.63ºC (Figure 7)
- SOA adjustment for switching frequency ≈ 2.12ºC (Figure 5)
- SOA adjustment for output inductor ≈ 0.91ºC (Figure 8)
- **Final calculated SOA adjustment = –0.24 + 0.63 + 2.12 + 0.91 ≈ 3.42C**

In the previous design example, the estimated power loss of the CSD87355Q5D would increase to 4 W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by 3.4ºC. Figure 32 graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board/ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 3.4ºC. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board/ambient temperature.

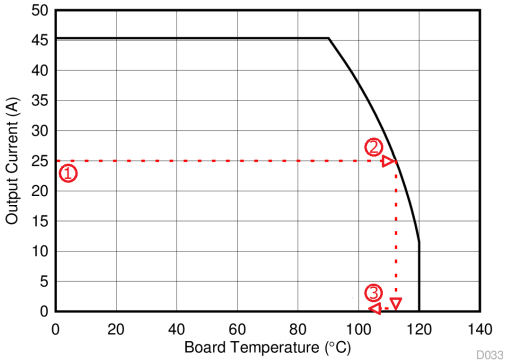


Figure 32. Power Block SOA

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7 Layout

7.1 Layout Guidelines

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout will yield maximum performance in both areas. The following sections provide a brief description on how to address each parameter.

7.1.1 Electrical Performance

The Power Block has the ability to switch voltages at rates greater than 10 kV/µs. Take special care with the PCB layout design and placement of the input capacitors, Driver IC, and output inductor.

- The placement of the input capacitors relative to the Power Block's VIN and PGND pins should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the VIN and PGND pins (see Figure 33). The example in Figure 33 uses 6 × 10-µF ceramic capacitors (TDK Part # C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the Power Block, C5, C7, C19, and C8 should follow in order.
- The Driver IC should be placed relatively close to the Power Block Gate pins. T_G and B_G should connect to the outputs of the Driver IC. The T_{GR} pin serves as the return path of the high-side gate drive circuitry and should be connected to the Phase pin of the IC (sometimes called LX, LL, SW, PH, etc.). The bootstrap capacitor for the Driver IC will also connect to this pin.
- The switching node of the output inductor should be placed relatively close to the Power Block VSW pins. Minimizing the node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level.
- In the event the switch node waveform exhibits ringing that reaches undesirable levels, the use of a Boost Resistor or RC snubber can be an effective way to reduce the peak ring level. The recommended Boost Resistor value will range between 1 Ω to 4.7 Ω depending on the output characteristics of Driver IC used in conjunction with the Power Block. The RC snubber values can range from 0.5 Ω to 2.2 Ω for the R and 330 pF to 2200 pF for the C. Refer to TI App Note SLUP100 for more details on how to properly tune the RC snubber values. The RC snubber should be placed as close as possible to the Vsw node and PGND see Figure 33. (1)

7.1.2 Thermal Considerations

The Power Block has the ability to use the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in Figure 33 uses vias with a 10 mil drill hole and a 16 mil capture pad.
- Tent the opposite side of the via with solder-mask.

In the end, the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

(1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

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7.2 Layout Example

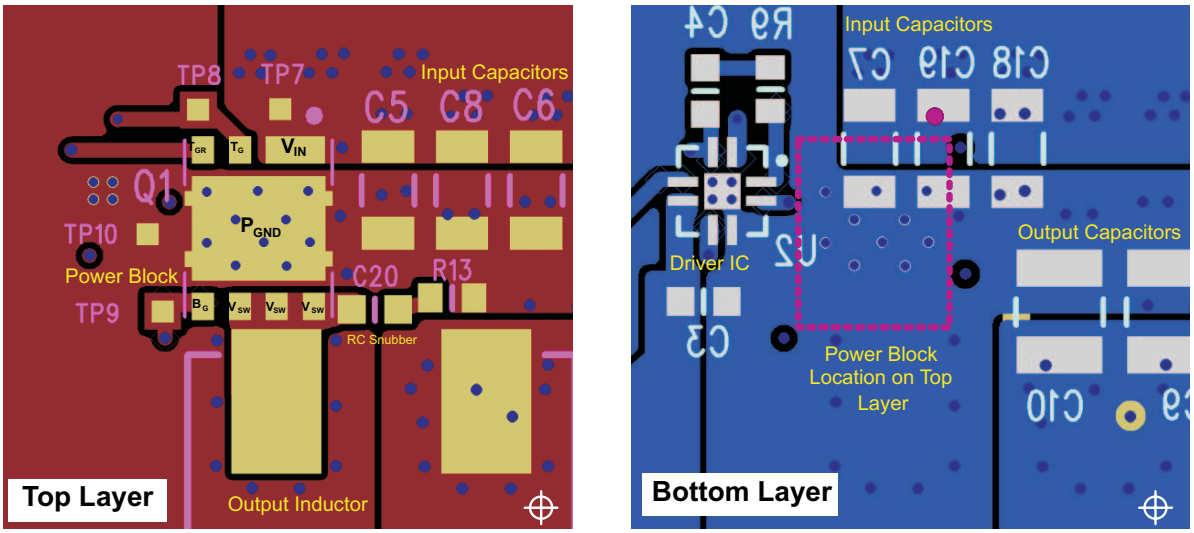


Figure 33. Recommended PCB Layout (Top View)

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8 Device and Documentation Support

8.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

8.2 Trademarks

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8.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

8.4 Glossary

SLYZ022 — *TI Glossary*.

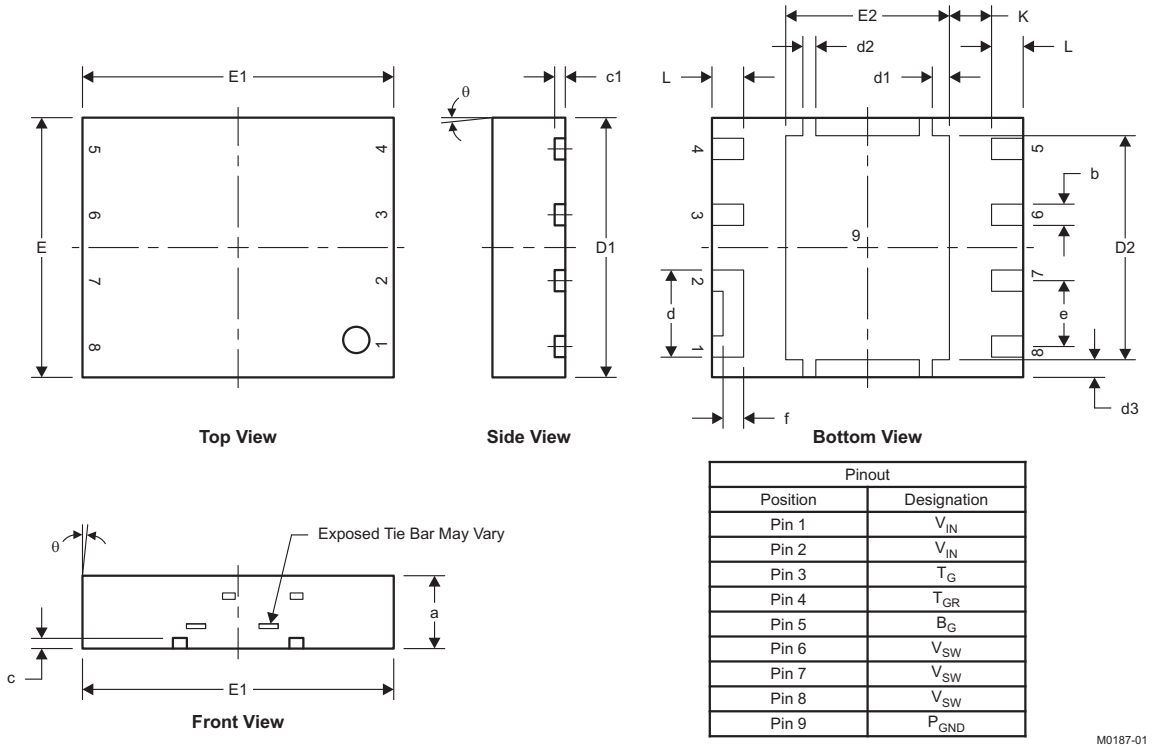
This glossary lists and explains terms, acronyms, and definitions.

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9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

9.1 Q5D Package Dimensions



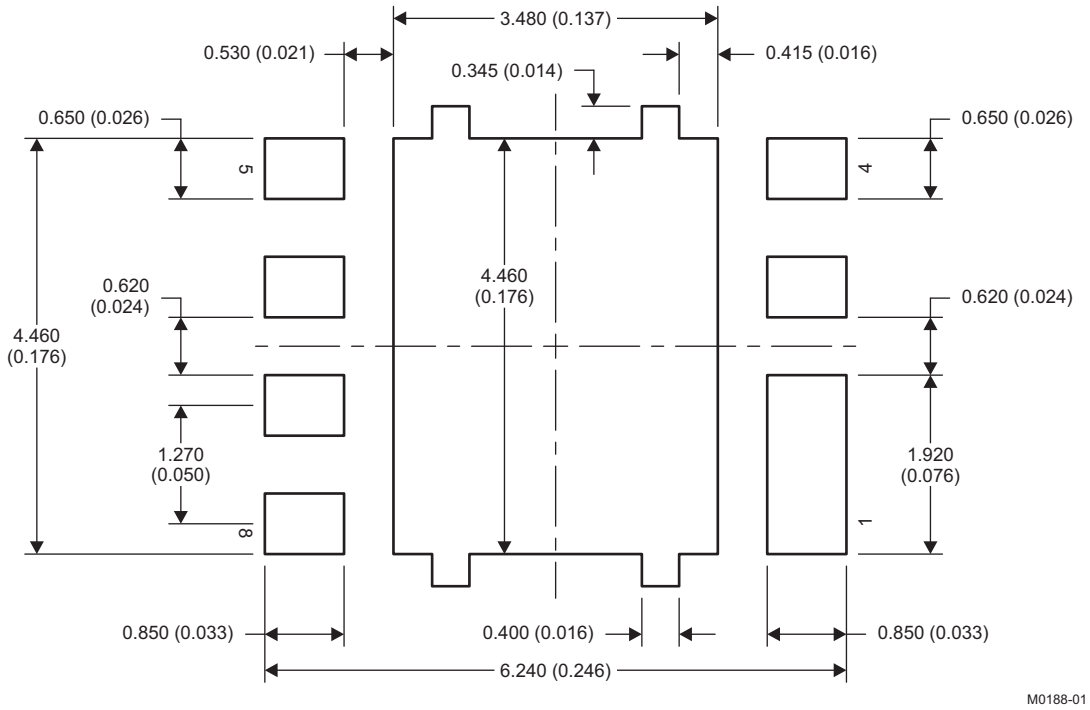
Pinout	
Position	Designation
Pin 1	V_{IN}
Pin 2	V_{IN}
Pin 3	T_G
Pin 4	T_{GR}
Pin 5	B_G
Pin 6	V_{SW}
Pin 7	V_{SW}
Pin 8	V_{SW}
Pin 9	P_{GND}

M0187-01

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
a	1.40	1.5	0.055	0.059
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
d	1.630	1.730	0.064	0.068
d1	0.280	0.380	0.011	0.015
d2	0.200	0.300	0.008	0.012
d3	0.291	0.391	0.012	0.015
D1	4.900	5.100	0.193	0.201
D2	4.269	4.369	0.168	0.172
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.106	3.206	0.122	0.126
e	1.27 TYP		0.050	
f	0.396	0.496	0.016	0.020
L	0.510	0.710	0.020	0.028
θ	0.00	—	—	—
K	0.812		0.032	

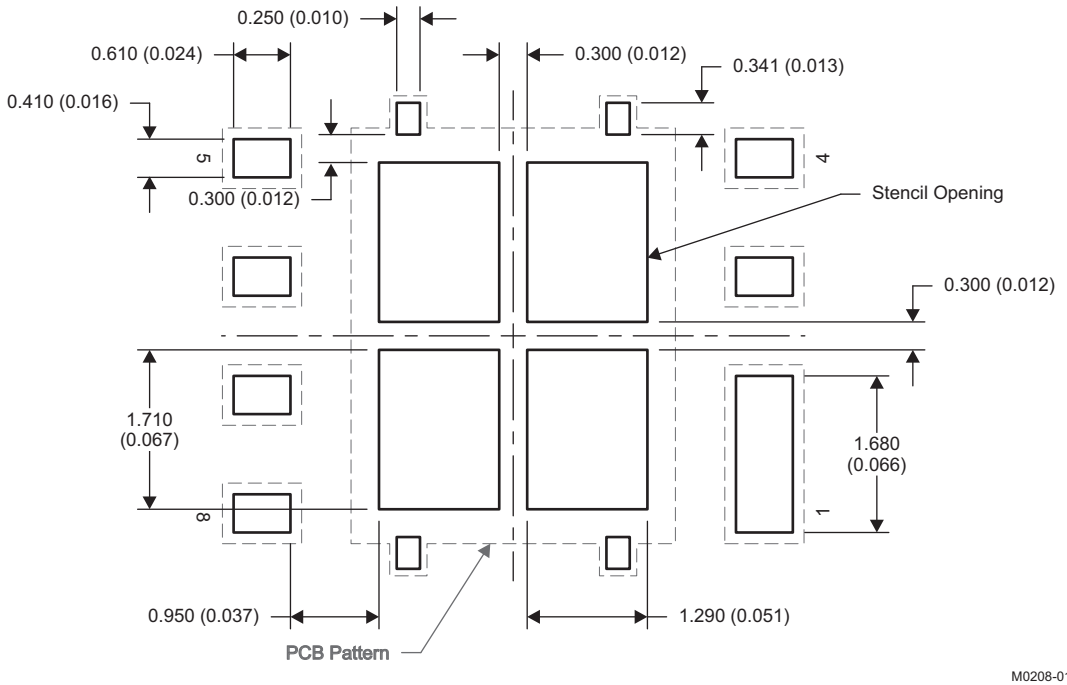
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9.2 Land Pattern Recommendation



NOTE: Dimensions are in mm (inches).

9.3 Stencil Recommendation



NOTE: Dimensions are in mm (inches).

For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD87355Q5D	ACTIVE	LSON-CLIP	DQY	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87355D	Samples
CSD87355Q5DT	ACTIVE	LSON-CLIP	DQY	8	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87355D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

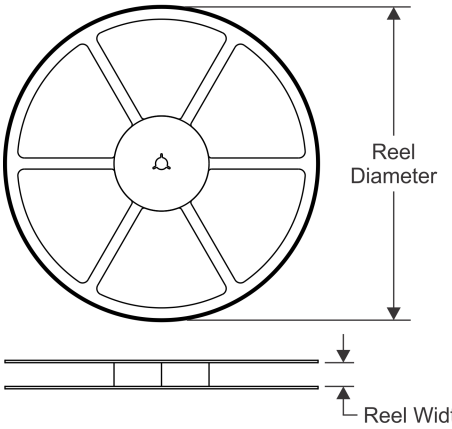
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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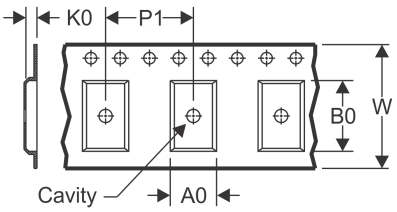
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

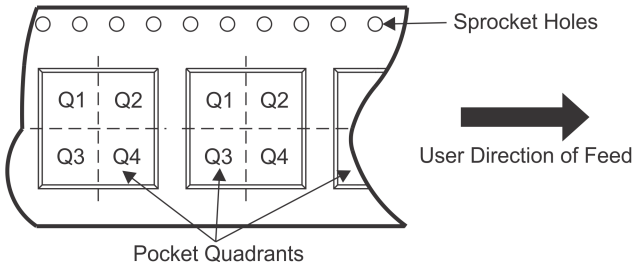


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

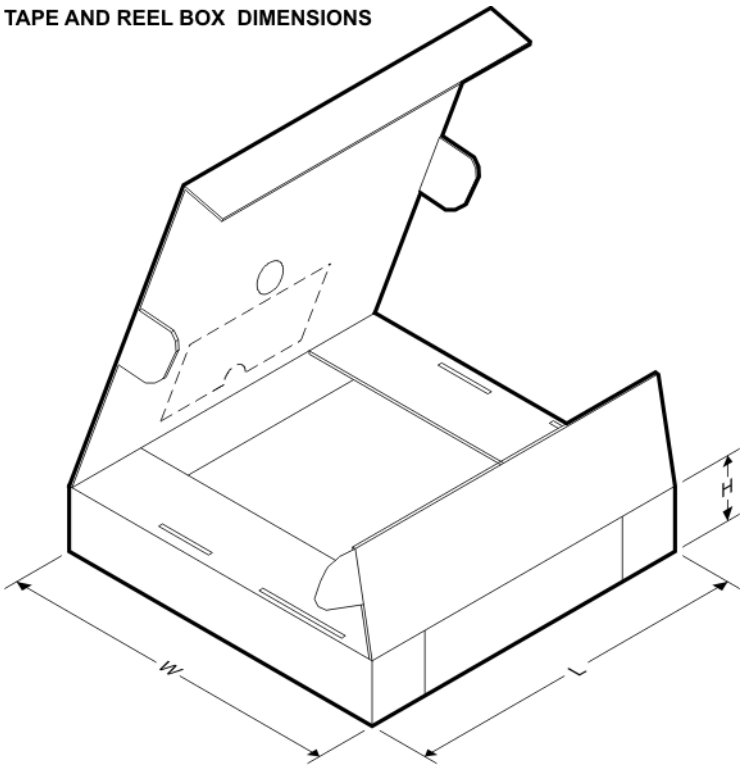
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD87355Q5D	LSON-CLIP	DQY	8	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q2
CSD87355Q5DT	LSON-CLIP	DQY	8	250	180.0	12.4	5.3	6.3	1.8	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD87355Q5D	LSON-CLIP	DQY	8	2500	367.0	367.0	35.0
CSD87355Q5DT	LSON-CLIP	DQY	8	250	182.0	182.0	20.0

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