CSD25485F5 –20-V P-Channel FemtoFET™ MOSFET

1 Features

- Low-On Resistance
- Low Q_g and Q_{gd}
- Ultra-Small Footprint
  - 1.53 mm × 0.77 mm
  - 0.50-mm Pad Pitch
- Low Profile
  - 0.35-mm Height
- Integrated ESD Protection Diode
  - Rated > 4-kV HBM
  - Rated > 2-kV CDM
- Lead and Halogen Free
- RoHS Compliant

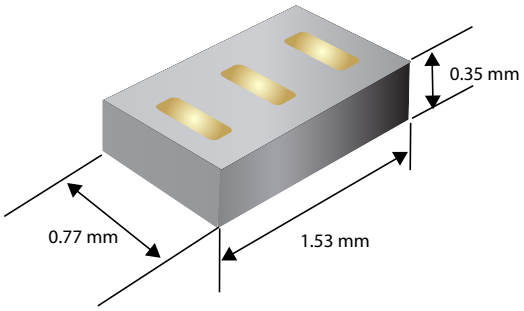
2 Applications

- Optimized for Industrial Load Switch Applications
- Optimized for General Purpose Switching Applications

3 Description

This 29.7-mΩ, –20-V, P-Channel FemtoFET™ MOSFET technology is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing a significant reduction in footprint size.

Typical Part Dimensions



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	–20		V
Q_g	Gate Charge Total (–4.5 V)	2.7		nC
Q_{gd}	Gate Charge Gate-to-Drain	0.56		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = –1.8 V	89	mΩ
		V_{GS} = –2.5 V	51	
		V_{GS} = –4.5 V	35	
		V_{GS} = –8 V	29.7	
$V_{GS(th)}$	Threshold Voltage	–0.95		V

Device Information(1)

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD25485F5	3000	7-Inch Reel	Femto 1.53-mm × 0.77-mm SMD Leadless	Tape and Reel
CSD25485F5T	250			

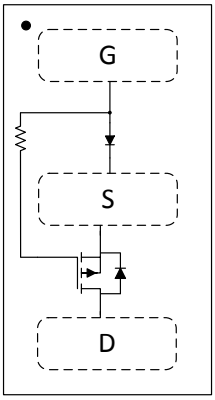
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	–20	V
V_{GS}	Gate-to-Source Voltage	–12	V
I_D	Continuous Drain Current(1)	–3.2	A
	Continuous Drain Current(2)	–5.3	
I_{DM}	Pulsed Drain Current(1)(3)	–31	A
P_D	Power Dissipation(1)	0.5	W
	Power Dissipation(2)	1.4	
$V_{(ESD)}$	Human-Body Model (HBM)	4000	V
	Charged-Device Model (CDM)	2000	
T_J, T_{stg}	Operating Junction, Storage Temperature	–55 to 150	°C

(1) Min Cu, typical $R_{\theta JA}$ = 245°C/W.
(2) Max Cu, typical $R_{\theta JA}$ = 90°C/W.
(3) Pulse duration ≤ 100 μs, duty cycle ≤ 1%.

Top View



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 **Features** ... 1
2 **Applications** ... 1
3 **Description** ... 1
4 **Revision History** ... 2
5 **Specifications** ... 3
5.1 Electrical Characteristics ... 3
5.2 Thermal Information ... 3
5.3 Typical MOSFET Characteristics ... 4
6 **Device and Documentation Support** ... 7
6.1 Receiving Notification of Documentation Updates ... 7
6.2 Community Resources ... 7
6.3 Trademarks ... 7
6.4 Electrostatic Discharge Caution ... 7
6.5 Glossary ... 7
7 **Mechanical, Packaging, and Orderable Information** ... 8
7.1 Mechanical Dimensions ... 8
7.2 Recommended Minimum PCB Layout ... 9
7.3 Recommended Stencil Pattern ... 9

4 Revision History

Changes from Original (August 2016) to Revision A **Page**

- Changed Min Cu $R_{\theta JA}$ from 90°C/W : to 245°C/W in Figure 11 ... 4
- Added Table 1 in the *Mechanical Dimensions* section ... 8

Copyright © 2016–2017, Texas Instruments Incorporated

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = –250 µA	–20			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = –16 V			–100	nA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = –12 V			–25	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = –250 µA	–0.7	–0.95	–1.3	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = –1.8 V, I_{DS} = –0.1 A		89	250	mΩ
		V_{GS} = –2.5 V, I_{DS} = –0.9 A		51	70	
		V_{GS} = –4.5 V, I_{DS} = –0.9 A		35	42	
		V_{GS} = –8 V, I_{DS} = –0.9 A		29.7	35	
g_{fs}	Transconductance	V_{DS} = –2 V, I_{DS} = –0.9 A		7		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = –10 V, f = 1 MHz		410	533	pF
C_{oss}	Output capacitance			212	276	pF
C_{rss}	Reverse transfer capacitance			17	23	pF
R_G	Series gate resistance			20		Ω
Q_g	Gate charge total (–4.5 V)	V_{DS} = –10 V, I_{DS} = –0.9 A		2.7	3.5	nC
Q_{gd}	Gate charge gate-to-drain			0.56		nC
Q_{gs}	Gate charge gate-to-source			0.67		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.40		nC
Q_{oss}	Output charge	V_{DS} = –10 V, V_{GS} = 0 V		4.4		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = –10 V, V_{GS} = –4.5 V, I_{DS} = –0.9 A, R_G = 2 Ω		14		ns
t_r	Rise time			6		ns
$t_{d(off)}$	Turnoff delay time			27		ns
t_f	Fall time			14		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = –0.9 A, V_{GS} = 0 V		–0.75	–1	V

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)		90		°C/W
	Junction-to-ambient thermal resistance(2)		245		

(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

Copyright © 2016–2017, Texas Instruments Incorporated

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

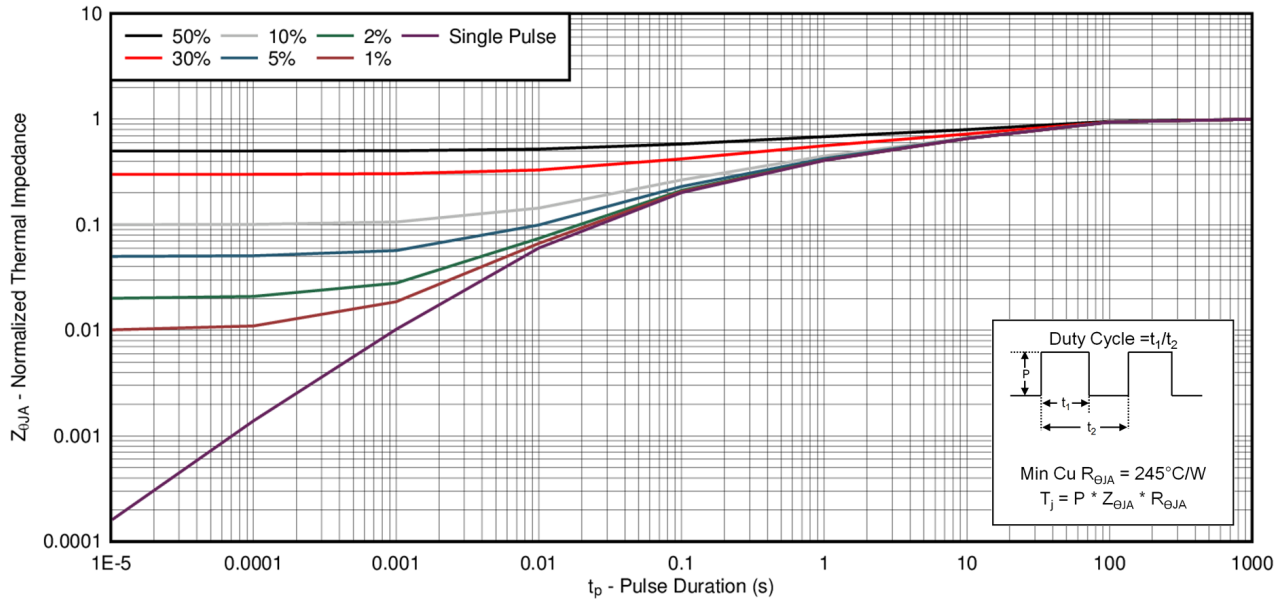


Figure 1. Transient Thermal Impedance

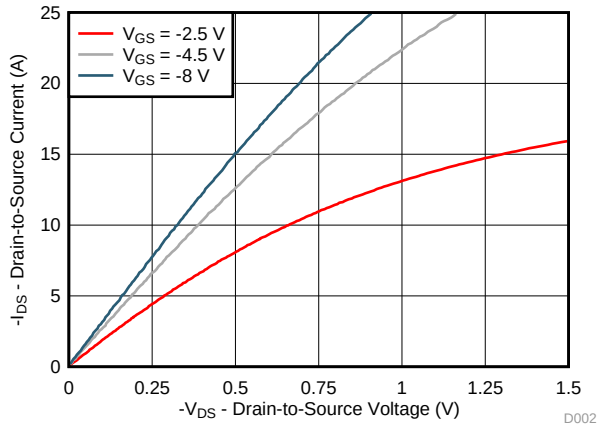


Figure 2. Saturation Characteristics

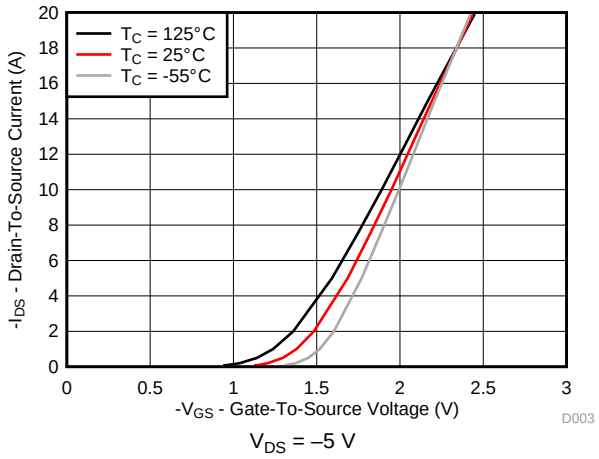


Figure 3. Transfer Characteristics

Copyright © 2016–2017, Texas Instruments Incorporated

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

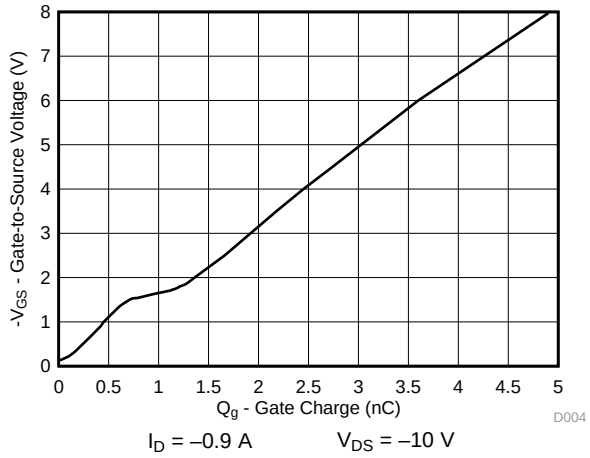


Figure 4. Gate Charge

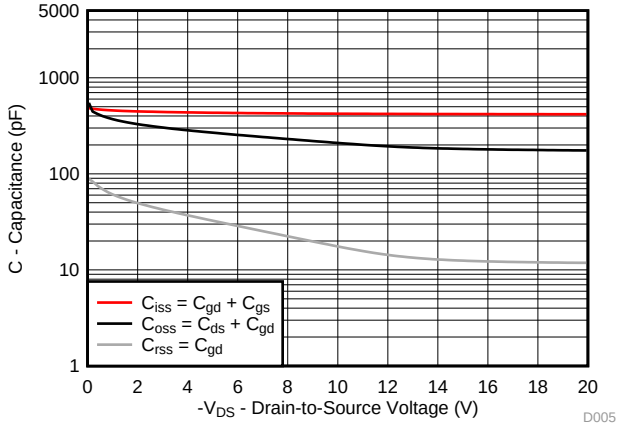


Figure 5. Capacitance

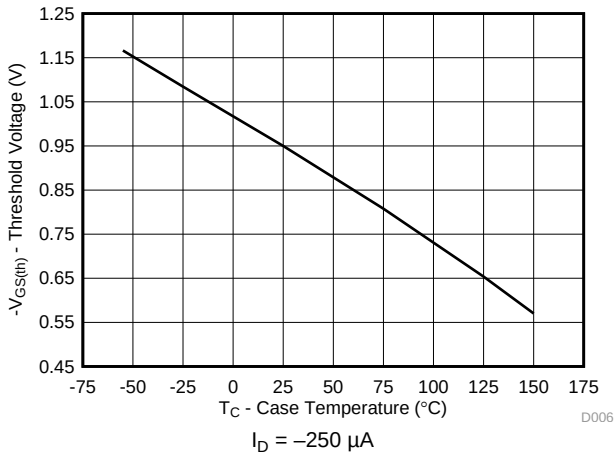


Figure 6. Threshold Voltage vs Temperature

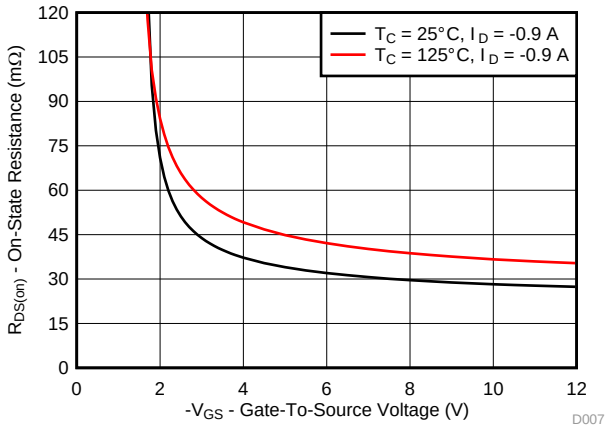


Figure 7. On-State Resistance vs Gate-to-Source Voltage

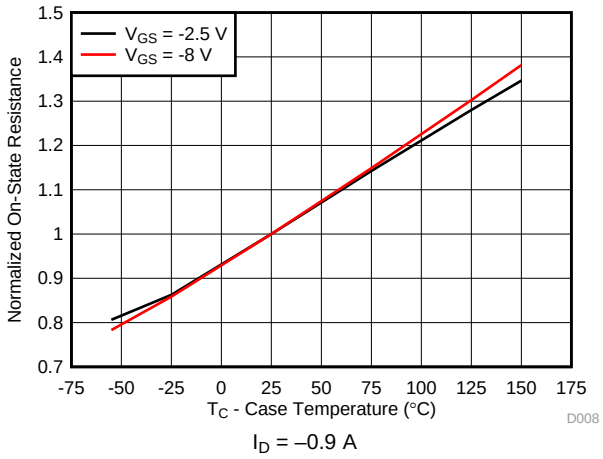


Figure 8. Normalized On-State Resistance vs Temperature

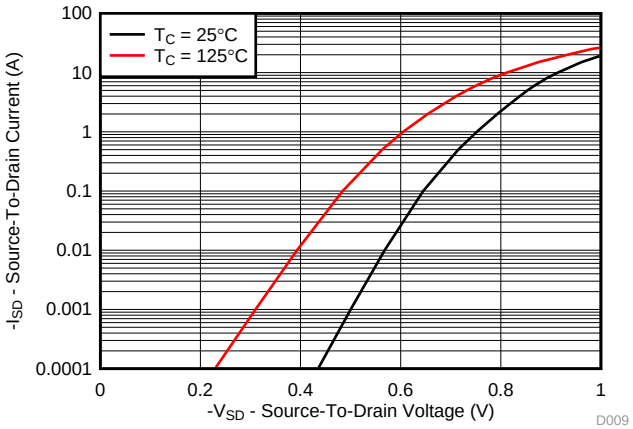
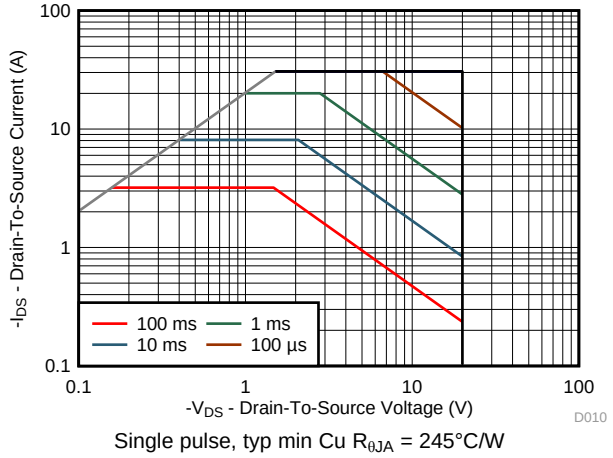


Figure 9. Typical Diode Forward Voltage

Copyright © 2016–2017, Texas Instruments Incorporated

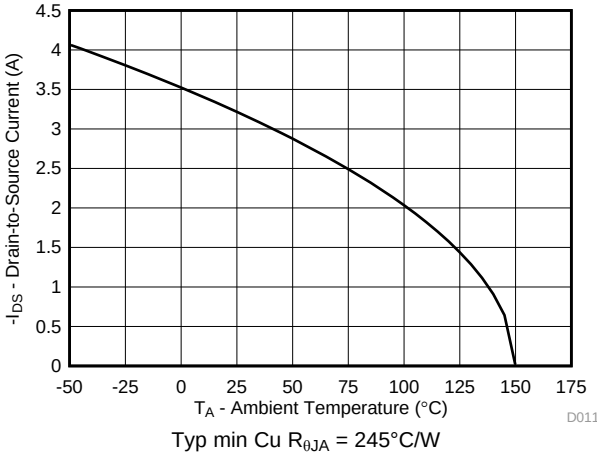
Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)



Single pulse, typ min Cu $R_{\theta JA}$ = 245°C/W

Figure 10. Maximum Safe Operating Area (SOA)



Typ min Cu $R_{\theta JA}$ = 245°C/W

Figure 11. Maximum Drain Current vs Temperature

Copyright © 2016–2017, Texas Instruments Incorporated

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

FemtoFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

SLYZ022 — *TI Glossary*.

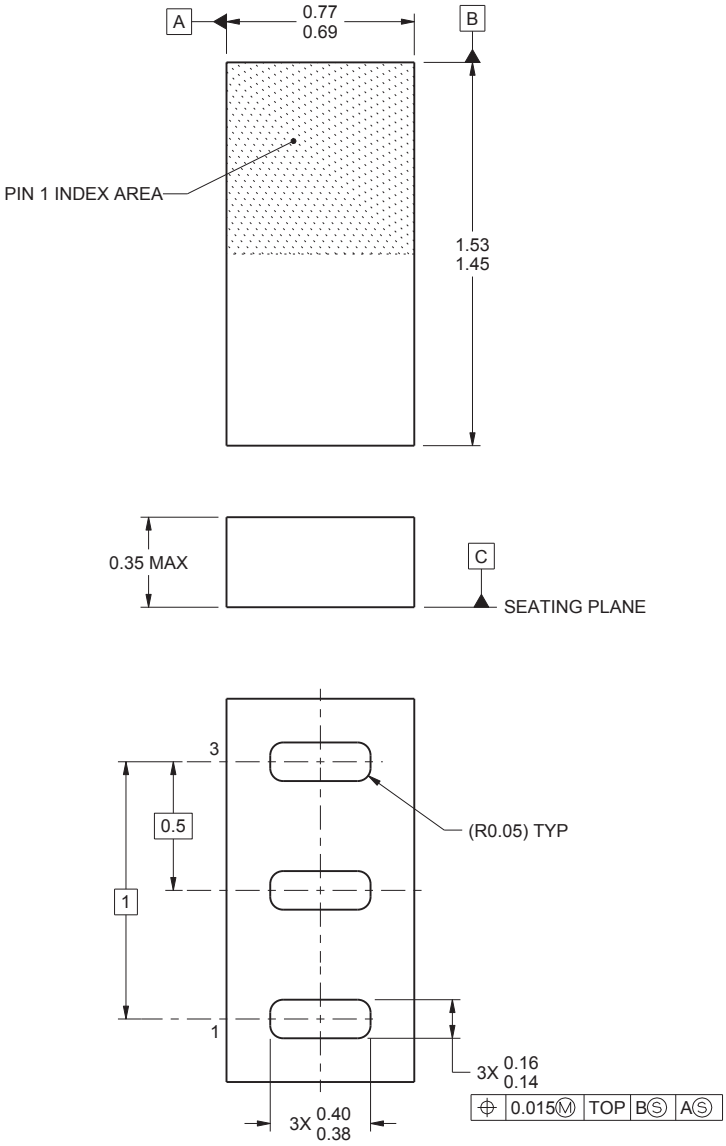
This glossary lists and explains terms, acronyms, and definitions.

Copyright © 2016–2017, Texas Instruments Incorporated

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions



(1) All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).

(2) This drawing is subject to change without notice.

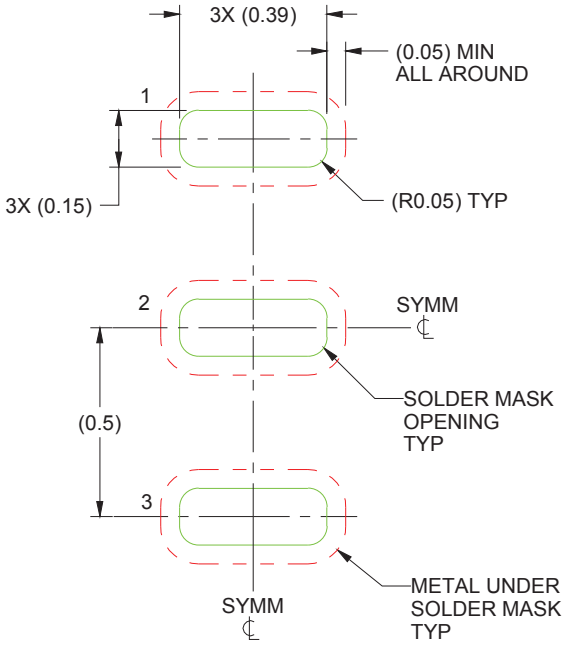
(3) This package is a PB-free solder land design.

Table 1. Pin Configuration

POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

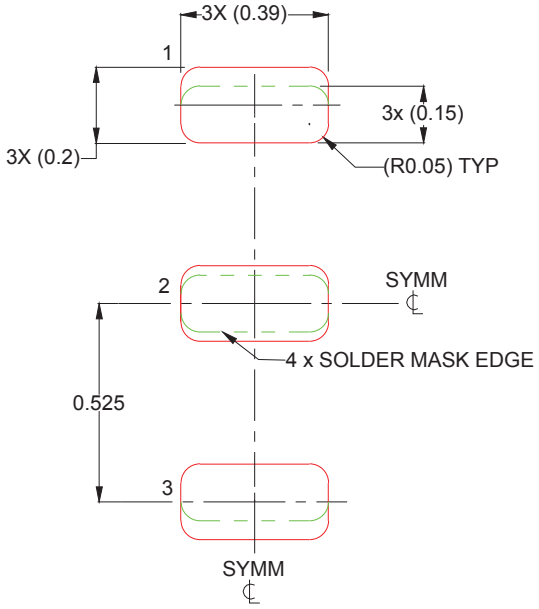
Copyright © 2016–2017, Texas Instruments Incorporated

7.2 Recommended Minimum PCB Layout



(1) All dimensions are in millimeters.

7.3 Recommended Stencil Pattern



(1) All dimensions are in millimeters.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25485F5	ACTIVE	PICOSTAR	YJK	3	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-55 to 150	3H	Samples
CSD25485F5T	ACTIVE	PICOSTAR	YJK	3	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-55 to 150	3H	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

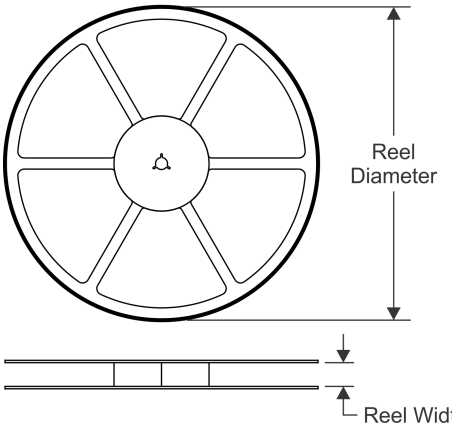
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

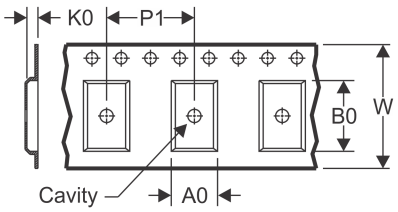
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

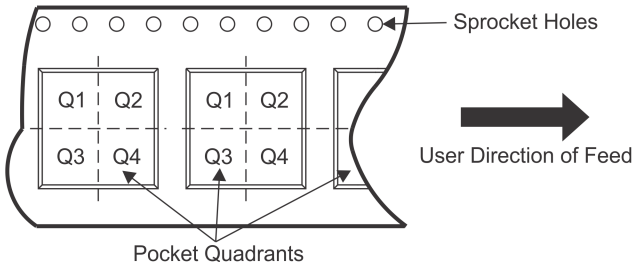


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

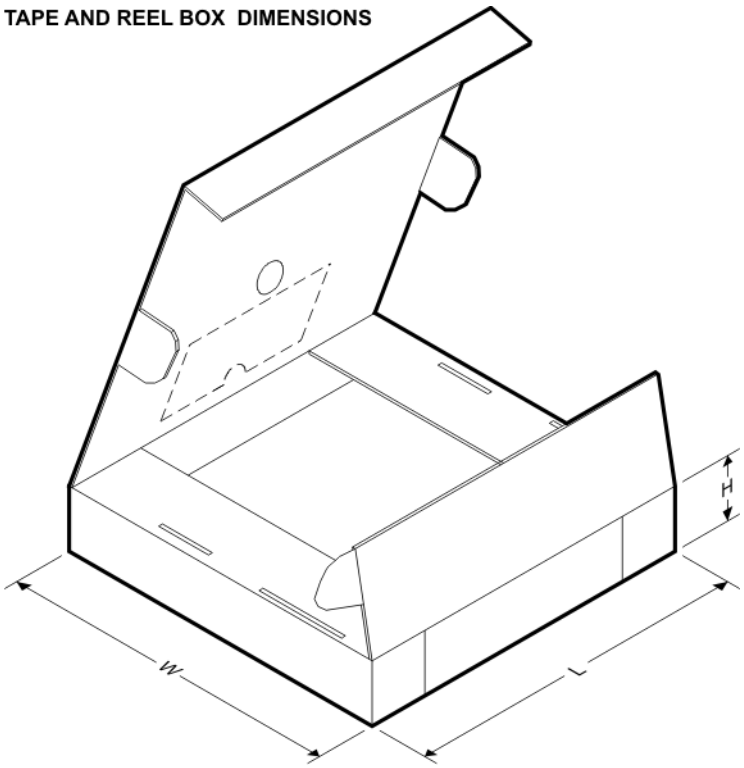
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25485F5	PICOSTAR	YJK	3	3000	180.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1
CSD25485F5T	PICOSTAR	YJK	3	250	180.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25485F5	PICOSTAR	YJK	3	3000	182.0	182.0	20.0
CSD25485F5T	PICOSTAR	YJK	3	250	182.0	182.0	20.0

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated