CSD25480F3 -20V P 沟道 FemtoFET™ MOSFET

1 特性

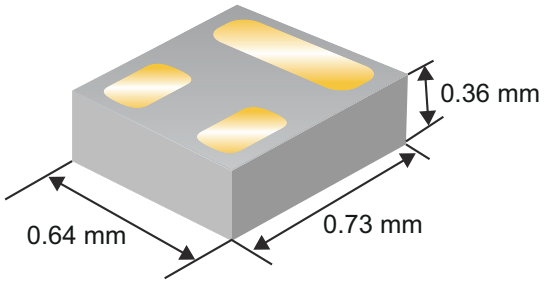
- 低导通电阻
- 超低 Q_g 和 Q_{gd}
- 超小尺寸
  - 0.73mm × 0.64mm
- 薄型封装
  - 最大厚度为 0.36mm
- 集成型 ESD 保护二极管
- 无铅且无卤素
- 符合 RoHS

2 应用

- 针对负载开关应用进行了优化
- 针对通用开关应用进行了优化
- 电池应用
- 手持式和移动类应用

3 说明

该 -20V、110mΩ P 沟道 FemtoFET™ MOSFET 经过设计和优化，能够最大限度地减小在许多手持式和移动应用中占用的空间。这项技术能够在替代标准小信号 MOSFET 的同时大幅减小封装尺寸。



典型器件尺寸

产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	-20		V
Q_g	栅极电荷总量 (-4.5V)	0.7		nC
Q_{gd}	栅极电荷（栅极到漏极）	0.10		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = – 1.8V	420	mΩ
		V_{GS} = -2.5V	203	
		V_{GS} = -4.5V	132	
		V_{GS} = -8.0V	110	
$V_{GS(th)}$	阈值电压	-0.95		V

器件信息(1)

器件	数量	介质	封装	配送
CSD25480F3	3000	7 英寸卷带	Femto 0.73mm × 0.64mm 基板栅格阵列 (LGA)	卷带包装
CSD25480F3T	250			

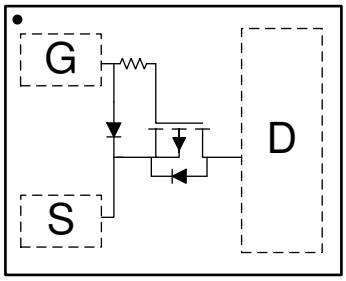
(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

绝对最大额定值

T_A = 25°C（除非另外注明）		值	单位
V_{DS}	漏源电压	-20	V
V_{GS}	栅源电压	-12	V
I_D	持续漏极电流(1)	– 1.7	A
I_{DM}	脉冲漏极电流(1) (2)	– 10.6	A
P_D	功率耗散(1)	500	mW
$V_{(ESD)}$	人体放电模型 (HBM)	4000	V
	充电器件模型 (CDM)	2000	
T_J、T_{stg}	工作结温、贮存温度	– 55 至 150	°C

(1) 安装在覆铜区域最小的 FR4 电路板上时的典型 $R_{\theta JA}$ = 255°C/W。

(2) 脉冲持续时间 ≤ 100 µs，占空比 ≤ 1%。



顶视图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

Changes from Revision A (August 2017) to Revision B (February 2022)	Page
• 将超薄型封装要点中的厚度从 0.35mm 更改为 0.36mm	1
• 将超薄型封装图片中的厚度从 0.35mm 更新为 0.36mm	1
• Changed ultra-low profile image height from 0.35 mm to 0.36 mm	8
• Added FemtoFET Surface Mount Guide note	9

Changes from Revision * (April 2016) to Revision A (August 2017)	Page
• Added the 节 *6.1* section in 节 *6*	7
• Added Recommended Minimum PCB Layout	9
• Updated the 节 *7.3*	9

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5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = –250 μA	–20			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = –16 V			–50	nA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = –12 V			–25	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = –250 μA	–0.70	–0.95	–1.20	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = –1.8 V, I_{DS} = –0.1 A		420	840	mΩ
		V_{GS} = –2.5 V, I_{DS} = –0.4 A		203	260	
		V_{GS} = –4.5 V, I_{DS} = –0.4 A		132	159	
		V_{GS} = –8 V, I_{DS} = –0.4 A		110	132	
g_{fs}	Transconductance	V_{DS} = –10 V, I_{DS} = –0.4 A		8.0		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = –10 V, f = 1 MHz		119	155	pF
C_{oss}	Output capacitance			48	62	pF
C_{rss}	Reverse transfer capacitance			3.6	4.7	pF
R_G	Series gate resistance			16		Ω
Q_g	Gate charge total (–4.5 V)	V_{DS} = –10 V, I_{DS} = –0.4 A		0.70	0.91	nC
Q_{gd}	Gate charge gate-to-drain			0.10		nC
Q_{gs}	Gate charge gate-to-source			0.26		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.15		nC
Q_{oss}	Output charge	V_{DS} = –10 V, V_{GS} = 0 V		1.3		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = –10 V, V_{GS} = –4.5 V, I_{DS} = –0.4 A, R_G = 10 Ω		9		ns
t_r	Rise time			5		ns
$t_{d(off)}$	Turnoff delay time			13		ns
t_f	Fall time			7		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = –0.4 A, V_{GS} = 0 V		–0.78	–1.0	V
Q_{rr}	Reverse recovery charge	V_{DS}= –10 V, I_F = –0.4 A, di/dt = 100 A/μs		1.2		nC
t_{rr}	Reverse recovery time			6.4		ns

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	90	°C/W
	Junction-to-ambient thermal resistance(2)	255	

(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz. (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

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5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

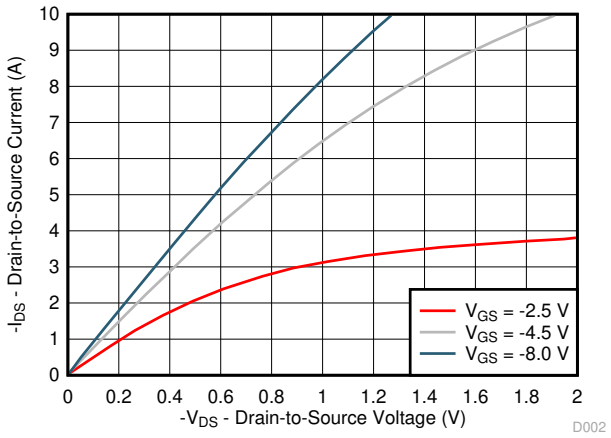
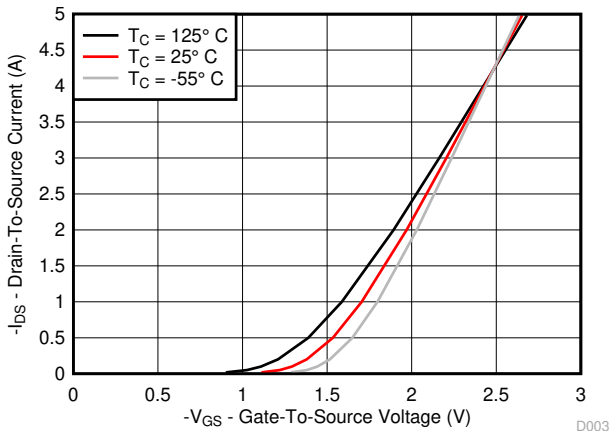


图 5-1. Saturation Characteristics



VDS = – 5 V

图 5-2. Transfer Characteristics

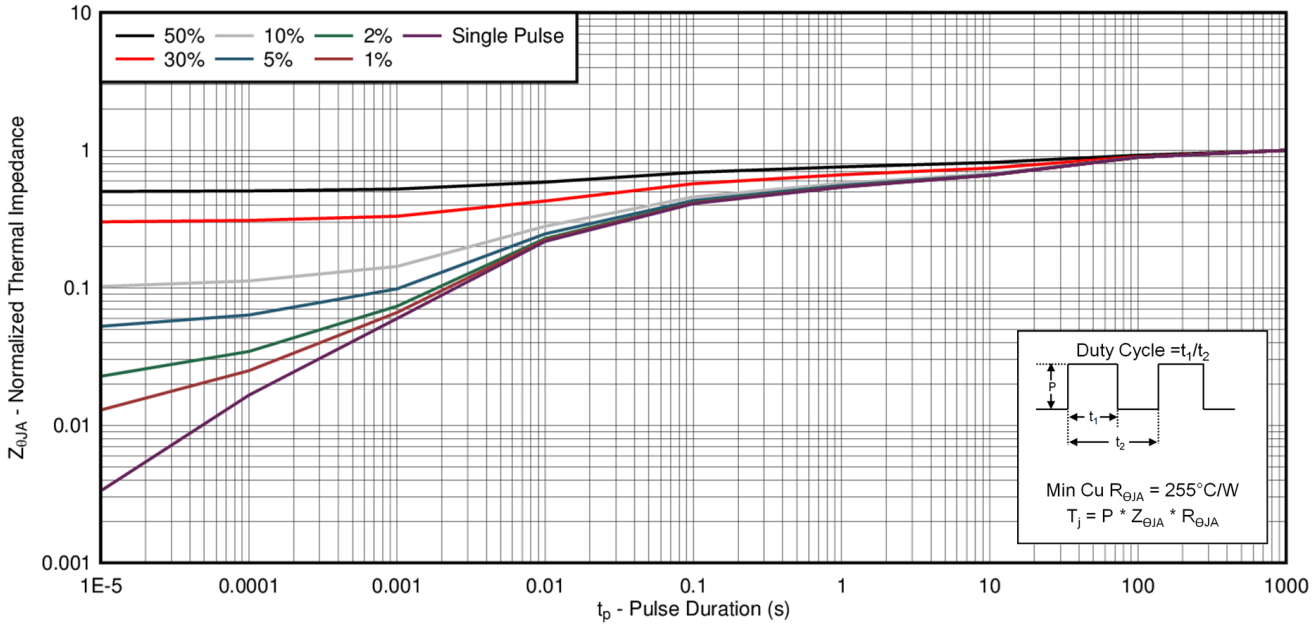
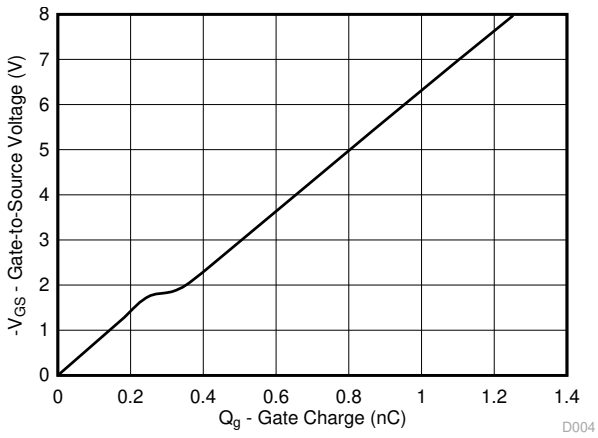


图 5-3. Transient Thermal Impedance

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I_D = –0.4 A V_{DS} = –10 V

图 5-4. Gate Charge

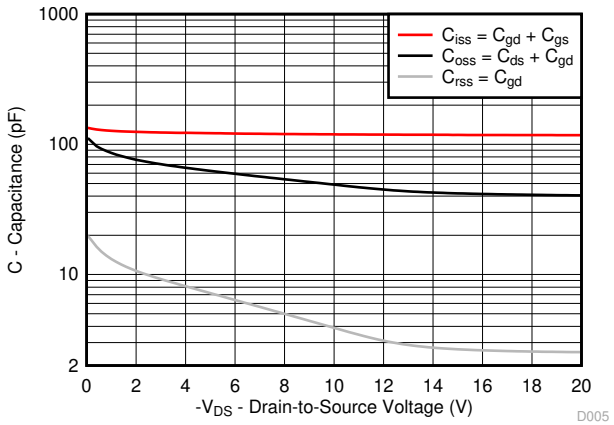
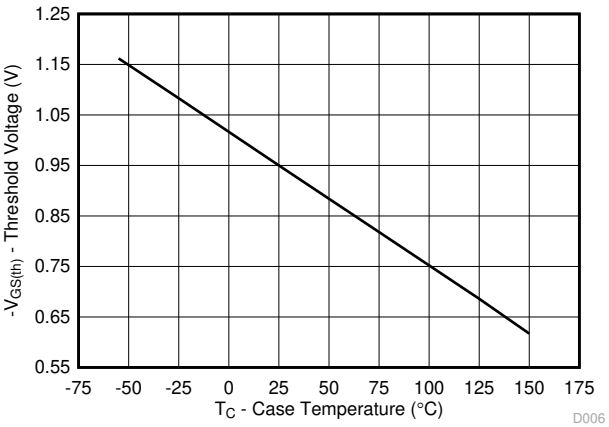


图 5-5. Capacitance



I_D = –250 µA

图 5-6. Threshold Voltage vs Temperature

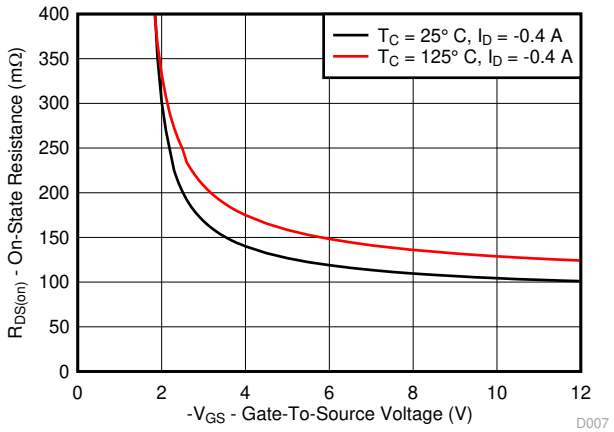
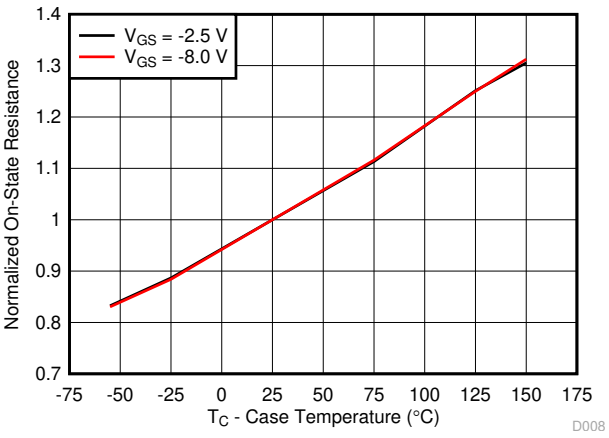


图 5-7. On-State Resistance vs Gate-to-Source Voltage



I_D = –0.4 A

图 5-8. Normalized On-State Resistance vs Temperature

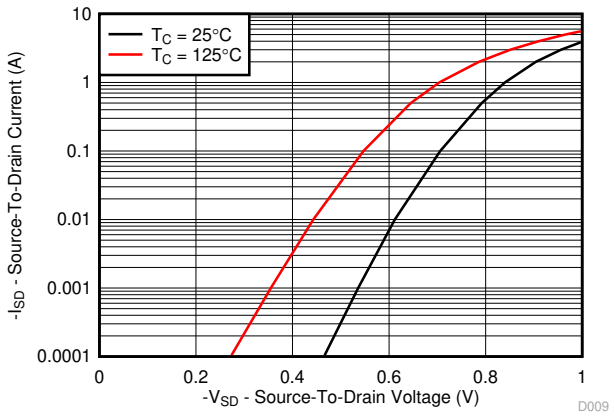
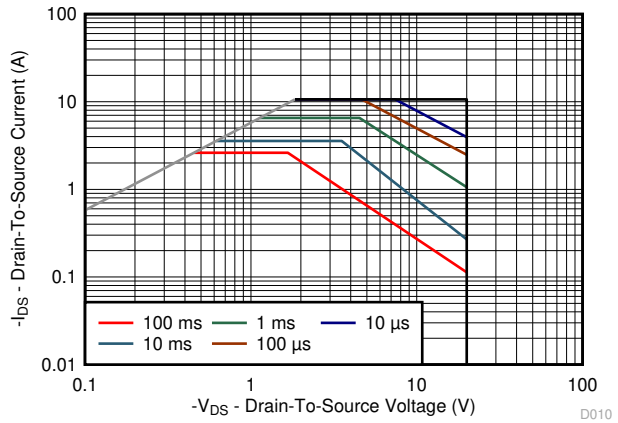


图 5-9. Typical Diode Forward Voltage

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Single pulse, max $R_{\theta JA}$ = 245°C/W

图 5-10. Maximum Safe Operating Area

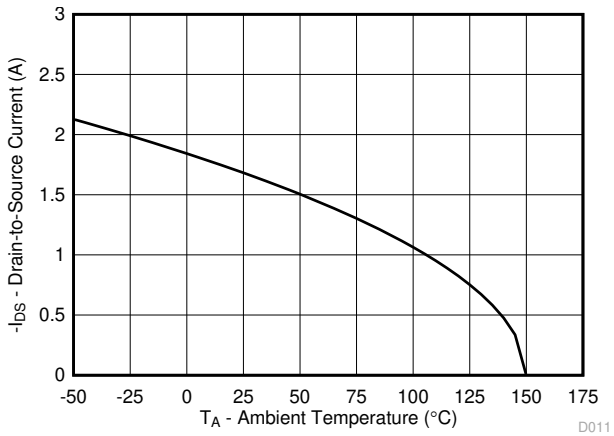


图 5-11. Maximum Drain Current vs Temperature

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6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Trademarks

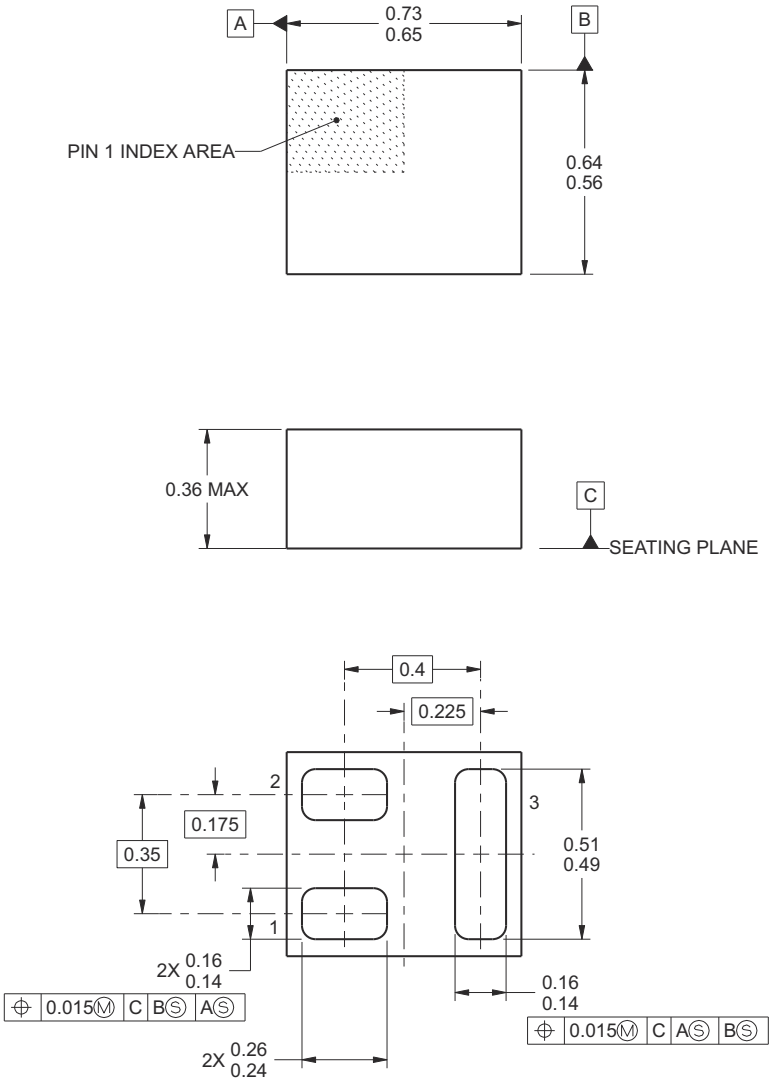
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7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions



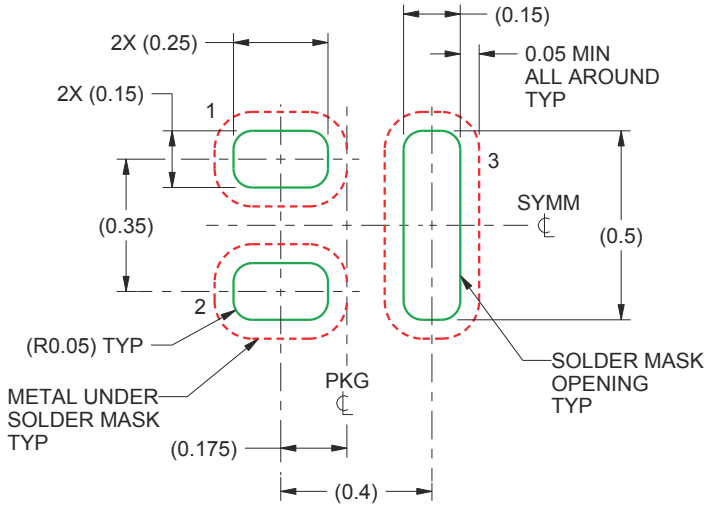
A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
B. This drawing is subject to change without notice.
C. This package is a lead-free solder land design.

表 7-1. Pin Configuration

POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

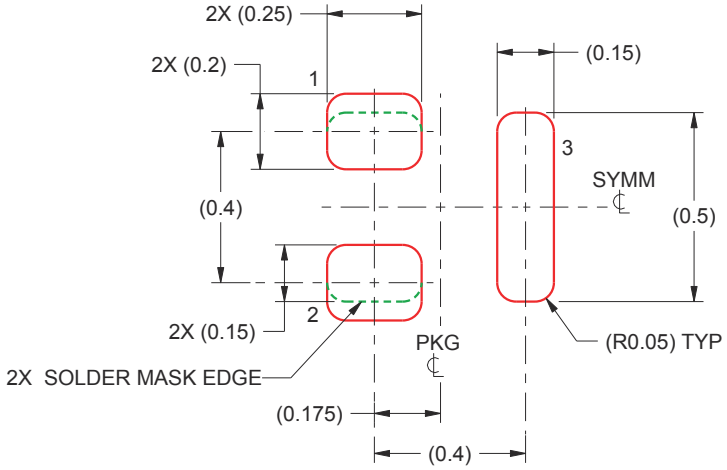
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7.2 Recommended Minimum PCB Layout



A. All dimensions are in millimeters.
B. For more information, see *FemtoFET Surface Mount Guide* (SLRA003D).

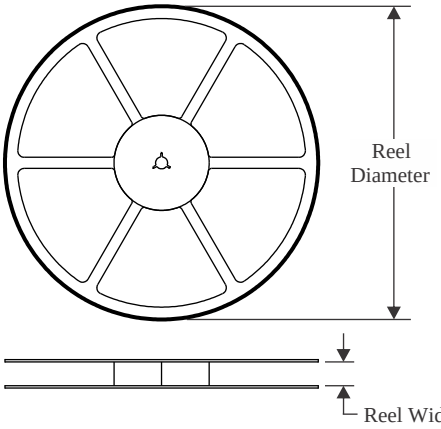
7.3 Recommended Stencil Pattern



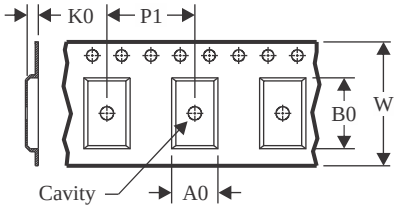
A. All dimensions are in millimeters.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

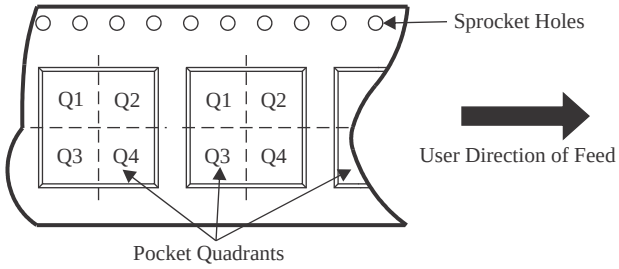


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

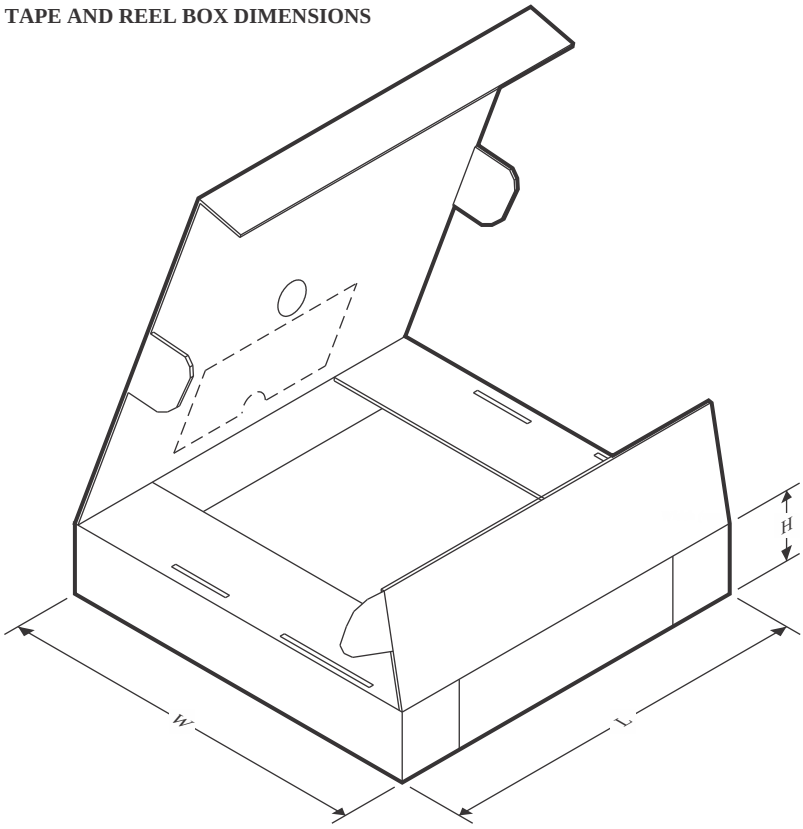
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25480F3	PICOSTAR	YJM	3	3000	180.0	8.4	1.94	0.79	0.44	4.0	8.0	Q2
CSD25480F3T	PICOSTAR	YJM	3	250	180.0	8.4	1.94	0.79	0.44	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

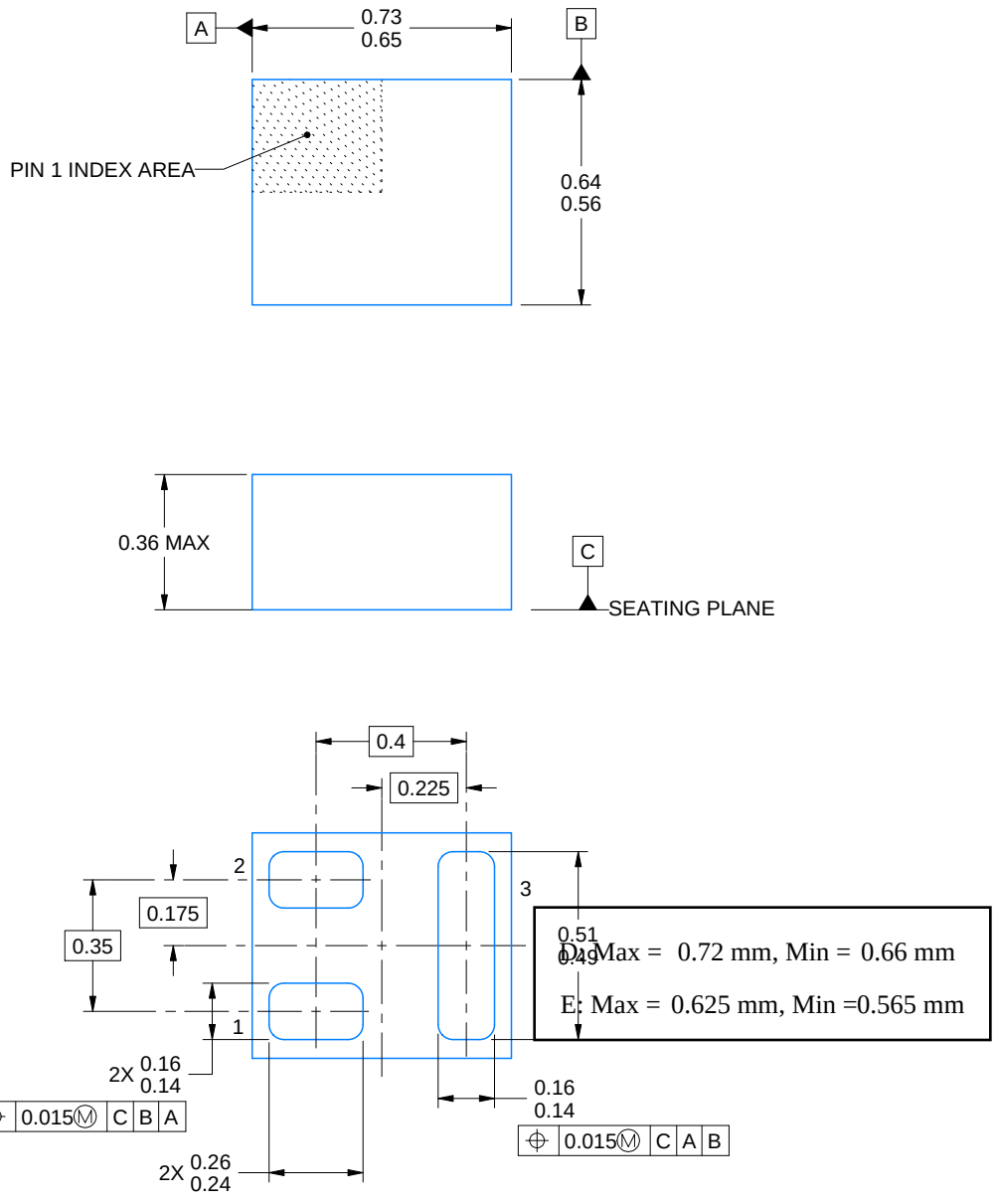
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25480F3	PICOSTAR	YJM	3	3000	182.0	182.0	20.0
CSD25480F3T	PICOSTAR	YJM	3	250	182.0	182.0	20.0

PACKAGE OUTLINE

YJM0003A

PicoStar™ - 0.36 mm max height

PicoStar™

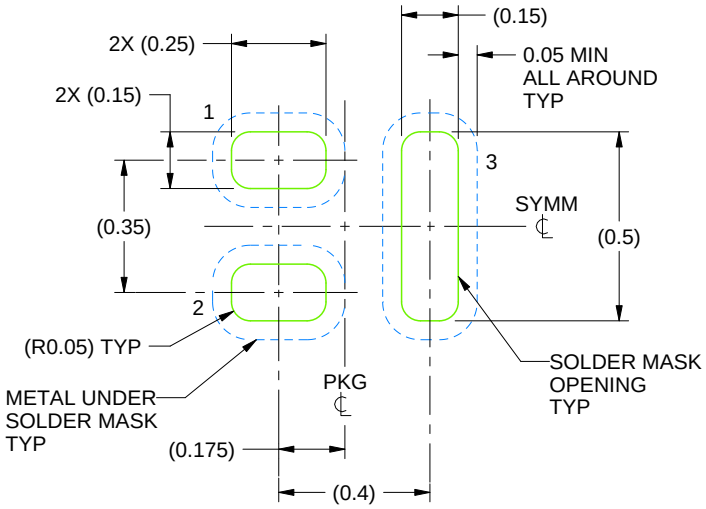


4222304/B 03/2022

PicoStar is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.
3. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.

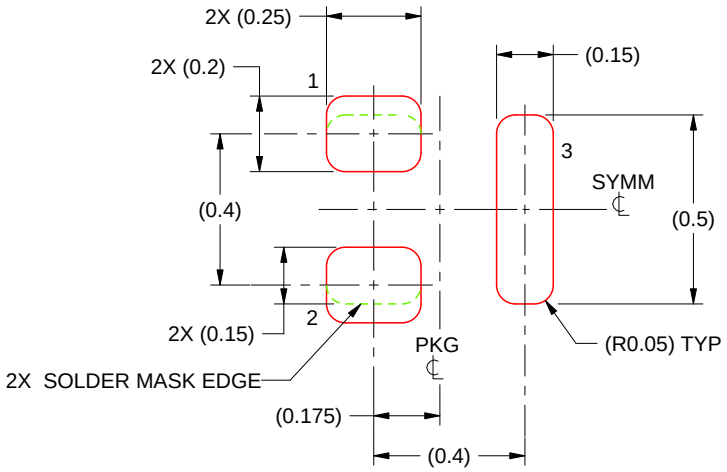


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

4222304/B 03/2022

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:50X

4222304/B 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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