CSD17556Q5B 30-V N-Channel NexFET™ Power MOSFET

1 Features

- Extremely Low Resistance
- Ultra-Low Q_g and Q_{gd}
- Low-Thermal Resistance
- Avalanche Rated
- Lead-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

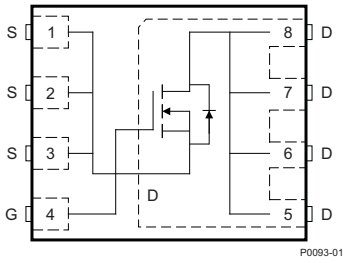
2 Applications

- Point of Load Synchronous Buck in Networking, Telecom, and Computing Systems
- Synchronous Rectification
- Active ORing and Hotswap Applications

3 Description

This 30-V, 1.2-mΩ, 5-mm × 6-mm NexFET™ power MOSFET is designed to minimize losses in synchronous rectification and other power conversion applications.

Top View



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	30		V
Q_g	Gate Charge Total (4.5 V)	30		nC
Q_{gd}	Gate Charge Gate-to-Drain	7.5		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V	1.5	mΩ
		V_{GS} = 10 V	1.2	
$V_{GS(th)}$	Threshold Voltage	1.4		V

Device Information(1)

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD17556Q5B	2500	13-Inch Reel	SON 5.00-mm × 6.00-mm Plastic Package	Tape and Reel
CSD17556Q5BT	250			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

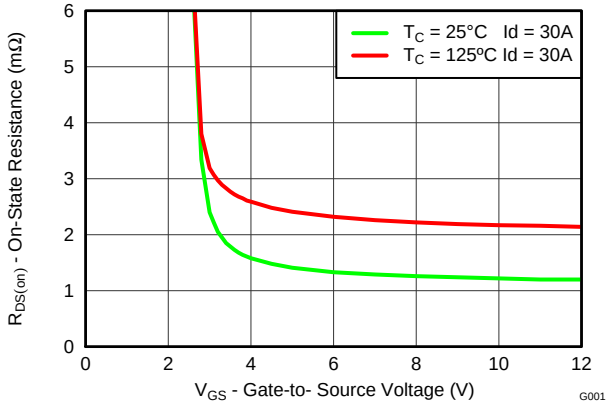
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package Limited)	100	A
	Continuous Drain Current (Silicon Limited), T_C = 25°C	215	
	Continuous Drain Current(1)	34	
I_{DM}	Pulsed Drain Current, T_A = 25°C(1)(2)	400	A
P_D	Power Dissipation(1)	3.1	W
	Power Dissipation, T_C = 25°C	191	
T_J, T_{stg}	Operating Junction, Storage Temperature	–55 to 150	°C
E_{AS}	Avalanche Energy, Single Pulse I_D = 100 A, L = 0.1 mH, R_G = 25 Ω	500	mJ

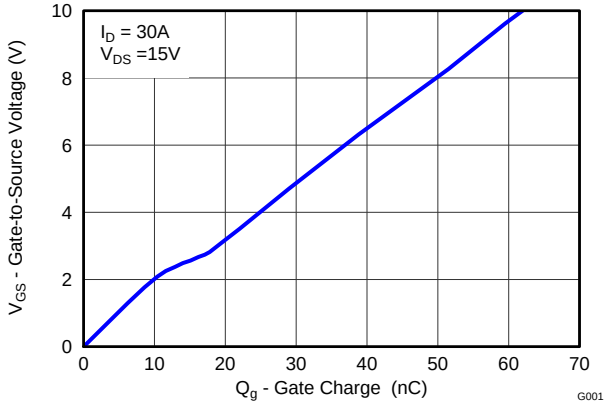
(1) Typical $R_{\theta JA}$ = 40°C/W on 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Max $R_{\theta JC}$ = 1.3°C/W, pulse duration ≤ 100 µs, duty cycle ≤ 1%.

$R_{DS(on)}$ vs V_{GS}



Gate Charge



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Specifications ... 3
5.1 Electrical Characteristics ... 3
5.2 Thermal Information ... 3
5.3 Typical MOSFET Characteristics ... 4
6 Device and Documentation Support ... 7
6.1 Receiving Notification of Documentation Updates ... 7
6.2 Community Resources ... 7
6.3 Trademarks ... 7
6.4 Electrostatic Discharge Caution ... 7
6.5 Glossary ... 7
7 Mechanical, Packaging, and Orderable Information ... 8
7.1 Q5B Package Dimensions ... 8
7.2 Recommended PCB Pattern ... 9
7.3 Recommended Stencil Pattern ... 9
7.4 Q5B Tape and Reel Information ... 10

4 Revision History

Changes from Revision C (January 2017) to Revision D — **Page**

- Corrected front page formatting error ... 1

Changes from Revision B (August 2014) to Revision C — **Page**

- Changed part numbers in the *Device Information* table ... 1
- Added *Receiving Notification of Documentation Updates* section and *Community Resources* section to the *Device and Documentation Support* section ... 7

Changes from Revision A (October 2013) to Revision B — **Page**

- Increased max pulsed drain current to 400 A. ... 1
- Updated pulsed drain current conditions ... 1
- Updated Figure 1 to a normalized $R_{\theta JC}$ curve ... 4
- Updated the SOA in Figure 10 ... 6
- Updated the mechanical drawing and dimensions table to show previously unknown dimensions ... 8

Changes from Original (March 2013) to Revision A — **Page**

- Updated the dimensions table in the Mechanical Data Section to include DIM "H" values ... 8

Copyright © 2013–2017, Texas Instruments Incorporated

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = 250 µA	30			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 24 V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 250 µA	1.15	1.4	1.65	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 4.5 V, I_{DS} = 40 A		1.5	1.8	mΩ
		V_{GS} = 10 V, I_{DS} = 40 A		1.2	1.4	
g_{fs}	Transconductance	V_{DS} = 15 V, I_{DS} = 40 A		197		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		5400	7020	pF
C_{oss}	Output capacitance			1770	2310	pF
C_{rss}	Reverse transfer capacitance			68	88	pF
R_G	Series gate resistance			0.7	1.4	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 15 V, I_{DS} = 40 A		30	39	nC
Q_{gd}	Gate charge gate-to-drain			7.5		nC
Q_{gs}	Gate charge gate-to-source			11		nC
$Q_{g(th)}$	Gate charge at V_{th}			6.1		nC
Q_{oss}	Output charge	V_{DS} = 15 V, V_{GS} = 0 V		48		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 15 V, V_{GS} = 4.5 V, I_{DS} = 40 A, R_G = 2 Ω		14		ns
t_r	Rise time			26		ns
$t_{d(off)}$	Turnoff delay time			27		ns
t_f	Fall time			12		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 40 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse recovery charge	V_{DD}= 15 V, I_F = 40 A, di/dt = 300 A/µs		68		nC
t_{rr}	Reverse recovery time			36		ns

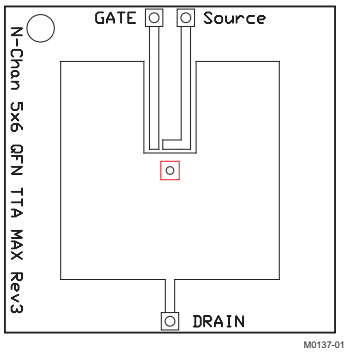
5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

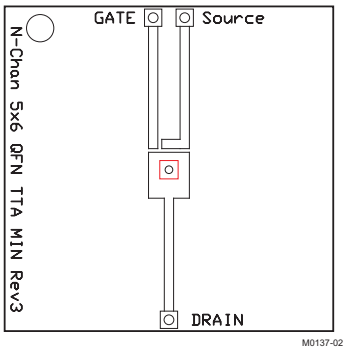
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance (1)			1.3	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1) (2)			50	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.

Copyright © 2013–2017, Texas Instruments Incorporated



Max $R_{\theta JA}$ = 50°C/W when mounted on 1-in^2 (6.45-cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2-oz (0.071-mm) thick Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

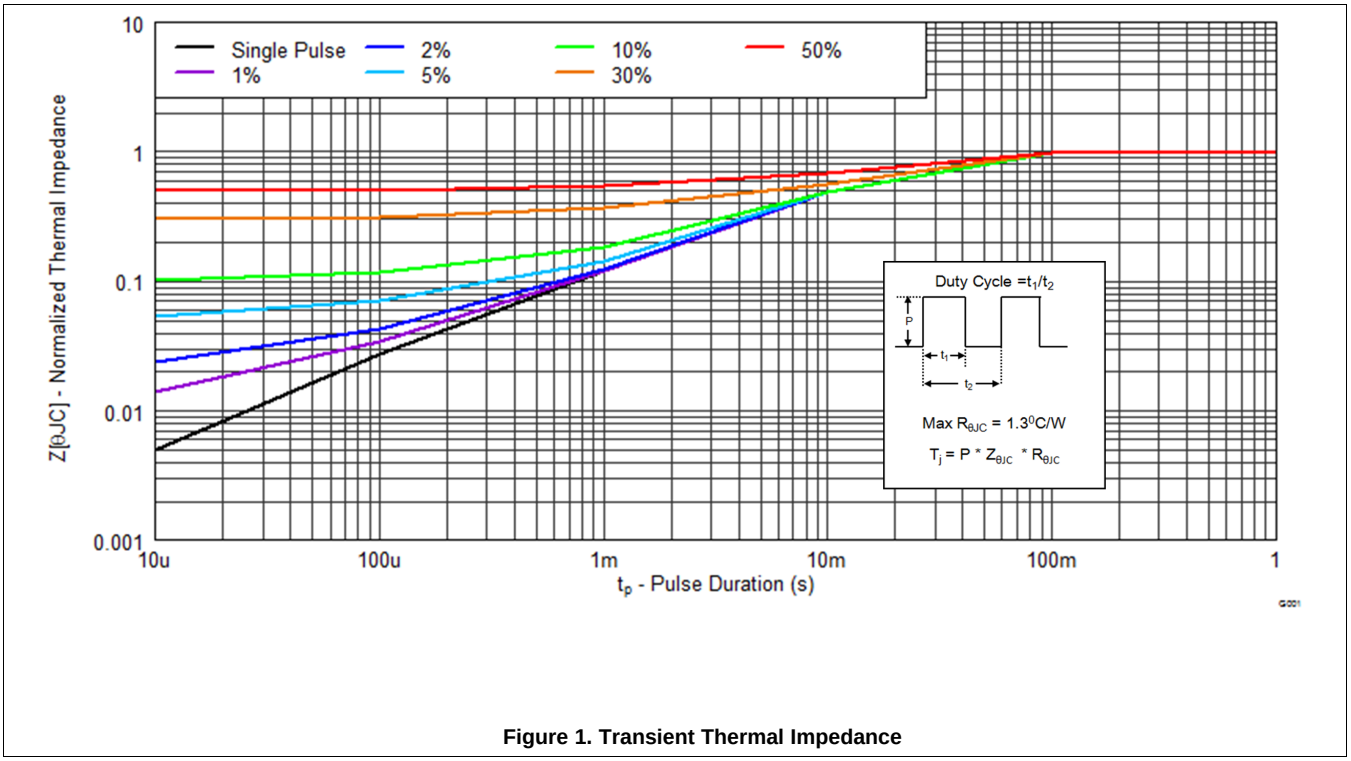


Figure 1. Transient Thermal Impedance

Copyright © 2013–2017, Texas Instruments Incorporated

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

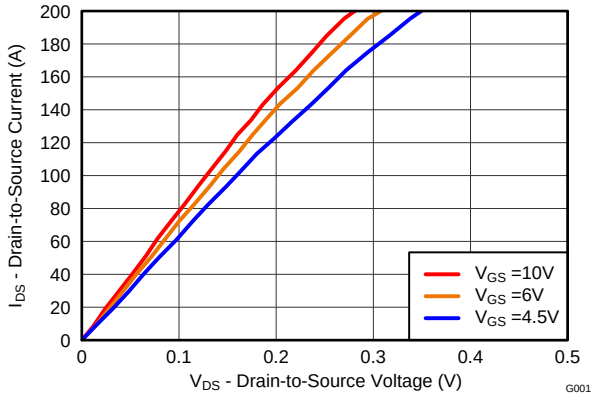


Figure 2. Saturation Characteristics

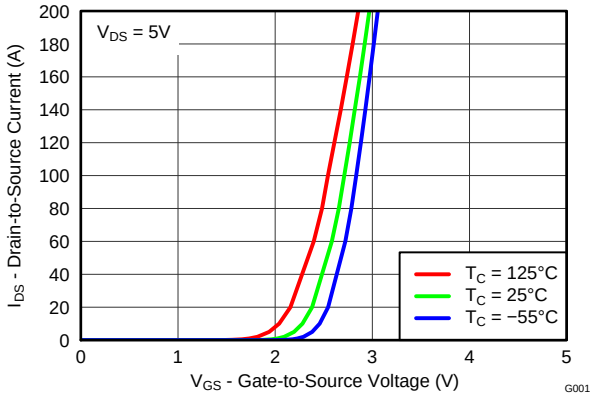


Figure 3. Transfer Characteristics

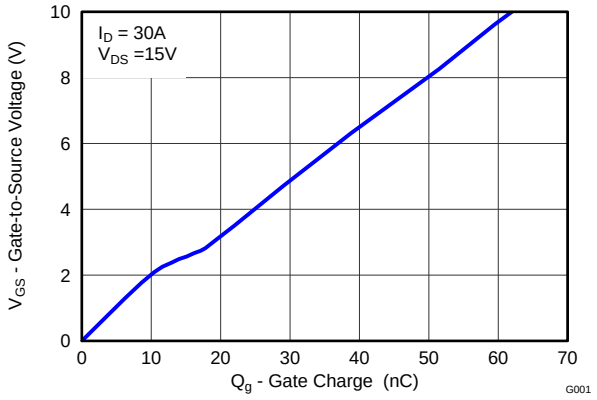


Figure 4. Gate Charge

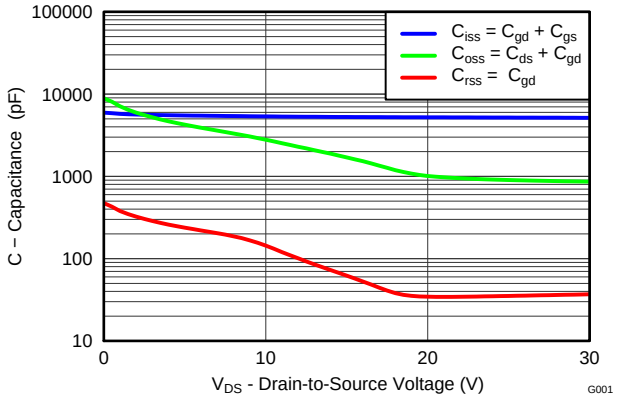


Figure 5. Capacitance

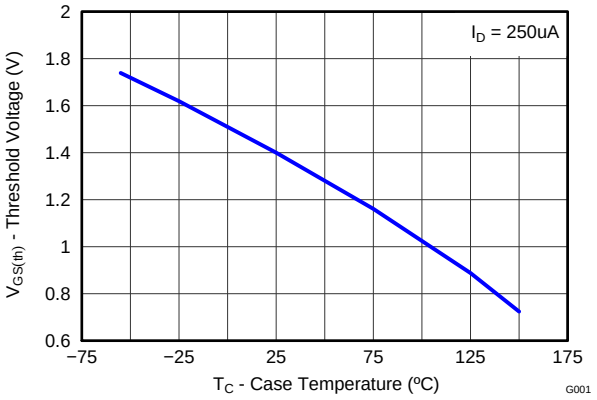


Figure 6. Threshold Voltage vs Temperature

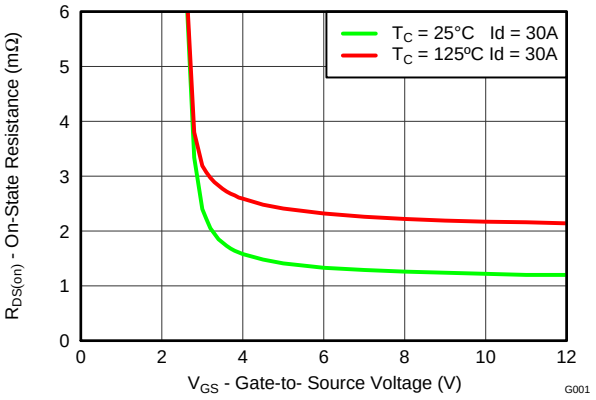


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Copyright © 2013–2017, Texas Instruments Incorporated

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

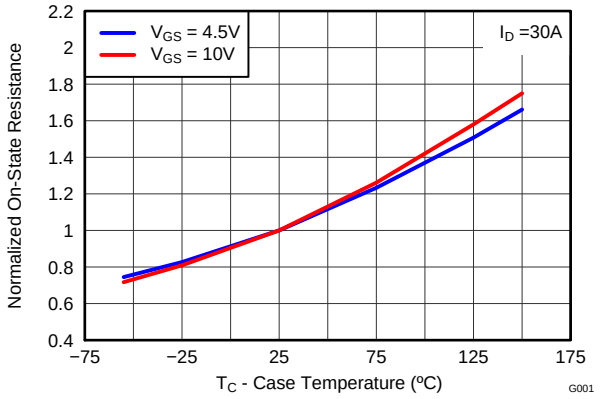


Figure 8. Normalized On-State Resistance vs Temperature

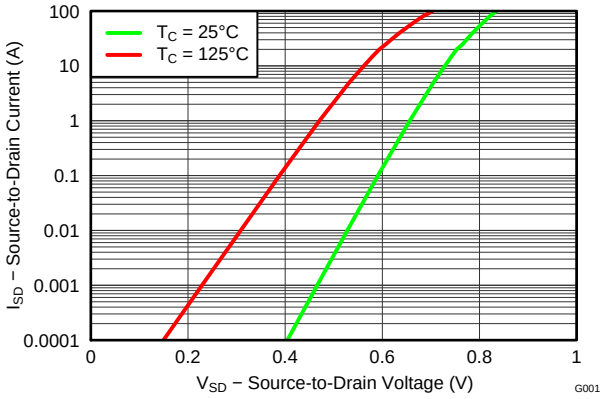


Figure 9. Typical Diode Forward Voltage

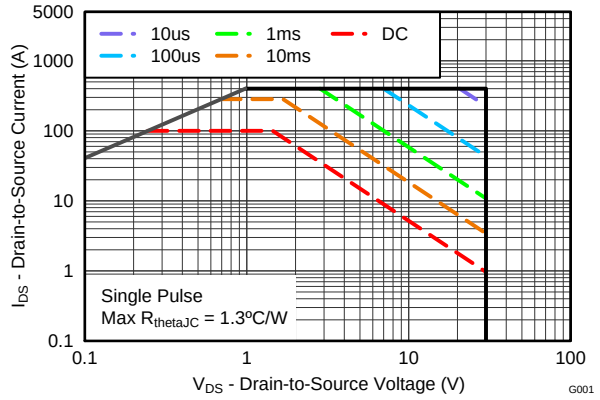


Figure 10. Maximum Safe Operating Area (SOA)

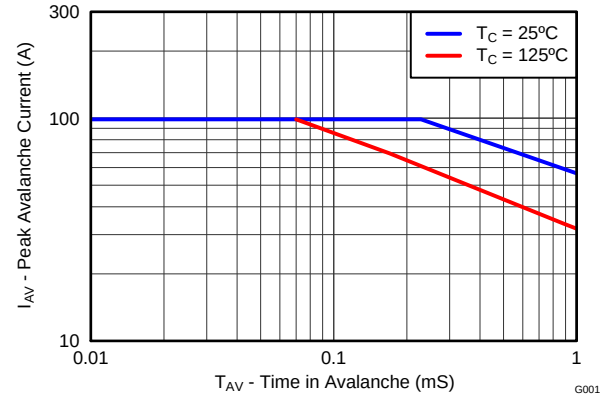


Figure 11. Single Pulse Unclamped Inductive Switching

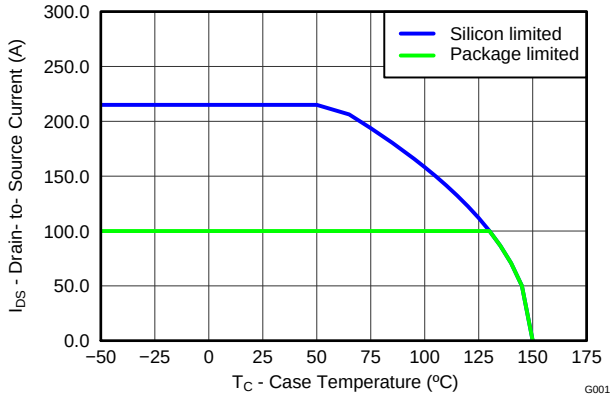


Figure 12. Maximum Drain Current vs Temperature

Copyright © 2013–2017, Texas Instruments Incorporated

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

SLYZ022 — *TI Glossary*.

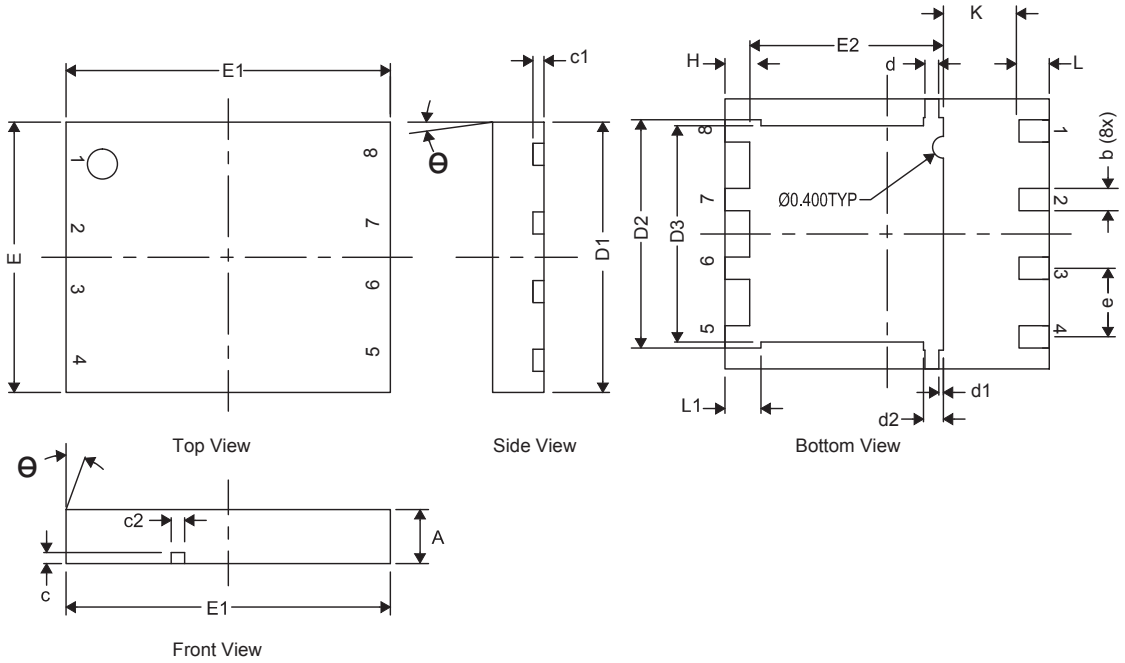
This glossary lists and explains terms, acronyms, and definitions.

Copyright © 2013–2017, Texas Instruments Incorporated

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

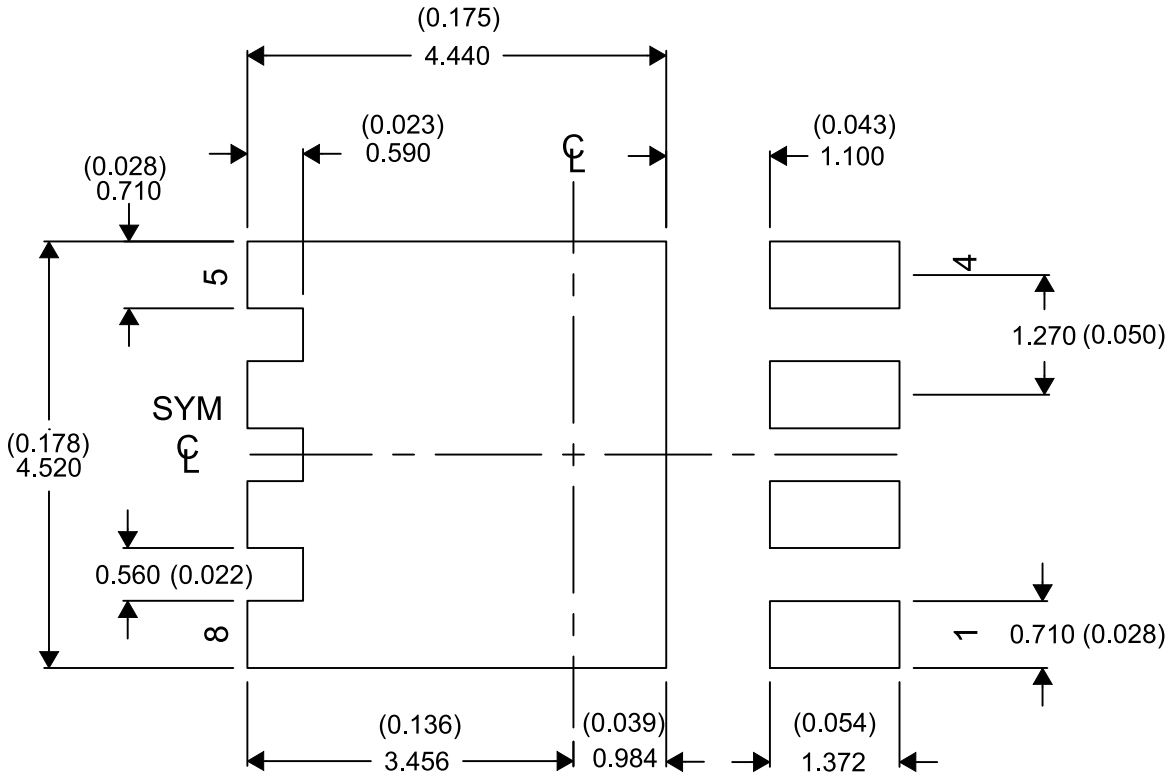
7.1 Q5B Package Dimensions



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	1.00	1.05
b	0.36	0.41	0.46
c	0.15	0.20	0.25
c1	0.15	0.20	0.25
c2	0.20	0.25	0.30
D1	4.90	5.00	5.10
D2	4.12	4.22	4.32
D3	3.90	4.00	4.10
d	0.20	0.25	0.30
d1	0.085 TYP		
d2	0.319	0.369	0.419
E	4.90	5.00	5.10
E1	5.90	6.00	6.10
E2	3.48	3.58	3.68
e	1.27 TYP		
H	0.36	0.46	0.56
L	0.46	0.56	0.66
L1	0.57	0.67	0.77
θ	0°	—	—
K	1.40 TYP		

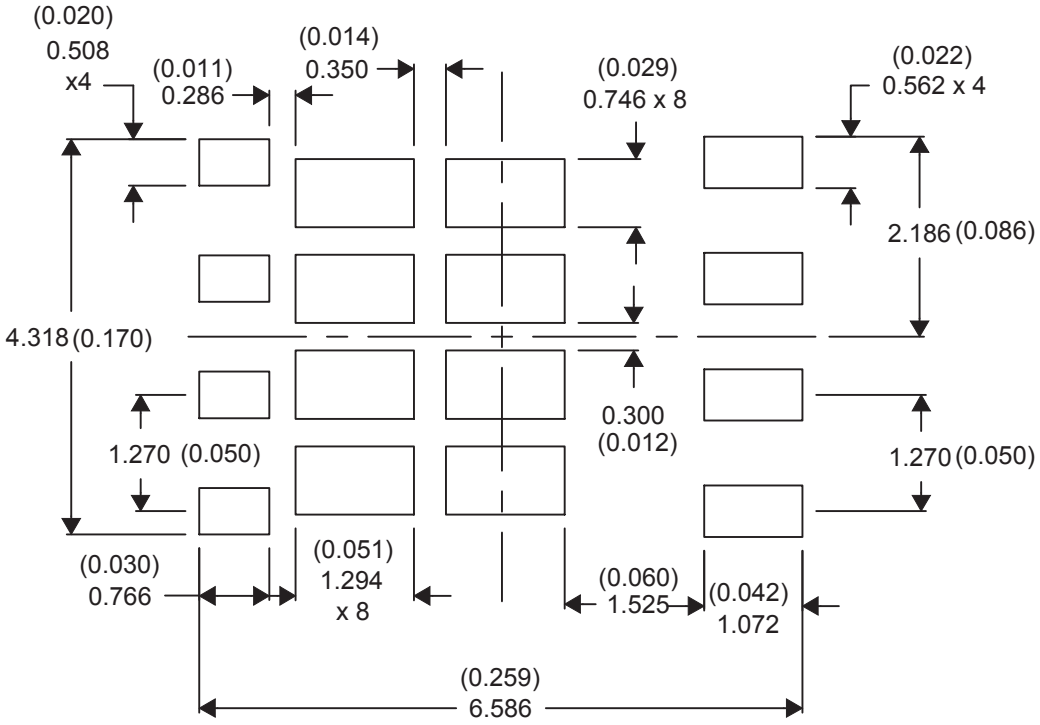
Copyright © 2013–2017, Texas Instruments Incorporated

7.2 Recommended PCB Pattern

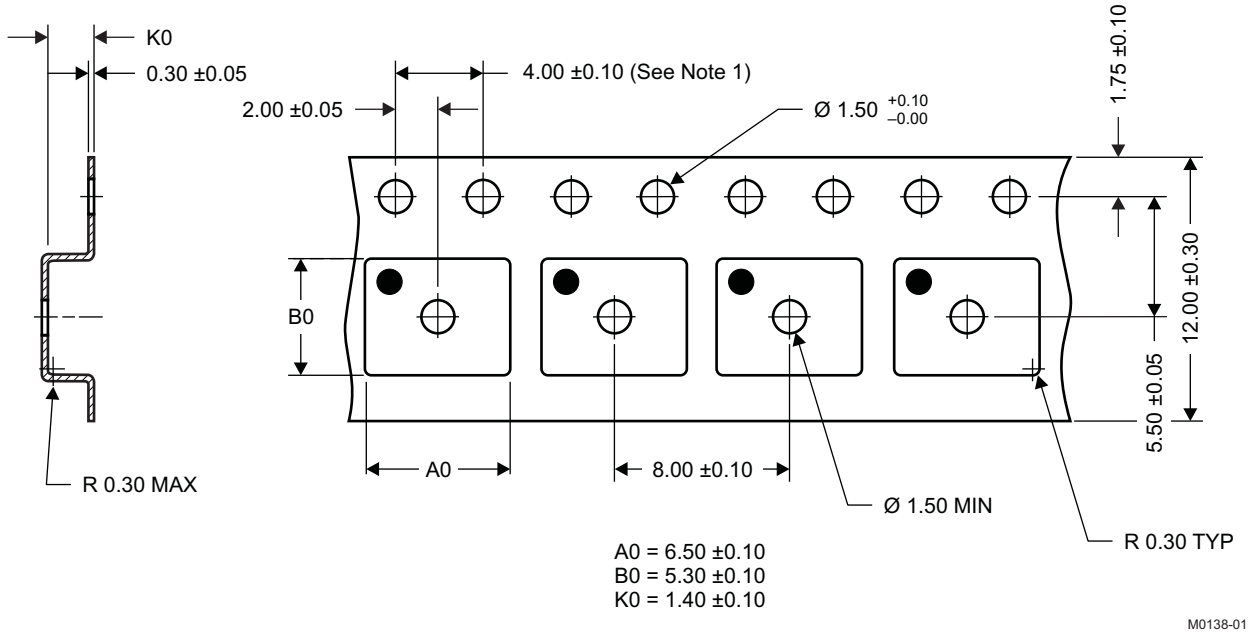


For recommended circuit layout for PCB designs, see *Reducing Ringing Through PCB Layout Techniques* (SLPA005).

7.3 Recommended Stencil Pattern



7.4 Q5B Tape and Reel Information



Notes:

1. 10-sprocket hole-pitch cumulative tolerance ±0.2.
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm.
3. Material: black static-dissipative polystyrene.
4. All dimensions are in mm (unless otherwise specified).
5. A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket.

Copyright © 2013–2017, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17556Q5B	ACTIVE	VSON-CLIP	DNK	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-55 to 150	CSD17556	Samples
CSD17556Q5BT	ACTIVE	VSON-CLIP	DNK	8	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-55 to 150	CSD17556	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated