CSD17313Q2 30-V N-Channel NexFET™ Power MOSFET

1 Features

- Optimized for 5-V Gate Drive
- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Pb-Free
- RoHS Compliant
- Halogen-Free
- SON 2-mm × 2-mm Plastic Package

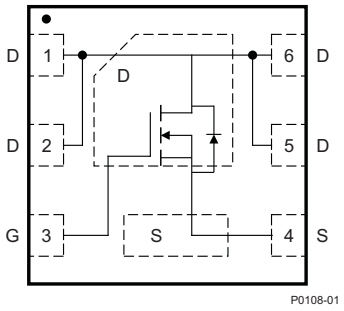
2 Applications

- DC-DC Converters
- Battery and Load Management Applications

3 Description

This 30-V, 24-mΩ, 2-mm x 2-mm SON NexFET™ power MOSFET is designed to minimize losses in power conversion applications and optimized for 5-V gate drive applications. The 2-mm × 2-mm SON offers excellent thermal performance for the size of the package.

Top View



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Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	30		V
Q_g	Gate Charge Total (4.5 V)	2.1		nC
Q_{gd}	Gate Charge Gate-to-Drain	0.4		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 3 V	31	mΩ
		V_{GS} = 4.5 V	26	mΩ
		V_{GS} = 8 V	24	mΩ
$V_{GS(th)}$	Threshold Voltage	1.3		V

Ordering Information(1)

PART NUMBER	QTY	MEDIA	PACKAGE	SHIP
CSD17313Q2	3000	13-Inch Reel	SON 2-mm × 2-mm Plastic Package	Tape and Reel
CSD17313Q2T	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

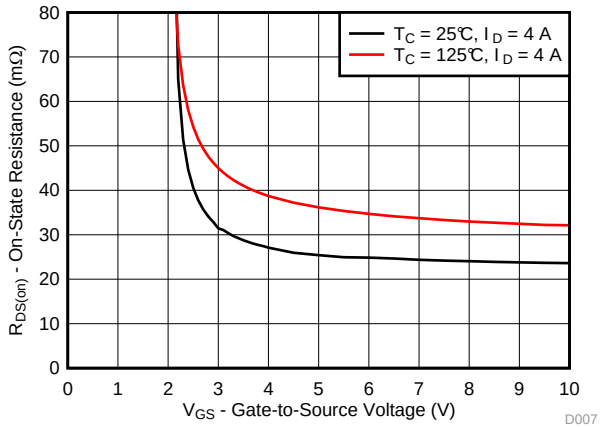
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	+10 / –8	V
I_D	Continuous Drain Current (package limited)	5	A
	Continuous Drain Current (silicon limited), T_C = 25°C	19	
	Continuous Drain Current(1)	7.3	
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	57	A
P_D	Power Dissipation(1)	2.4	W
	Power Dissipation, T_C = 25°C	17	
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, Single Pulse, I_D = 19A, L = 0.1mH, R_G = 25Ω	18	mJ

(1) Typical $R_{\theta JA}$ = 53°C/W on a 1-inch², 2-oz. Cu pad on a 0.06-inch thick FR4 PCB.

(2) Max $R_{\theta JC}$ = 7.4°C/W, pulse duration ≤100 µs, duty cycle ≤1%.

On State Resistance vs Gate to Source Voltage



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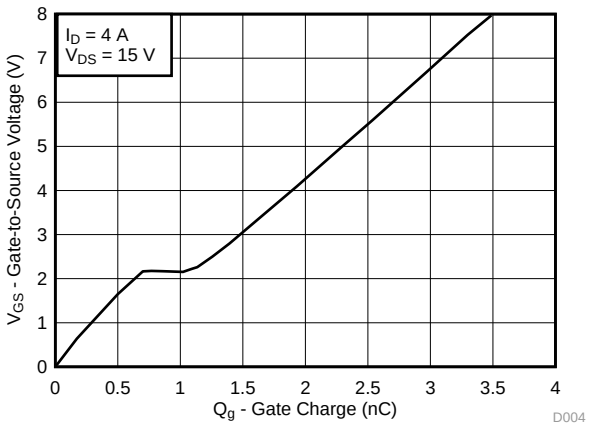
Gate Charge



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An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2013) to Revision E — **Page**

- Added part number to title ... 1
- Enhanced description ... 1
- Added 7-inch reel to *Ordering Information* table ... 1
- Updated Continuous Drain Current ... 1
- Updated pulsed current conditions ... 1
- Updated Figure 1 to show $R_{\theta JC}$ curves ... 4
- Added V_{GS} = 4.5 V line in Figure 8 ... 6
- Updated the SOA in Figure 10 ... 6
- Added *Community Resources* ... 7
- Added *Device and Documentation* section. ... 10

Changes from Revision C (January 2013) to Revision D — **Page**

- Changed Figure 10, Maximum Safe Operating Area ... 6

Changes from Revision B (October 2010) to Revision C — **Page**

- Changed the Recommended PCB Pattern ... 9
- Added the Recommended Stencil Pattern ... 9

Changes from Revision A (March 2010) to Revision B — **Page**

- Deleted the Package Marking Information section ... 10

Changes from Original (March 2010) to Revision A — **Page**

- Changed Q_{rr} - Reverse Recovery Charge From: 10.2 nC To: 6.4 nC ... 3

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5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Drain-to-source leakage	V_{GS} = 0 V, V_{DS} = 24 V			1	µA
I_{GSS}	Gate-to-source leakage	V_{DS} = 0 V, V_{GS} = +10 / –8 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.9	1.3	1.8	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 3 V, I_D = 4 A		31	42	mΩ
		V_{GS} = 4.5 V, I_D = 4 A		26	32	mΩ
		V_{GS} = 8 V, I_D = 4 A		24	30	mΩ
g_{fs}	Transconductance	V_{DS} = 15 V, I_D = 4 A		16		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		260	340	pF
C_{oss}	Output capacitance			140	180	pF
C_{rss}	Reverse transfer capacitance			13	17	pF
R_G	Series gate resistance			1.3	2.6	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 15 V, I_D = 4 A		2.1	2.7	nC
Q_{gd}	Gate charge – gate-to-drain			0.4		nC
Q_{gs}	Gate charge – gate-to-source			0.7		nC
$Q_{g(th)}$	Gate charge at Vth			0.3		nC
Q_{oss}	Output charge	V_{DS} = 13.5 V, V_{GS} = 0 V		3.8		nC
$t_{d(on)}$	Turn on delay time	V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 4 A, R_G = 2 Ω		2.8		ns
t_r	Rise time			3.9		ns
$t_{d(off)}$	Turn off delay time			4.2		ns
t_f	Fall time			1.3		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 4 A, V_{GS} = 0 V		0.85	1	V
Q_{rr}	Reverse recovery charge	V_{DD}= 13.5 V, I_F = 4 A, di/dt = 300 A/µs		6.4		nC
t_{rr}	Reverse recovery time			12.9		ns

5.2 Thermal Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal resistance junction-to-case(1)			7.4	°C/W
$R_{\theta JA}$	Thermal resistance junction-to-ambient(1)(2)			67	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inch × 1.5 inch (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu.

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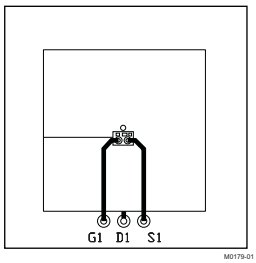
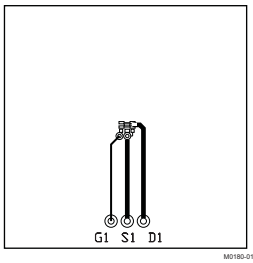


Max $R_{\theta JA}$ = 67°C/W when mounted on 1-inch^2 (6.45-cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 228°C/W when mounted on a minimum pad area of 2-oz. (0.071-mm thick) Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise noted)

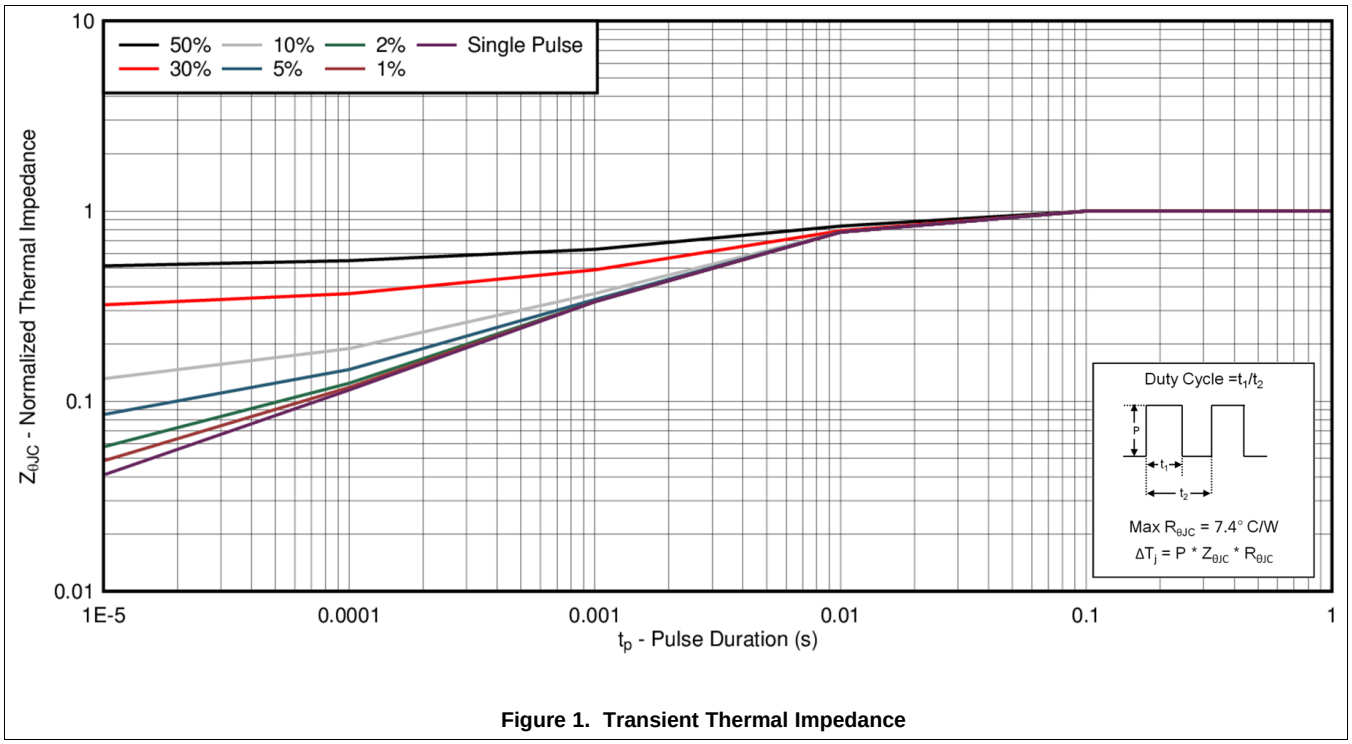


Figure 1. Transient Thermal Impedance

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Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise noted)

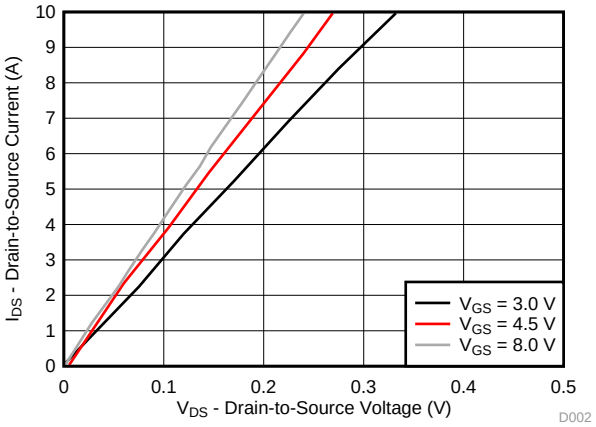

Figure 2. Saturation Characteristics

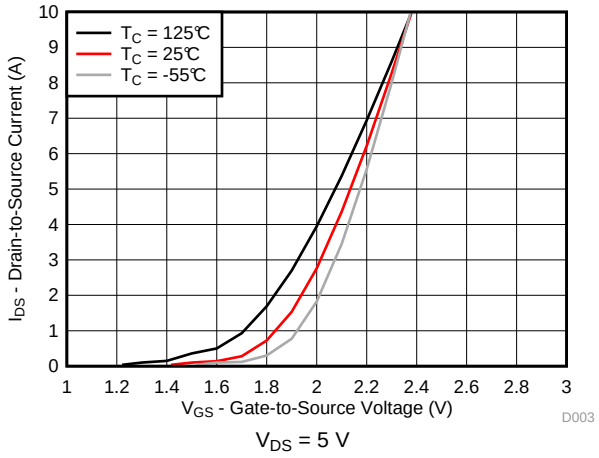

Figure 3. Transfer Characteristics

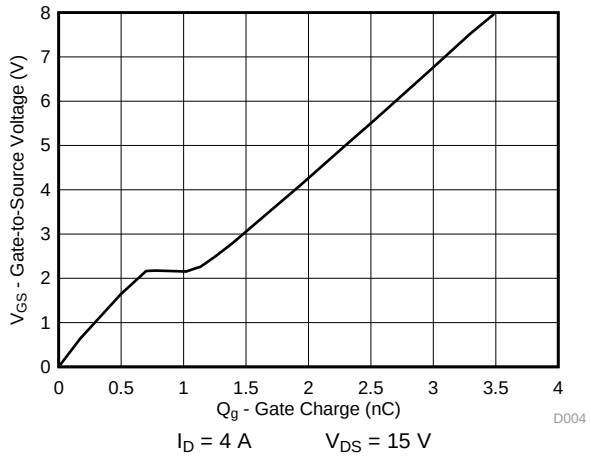

Figure 4. Gate Charge

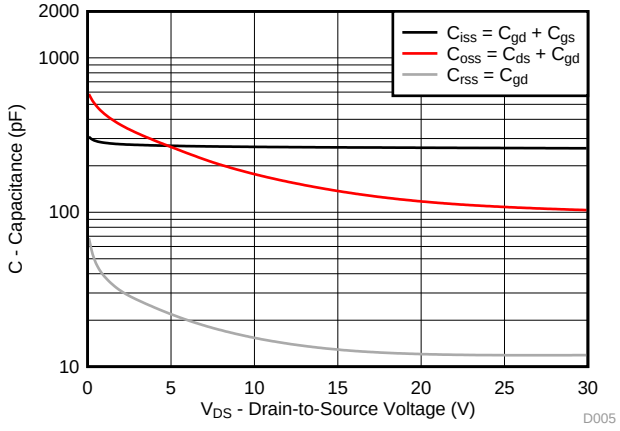

Figure 5. Capacitance

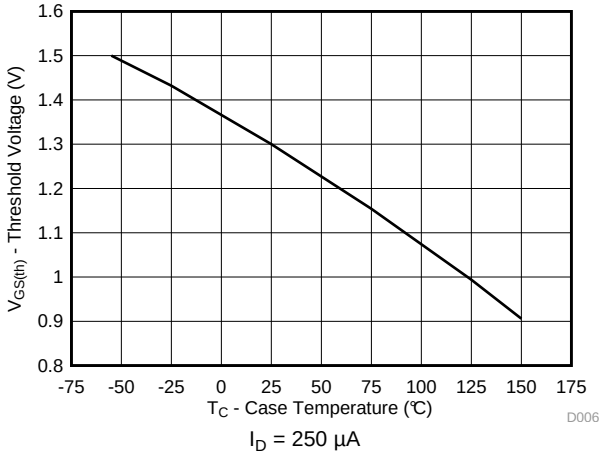

Figure 6. Threshold Voltage vs Temperature

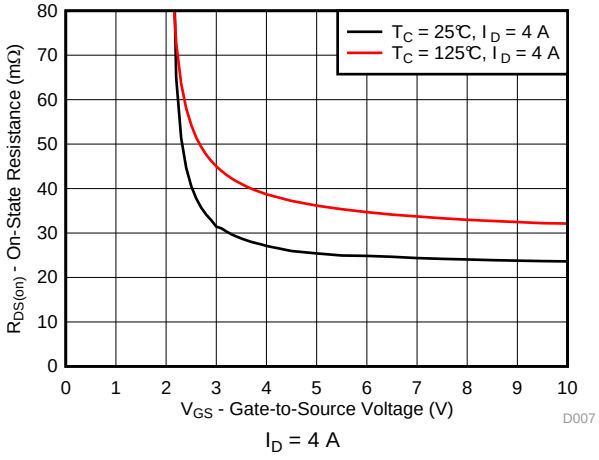

Figure 7. On-State Resistance vs Gate-to-Source Voltage

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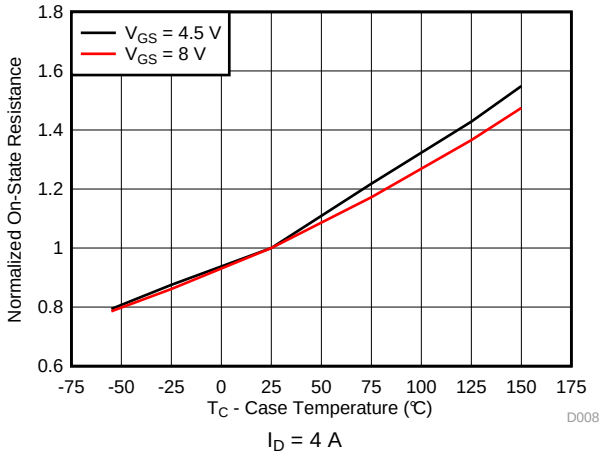
Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise noted)



I_D = 4 A

Figure 8. Normalized On-State Resistance vs Temperature

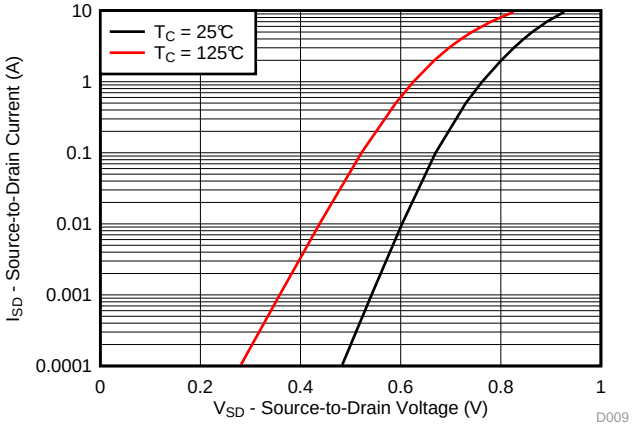
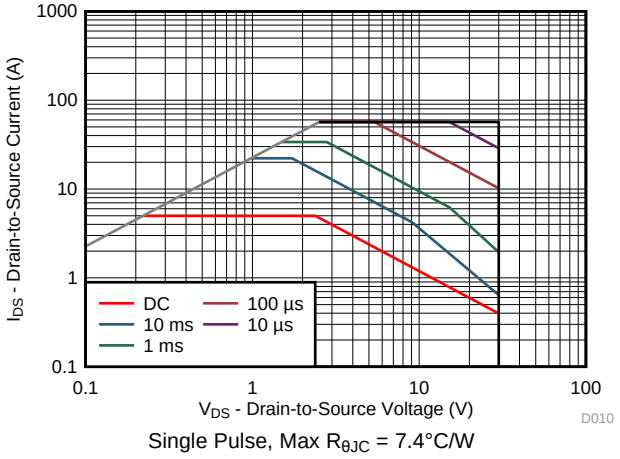


Figure 9. Typical Diode Forward Voltage



Single Pulse, Max $R_{\theta JC}$ = 7.4°C/W

Figure 10. Maximum Safe Operating Area

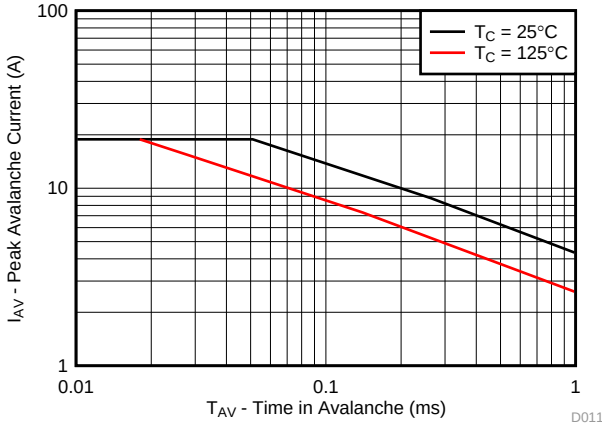


Figure 11. Single Pulse Unclamped Inductive Switching

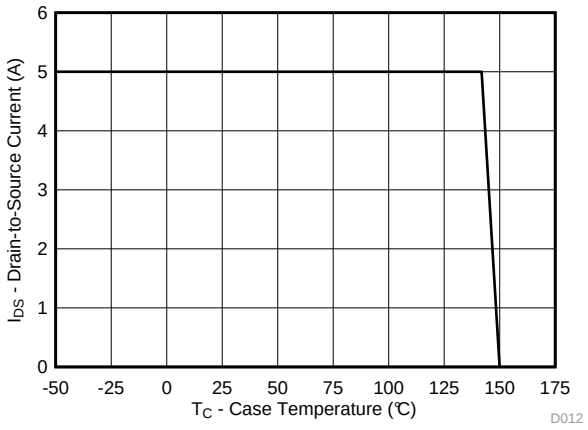


Figure 12. Maximum Drain Current vs Temperature

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6 Device and Documentation Support

6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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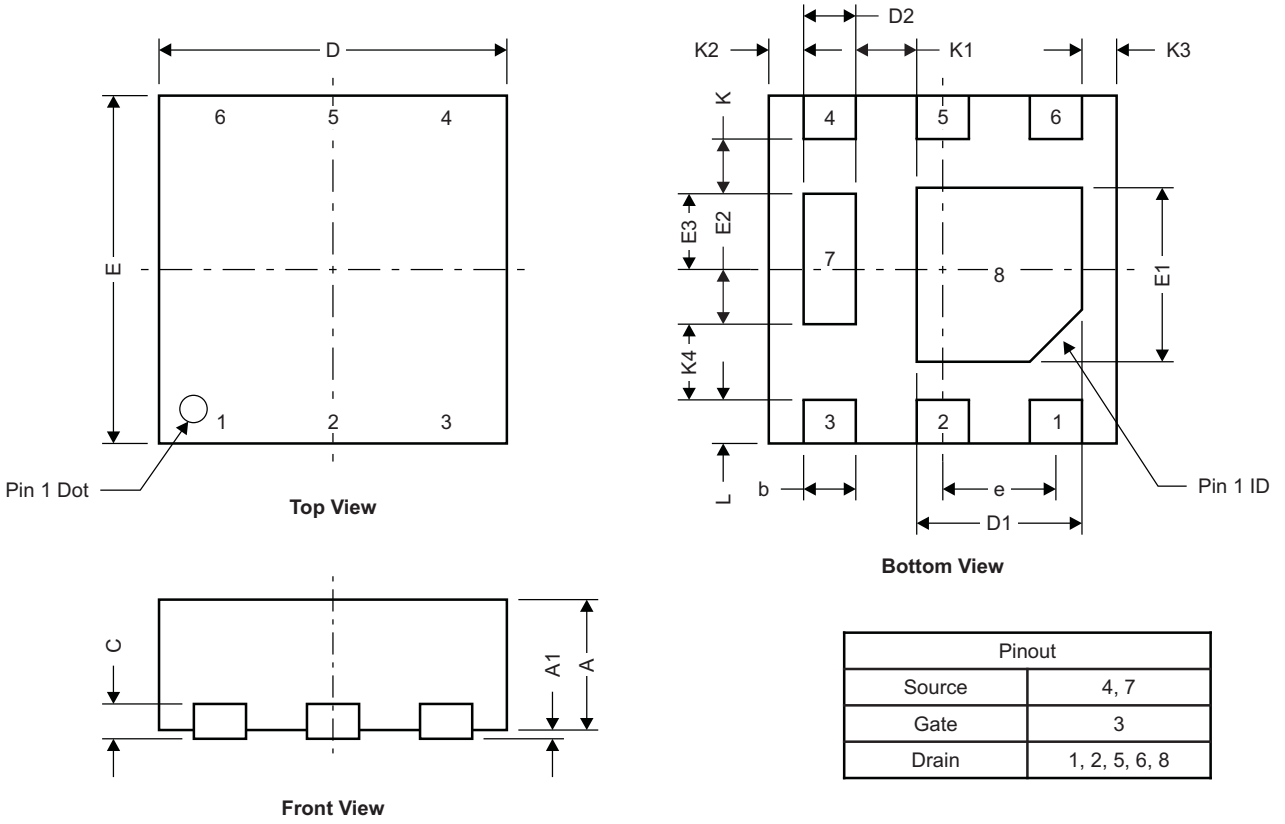
7 Mechanical, Packaging, and Orderable Information

7.1 Q2 Package Dimensions



Pinout	
Source	4, 7
Gate	3
Drain	1, 2, 5, 6, 8

M0175-02

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.032
A1	0.000		0.050	0.000		0.002
b	0.250	0.300	0.350	0.010	0.012	0.014
C		0.203 TYP			0.008 TYP	
D		2.000 TYP			0.080 TYP	
D1	0.900	0.950	1.000	0.036	0.038	0.040
D2		0.300 TYP			0.012 TYP	
E		2.000 TYP			0.080 TYP	
E1	0.900	1.000	1.100	0.036	0.040	0.044
E2		0.280 TYP			0.0112 TYP	
E3		0.470 TYP			0.0188 TYP	
e		0.650 BSC			0.026 TYP	
K		0.280 TYP			0.0112 TYP	
K1		0.350 TYP			0.014 TYP	
K2		0.200 TYP			0.008 TYP	
K3		0.200 TYP			0.008 TYP	
K4		0.470 TYP			0.0188 TYP	
L	0.200	0.25	0.300	0.008	0.010	0.012

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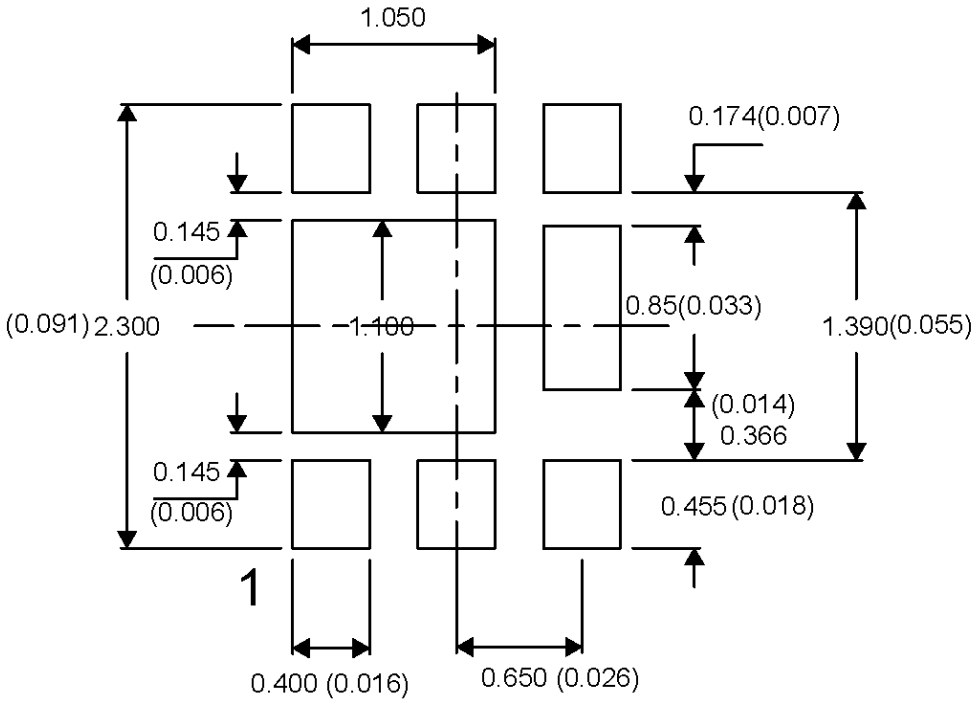
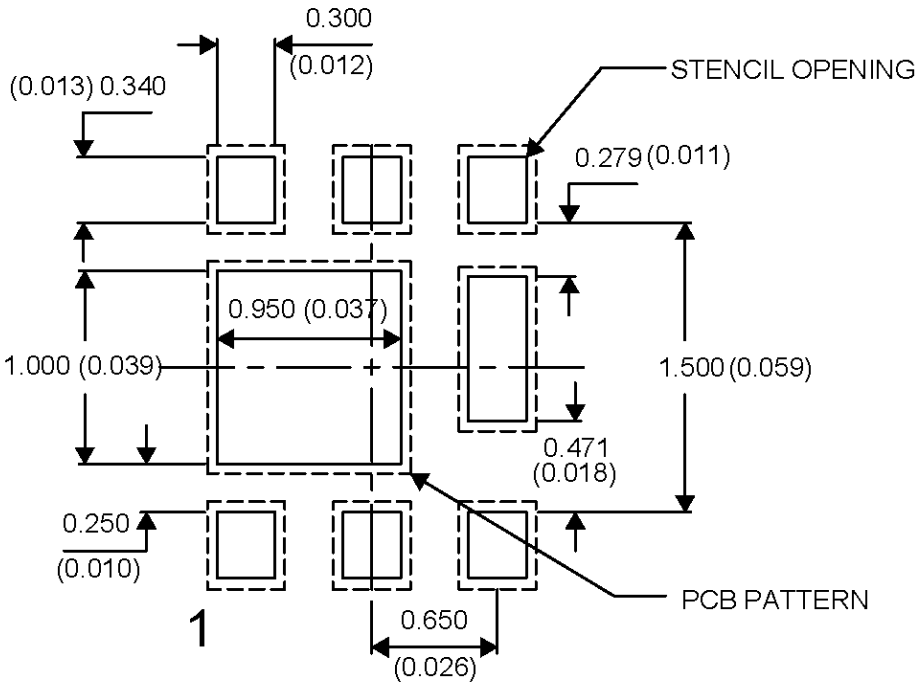
7.2 Recommended PCB Pattern



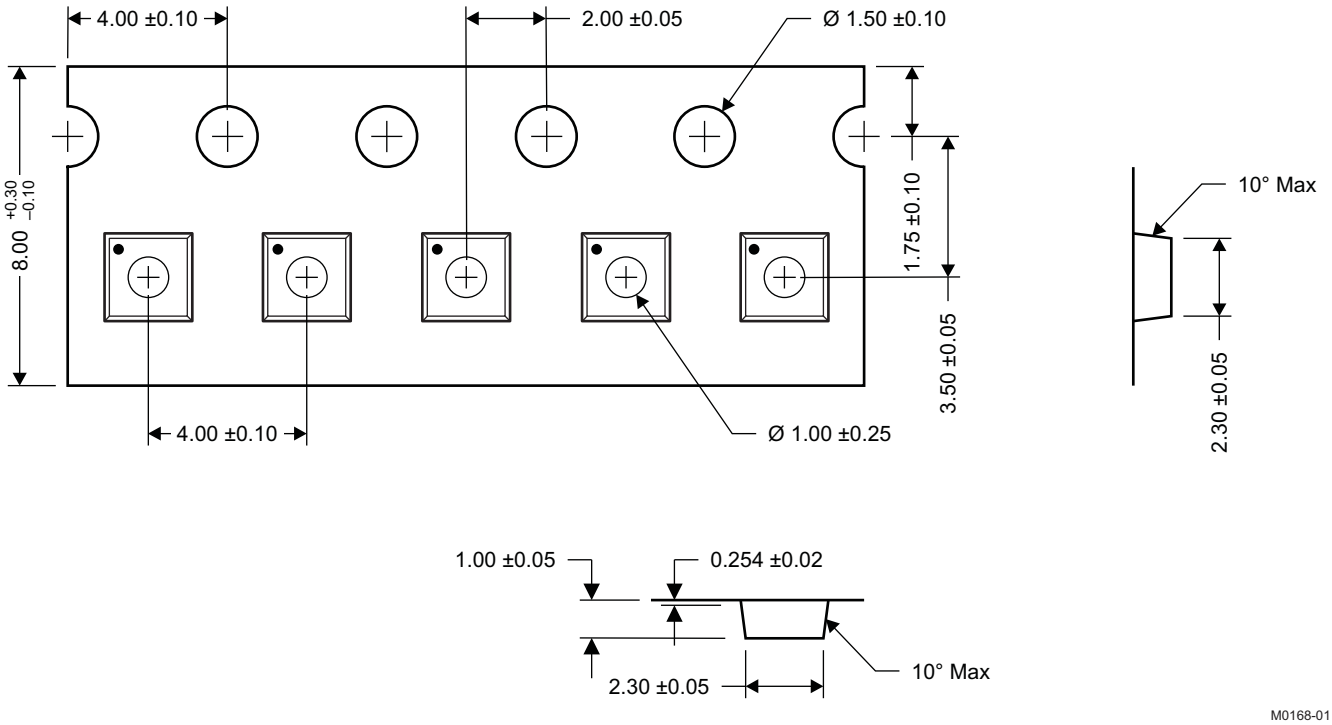
For recommended circuit layout for PCB designs, see application note SLPA005 – Reducing Ringing through PCB Layout Techniques.

7.3 Recommended Stencil Pattern



Note: All dimensions are in mm, unless otherwise specified.

7.4 Q2 Tape and Reel Information



Notes: 1. Measured from centerline of sprocket hole to centerline of pocket
2. Cumulative tolerance of 10 sprocket holes is ±0.20
3. Other material available
4. Typical SR of form tape Max 10^8 OHM/SQ
5. All dimensions are in mm, unless otherwise specified.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17313Q2	ACTIVE	WSON	DQK	6	3000	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 150	1733	Samples
CSD17313Q2T	ACTIVE	WSON	DQK	6	250	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 150	1733	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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