Crystal LAN™
CS8920
Ethernet Controller
Technical Reference
Manual

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A Cirrus Logic Company

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TABLE OF CONTENTS

CS8920 ETHERNET CONTROLLER TECHNICAL REFERENCE MANUAL 1

1.0 INTRODUCTION TO CS8920 TECHNICAL REFERENCE MANUAL 6

2.0 HARDWARE DESIGN 9

2.1 ETHERNET HARDWARE DESIGN FOR EMBEDDED SYSTEMS AND MOTHERBOARDS 9

2.1.1 General Description 9

2.1.2 Board Design Considerations 9

2.1.2.1 Crystal Oscillator 9

2.1.2.2 ISA Bus Interface 9

2.1.2.4 EEPROM 10

2.1.2.5 LEDs 10

2.1.2.7 10BASE-2 and AUI Interfaces 10

2.1.3 Logic Schematics 10

2.1.4 Component Placement and Signal Routing 10

2.2 LAYOUT CONSIDERATIONS FOR THE CS8920 20

2.2.1 General guidelines 20

2.2.2 Power supply connections 20

2.2.2.1 Two layered printed circuit board (PCB) 22

2.2.2.2 Multi-layered printed circuit board 22

2.2.3 Routing of the digital signals 32

2.2.4 Routing of the analog signals 32

2.2.4.1 Routing of the clock signals: 32

2.2.4.2 Biasing resistor at RES pin of the CS8920 32

2.2.4.3 Routing of the 10BASE-T signals 32

2.2.4.4 Routing of the AUI signals 32

2.3 RECOMMENDED MAGNETICS FOR THE CS8920 34

3.0 EEPROM-BASED CONFIGURATION 36

3.1 FORMAT OF CONFIGURATION DATA 36

3.2 RESET CONFIGURATION BLOCK 36

3.2.1 Reset Configuration Block Format 36

3.2.1.1 Reset Configuration Block Header....37
3.2.1.2 Configuration Data....37
3.2.1.3 Checksum....37
3.2.2 Typical Reset Blocks....38
3.2.2.1 Recommended Reset Configuration Block for a Legacy Adapter....38
3.2.2.2 Recommended Reset Configuration Block for a PnP Adapter....39
3.2.2.3 PnP with Automatic Wakeup Feature Enabled....39
3.2.2.4 BootPROM Considerations....40
3.2.2.5 Performance Considerations of Reset Configuration Block....40
3.3 FORMAT OF THE DRIVER CONFIGURATION BLOCK....40
3.3.1 IEEE Physical Address....43
3.3.2 ISA Configuration Flags....43
3.3.3 PacketPage Memory Base....43
3.3.4 Boot PROM Memory Base....44
3.3.5 Boot PROM Mask....44
3.3.6 Transmission Control....44
3.3.7 Adapter Configuration Word....44
3.3.8 Manufacturing Date....45
3.3.9 IEEE Physical Address (copy)....45
3.3.10 16-bit Checksum....46
3.3.11 EISA ID....46
3.3.12 Serial Number....46
3.3.13 LFSR Checksum....46
3.4 RECOMMENDED PLUG AND PLAY RESOURCE DATA....46
3.4.1 Serial Identifier....47
3.4.2 Resource Descriptors....47
3.5 PROGRAMMING AND INITIALIZING THE EEPROM....53
3.5.1 Maintaining EEPROM Configuration Data....53
3.6 OBTAINING IEEE ADDRESSES....54
4.0 CS8920 INSTALLATION AND CONFIGURATION....55
4.1 CS8920 EVALUATION KIT DEVICE DRIVERS AND SOFTWARE UTILITIES....55

4.1.1 Software Distribution 55
4.1.2 Crystal's Software Licensing Procedures 55
4.2 ADAPTER INSTALLATION AND CONFIGURATION 60
4.2.1 Installing the CS8920 Adapter 60
4.2.2 Configuring the CS8920 Adapter 60
4.2.2.1 EISA System Installation 61
4.2.3 Testing the CS8920 Adapter 61
4.2.3.1 Diagnostic Self-Test 62
4.2.3.2 Diagnostics Network Test 62
4.2.4 Installing Network Device Drivers 63
5.0 CONTACTING CUSTOMER SUPPORT AT CRYSTAL 64
5.1 CRYSTAL BBS 64
5.1.1 Connecting to the BBS 64
5.1.2 Guests 64
5.1.3 Registered Callers 64
6.0 INDEX 65

1.0 Introduction to CS8920 Technical Reference Manual

This Manual provides the information which will be helpful in designing a board using the CS8920, programming the associated EEPROM, and installing and running the CS8920 device drivers. It is expected that the user of this Technical Reference Manual will have a general knowledge of hardware design, Ethernet, the ISA bus, and networking software. Recommended sources of background information are:

a) ISA System Architecture by Shanley and Anderson, Mindshare Press, 1992, ISBN 1-881609-05-7

b) Ethernet, Building a Communication Infrastructure, by Hegering and Lapple, Addison-Wesley, 1993, ISBN 0-201-62405-2

c) Netware Training Guide: Networking Technologies, by Debra Niedenmiller-Chaffis, New Riders Publishing, ISBN 1-56205-363-9

As shown in the Figure 1.1, the CS8920 requires a minimum number of external components. The EEPROM stores configuration information such as interrupt number, DMA channel, I-O base address, memory base address, and IEEE Individual Address. The EEPROM can be eliminated on a PC motherboard if that information in stored in the system CMOS. Note also that the Boot PROM is only needed for diskless workstations that boot DOS at system power up, over the network. Also, the LEDs are optional.

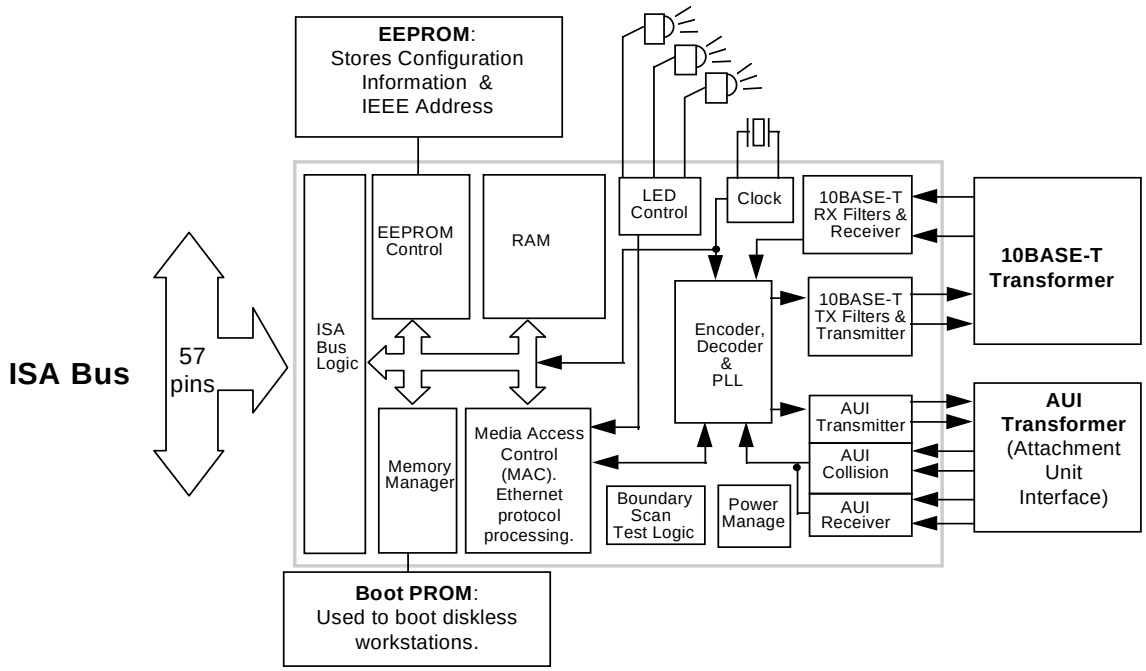


Figure 1.1 - Hardware Application Summary

The hardware design considerations for both motherboards and adapter cards are discussed in Chapter 2.0. The EEPROM programming considerations are described in Chapter 3.0. The current CS8920 data sheet can be found in section 6.0.

Crystal provides a complete set of device drivers, as discussed in Chapter 4.0. The drivers reside between the networking operating system (NOS) and the CS8920. On the CS8920 side, the drivers understand how to program and read the CS8920 control and status registers, and how to transfer user data between the CS8920 and the PC main memory via the ISA bus. On the NOS side, the drivers provide the standardized services and functions required by the NOS, and hide all details of the CS8920 hardware from the NOS. The EEPROM device programs the CS8920 whenever a hardware reset occurs, and call also store state/configuration information for the driver.

Crystal's Software Driver Distribution Policy is as follows. This developer kit contains a single-user copy of object code which is available only for internal testing and evaluation purposes. This object code may not be distributed without first signing a LICENSE FOR DISTRIBUTION OF EXECUTABLE SOFTWARE, which may be obtained by contacting your sales representative. The LICENSE FOR DISTRIBUTION OF EXECUTABLE SOFTWARE gives you unlimited, royalty-free rights to distribute Crystal-provided object code.

The drivers supported are shown in Table 1.1.

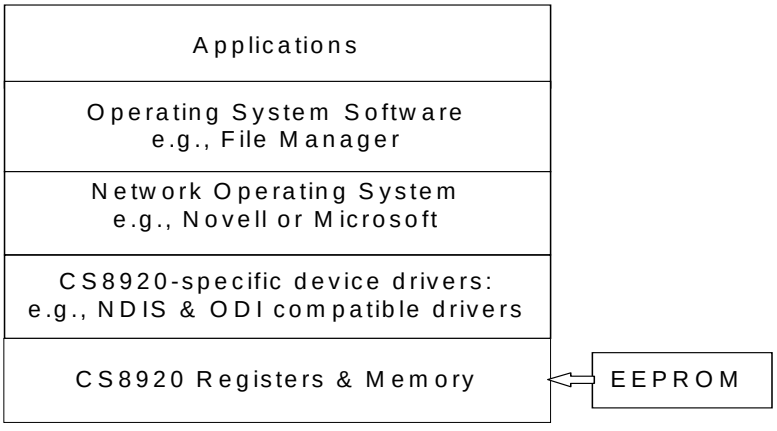


Figure 1.2 - Software Application Summary

Driver	Operating System	Network Operation System
DOS ODI Client	DOS 6.2 to 3.3, Win 3.1, Windows for Workgroups 3.11	Novell 4.X, 3.12
OS/2 ODI Client	OS/2 2.2, 2.1, Warp	Novell 4.X, 3.12
Netware Server		Novell 4.X, 3.12
NDIS 2.0.1 - DOS	DOS 6.2 to 3.3 Win 3.1	LAN Manager, LAN Server, Windows for Workgroups 3.11
NDIS 2.0.1 - OS/2	OS/2 2.2, 2.1, 3.0 (Warp)	LAN Manager, LAN Server, LANtastic
NDIS 3.x	Windows NT Windows '95 Windows for Workgroups	NT Server, NT Workstation, Novell 4.X, 3.X
Packet V1.09	DOS 6.2 to 3.3	TCP/IP stacks including: PC/TCP, SUN PC-NFS, Wollongong
SCO UNIX	SCO Unix Rel 3.2 V4.0, 4.2	SCO Open Server 3.0, 5.0
Boot PROM		Novell 4.X, 3.12 LAN Manager, LAN Server
Setup & Installation Utility	DOS 6.2 to 3.3	

Table 1.1 - Supported Drivers

2.0 Hardware Design

This section gives design guidance for both embedded and adapter card designs, including design considerations such as choosing transformers, and laying out the board.

2.1 Ethernet Hardware Design for Embedded Systems and Motherboards

This section describes the hardware design of a four-layer, 10BASE-T solution intended for use on PC motherboards, or in other embedded applications. The goal of this design is use minimal board space and minimal material cost. Therefore, a number of features (BootPROM, AUI, 10BASE-2) are not supported in this particular PCB design. An example of this circuit is included in the CS8900 Technical Reference Manual, and is implemented in an ISA form factor. This same circuit can be implemented directly on the processor PCB.

2.1.1 General Description

The small footprint, high performance and low cost of the CS8920 Ethernet solution, makes the CS8920 an ideal choice for embedded systems such as personal computer (PC) mother boards. The very high level of integration in the CS8920 results in a very low component count Ethernet design. This makes it possible to have a complete solution fit in an area of 1.75 square inches. The full Plug & Play support, Wake-Up frame and Advanced Power Management make the CS8920 ideal for design of new generation of Green PC platforms. Features like full duplex and Auto-Negotiation (N-Way) make designs using CS8920 suitable for LANs that are getting upgraded with full duplex and switching hubs. Since the analog filters are integrated in to the CS8920, a card can more easily made compliant with FCC part 15 class (B).

2.1.2 Board Design Considerations

2.1.2.1 Crystal Oscillator

The CS8920, in this reference design, uses a 20.000 MHz crystal oscillator. The crystal has a maximum load capacitance of 18 pF. The rest of the oscillator circuitry is built internal to the CS8920. Please note that the crystal must be placed very close to XTL1 and XTL2 pins of the CS8920.

This crystal oscillator can be eliminated if there is an accurate clock signal (20.00 MHz +/- 0.01% and 45-55 duty cycle) available in the system.

2.1.2.2 ISA Bus Interface

The CS8920 has a direct ISA bus interface. Note that the ISA bus interface is simple enough to allow the CS8920 to interface with variety of microprocessors directly or with the help of simple programmable logic such as a PAL or a GAL.

This reference design actually has the form factor of an ISA adapter card. In this design, all the ISA bus connections from the CS8920 are directly routed to the ISA connector. The pin-out of the CS8920 is such that if the CS8920 is placed as shown in Figure 2.1.1a, there will be no cross-over of the ISA signals.

The CS8920 can be accessed in I/O mode or memory mode. In memory mode, the CS8920 can be in the conventional or upper memory of the PC (the lower 1 Mega

bytes of address space) or in extended memory address space. Address decoders for I/O as well as memory mode are on chip for the CS8920.

2.1.2.4 EEPROM

A 128 word (128 X16 bit) EEPROM (location U3) is used in the reference design to interface with the CS8920. This EEPROM holds the IEEE assigned Ethernet MAC (physical) address for the board (see Section 3.3.1). The EEPROM also holds other configuration information for the CS8920. The EEPROM also holds the Plug & Play resource information. The last few bytes of the EEPROM are used to store information about the hardware configuration and software requirements.

Since the CS8920 has full Plug & Play support, it requires an EEPROM to configure itself after a reset.

Please refer to the CS8920 data sheet for information about programming the EEPROM. Please refer to the Section 3.0 of this document for information about EEPROM internal word assignments.

2.1.2.5 LEDs

Many embedded systems do not require LEDs for Ethernet traffic. Therefore this reference design does not implement any LEDs. However, the CS8920 has direct drives for the four LEDs. Please refer to the data sheet for the CS8920 for a description of the LED functions available.

2.1.2.6 10BASE-T Interface

The 10BASE-T interface for the CS8920 is straight forward. Please refer to Figure 2.1.4 for connections and components of this circuit. Transmit and receive signal lines from the CS8920 are connected to an isolation transformer at location T1. This isolation transformer has a 1:1 ratio between the primary and the secondary windings on the receive side, and a 1:$\sqrt{2}$ (1:1.41) ratio between the primary and the secondary windings for the transmit lines. Resistor R1 provides termination for the receive lines. Resistors R2 and R3 are in series with the differential pair of transmit lines for impedance matching.

2.1.2.7 10BASE-2 and AUI Interfaces

As many embedded systems require only a 10BASE-T interface, this reference design implements only the 10BASE-T interface. However, should a user require a 10BASE-2 or AUI interface, the CS8920 provides a direct interface to the AUI. Please refer to the CS8900 Technical Reference Manual or the CS8920 datasheet for details about the AUI interface.

2.1.3 Logic Schematics

Figures 2.1.2 and 2.1.4 detail the logic schematics for the various circuits used in the reference design.

2.1.4 Component Placement and Signal Routing

Please refer to the Section 2.2 of this document for more details on the placement of components on the board. It is important to provide very clean and adequate +5 V and ground connections to the CS8920.

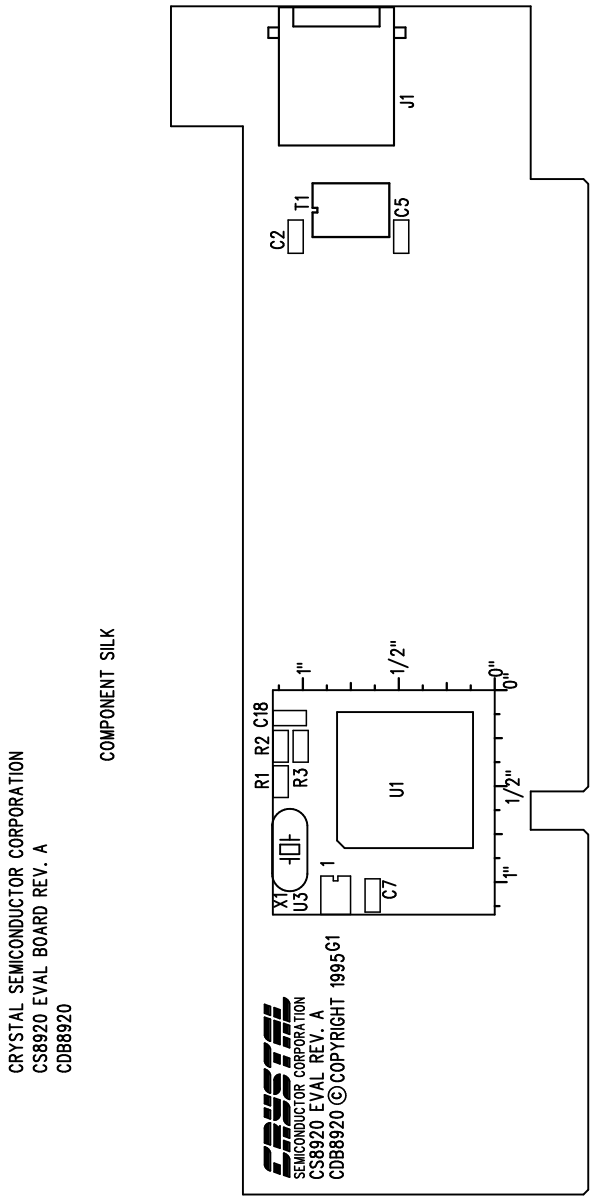
2.1.5 Bill of Material

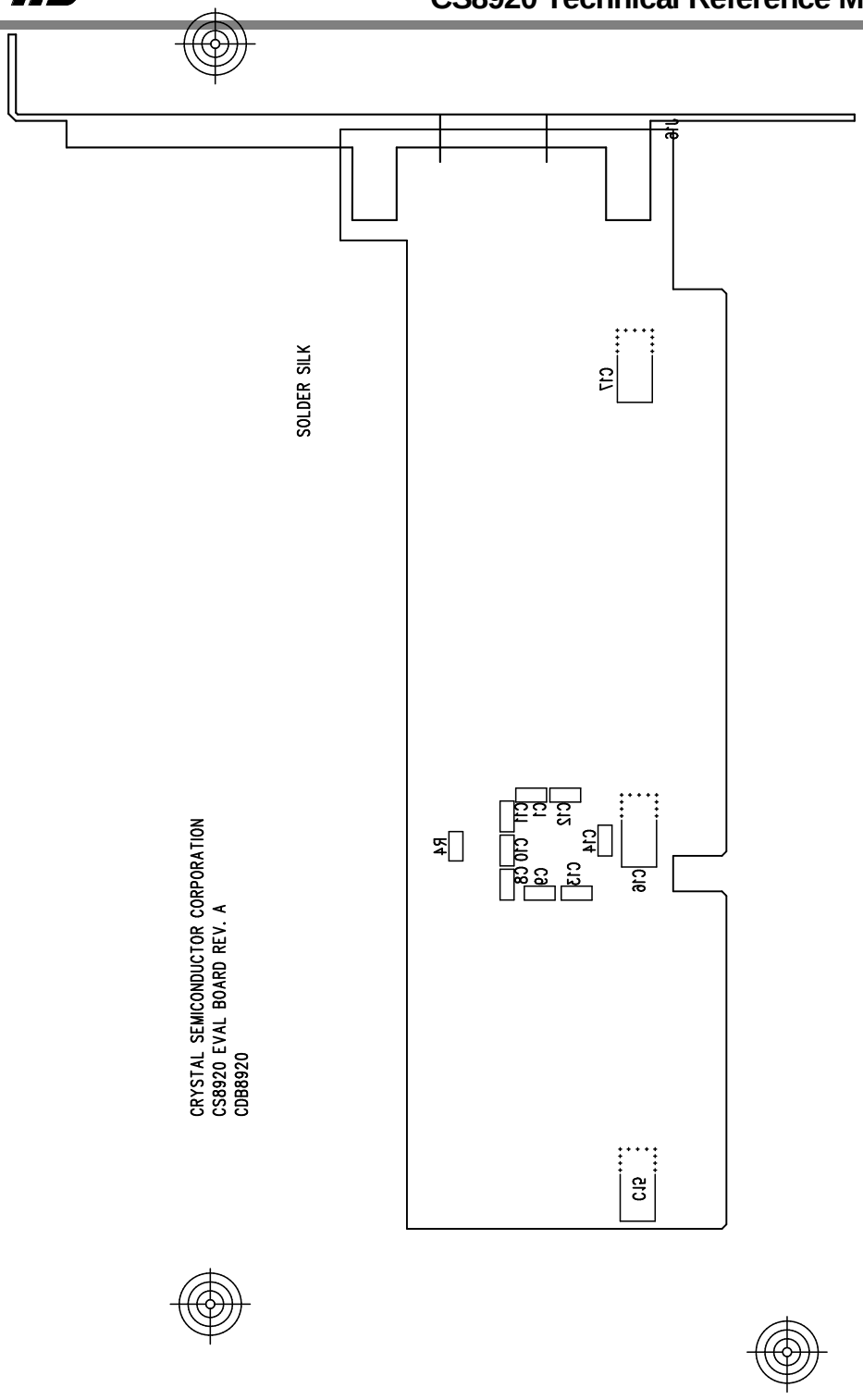
Table 2.1 has a list components that are typically used to assemble this adapter card. For most of the components, there are several alternative manufacturers.

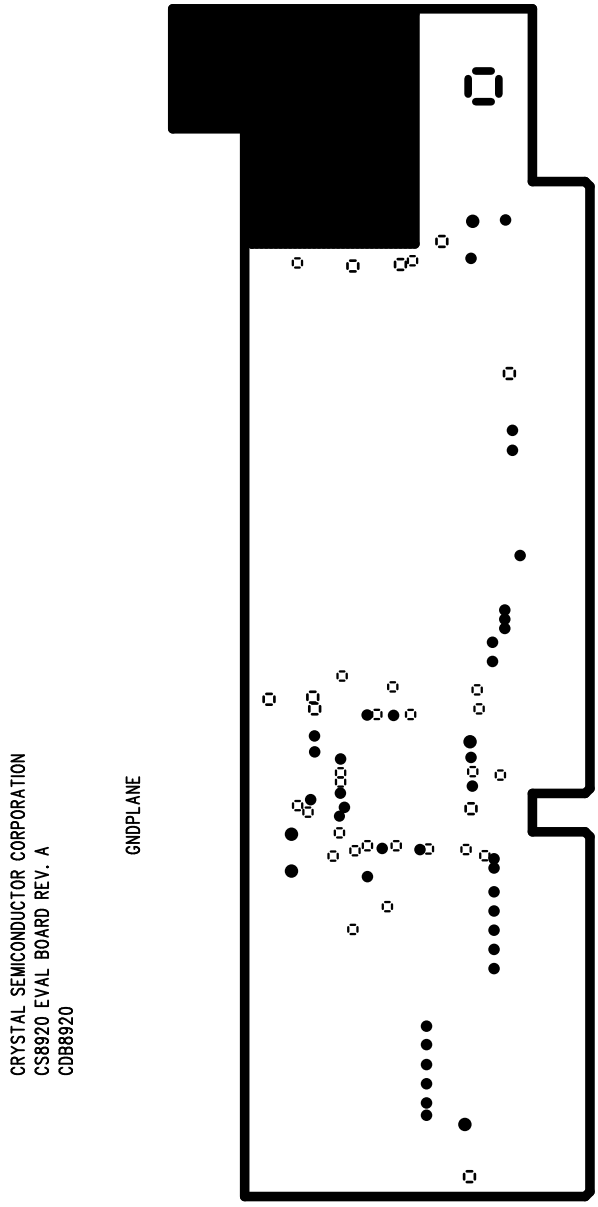
Item	Reference #	Description	Quantity	Vendor	Part Number
1	C1, C2, C5, C7, C8, C9, C10, C11, C12, C13, C14	Capacitor, 0.1 µF, X7R, SMT 0805	11		
2	C15, C16,	Capacitor, 22 µF, SMT 7343	3		
3	C18	Capacitor, 68 pF, NPO, SMT	1		
4	R2, R3	Resistor, 24.3, 1%, 1/8W, SMT	2		
5	R1	Resistor, 100, 1%, 1/8W, SMT	1		
6	R4	Resistor, 4.99K, 1%, SMT	1		
7*	X1	Crystal, 20.000 MHz	1	M-tron	ATS-49.20.000
8	J1	Connector, RJ45, 8 pin	1	AMP	555164-1
9	T1	Transformer, 2, 1:1, 1:1.41	1	Valor	ST7011 (SOIC)
10	U1	ISA Ethernet Controller	1	Crystal	CS8920
11*	U3	2K EEPROM	1	Microchi	93C56 (8 pin SOIC)
12		Board bracket	1	Gompf	9340
13		CDB8920 PCB Rev A	1		
14		4/40 Screws	2		

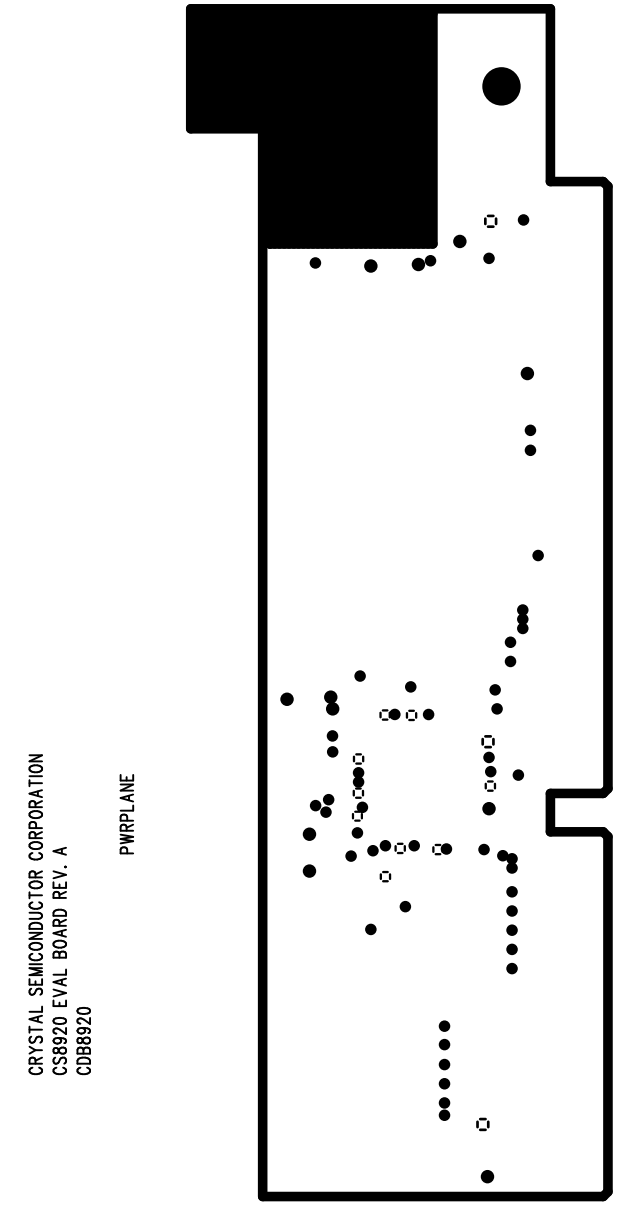
* Depending on system resources, these parts may not be needed.

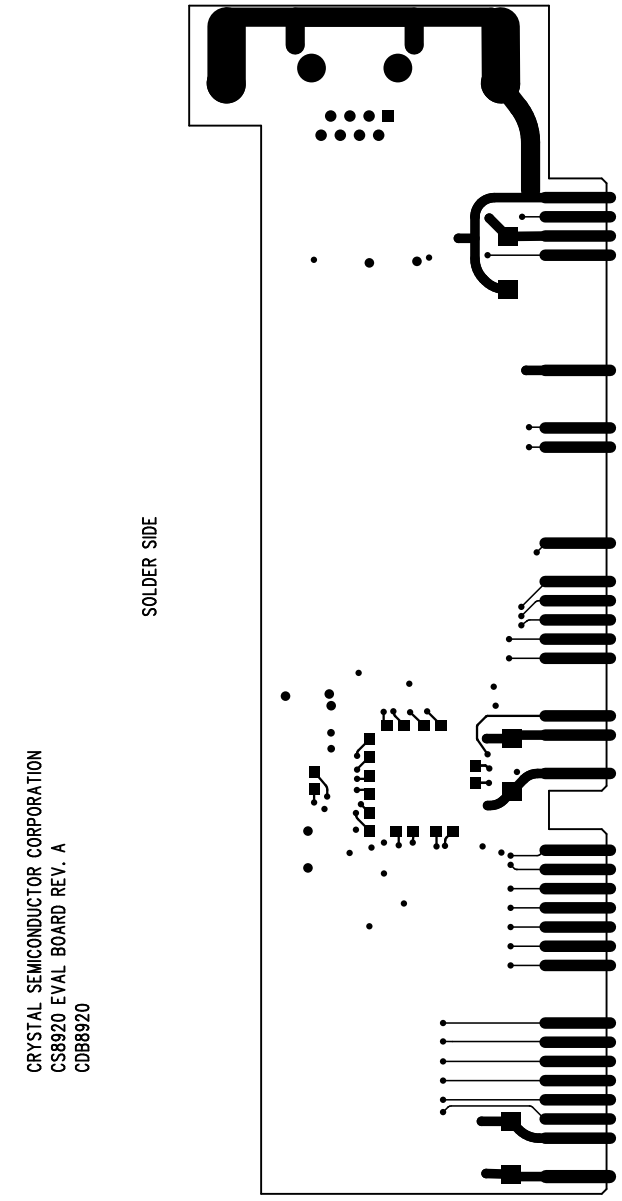
Table 2.1. CS8920 Motherboard Design Bill of Materials

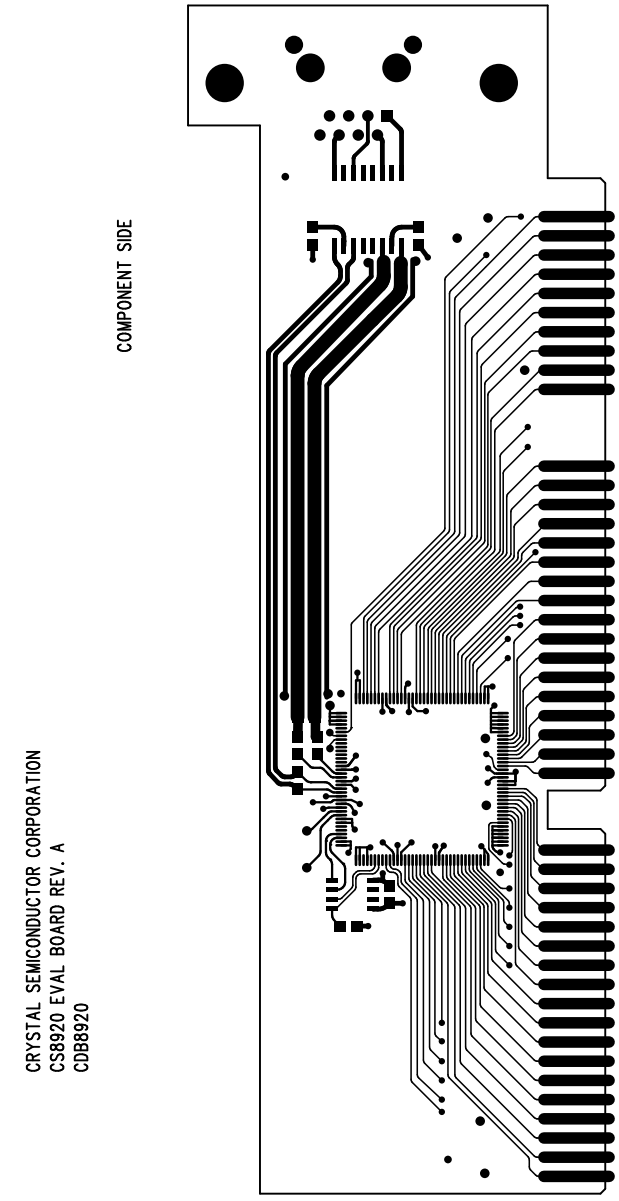

J1
T1
C2
C5
R1 R2 C18
R3
U1
X1
U3
C7
1"
1/2"
0"
1/2"
1"
SEMICONDUCTOR CORPORATION
CS8920 EVAL REV. A
CDB8920 ©COPYRIGHT 1995G1
COMPONENT SILK
CRYSTAL SEMICONDUCTOR CORPORATION
CS8920 EVAL BOARD REV. A
CDB8920


SOLDER SILK
CRYSTAL SEMICONDUCTOR CORPORATION
CS8920 EVAL BOARD REV. A
CDB8920


CRYSTAL SEMICONDUCTOR CORPORATION
CS8920 EVAL BOARD REV. A
CDB8920
GNDPLANE


CRYSTAL SEMICONDUCTOR CORPORATION
CS8920 EVAL BOARD REV. A
CDB8920
PWRPLANE


SOLDER SIDE
CRYSTAL SEMICONDUCTOR CORPORATION
CS8920 EVAL BOARD REV. A
CDB8920


COMPONENT SIDE
CRYSTAL SEMICONDUCTOR CORPORATION
CS8920 EVAL BOARD REV. A
CDB8920

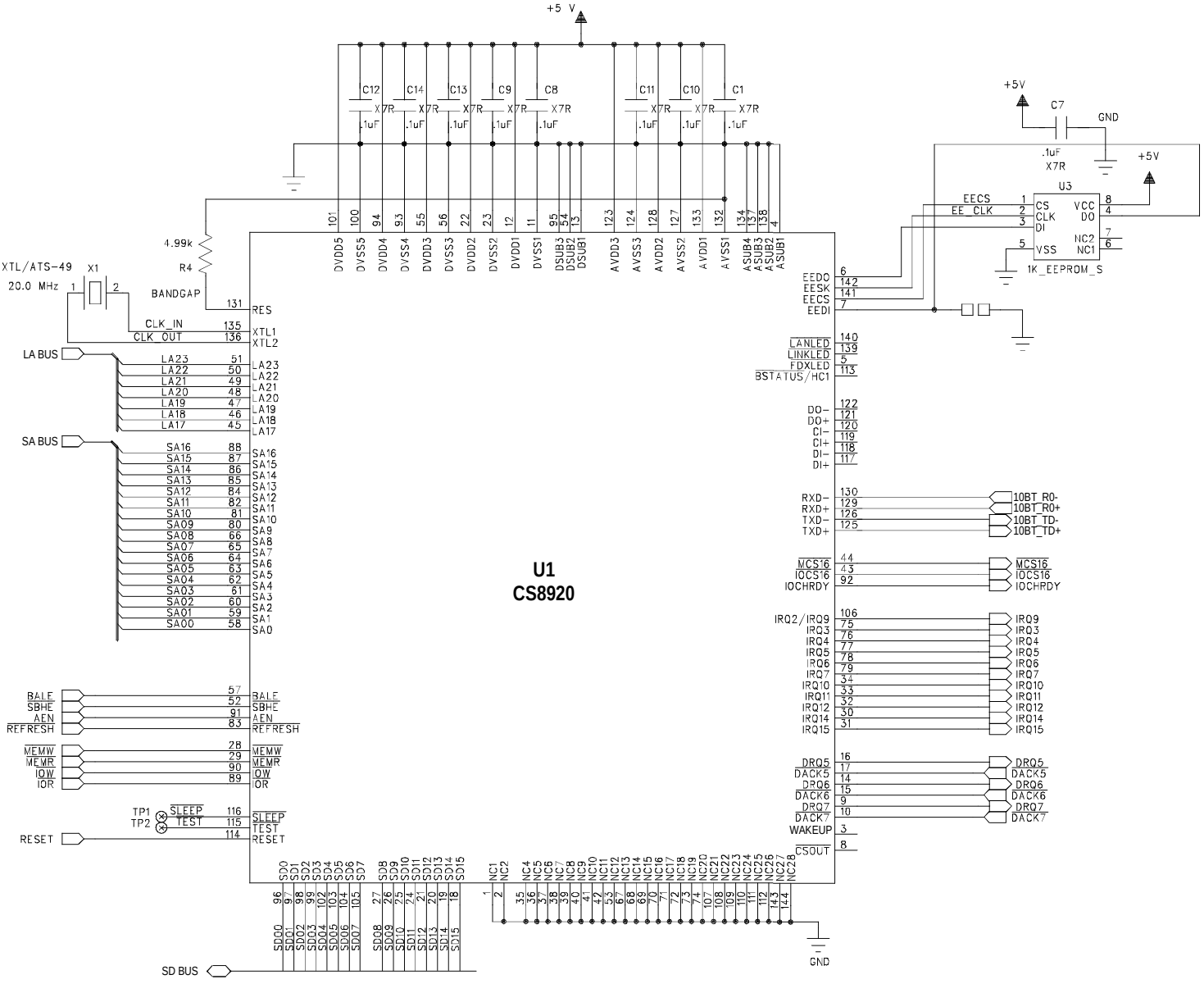


Figure 2.1.2. Overall Schematic

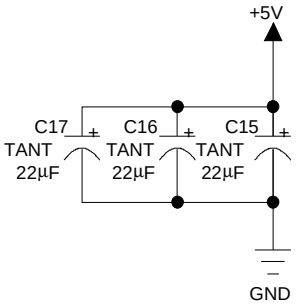


Figure 2.1.3. Decoupling Capacitors Schematic

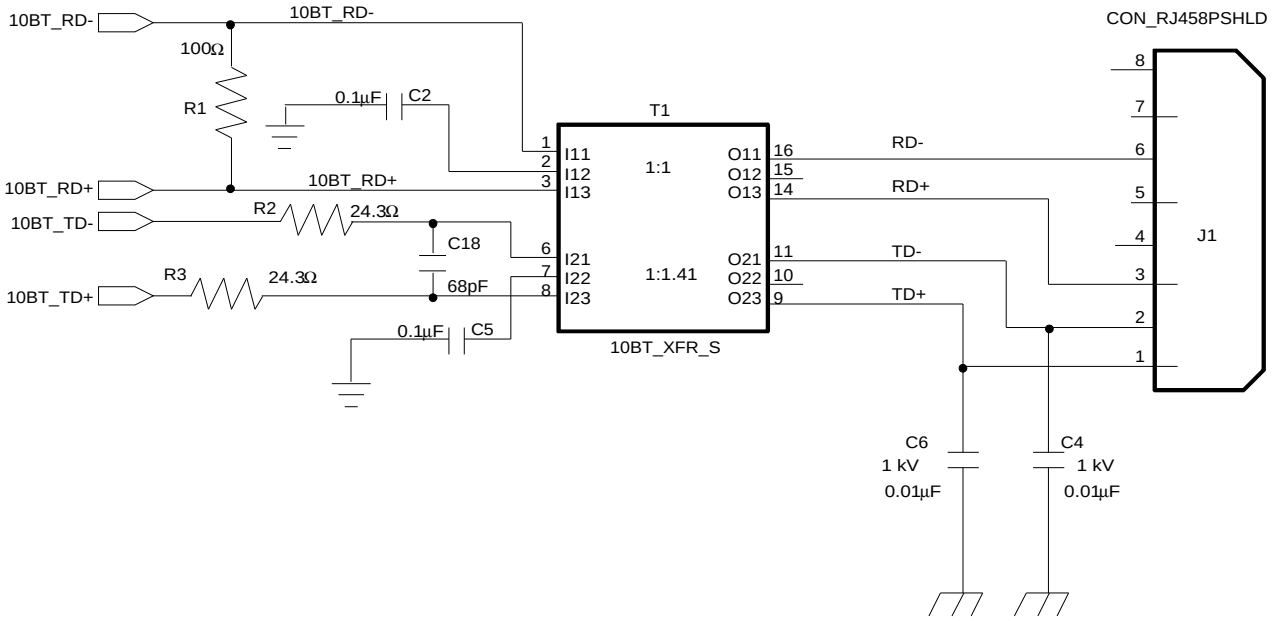


Figure 2.1.4. 10BASE-T Schematic

2.2 Layout considerations for the CS8920

The CS8920 is a mixed signal device having digital and analog circuits for an Ethernet communication. While doing the PCB layout and signal connections, it is important to take the following precautions:

(a) Provide a low inductive path to reduce power and ground connection noise.

(b) Provide proper impedance matching especially to the Ethernet analog signals.

(c) Provide low inductive path, wider and short traces, for all analog signals.

It is important that a PCB designer follow suggestions made in this document for proper and reliable operation of the CS8920. These guidelines will also help to ensure good EMI test results.

2.2.1 General guidelines

Figure 2.2.1 shows component placement for an ISA COMBO Ethernet adapter card using a CS8900. For a CS8920 Combo card, substitute CS8920 in place of CS8900. The placement of the CS8920 should be such that the routes of the analog signals and the digital signals are not intermixing. No signal should route beneath the CS8920 on any plane.

2.2.2 Power supply connections

The CS8920 has 3 analog and 5 digital power pin pairs (Vcc and GND). Additional ground connections are provided. Each power pin pair should be connected to a 0.1 µF bypass capacitor. Connect the extra ground pins directly to the ground plane.

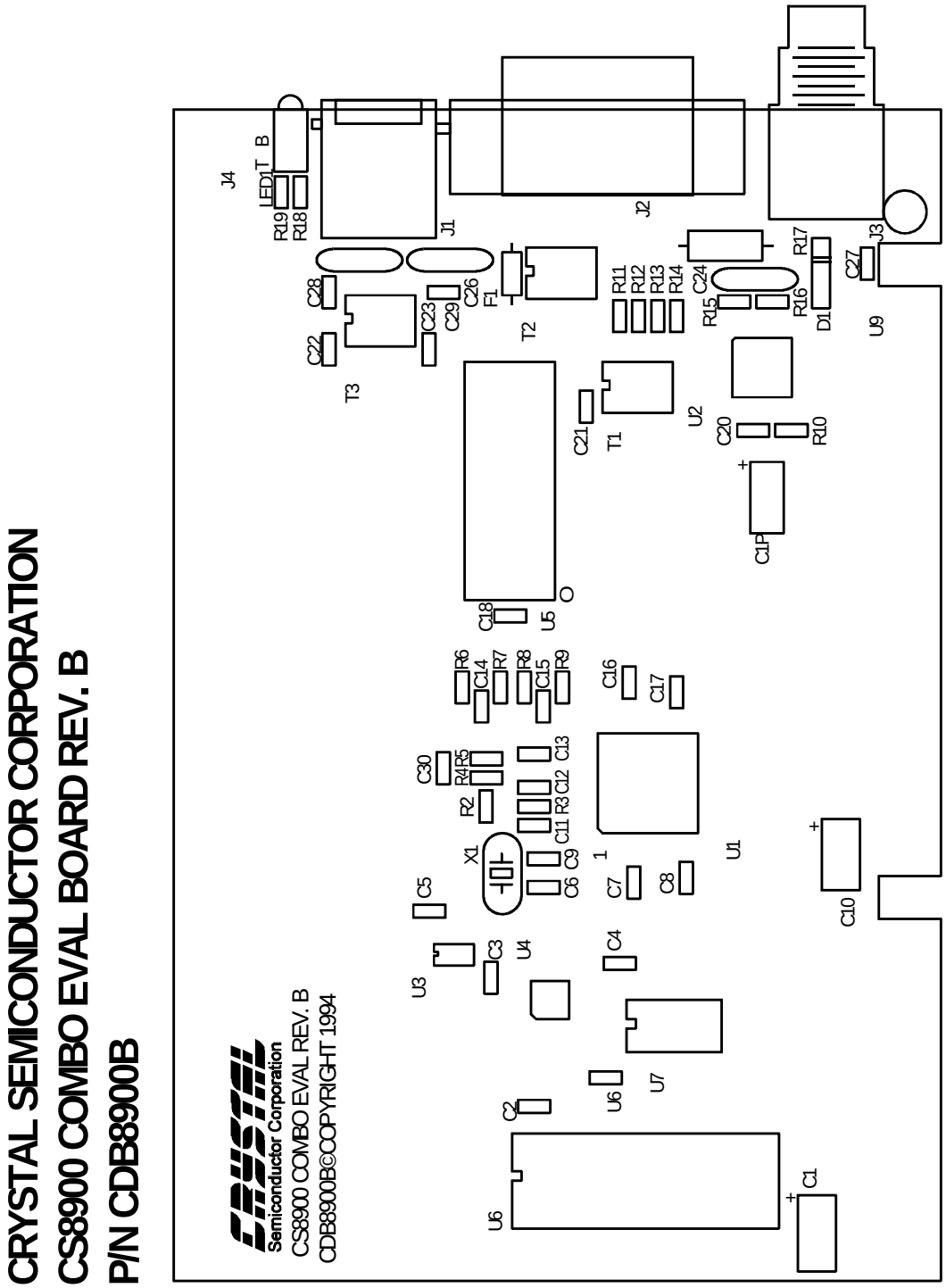


Figure 2.2.1. General placement on an ISA adapter card

2.2.2.1 Two layered printed circuit board (PCB)

A two layered PCB has signal traces on the component and solder side of the PCB. Fill unused areas with copper planes. Typically, planes on the component side of the PCB are connected to ground and those on the solder side are connected to VCC or +5 volts.

Provide each pair of power pin with a 0.1 µF bypass capacitor. Place each bypass capacitor as close as possible to the corresponding power pin pair. Connect the capacitor to the pads of the power pins by short, wide traces, the other end of these traces should be connected to VCC and GND planes. Figure 2.2.2 and Figure 2.2.3 illustrate ground and power (Vcc) plane connections, respectively.

2.2.2.2 Multi-layered printed circuit board

A multi-layered printed circuit board (PCB) typically has separate ground and power (VCC) planes. Multi-layered PCBs are required when the component and trace density is high. Often discrete components like resistors and capacitors are placed on the solder side of a printed circuit board.

For a multi layer PCB with all components on one side of the board, follow the power connection guide lines as explained in section 2.2.2.1. Instead of connecting the ground and VCC to the copper fills on the component and solder side of the board, connect them to the internal ground and VCC planes. Figures 2.2.4 through 2.2.9 show the four layers of the four-layer card.

For a multi-layered board the discrete components are to be placed on the solder side of the PCB, bypass capacitors for the CS8920 can be placed on the solder side of the PCB. Each bypass capacitor should be placed beneath the CS8920 and closest to its corresponding power pin pair. Figures 2.2.10 and 2.2.11 illustrate the placement and routing of one bypass capacitor.

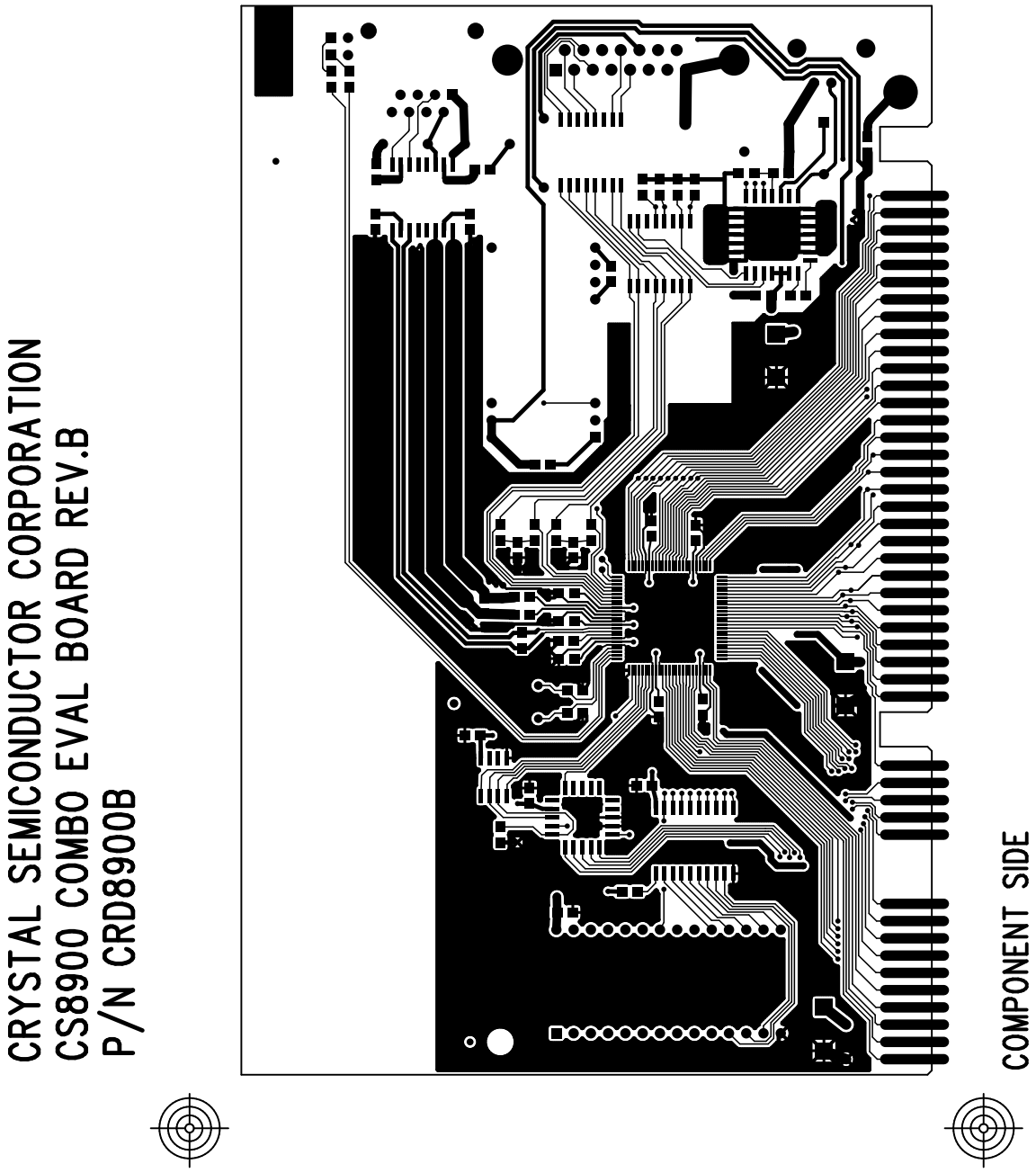


Figure 2.2.2. Ground connection.
Top layer of two-layer Combo Card

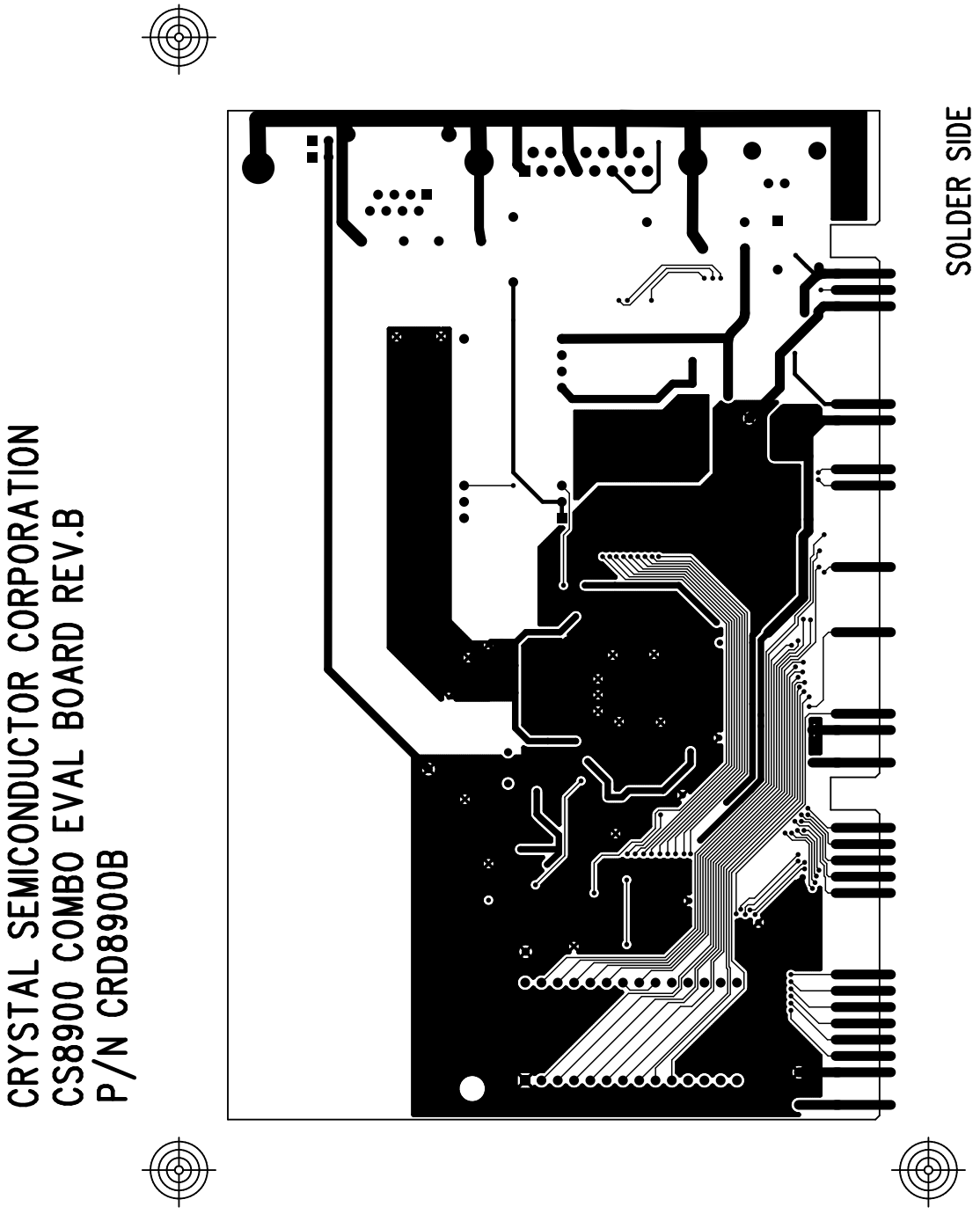
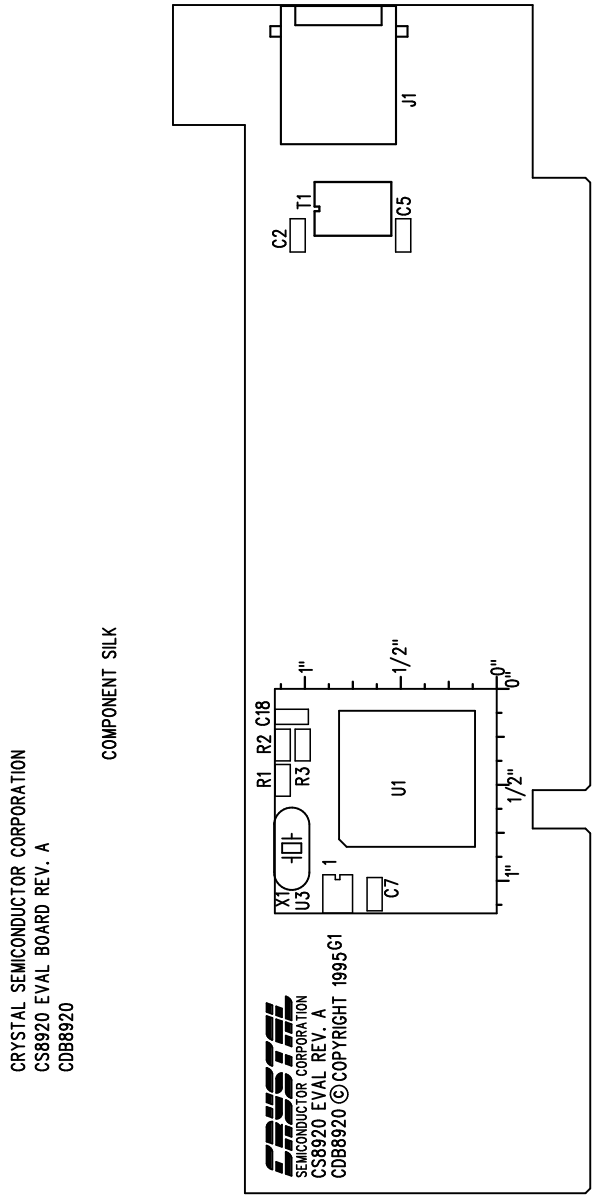
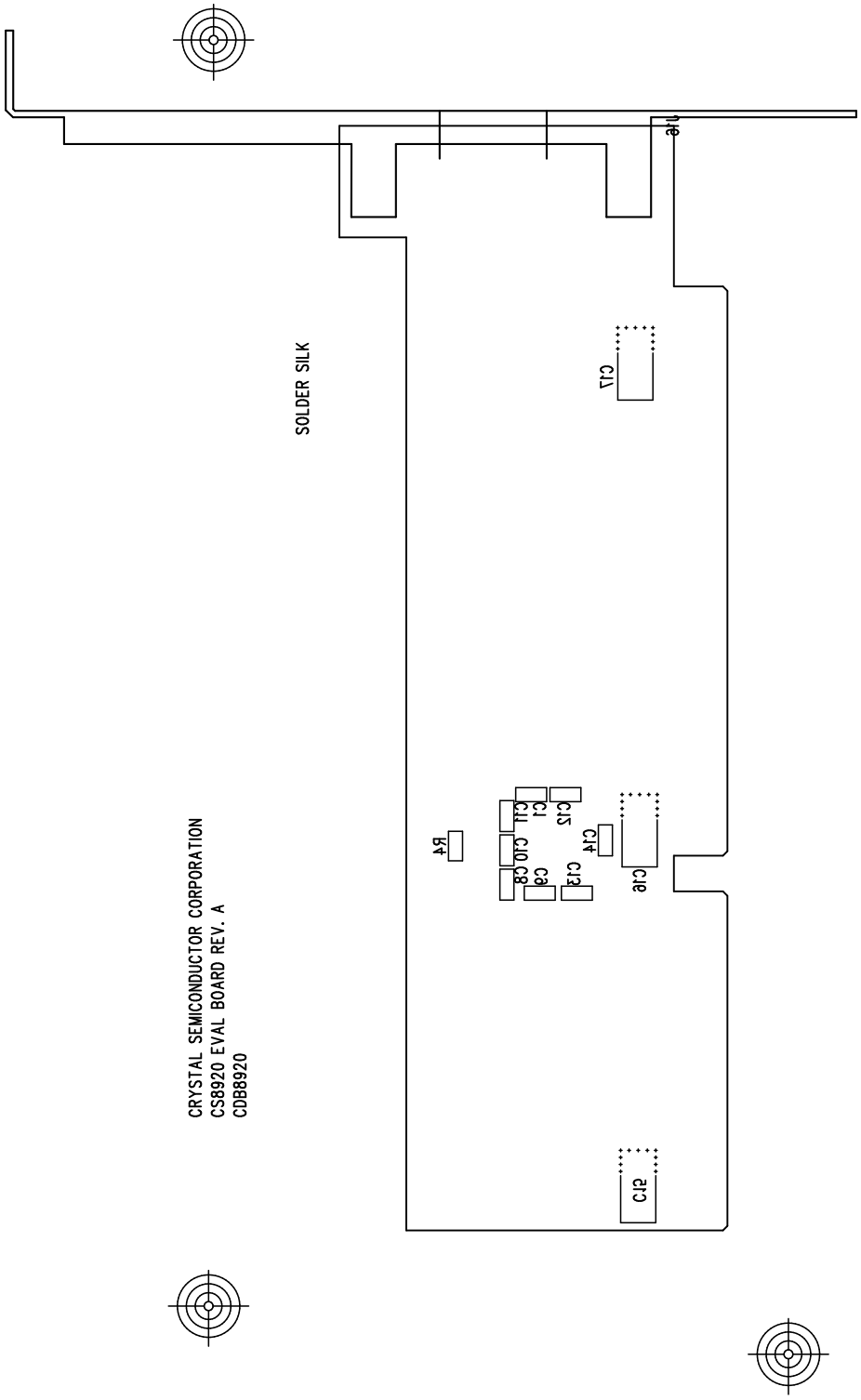
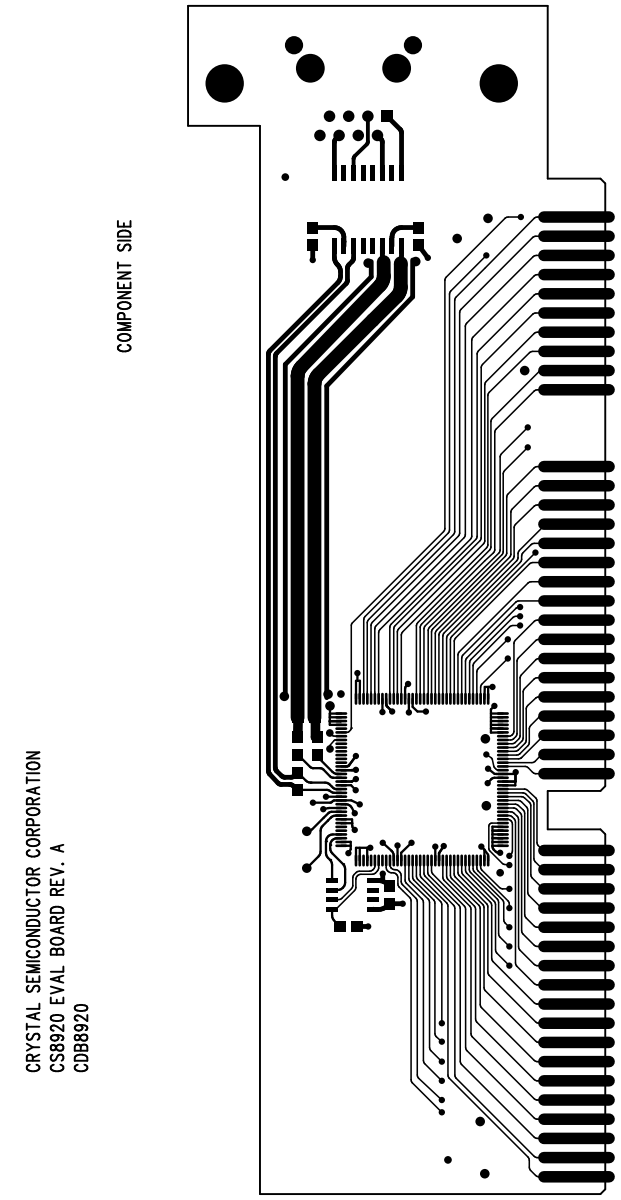
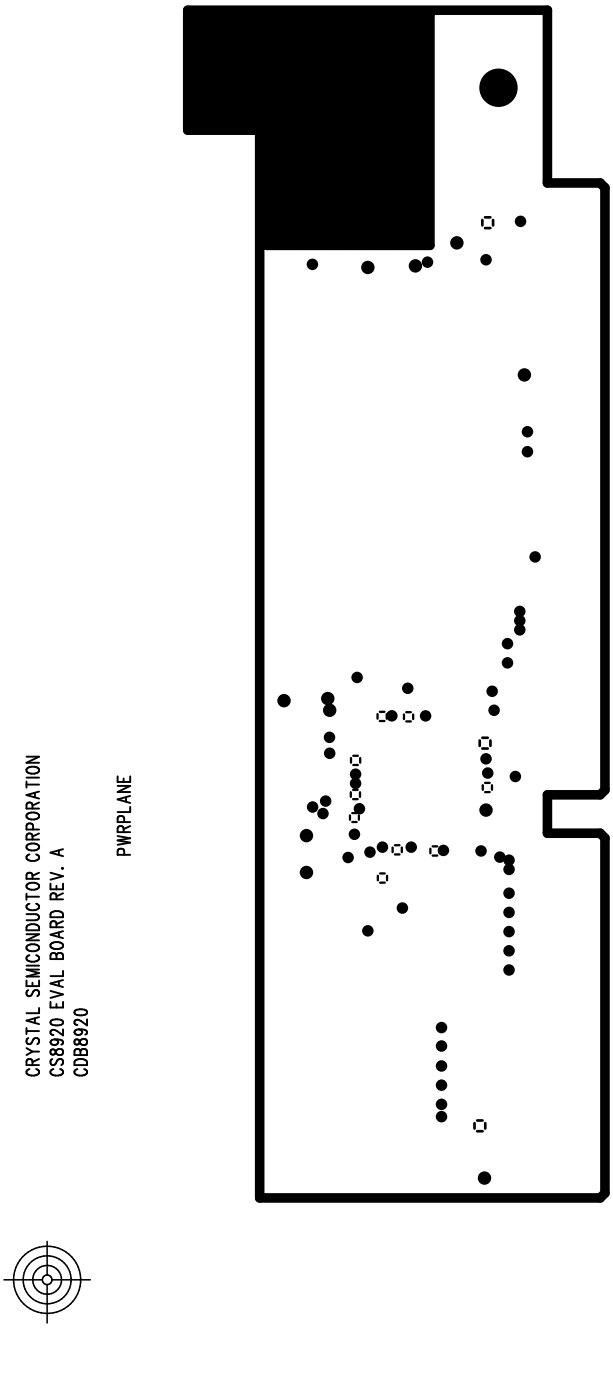


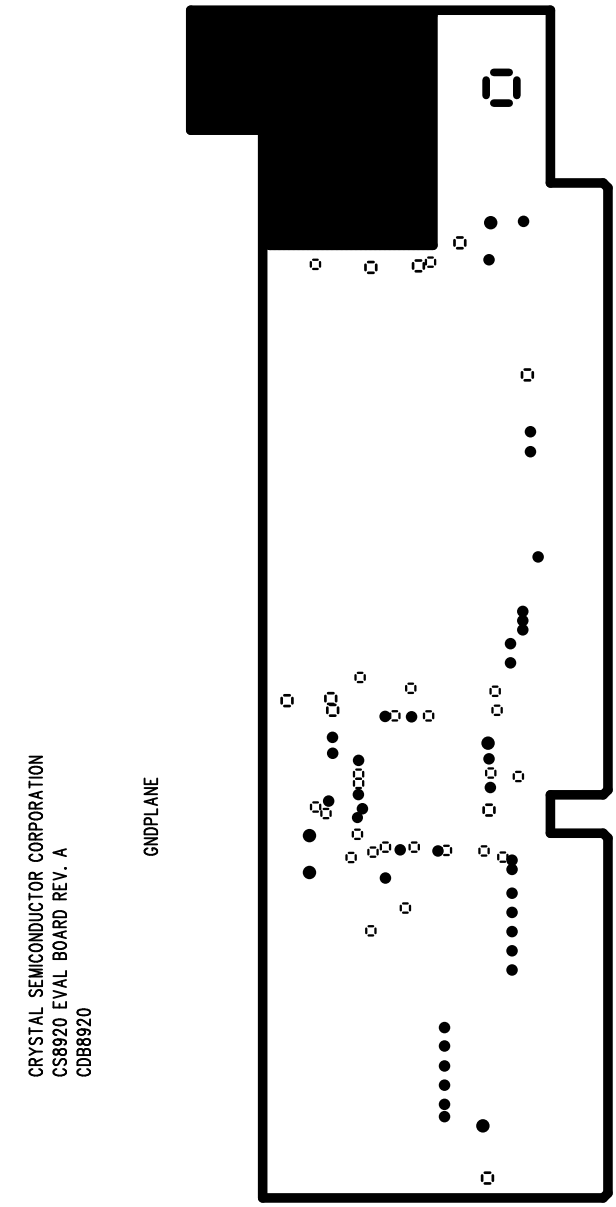
Figure 2.2.3. Power (Vcc) Connection.
Bottom layer of two-layer Board


J1
T1
C5
C2
1"
1/2"
0"
R1 R2 C18
R3
U1
1/2"
1"
X1
U3
1
C7
SEMICONDUCTOR CORPORATION
CS8920 EVAL REV. A
CDB8920 ©COPYRIGHT 1995G1
COMPONENT SILK
CRYSTAL SEMICONDUCTOR CORPORATION
CS8920 EVAL BOARD REV. A
CDB8920


SOLDER SILK
CRYSTAL SEMICONDUCTOR CORPORATION
CS8920 EVAL BOARD REV. A
CDB8920


COMPONENT SIDE
CRYSTAL SEMICONDUCTOR CORPORATION
CS8920 EVAL BOARD REV. A
CDB8920


CRYSTAL SEMICONDUCTOR CORPORATION
CS8920 EVAL BOARD REV. A
CDB8920
PWRPLANE


CRYSTAL SEMICONDUCTOR CORPORATION
CS8920 EVAL BOARD REV. A
CDB8920
GNDPLANE

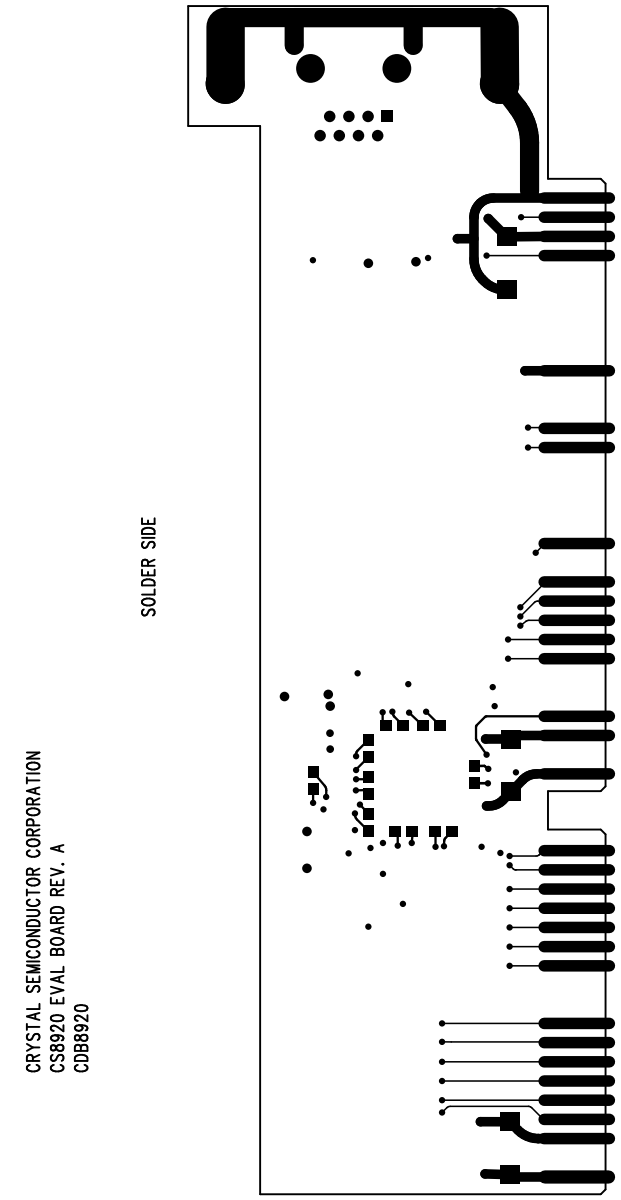

SOLDER SIDE
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CS8920 EVAL BOARD REV. A
CDB8920



Figure 2.2.10. Placement of Decoupling Capacitor (Bottom side, under CS8920)

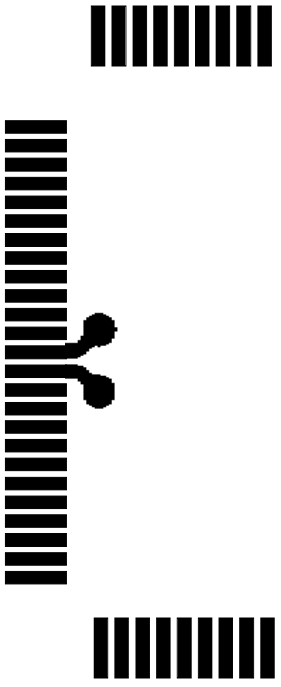


Figure 2.2.11. Routing of Decoupling Capacitor (Top side, component side)

2.2.3 Routing of the digital signals

Most of the digital signals from the CS8920 go to the ISA bus connector. Route these signals directly to the connector. Isolate the digital signals from analog signals.

2.2.4 Routing of the analog signals

2.2.4.1 Routing of the clock signals:

Place the 20.000 MHz crystal within one inch of XTL1 (pin #135) and XTL2 (pin #136) pins of the CS8920. The 20.000 MHz crystal traces should be short, have no via, and run on the component side.

2.2.4.2 Biasing resistor at RES pin of the CS8920

A 4.99 K Ohm resistor is connected between pins RES (pin #131) and AVSS3 (pin #132) of the CS8920. This resistor biases internal analog circuits of the CS8920, and should be placed as close as possible to RES pin (pin #131) of the CS8920.

2.2.4.3 Routing of the 10BASE-T signals

Four signals are used for 10BASE-T communication, two differential transmit signals and two differential receive signals. An isolation transformer is placed between the transmit and receive traces and a RJ-45 (modular phone jack) connector. The isolation transformer should be placed as close as possible to the RJ-45 connector. Both transmit and receive signal traces should be routed so they are parallel and of equal length. The signal traces should be on the component side and should have direct and short paths. The widths of the receive signal traces should at least be 25 mil. while widths of the transmit signal traces should be at least 100 mil. This will provide a good impedance matching for the transmit and receive circuitry inside the CS8920. A ground trace should be run parallel to the transmit traces. Also, a ground plane should run underneath the transmit and receive traces on the solder side of a two layered PCB. Please refer to the Figures 2.2.12 and 2.2.13 for illustration of the above guide lines.

2.2.4.4 Routing of the AUI signals

The CS8920 has three pairs of differential signals connecting it to an Auxiliary Unit Interface (AUI). An isolation transformer separates the three signal pairs and the AUI connector (a 15 pin sub-D connector). The isolation transformer should be placed as close as possible to the AUI connector. Signal traces of each differential pair should be in parallel with equal length and impedance. Thus minimizing differential noise due to impedance mis-match. Place the AUI signal traces on the component side.

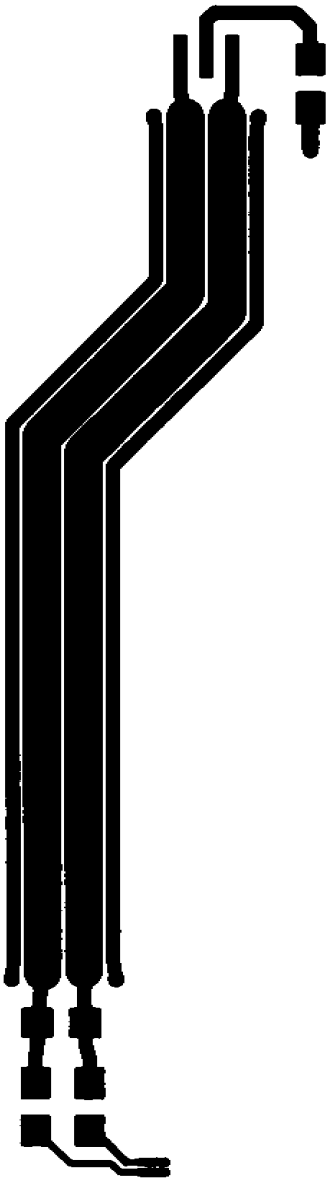


Figure 2.2.12. 10BASE-T Transit Layout Details



Figure 2.2.13. 10BASE-T Receive Layout Details

2.3 Recommended Magnetics for the CS8920

The CS8920 is has two types of Ethernet interfaces 10BASE-T and AUI. For both the interfaces, analog filters are on the chip. The Figure 2.3.1 shows typical connection required for either of these interfaces. Please refer to the data sheet of the CS8920 for values of the terminating resistors.

For an AUI interface, an isolation transformer without a common mode choke (CMC) is used.

For the 10BASE-T interface, choice between isolation transformer and isolation transformer with a common mode choke (CMC) depends on the common mode noise that exists on the 10BASE-T lines in a particular system. A common mode choke reduces common mode noise emitted by the 10BASE-T lines. A CMC may be required in certain applications to meet EMI requirements and to meet 10BASE-T common mode output voltage noise specification. The physical dimensions of the isolation transformer and the isolation transformer with a CMC are the same. Both are typically available in a 16 pin DIP or 16 pin SOIC package.

The table 2.3.1 thru 2.3.3 provides information regarding recommended transformers and contacts for some of the vendors. Several other vendors also make transformers that are compatible with the ones these tables.

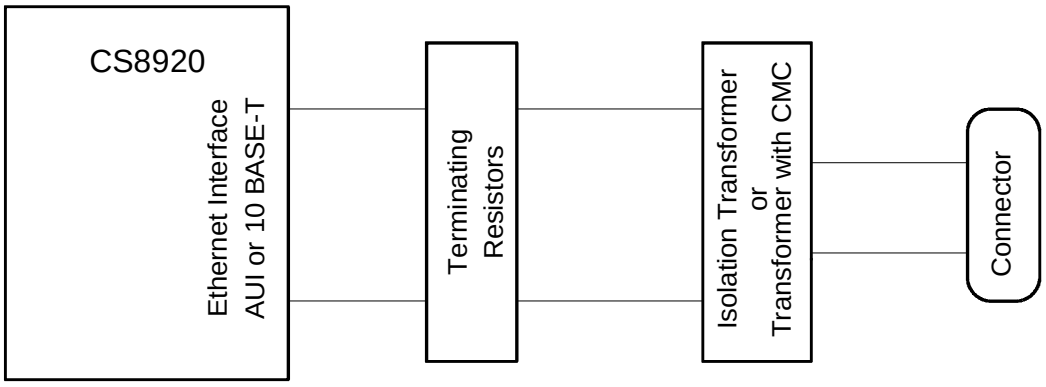


Figure 2.3.1. Typical CS8920 Ethernet Connection

Vendor name	Description	Through-hole	Surface-mount
Pulse Engineering	Isolation transformer, 100 µH	PE-64503	PE-65728
Valor Electronics	Isolation transformer, 100 µH	LT6033	ST7033

Table 2.3.1. Partial List of Recommended AUI Transformers

Vendor name	Description	Through-hole	Surface-mount
Pulse Engineering	Isolation transformer 1:1::1:1.41	PE-65994	PE-65745
	Transformer with CMC	PE-65998	PE-65746
Valor Electronics	Isolation transformer 1:1::1:1.41	PT4069	ST7011
	Transformer with CMC	PT4068	ST7010

Table 2.3.2. Partial list of Recommended 10BASE-T Transformers

Company and Address	Telephone	FAX
Pulse Engineering PO Box 12235 San Diego, CA 92112	(619)-674-8100	(619)-674-8262
Valor Electronics 9715 Business Park Avenue, San Diego, CA 92131	(619)-537-2500	(619)-537-2525

Table 2.3.3. Transformer Vendors

3.0 EEPROM-based Configuration

The CS8920 and media access control (MAC) driver obtain configuration data from a serial EEPROM connected via the CS8920's serial interface. This eliminates the need for configuration jumpers or switches on the ISA adapter or motherboard.

3.1 Format of Configuration Data

Three types of configuration data are stored in the EEPROM: configuration data automatically loaded into the CS8920 after each reset, configuration data used by the MAC driver, and Plug and Play (PnP) resource data.

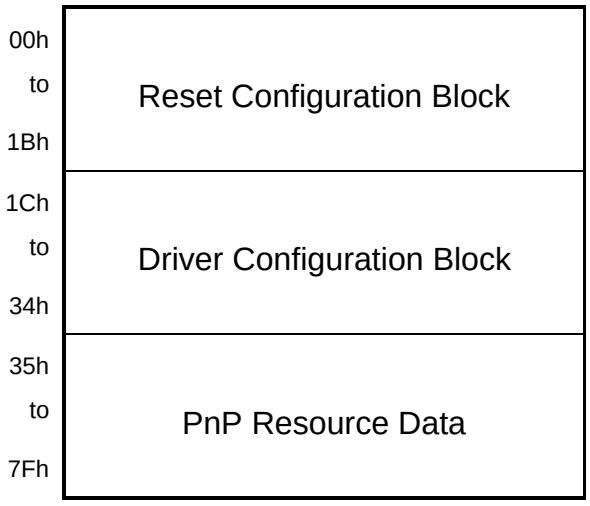


Figure 3.1 EEPROM Data Blocks

Each type of configuration data is grouped together, organized as 16-bit words, in a separate block of the EEPROM. The arrangement and location of the three blocks of configuration data are shown in Figure 3.1.

3.2 Reset Configuration Block

After each reset (except EEPROM reset) the CS8920 checks to see if an EEPROM is connected. If an EEPROM is present, the CS8920 automatically loads first block of data stored in the EEPROM into its internal registers. This block of data is referred to as the Reset Configuration Block. It is used to initialize the CS8920 after each reset. If an EEPROM is not present (or a checksum error indicates the Reset Configuration Block is invalid) the CS8920 executes an EEPROM reset causing all PacketPage registers to be loaded with their default values.

Note: The default state of the CS8920 after an EEPROM reset is inactive (i.e., all normal ISA bus IO to or from the CS8920 is disabled). Communication with the CS8920 must then be established using the Crystal auxiliary key written to the CS8920 via the PnP write-data port. Refer to Section 3.5 for more information on using the CS8920 auxiliary key and its use in programming and initializing the EEPROM.

3.2.1 Reset Configuration Block Format

The Reset Configuration Block must begin at EEPROM word address 0x00 and can vary in length up to a maximum of 28 words (word address 0x1B).

3.2.1.1 Reset Configuration Block Header

The word at EEPROM address 0x00 is the Reset Configuration Block header. The header indicates the type of EEPROM in use and the length of the Reset Configuration Block (the number of bytes loaded into the CS8920 after reset). It can also be used to disable the PnP feature of the CS8920.

The presence of bit patterns 1010b (0xA) or 1011b (0xB) in bits 15-12 of the header indicate the presence of a Reset Configuration Block. The plug and play circuitry of the CS8920 can be disabled by setting bits 15-12 (high nibble) of the header to 0xB.

Bit 8 (bit 0 being the LSB of the word) of the header specifies the type of EEPROM used. A value of 0 in bit 8 indicates a sequential EEPROM is used. A value of 1 in bit 8 indicates a non-sequential EEPROM is used. (The CS8920 works equally well with either type of EEPROM. It will automatically generate sequential addresses while reading the Reset Configuration Block from non-sequential type EEPROMs.)

The low byte of the header (bits 7-0) specify the number of bytes of configuration data in the Reset Configuration Block including the first word and checksum at the end of the block.

Example: a Reset Configuration Block of 0xA10A indicates a valid configuration block, non-sequential EEPROM, 10 bytes of configuration data follow, and PnP is enabled.

3.2.1.2 Configuration Data

Following the Reset Configuration Block header are one or more groups of configuration data that are to be automatically loaded into the CS8920's PacketPage registers.

Each group of configuration data consists of a group header (the first word in the group) and one or more words of configuration data. The group header indicates the number of words in the group along with the address of the PacketPage register into which the first word of configuration data are to be loaded.

The value in bits 15-12 of the group header is one less than the total number of configuration data words in the group. For example, if bits 15-12 equal 0001, there are two words of configuration data in the group.

Bits 9 through 0 of the group header indicate the 10-bit address of the PacketPage register the first word of configuration data in the group is to be loaded into. If there are additional configuration data words in the group, they are loaded in successive PacketPage registers. See Table 3.1 for an example.

Bits 11 and 10 of the group header are forced to 0 when read by the CS8920, restricting the destination address range of the configuration to the first 1024 bytes of the PacketPage memory.

3.2.1.3 Checksum

The last word of the Reset Configuration Block contains an 8-bit checksum in the

high byte of the word (bits 15-8). The checksum value is the 2's complement of all the bytes in the Reset Configuration Block excluding the checksum byte. (The low byte of the checksum word is not used and it is recommended that it be set to 0x00.) Since the checksum is the 2's complement of all the bytes in the Reset Configuration Block, a total sum of 0 should result when the checksum value is added to the sum of all the preceding bytes.

3.2.2 Typical Reset Blocks

The contents of the Reset Configuration Block depend on the CS8920's intended mode of operation and adapter configuration. Following are examples of typical Reset Configuration Blocks for three different modes of operation: as a legacy adapter, as a PnP adapter, and as a PnP adapter with the Auto-wakeup feature enabled.

3.2.2.1 Recommended Reset Configuration Block for a Legacy Adapter

Table 3.2 shows the recommended Reset Configuration Block for a CS8920 adapter installed in a legacy system. The definition of a legacy system as used in this chapter is any PC system that does not rely on a function of PnP to automatically configure and activate the adapter.

The default state of the CS8920 after an ISA reset is inactive with its IO base address set to 0x00. Therefore, the adapter must be activated and the IO base address set from the EEPROM after each ISA reset.

Note: In systems that have an autoconfiguring PnP BIOS but an ESCD database is not maintained or the BIOS does not activate the adapter, it will be necessary to manually configure the CS8920 as if in a legacy system. However, it may still be advantageous to leave the PnP functions of the CS8920 enabled.

Addr	Word	Description
00h	B112h	PnP Disabled, 18 bytes follow
01h	2158h	3 words, start with PacketPage 158h (IA)
02h	0100h	Individual Address
03h	0302h	of
04h	0504h	000102030405h
05h	0360h	1 word to PacketPage 360h (IO Base)
06h	0003h	IO Base Address = 300h
07h	0330h	1 word to PacketPage 330h (RegActivate)
08h	0001h	Activate Adapter
09h	2B00h	Checksum of 20 bytes

Table 3.1. Reset Configuration Block for Legacy System

This will allow the PnP BIOS or other autoconfiguring components to be aware of the CS8920 installed in the system and the resources used by it. This will help insure other PnP devices are not assigned resources used by the CS8920. See section 3.4 for a discussion on manually configuring the CS8920 using the PnP resource tree.

3.2.2.2 Recommended Reset Configuration Block for a PnP Adapter

The Reset Configuration Block for an adapter installed in a PnP system should not assign an IO base address or activate the adapter from the EEPROM. The exception to this case is when a BootPROM is installed on the adapter. If the CS8920 is a boot device it must be activated from the Reset Configuration Block of the EEPROM after each reset.

Addr	Word	Description
00h	A10Ah	PnP enabled, 10 bytes follow
01h	2158h	3 words, start with PacketPage 158h (IA)
02h	0100h	
03h	0302h	Individual Address of 000102030405h
04h	0504h	
05h	CD00h	Checksum of 12 bytes

Table 3.2. Reset Configuration Block for PnP System

3.2.2.3 PnP with Automatic Wakeup Feature Enabled

The CS8920 can be configured to assert an active-high signal on the EEWAKE pin (pin 3) when a specific bit pattern is detected by its *receiver circuitry*.

This pin can be connected to the system board's power management circuitry. Refer to the *CS8920 Data Sheet* for more information on the operation of the wakeup feature.

To enable the wake-up feature of the CS8920, the CS8920 must be configured to receive frames across the ISA bus from the appropriate LAN media after following a reset. This requires specifying the media type, enabling the receiver, and setting the LineCTL register to enable the wake-up function. Following is an example Reset Configuration Block that would enable the CS8920's wakeup feature.

Addr	Word	Description
00h	A116h	PnP enabled, 22 bytes follow
01h	2158h	3 words, start with PacketPage 158h (IA)
02h	0100h	
03h	0302h	Individual Address of 000102030405h
04h	0504h	
05h	0112h	1 word to PacketPage 122h (LineCTL)
06h	8240h	Wakeup Enable, Detect media, RxOK
07h	0104h	1 word to PacketPage 104h (RxCTL)
08h	0D00h	Accept Rx Broadcast, IA, and OK
09h	011Ch	1 word to PPage 11Ch (AutoNegCTL)
0Ah	0100h	Enable Auto-negotiate
0Bh	BC00h	Checksum of 24 bytes

Table 3.3. Reset Configuration Block for PnP System with Automatic Wakeup Feature

Note: It is not necessary to configure the adapter for the transmission of frames from the Reset Configuration Block. Furthermore, setting the TxOn bit of the TxCTL register during the reset cycle will cause the CS8920 to function improperly.

Typically, transmission is enabled by the MAC driver during its initialization stage.

3.2.2.4 BootPROM Considerations

In all cases, if a BootPROM is installed to the CS8920 adapter, the adapter should be activated from the Reset Configuration Block. In legacy systems, the BootPROMs base address and address mask must also be loaded into PacketPage registers from the Reset Configuration Block as shown in Table 3.4.

Addr	Word	Description
...	...	...
07h	2340	3 words into PacketPage 340h
08h	800Ch	Base Address = 0C8000h
09h	FF00h	Use address lines [23:16], 8-bit device
0Ah	00C0h	Use address lines [15:14]
0Bh	0330h	1 word to PacketPage 330h (RegActivate)
0Ch	0001h	Activate Adapter
0Dh	XX00h	Checksum on 28 bytes

Table 3.4. Configuration of BootPROM from Reset Configuration Block.

If the adapter is installed in a PnP system with an autoconfiguring BIOS, the BootPROM address and mask will be assigned during the PnP configuration sequence and should not be loaded from the Reset Configuration Block.

3.2.2.5 Performance Considerations of Reset Configuration Block

Software resets may occur frequently and performance will be enhanced if chip re-initialization takes as little time as possible. Therefore, since EEPROM readout takes approximately 25 µsec. per word, the length of the Reset Configuration Block should be kept to a minimum.

3.3 Format of the Driver Configuration Block

The region of EEPROM addressed as word addresses 1Ch to 34h is referred to as the Driver Configuration Block. It is used by the MAC driver to determine adapter configuration information such as the unique IEEE physical address , hardware version, media capabilities, and bus configuration (IRQ, DMA, and memory). This region is called the Driver Configuration Block.

Table 3.2 defines the format for the Driver Configuration Block required for use with MAC drivers provided by Crystal. Crystal recommends all fields be initialized to their default values before shipping the adapter. Default values for each field are indicated in sections 3.3.1 through 3.3.13. All reserved fields should be set to zero.

Note: words 30h - 34h are also used as by PnP as the Serial Identifier block for the adapter.

Addr.	Description	Bit(s)	Function
1Ch	IA bits[39-32], bits[47-40]	15-0	IEEE individual node address
1Dh	IA bits[23-16], bits[31-24]	15-0	IEEE individual node address
1Eh	IA bits[7-0], bits[15-8]	15-0	IEEE individual node address
1Fh	ISA Configuration Flags		
	Memory Mode Flag	15	0 = memory mode disabled, 1 = memory mode enabled
	Boot PROM Flag	14	0 = no Boot PROM, 1= Boot PROM installed
	StreamTransfer	13	0 = disabled, 1 = enabled
	DMA Burst	12	0 = disabled, 1 = enabled
	RxDMA Only	11	0 = disabled, 1 = enabled
	Auto RxDMA	10	0 = disabled, 1 = enabled
	DMA Buffer Size	9	0 = 16K, 1 = 64K
	IOCHRDY Enable	8	0 = disabled, 1 = enabled
	Use SA	7	0 = disabled, 1 = enabled
	DMA Channel	6-4	5 = DRQ5, 6 = DRQ6, etc. (same as PP_374) **
	IRQ	3-0	10 = IRQ10, 5 = IRQ5, etc. (same as PP_370) **
20h	PacketPage Mem Base	15-4	12 MSBs of 24-bit address (lower 12 bits assumed = 0)
	Reserved	3-0	Reserved for future use, set to 0
21h	Boot PROM Base	15-4	12 MSBs of 24-bit address (lower 12 bits assumed = 0)
	Reserved	3-0	Reserved for future use, set to 0
22h	Boot PROM Mask	15-4	12 MSBs of 24-bit addr mask (lower 12 bits assumed = 0)
	Reserved	3-0	Reserved for future use, set to 0
23h	AutoNegCTL		
	Force FDX	15	0 = Do not force FDX, 1 = Force FDX
	Reserved	14-10	Reserved for future use, set to 0
	NLP Enable	9	0 = disabled, 1 = enabled
	AutoNeg Enable	8	0 = disabled, 1 = enabled
	Allow FDX	7	0 = disabled, 1 = enabled
	Reserved	6-0	Reserved for future use, set to 0
24h	Adapter Configuration		
	Ext. 10B-2 Cable Circuitry	15	0 = Not Present, 1 = Present
	LoRx Squelch	14	0 = LoRx Squelch disabled, 1 = LoRx Squelch enabled
	PolarityDis	13	0 = polarity correction enabled, 1= polarity correction disabled
	Optimization Flags	12-11	00 = Server, 01 = DOS Client, 10 = Multi-OS Client

	Wake-up Capable	10	0 = Wake-up not supported, 1=Wake-up supported
	Wake-up Configured	9	0 = Not configured for Wake-up, 1 = Configured for Wake-up
	Wake-up Enabled	8	0 = Wake-up Disabled, 1 = Wake-up Enabled (default)
	DC/DC Converter Polarity	7	0 = Low enable, 1 = High enable (for 10Base-2)
	Media Type in Use	6-5	0 = Auto Detect, 1 = 10Base-T, 2 = AUI, 3 = 10Base-2
	Reserved	4	Reserved for future use, set to 0
	HW Standby	3	0 = HW Standby not supported, 1 = HW Standby supported
	10Base-2 Circuitry	2	0 = Not Present, 1 = Present
	AUI Circuitry	1	0 = Not Present, 1 = Present
	10Base-T Circuitry	0	0 = Not Present, 1 = Present
25h	Reserved	15-0	Reserved for future use, set to 0
26h	Reserved	15-0	Reserved for future use, set to 0
27h	Mfg Date		
	Year	15-9	e.g. 1011111b = 1995, 0000001b = 2001
	Month	8-5	e.g. 1b = Jan, 1100b = Dec
	Day	4-0	e.g. 1b = 1, 11111b = 31
28-2Ah	IEEE Individual Addr	47-0	Copy of words at 1C-1Eh
2Bh	Reserved	15-0	Reserved for future use, set to 0
2Ch	Reserved	15-0	Reserved for future use, set to 0
2Dh	Reserved	15-0	Reserved for future use, set to 0
2Eh	Reserved	15-0	Reserved for future use, set to 0
2Fh	Checksum	15-0	Word-wide checksum of words 1Ch to 2Fh (zero sum)
30h	EISA ID (low word)	15-0	EISA ID bits[7-0], EISA ID bits[15-8]
31h	EISA ID (high word)	15-0	EISA ID bits[23-16], EISA ID bits[31-24]
32h	Serial No (low word)	15-0	32-bit OEM assigned serial number, bits[15-8], bits[7-0]
33h	Serial No (high word)	15-0	32-bit OEM assigned serial number, bits[31-24], bits[23-16]
34h	Serial ID Checksum		
	Marker Byte - 0Ah	15-8	0Ah in high byte of checksum - start of PnP resources
	LFSR Checksum	7-0	8-bit LFSR checksum of words 30h to 33h

Table 3.2. Format of EEPROM the Driver Configuration Block (cont.)

3.3.1 IEEE Physical Address

The format of the 48-bit IEEE physical address as expected by the MAC driver is illustrated by the following example. (Must be initialized by OEM before shipping adapter.)

Example physical address:

000102030405h

Addr	Word	Description
1Ch	0100h	bits[39-32], bits[47-40] of IEEE addr.
1Dh	0302h	bits[23-16], bits[31-24] of IEEE addr.
1Eh	0504h	bits[7-0], bits[15-8] of IEEE addr.

3.3.2 ISA Configuration Flags

The ISA Configuration Flags specify how the CS8920 will utilize ISA system resources.

Bit 15: Memory Mode Flag

Indicates the CS8920 will use shared memory for IO operations. Refer to the *CS8920 Data Sheet* for description of shared memory interface. Default is disabled.

Bit 14: Boot PROM Flag

Indicates a Boot PROM is installed. Refer the *CS8920 Data Sheet* for a discussion of the Boot PROM . (Must be initialized by OEM before shipping adapter.)

Bit 13: Reserved (set to 0)

Bit 12: DMA Burst

Refer to the *CS8920 Data Sheet* for a discussion of DMA Burst control. Default is enabled.

Bits 11-10: Reserved (set to 0)

Bit 9: DMA Buffer Size

Indicates whether the DMA buffer size should be 16K or 64K. Refer to the *CS8920 Data Sheet* for a discussion of DMA Buffer size. Default is 16K.

Bit 8: IOCHRDY Enable

Refer to the *CS8920 Data Sheet* for a discussion of IOCHRDY control. Default is enabled.

Bit 7: UseSA

Refer to the *CS8920 Data Sheet* for a discussion of UseSA control. Default is enabled.

Bits 6-4: DMA Channel Select

Refer to the *CS8920 Data Sheet* for a discussion of DMA channel selection for the CS8920. Default is DRQ4 (disabled).

Bits 3-0: IRQ Channel Select

Refer to the *CS8920 Data Sheet* for a discussion of IRQ channel selection for the CS8920. Default is IRQ 10.

3.3.3 PacketPage Memory Base

Bits 15-4: 12 MSB of Memory Base Address

The twelve most significant bits of the 24-bit address locating the base of the CS8920's PacketPage memory. The lower twelve bits are assumed to be 0. Default is 0.

Bits 3-0: Reserved (set to 0)

3.3.4 Boot PROM Memory Base

Bits 15-4: 12 MSB of Memory Base Address

The twelve most significant bits of the 24-bit address locating the base of the CS8920's PacketPage memory. The lower twelve bits are assumed to be 0. Default is 0.

Bits 3-0: Reserved (set to 0)

3.3.5 Boot PROM Mask

Bits 15-4: 12 MSB of Boot PROM Addr. Mask

Twelve-bit Boot PROM address mask. The lower twelve bits are assumed to be 0. Refer to the *CS8920 Data Sheet* for a discussion of the Boot PROM mask. Default is 0.

Bits 3-0: Reserved (set to 0)

3.3.6 Transmission Control

Bit 15: Force Full Duplex

Force transmission in full duplex mode (10Base-T only). Default is disabled.

Bits 14-10: Reserved (set to 0)

Bit 9: NLP Enable

Enable normal link pulses (10Base-T only). In effect, this forces transmission in half duplex mode. Default is disabled.

Bit 8: AutoNeg Enable

Allow the CS8920 to auto-negotiate between full duplex or half duplex if connected to a hub capable of autonegotiation (10Base-T only). Default is enabled.

Bit 7: Allow FDX

Enable full duplex transmission if full duplex capabilities are detected from contents of fast link pulses. Default is enabled.

Bit 6-0: Reserved (set to 0)

3.3.7 Adapter Configuration Word

Bit 15: Extended 10Base-2 Cable Circuitry

Indicates the adapter has the required circuitry to support operation over extended length 10Base-2 cable. Default is not present.

Bit 14: LoRx Squelch

Enable 10Base-T extended range feature (reduce receive squelch threshold). Default is disabled.

Bit 13: Polarity Correction Disable

Enable the CS8920 to automatically correct the polarity of a connected 10Base-T cable. Default is enabled.

Bits 12-11: Optimization Flags

Used to indicate the platform's OS configuration. Each driver configures the CS8920 for optimum performance based on the platform's OS and driver architecture

(NDIS 2X, ODI, NDIS 3X, etc.). Default is DOS (single threaded OS).

Bit 10: Wakeup Capable

Indicates the adapter is capable of supporting the Automatic Wakeup feature. Default is not supported.

Bit 9: Wakeup Configured

Indicates the adapter is configured to support Automatic Wakeup. (Reset block of EEPROM contains proper information to support Automatic Wakeup.) Default is not configured for Automatic Wakeup.

Bit 8: Wakeup Enabled

Indicates the Automatic Wakeup feature is enabled. Default is disabled.

Bit 7: DC to DC Converter Polarity

Refer to Section 2.2.2.9. (Must be initialized by OEM before shipping adapter.)

Bit 6-5: Media Type In Use

Indicates the type of media the driver should use (10Base-T, AUI, 10Base-2) or if driver should auto-detect media in use. Default is auto-detect.

Bit 4: Reserved (set to 0)

Bit 3: Adapter Provides HW Standby Circuitry

Indicates the presence of hardware standby circuitry on the adapter. Refer to Section 3.7 of the *CS8920 Data Sheet*. (Must be initialized by OEM before shipping adapter.)

Bit 2: Adapter Provides 10Base-2 Circuitry

Indicates the presence of 10Base-2 circuitry on the adapter. (Must be initialized by OEM before shipping adapter.)

Bit 1: Adapter Provides AUI Circuitry

Indicates the presence of AUI circuitry on the adapter. (Must be initialized by OEM before shipping adapter.)

Bit 0: Adapter Provides 10Base-T Circuitry

Indicates the presence of 10Base-T circuitry on the adapter. (Must be initialized by OEM before shipping adapter.)

3.3.8 Manufacturing Date

This word is the adapter's manufacture date encoded in 16 bits, YR-MO-DY format. (Must be initialized by OEM before shipping adapter.)

Bits 15-9: Two Least-significant Digits of Year

Seven bits for a range of 00 to 99 decimal. A roll-over to 00 will be interpreted as the year 2000.

Bits 8-5: Month

Four bits for a range of 01 to 12.

Bits 4-0 Day

Five bits for a range of 01 to 31.

3.3.9 IEEE Physical Address (copy)

This field is a copy of the three words at address 1Ch to 1Eh. (Must be initialized by OEM before shipping adapter.)

3.3.10 16-bit Checksum

The checksum stored at the end of the block is the 2's complement of the 16-bit sum of all the preceding words in the Driver Configuration Block. (The drivers access the Configuration Block as 16-bit words.) Any carry out of the 16th bit is ignored. Since this checksum value is calculated as the 2's complement of the sum of all the preceding words in the block, a total of 0 should result when the checksum value is added to the sum of the previous words. (Must be initialized by OEM before shipping adapter.)

3.3.11 EISA ID

The two EISA words make up the 32-bit EISA Product Identification Code.

Low Word

These 16 bits make up the 3-letter identifier string of the OEM's EISA ID in 5-bit compressed ASCII. (A = 00001, B = 00010, C = 00011, etc.)

Bits 7-0: High order 8 bits of 16-bit value

Bits 15-8: Low order 8 bits of 16-bit value

High Word

These 16 bits make up the OEM's product ID No.

The upper order 11 bits are the product ID number and the lower order 5 bits are the revision number.

Bits 7-0: High order 8 bits of 16-bit value

Bits 15-8: Low order 8 bits of 16-bit value

3.3.12 Serial Number

The two serial number words make up the unique 32-bit OEM serial number for the adapter.

Low Word

Bits 7-0: bits[7-0] of 32-bit serial number

Bits 15-8: bits[15-8] of 32-bit serial number

High Word

Bits 7-0: bits[31-24] of 32-bit serial number

Bits 15-8: bits[23-16] of 32-bit serial number

3.3.13 LFSR Checksum

Word 34h contains an 8-bit LFSR checksum calculated on the EISA ID and OEM serial number (words 30h to 33h). The 8-bit LFSR checksum is placed in the low byte of 34h. The high byte is padded with the constant 0Ah.

3.4 Recommended Plug and Play Resource Data

Card resource data stored in the EEPROM starting at word Address 30h is required for the CS8920 to implement Plug and Play operation in accordance with the Microsoft/Intel Plug and Play Specification. This information is used by the PnP BIOS and/or PnP operating system to isolate the CS8920 adapter and attempt to assign conflict-free ISA resources.

3.4.1 Serial Identifier

The Serial Identifier block is used to isolate each individual ISA adapter in the system during the PnP isolation sequence. The Plug and Play ISA Specification defines the Serial Identifier as consisting of a 32-bit Vendor ID in compressed ASCII format (typically the OEM's EISA ID), a 32-bit unique serial number and an 8-bit LFSR checksum calculated on the Vendor ID and serial number. Refer to Section 6.1 of the *Plug and Play ISA Specification 1.0a* for more information on the definition of the Serial Identifier.

The Serial Identifier of each ISA adapter must be unique. It is the responsibility of the OEM to ensure that each adapter using the same Vendor ID (EISA ID) is assigned a unique serial number.

Note: All adapters using Crystal Semiconductor's EISA ID of "CSC" for bytes 0 and 1 of the Vendor ID must set bit 6 of byte three to a 1 and bit 5 of byte three to 0 (i. e., byte 3 must be X10X XXXX where X is a don't care).

Words 30h to 34h defined above in the Driver Configuration Block are also used as the PnP Serial Identifier. Refer to Figure 3.4.1 for an example of the Serial Identifier Block

3.4.2 Resource Descriptors

Immediately following the Serial Identifier are a series of data structures describing the resource requirements of the adapter. The format of this resource data for a typical CS8920 ISA adapter is:

1. Plug and Play version number
2. Identifier String (variable length)
3. Logical Device ID
    - Resource descriptors (as needed)
        - IRQ
        - IO Ports
        - Memory Descriptor 0
        - Memory Descriptor 1
        - DMA Channel
4. End Tag

The identifier string is a variable length string of ASCII characters and is used by the operating system when reporting configuration and error messages.

Following the Identifier String is the Logical Device ID. The Logical Device ID is used by PnP to identify multiple logical devices embedded in a single physical ISA card. However, the CS8920 PnP interface only supports one logical device.

For logical device 0 (the CS8920), a list of resource descriptors specify the ISA resources required by the CS8920 (e.g. DMA channel, IRQ, etc.) along with acceptable values for each resource. The order in which the resource descriptors are listed is not important. Refer to the CS8920 Data Sheet for the acceptable ISA resources for the CS8920.

The PnP configuration process will attempt to reserve and assign available ISA resources for all resource descriptors specified in the resource descriptor list, regardless of whether or not the resource is

utilized by the CS8920 in its current operational mode (e.g., IO mode only -- no shared memory or DMA channel required). Therefore, in order to avoid wasting ISA resources and decrease the likelihood of an unsuccessful autoconfiguration of the CS8920 or other PnP device, the resource descriptor for those resources not used should be omitted from the resource descriptor list.

One exception to this guideline concerns the resource descriptors for the BootPROM (Memory Descriptor 0) and shared memory for memory-mapped access to the PacketPage registers (Memory Descriptor 1). Memory Descriptor 1 will only be processed if Memory Descriptor 0 is defined. Therefore, if shared memory is used (Memory Descriptor 1), a resource descriptor for a BootPROM (Memory Descriptor 0) must be placed in the descriptor list regardless of whether or not a BootPROM is used.

Note: Some PnP BIOSs have been observed to ignore a memory descriptor with a range length of zero bytes. Therefore, to provide compatibility with as many BIOS versions in the field as possible, yet keep the amount of unused memory reserved by PnP to a minimum, Crystal suggests using a 256-byte range length value for Memory Descriptor 0 when a BootPROM is not used but shared memory is requested.

Figure 3.4.1 below is an example PnP resource data record for a CS8920 ISA Ethernet Adapter. This example assumes the CS8920 will use IO space, shared memory, IRQ, DMA, and a BootPROM is installed. The record starts at EEPROM word address 30h.

Refer to Section 6.2 of the *Plug and Play ISA Specification 1.0a* for more information on Plug and Play resource data types.

```
;-------------------------------------------------------------
; Serial Identifier.  This block is also defined in the Driver
; Configuration Block as words 30h to 34h.
;-------------------------------------------------------------
DB      0x0E                ; Vendor ID bits 15-8
DB      0x63                ; Vendor ID bits 7-0
DB      0x00                ; Vendor ID bits 32-24
DB      0x40                ; Vendor ID bits 23-16
DB      0x00                ; Serial Number bits 7-0
DB      0x00                ; Serial Number bits 15-8
DB      0x00                ; Serial Number bits 23-16
DB      0x01                ; Serial Number bits 31-24
DB      LFSR_ChkSum         ; LFSR checksum on 8 preceding bytes

;---------------------------------------------------------------------
; PnP version number
;---------------------------------------------------------------------
DB      0x0A                ; Small Item, PnP version
DB      0x10                ; PnP version number
DB      0x10                ; Vendor specific version number 1.0

;-------------------------------------------------------------
; Identifier String
;-------------------------------------------------------------
DB      0x82            ; Large Item flag
DB      0x17                    ; Bits 7-0 of item's length (fixed at 23 here)
DB      0x00                    ; Bits 15-8 of item's length
DB      "CS8920 Ethernet Adapter"   ;ASCII Identifier string
```

Figure 3.4.1. Example PnP Resource Data Record (part 1 of 4).

```
;-------------------------------------------------------------
; Logical Device ID
;-------------------------------------------------------------
DB      0x15            ; Small Item flag
DB      0x0E            ; Vendor EISA ID Byte 0
DB      0x63            ; Vendor EISA ID Byte 1
DB      0x00            ; Vendor Product ID Byte 0
DB      0x40            ; Vendor Product ID Byte 1
DB      0x03            ; Supports I/O range check, boot device

;-------------------------------------------------------------
; IRQ Format - byte 3 omitted, assume ISA compatible edge sensitive
;-------------------------------------------------------------
DB      0x22            ; Small Item, IRQ format
DB      0xF8            ; Can use IRQ, 3,4,5,6,7
DB      0xDE            ; Can use IRQ 9-12,14,15

;-------------------------------------------------------------
; DMA Format
;-------------------------------------------------------------
DB      0xDE            ; Small Item, DMA format
DB      0xE0            ; DMA Mask, Channels 5,6,7
DB      0x12            ; 16-bit only, execute in count by word mode

;-------------------------------------------------------------
; IO Port Descriptor
;-------------------------------------------------------------
DB      0x47            ; Small Item, IO port descriptor
```

Figure 3.4.1. Example PnP Resource Data Record (part 2 of 4).

```
DB      0x01            ; Decode 16-bit ISA addresses
DB      0x00            ; Bits 7:0 of IO base min address
DB      0x02            ; Bits 15:8 OF IO base min address
DB      0x60            ; Bits 7:0 of IO base max address
DB      0x03            ; Bits 15:8 OF IO base max address
DB      0x10            ; 16 ports needed
DB      0x10            ; IO base paragraph aligned

;------------------------------------------------------------
; Memory Descriptor 0, 16K Boot ROM
;------------------------------------------------------------
DB      0x81            ; Large Item, Memory Descriptor 0
DB      0x09            ; Descriptor length = 9 bytes
DB      0x00
DB      0x40            ; 8-bit ROM, non-shadowable, non-cacheable
DB      0x80
DB      0x0C            ; Min Base Address = 0xC8000
DB      0x00
DB      0x0F            ; Max Base Address = 0xF0000
DB      0x00
DB      0x20            ; Base Alignment
DB      0x40
DB      0x00            ; Range Length

;------------------------------------------------------------
; Memory Descriptor 1 - 4K Shared Memory (RAM)
;------------------------------------------------------------
DB      0x81            ; Large Item, Memory Descriptor 1
DB      0x09            ; Descriptor length = 9 bytes
```

Figure 3.4.1. Example PnP Resource Data Record (part 3 of 4)

```
DB      0x00
DB      0x09            ; 16-bit RAM, non shadowable, non-cacheable
DB      0x00
DB      0x0B            ; Min Base Address = 0xB0000
DB      0xC0
DB      0x0D            ; Max Base Address = 0xDC000
DB      0x00
DB      0x08            ; Base Alignment
DB      0x10
DB      0x00            ; Range Length

;-------------------------------------------------------------
; End Tag and Checksum
;-------------------------------------------------------------
DB      0x79            ; Small Item, End tag
DB      ChkSum          ; 8-bit checksum
```

Figure 3.4.1. Example PnP Resource Data Record (part 4 of 4).

3.5 Programming and Initializing the EEPROM

The contents of the EEPROM may either be pre-programmed in an stand-alone EEPROM programmer or programmed after installation through the CS8920's serial interface.

When programming an EEPROM for the first time via the CS8920's serial interface after the EEPROM has been installed on the adapter, the CS8920's auxiliary key must be used.

On reset, if the Reset Configuration Block's checksum is invalid (typically the case with a new EEPROM installation), the CS8920 performs an EEPROM reset. This reset reloads all of the CS8920's PacketPage registers with their default values, thereby leaving the CS8920 inactive. In this state, all communication with the CS8920 using normal IO is disabled. Further, the CS8920 will no longer respond to the standard PnP initiation key.

However, writing the CS8920-specific auxiliary initiation key to the PnP write-data port after an EEPROM reset will enable the CS8920 to respond to standard PnP commands. The adapter is then configured with an IO base and made active by writing the appropriate commands and data to the PnP write-data port. Once the CS8920 has been made active and the IO base address is assigned via the PnP interface, the EEPROM may be programmed in the usual manner. Refer to the *CS8920 Data Sheet* for more information on programming the EEPROM via the CS8920's serial interface.

WARNING: The CS8920 will respond to the auxiliary key only after an EEPROM reset has occurred. In addition, the CS8920 will not respond to the auxiliary initiation key if the PnP functions of the CS8920 are disabled. Therefore, it is important to ensure that the CS8920 is explicitly activated from the Reset Configuration Block whenever a valid Reset Configuration Block is present and the CS8920's PnP functions are disabled. Failure to do so will make it impossible to communicate with the CS8920 and to re-program the EEPROM without first removing it from the adapter and installing in another adapter or stand-alone EEPROM programming device.

3.5.1 Maintaining EEPROM Configuration Data

Crystal provides two utilities for maintaining the configuration information stored in the EEPROM. One is designed to be used by OEMs to initialize the EEPROM's contents before shipping to the end-user (OEM EEPROM Programming Utility).

The other is a DOS-based Setup and Installation utility run by the end-user at the time the adapter is installed. The Setup and Installation utility allows the end-user to configure the adapter for a specific system. Refer to Section 4.2 for more information on the DOS Setup and Installation utility.

The OEM is left to determine the best procedure for programming EEPROMs

via a stand-alone EEPROM programmer.

3.6 Obtaining IEEE Addresses

Each node of a Local Area Network has a unique address for the media access control (MAC). This makes it possible for that particular node to have unique identity for data communication. This address, known as the IEEE physical address, consists of 48 bits of data. This address is assigned to a LAN physical interface node by the manufacturer of the network interface card.

To ensure uniqueness of the address, 24 bits of out of the 48 bits of the physical address are assigned to the manufacturer by the IEEE standards committee. This 24 bit address is known as Organizationally Unique Identifier (OUI).

The remaining 24 bits of the address are assigned by the manufacturer. For further information and an application for an OUI, please contact the IEEE at the following address:

IEEE Registration Authority,
IEEE Standards Department,
445 Hoes Lane, PO Box 1331
Piscataway, NJ 08855-1331, USA

Telephone: (908) 562-3813
FAX: (908) 562-1571

Adapter boards shipped as part of Crystal's CS8920 Evaluation Kit are programmed with an IEEE Physical Address obtained from an allotment assigned to Crystal Semiconductor Corp. by the IEEE.

4.0 CS8920 Installation and Configuration

This chapter discusses the procedures for installing and configuring the CS8920 adapter and software provided with the CS8920 Evaluation Kit. It is intended to provide the information necessary to install and configure the CS8920 and device driver required in a typical network environment. The procedures required for your particular network may be different.

4.1 CS8920 Evaluation Kit Device Drivers and Software Utilities

The CS8920 Evaluation Kit includes two diskettes containing the following network device drivers and utilities:

- Novell Netware DOS and OS/2 ODI
- Novell 3.1x, 4.x server
- Microsoft Windows 95, Windows NT, and Windows for Workgroups 3.11 (NDIS3.0)
- Microsoft NDIS 2.0.1 drivers for DOS and OS/2 (compatible with many networks including: Windows for Workgroups 3.1, LANtastic, IBM LAN Server, Microsoft LAN Manager)
- Packet Driver V1.09 (for use with TCP/IP protocol stacks, including PC/TCP and SUN PC-NFS). Source code is included.
- SCO UNIX driver and installation script
- DOS-based Setup and Installation Utility
- Universal Boot PROM for Novell Netware and IBM LAN Server.

In addition, an EEPROM Programming Utility for use in OEM manufacturing environments is available from Crystal upon request.

4.1.1 Software Distribution

Diskette 1, labeled "CS8900/CS8920 Setup and Device Driver Software", contains a DOS-based Setup and Installation utility and all of the programs and data files needed to install device drivers for the operating systems listed above except for SCO UNIX. The directory structure of diskette 1 is shown in Figure 4.1.1.

Diskette 2, labeled "CS8900/CS8920 SCO UNIX Driver", is an archive in 'tar' format and includes the files and scripts needed to install the SCO UNIX driver using the SCO UNIX 'custom' command.

In addition, each diskette includes a number of README.TXT files in ASCII text format containing the latest installation information for each driver.

4.1.2 Crystal's Software Licensing Procedures

The CS8920 Evaluation Kit contains a single-user copy of executable network device drivers and utilities. This software is for use for the purpose of internal testing and evaluation only. This software may not be distributed without first signing a LICENSE FOR DISTRIBUTION OF EXECUTABLE

SOFTWARE, which may be obtained by contacting your sales representative. The LICENSE FOR DISTRIBUTION OF EXECUTABLE SOFTWARE gives you unlimited, royalty-free rights to distribute Crystal-provided executable software.

```
root:\
        SETUP.EXE
        README.TXT
        !CS89XX.CFG  {EISA configuration file}
        ARTISOFT\
                ENDS2ISA.DOIS  {NDIS 2 DOS driver}
                ENDS2ISA.OS2   {NDIS 2 OS/2 driver}
                README.TXT
        BOOTPROM\
                README.TXT
        LANSRVR\
                ENDS2ISA.OS2  {NDIS 2 OS/2 driver}
                ENDS2ISA.NIF
                README.TXT
        MSLANMAN.DOS\
                DRIVERS\
                        ETHERNET\
                                ENDS2ISA\
                                        ENDS2ISA.DOS  {NDIS 2 DOS driver}
                                        PROTOCOL.INI
                                        README.TXT
                        NIF\
                                ENDS2ISA.NIF
```

{continued on next page}

Figure 4.1.1. File Structure on Disk (part 1 of 3)

```
root:\
        {continued from previous page}
        MSLANMAN.OS2\
                DRIVERS\
                        ETHERNET\
                                ENDS2ISA\
                                        ENDS2ISA.OS2  {NDIS 2 OS/2 driver}
                                        PROTOCOL.INI
                                        README.TXT
                        NIF\
                                ENDS2ISA.NIF
        NETWARE\
                CLIENT\
                        DOSODI\
                                EODIISA.COM  {ODI DOS driver}
                                EODIISA.INS
                                NET.CFG
                                README.TXT
                        OS2ODI\
                                EODIISA.SYS  {ODI OS/2 driver}
                                README.TXT
                SERVER\
                        NW3.12\
                                EODIISA.LAN {Server driver}
                                EODIISA.LDI
                                README.TXT
                        NW4.X\
                                EODIISA.LAN  {Server driver}
                                EODIISA.LDI
                                README.TXT
                                 {continued on next page}
```

Figure 4.1.1. File Structure on Disk (part 2 of 3)

```
root:\
        {continued from previous page}
        PCNFS\
                ENDS2ISA.DOS  {NDIS 2 DOS driver}
                README.TXT
        PKTDRVR\
                EPKTISA.COM  {Packet driver}
                README.TXT
                SOURCE.ZIP
        WFW3.1\
                ENDS2ISA.DOS  {NDIS 2 DOS driver}
                PROTOCOL.INI
                OEMSETUP.INF
                README.TXT
        WFW3.11\
                ENDS3ISA.386  {NDIS 3 DOS driver}
                EODIISA.COM  {ODI DOS driver for Netware client}
                OEMSETUP.INF
                README.TXT
        WINNT\
                DISK1
                ENDS3ISA.SYS  {NDIS 3 driver}
                OEMSETUP.INF
                README.TXT
        WIN95\
                DISK1
                ENDS3ISA.VXD  {NDIS 3 driver}
                ENDS3ISA.INF
                README.TXT
```

Figure 4.1.1. File Structure on Disk (part 3 of 3)

4.2 Adapter Installation and Configuration

The installation and configuration of the CS8920 for most network operating systems is accomplished by performing the following four steps:

1. **Install the CS8920 adapter**
   Install the adapter in an available ISA/EISA slot and connect the appropriate type cable.
2. **Configure the adapter**
   Select the desired hardware settings and store them in EEPROM using the DOS-based Setup and Installation utility.
3. **Test the adapter's operation**
   Using the Setup and Installation utility's diagnostic option, test the operation of the adapter with the chosen hardware configuration.
4. **Install the appropriate device driver**
   Install the device driver that provides the interface between the CS8920 adapter and your network operating system.

Note: The installation procedure for installing the CS8920 with SCO UNIX differs from the procedure discussed in this section. Please refer to the README.TXT file (ASCII text format) on the "CS8900/CS8920 SCO UNIX Driver" diskette for the correct installation of the CS8920 under SCO UNIX operating system.

4.2.1 Installing the CS8920 Adapter

The CS8920 adapter may be installed in any available 16-bit ISA or EISA slot. Be sure to connect a network cable before running the provided Setup and Installation Utility or loading a network device driver.

More than one CS8920 may be installed in the same PC, limited only by the number of available slots in the PC, available system resources, and the limitations of the network operating system you will be using. Refer to the README.TXT file in the root directory of the "CS8900/CS8920 Setup and Device Driver Software" diskette for installation considerations when installing more than one CS8920 adapter in the same PC.

4.2.2 Configuring the CS8920 Adapter

The provided DOS-based Setup and Installation utility is used to configure the CS8920 adapter card. It allows the user to select the system resources to the CS8920 adapter such as an interrupt number, DMA channel, IO base address, and memory base address. Once selected, the specified hardware configuration is stored in the CS8920's EEPROM. There are no jumpers or switches on the adapter board used to specify the hardware configuration.

To configure the CS8920 adapter using the Setup and Installation utility:

1) Install the CS8920-based adapter card into the PC. The adapter must be installed before running the Setup and Installation utility.
2) Boot the PC. If the PC is already running and network device drivers are loaded, restart the PC without loading the network device drivers.
3) Place the "CS8900/CS8920 Setup and Device Driver Software" diskette in a floppy drive and change to that drive.
4) At the DOS prompt, type: SETUP The CS8920's current configuration is displayed. Hit the RETURN key to get to the main menu.
5) Select "Adapter" (ALT-A) from the main menu. Then select "Automatic Setup" or "Manual Setup". Automatic Setup suggests a set of system resources to use for the hardware configuration. Manual Setup lets you select and assign individual system resources.

Additional information on using the Setup and Installation Utility can be found in the README.TXT file in the root directory of the "CS8900/CS8920 Setup and Device Driver Software" diskette.

4.2.2.1 EISA System Installation

An EISA configuration file is provided in the root directory of the "CS8900/CS8920 Setup and Device Driver Software" diskette named !CS89XX.CFG.

Run the EISA configuration utility provided with your EISA PC and enter the path to the !CS89XX.CFG file when prompted. The utility will determine the system resource assignments available for that system. (Write down the available resource settings). Next, run the CS8920 Setup and Installation utility and assign the hardware configuration using the system resources reported by the EISA configuration utility.

4.2.3 Testing the CS8920 Adapter

Once the adapter has been installed and configured, the diagnostic option of the Setup and Installation utility can be used to test the functionality of the adapter and the network connection. Use the Diagnostics "Self Test" option to test the functionality of the adapter with the hardware configuration you have assigned. You can use the diagnostics "Network Test" to test the ability of the adapter to communicate across the Ethernet with another PC equipped with a CS8920 adapter card (it must also be running the Setup and Installation utility).

To run the diagnostics tests on the CS8920 adapter:

1) Boot the PC. If the PC is already running and network device drivers are loaded, restart the PC without loading the network device drivers.
2) Place the "CS8900/CS8920 Setup and Device Driver Software" diskette in a driver and change to that drive.
3) At the DOS prompt, type: SETUP The CS8920's current configuration is displayed. Hit the RETURN key to get to the main menu.

4) Select "Diagnostics" (ALT-G) from the main menu.
   - Select "Self-Test" to test the adapter's basic functionality.
   - Select "Network Test" to test the network connection and cabling.

4.2.3.1 Diagnostic Self-Test

The diagnostic self-test checks the adapter's basic functionality as well as its ability to communicate across the ISA bus based on the system resources assigned during hardware configuration. The following tests are performed:

- **IO Register Read/Write Test**
  The IO Register Read/Write test insures that the CS8920 can be accessed in IO mode, and that the IO base address is correct.
- **Shared Memory Test**
  The Shared Memory test insures the CS8920 can be accessed in memory mode and that the range of memory addresses assigned does not conflict with other devices in the system.
- **Interrupt Test**
  The Interrupt test insures there are no conflicts with the assigned IRQ signal.
- **DMA Channel Test**
  The DMA channel test insures there are no conflicts with the assigned DMA channel.
- **EEPROM Test**
  The EEPROM test insures the EEPROM can be read.
- **Chip RAM Test**
  The Chip RAM test insures the 4K of memory internal to the CS8920 is working properly.
- **Internal Loop-back Test**
  The Internal Loop Back test insures the adapter's transmitter and receiver are operating properly. If this test fails, make sure the card is properly attached to the network (check for LED activity for example).
- **Boot PROM Test**
  The Boot PROM test insures the Boot PROM is present and can be read. Failure indicates the Boot PROM was not successfully read due to a hardware problem or due to a conflicts on the Boot PROM address assignment. (Test only applies if the adapter is configured to use the Boot PROM option.)

Failure of a test item indicates a possible system resource conflict with another device on the ISA bus. In this case, you should use the Manual Setup option to reconfigure the adapter by selecting a different value for the system resource that failed (see section 4.2.2).

4.2.3.2 Diagnostics Network Test

The Diagnostic Network Test verifies a working network connection by transferring data between two CS8920 adapters installed in different PCs on the same network. (Note: the diagnostic network test should not be run between two nodes across a router.)

This test requires that each of the two PCs have a CS8920 card installed and

have the network test running. The first PC is configured as a Responder and the other PC is configured as an Initiator. Once the Initiator is started, is sends data frames to the Responder which returns the frames to the Initiator.

The total number of frames received and transmitted are displayed on the Initiator's display, along with a count of the number of frames received/transmitted OK in error. The test can be terminated anytime by the user at either PC.

To setup the Diagnostic Network Test:

1. Select a PC with a CS8920 and a known working network connection to act as the Responder. Run the Setup and Installation utility and select "Diagnostics/Network Test/Responder" from the main menu. Hit RETURN to start the Responder.

2. Return to the PC with the CS8920 installed that you want to test, run the Setup and Installation utility, and select "Diagnostic/Network Test/Initiator" from the main menu. Hit RETURN to start the test

You may stop the test on the Initiator at any time while allowing the Responder to continue running. In this manner, you can move to additional PCs and test them by starting the Initiator on another PC without having to stop/start the Responder.

4.2.4 Installing Network Device Drivers

A network device driver is required to provide an interface between the CS8920 adapter and your network operating system. Installation procedures for network device drivers differ significantly for the various network operating systems and can change frequently. Therefore,

a README.TXT file for each specific driver is included on the Driver diskette.

Refer to the README.TXT file for your particular network operating system for the most recent detailed installation instructions. (A separate README.TXT file exists for each network operating system and is located in the same subdirectory on the Driver diskette as the device driver for that operating system. See Figure 4.2.1).

5.0 Contacting Customer Support at Crystal

Crystal Semiconductor is committed to providing the industry's most easily implemented Ethernet solution. We invite you to contact us for assistance at any time during the design process. Our Application Engineering department offers free schematic and layout review services and provides software support for Crystal's network drivers. Let Crystal's application engineers help you confirm the optimum design for your specific application.

To contact Crystal Application Engineering, call **(800) 888-5016** (from the US and Canada) or **512-442-7555** (from outside the US and Canada), and ask for CS8920 Application Support, or send an email to: ethernet@crystal.cirrus.com.

5.1 Crystal BBS

Crystal also offers free updates to the of the network driver software using the Crystal Semiconductor BBS (Bulletin Board System).

5.1.1 Connecting to the BBS

Access to the bulletin board system is available 24 hours a day, 7 days a week. Baud rates from 300 to 14.4K are supported as well as LAPM/MNP error control and compression. To access the BBS:

1. Set your terminal software for 8-bits, no parity, and 1 stop bit (8-N-1).

2. Dial (512) 441-3265**.**

3. Type **<RETURN>** after connection is made.

4. Enter your assigned username at the prompt. If you are not a registered user, enter "guest" (without quotes). The username is **not** case sensitive.

5. If you are a registered user, enter your assigned password when prompted. You have the option to change your password on-line after your initial logon. Note: Passwords should consist of 3 to 8 alphanumeric characters and are case sensitive.

5.1.2 Guests

If you are a guest caller, you will be asked to fill out a short questionnaire consisting of your full name, company name, the city and state you are calling from, and a daytime phone number. Once the questionnaire is completed, you will be able to download files from the Public File Area.

5.1.3 Registered Callers

Registered callers can upload or download files to/from their own private file areas as well as download files from the Public File Area. To access your private file area select option 5, "Enter Your Private File Area", from the main menu.

Only you and the BBS system operator (sysop) can access your private file area. Files you upload to your private file area will be scanned and passed on to the appropriate Crystal applications engineer.

6.0 Index

1

10BASE-2 • 9, 10

10BASE-T • 9, 10, 19, 32, 33, 34, 35

A

address • 6, 10, 60, 62

AUI • 9, 10, 32, 34, 35

B

BBS • *See* Bulletin Board System

Boot PROM • 6, 8, 62

Bulletin Board System • 64

C

capacitor

bypass • 20, 22

CMC • *See* common mode

Combo Card • 23

common mode • 34

crystal • *See* oscillator

crystal oscillator • 9

Customer Support • 64

D

Diagnostics/Network Test • 62

DMA • 6, 60, 62

DOS • 6, 8, 55, 57, 58, 59, 60

E

EEPROM • 6, 7, 10, 55, 62

Embedded Systems • 9

EMI • 20, 34

F

FCC part 15 • 9

filters • 9, 34

G

ground trace • 32

I

I/O mode • 9

IEEE • 6, 10

IRQ • 62

ISA bus • 6, 7, 9, 32

L

LED • 10, 62

Loop Back test • 62

M

memory

extended • 10

lower • 9

shared • 62

upper • 9

memory mode • 9

Motherboards • 9

N

NDIS • 8, 55, 57, 58, 59

NET.CFG • 58

NETWARE • 58

Novell • 8, 55

O

ODI • 8, 55, 58

OEM • 55
OS/2 • 8, 57, 58

P

Packet Driver V1.09 • 55
PAL • 9
printed circuit board
four-layer • 9, 22, 27, 28, 29, 30
multi layer • 22
printed circuit card
two layered • 22, 32
PROTOCOL.INI • 57

R

RAM • 62
README.TXT • 57, 58, 59
resistor • 32
RJ-45 • 32

S

SCO UNIX • 8, 55
Software Licensing • 55

T

transformer • 10, 32, 34, 35

W

Windows • 8, 55