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CS8413
CS8414

96 kHz Digital Audio Receiver

Features

- Sample Rates to >100 kHz
- Low-Jitter, On-Chip Clock Recovery 256xFs Output clock Provided
- Supports: AES/EBU, IEC 958, S/PDIF, & EIAJ CP340/1201 Professional and Consumer Formats
- Extensive Error Reporting Repeat Last Sample on Error Option
- On-Chip RS422 Line Receiver
- Configurable Buffer Memory (CS8413)
- Pin Compatible with CS8411 and CS8412

Description

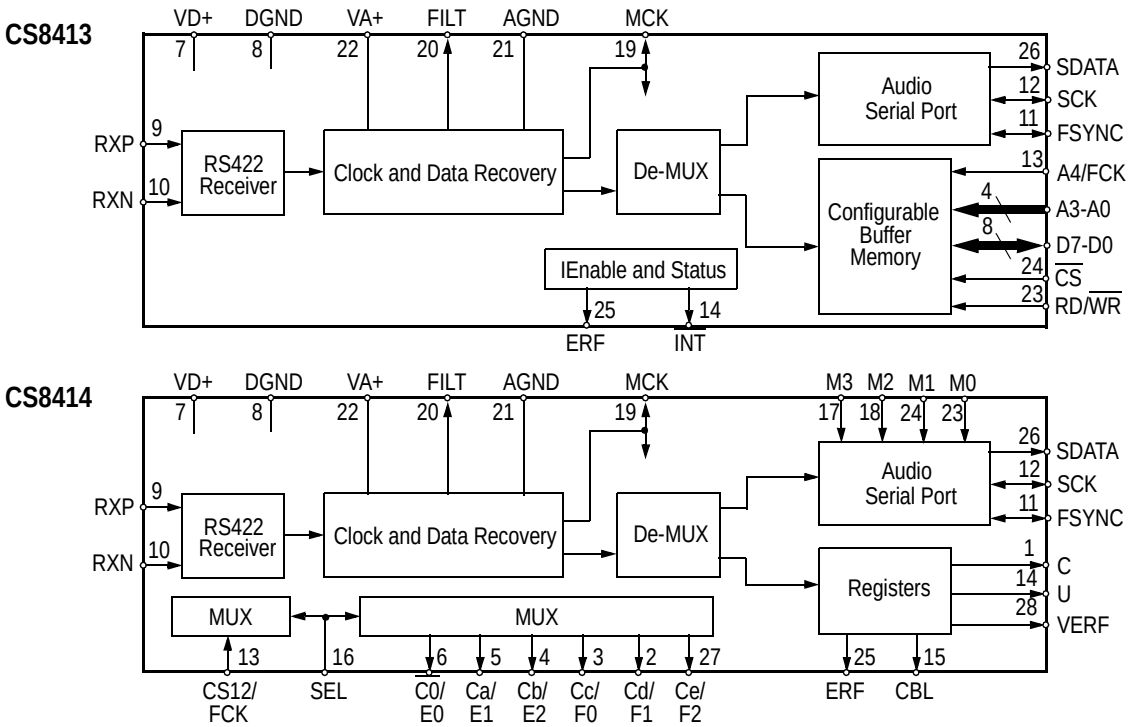
The CS8413 and CS8414 are monolithic CMOS devices which receive and decode audio data up to 96kHz according to the AES/EBU, IEC958, S/PDIF, and EIAJ CP340/1201 interface standards. The CS8413 and CS8414 receive data from a transmission line, recover the clock and synchronization signals, and de-multiplex the audio and digital data. Differential or single ended inputs can be decoded.

The CS8413 has a configurable internal buffer memory, read through a parallel port, which may be used to buffer channel status, auxiliary data, and/or user data.

The CS8414 de-multiplexes the channel, user, and validity data directly to serial output pins with dedicated output pins for the most important channel status bits.

ORDERING INFORMATION

CS8413-CS	0° to 70° C	28-pin Plastic SOIC
CS8414-CS	0° to 70° C	28-pin Plastic SOIC



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CHARACTERISTICS/SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (GND = 0V, all voltages with respect to ground)

Parameters	Symbol	Min	Max	Units
Power Supply Voltage	VD+, VA+	-	6.0	V
Input Current, Any Pin Except Supply (Note 1)	I_{in}	-	±10	mA
Input Voltage, Any Pin Except RXP, RXN	V_{IN}	-0.3	(VD+) + 0.3	V
Input Voltage, RXP and RXN	V_{IN}	-12	12	V
Ambient Operating Temperature (power applied)	T_A	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

Notes: 1. Transient currents of up to 100 mA will not cause SCR latch-up

RECOMMENDED OPERATING CONDITIONS (GND = 0V, all voltages with respect to ground)

Parameters	Symbol	Min	Typ	Max	Units
Power Supply Voltage	VD+, VA+	4.75	5.0	5.25	V
Supply Current VA+	I_A	-	20	30	mA
VD+	I_D	-	20	30	mA
Ambient Operating Temperature: (Note 2)	T_A	0	25	70	°C
Power Consumption	P_D	-	175	315	mW

Notes: 2. The '-CS' parts are specified to operate over 0 to 70 °C but are tested at 25 °C only.

DIGITAL CHARACTERISTICS (T_A = 25 °C; VD+, VA+ = 5V ± 5%)

Parameters	Symbol	Min	Typ	Max	Units
High-Level Input Voltage except RXP, RXN	V_{IH}	2.0	-	-	V
Low-Level Input Voltage except RXP, RXN	V_{IL}	-	-	+0.4	V
High-Level Output Voltage (I_O = 200 µA)	V_{OH}	(VD+) - 1.0	-	-	V
Low-Level Output Voltage (I_O = -3.2 mA)	V_{OL}	-	-	0.5	V
Input Leakage Current	I_{in}	-	1.0	10	µA
Input Sample Frequency: (Note 3)	F_S	28.4	-	100	kHz
Master Clock Frequency (Note 3)	MCK	7.28	256xF_S	25.6	MHz
MCK Clock Jitter	t_j	-	200	-	psRMS
MCK Duty Cycle (high time/cycle time)		-	50	-	%

Notes: 3. F_S is defined as the incoming audio sample frequency per channel.

DIGITAL CHARACTERISTICS - RS422 RECEIVERS

(RXP, RXN pins only; VD+, VA+ = 5V ± 5%)

Parameters			Symbol	Min	Typ	Max	Units
Input Resistance	(-7V < V_{CM} < 7V)	(Note 4)	Z_{IN}	-	10	-	kΩ
Differential Input Voltage, RXP to RXN	(-7V < V_{CM} < 7V)	(Notes 4 and 5)	V_{TH}	200	-	-	mV
Input Hysteresis			V_{HYST}	-	50	-	mV

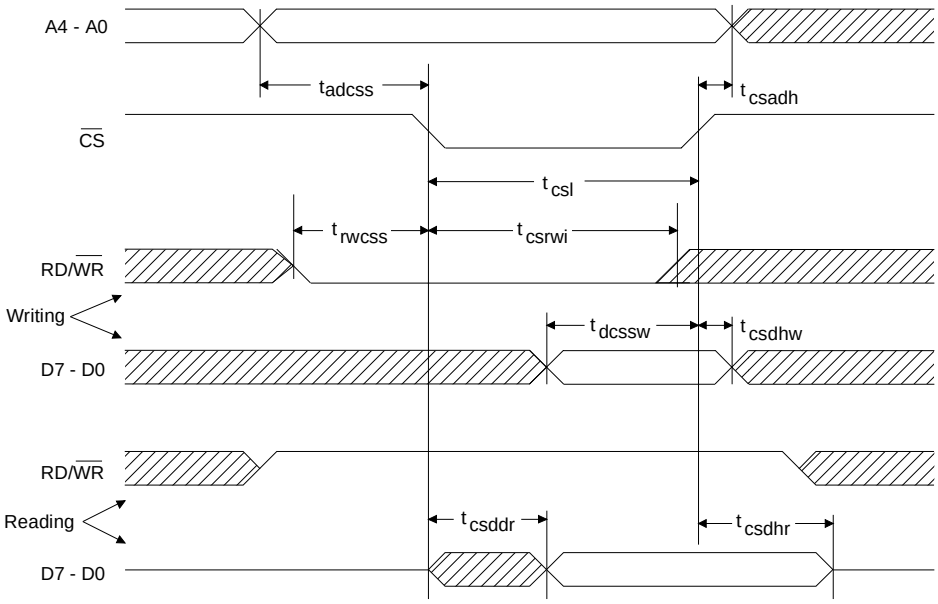
Notes: 4. V_{CM} - Input Common Mode Range

5. When the receiver inputs are configured for single ended operation (e.g. consumer configuration) the signal amplitude must exceed 400 mVp-p for the differential voltage on RXP to RXN to exceed 200 mV. This represents twice the minimum signal level of 200 mVp-p specified in CP340/1201 and IEC-958 (which are not RS-422 compliant).

SWITCHING CHARACTERISTICS - CS8413 PARALLEL PORT

(T_A = 25 °C;VD+, VA+ = 5V ± 5%; Inputs: Logic 0 = DGND, Logic 1 = VD+; C_L = 20 pF)

Parameters		Symbol	Min	Typ	Max	Units
ADDRESS valid to $\overline{CS}$ low		t_{adcss}	13.5	-	-	ns
$\overline{CS}$ high to ADDRESS invalid		t_{csadh}	0	-	-	ns
RD/$\overline{WR}$ valid to $\overline{CS}$ low		t_{rwcss}	10	-	-	ns
$\overline{CS}$ low to RD/$\overline{WR}$ invalid		t_{csrwi}	35	-	-	ns
$\overline{CS}$ low		t_{csl}	35	-	-	ns
DATA valid to $\overline{CS}$ rising	RD/$\overline{WR}$ low (writing)	t_{dcssw}	32	-	-	ns
$\overline{CS}$ high to DATA invalid	RD/$\overline{WR}$ low (writing)	t_{csdhw}	0	-	-	ns
$\overline{CS}$ falling to DATA valid	RD/$\overline{WR}$ high (reading)	t_{csddr}	-	-	35	ns
$\overline{CS}$ rising to DATA Hi-Z	RD/$\overline{WR}$ high (reading)	t_{csdhr}	5	-	-	ns



CS8413 Parallel Port timing

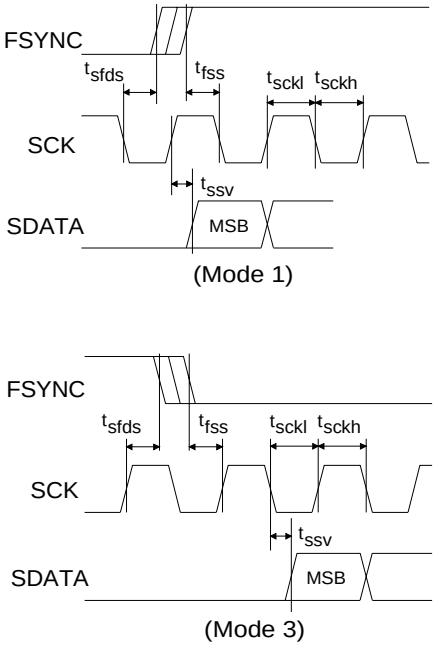
SWITCHING CHARACTERISTICS - SERIAL PORTS

(T_A = 25 °C; VD+, VA+ = 5V ± 5%; Inputs: Logic 0 = DGND, Logic 1 = VD+; C_L = 20 pF)

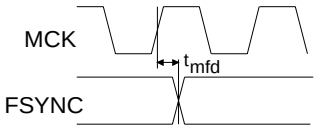
Parameters			Symbol	Min	Typ	Max	Units
SCK Frequency	Master Mode	(Notes 6 and 7)	f_{sck}	-	OWRx32	-	Hz
	Slave Mode	(Note 7)		OWRx32	-	128 x F_S	Hz
SCK falling to FSYNC delay	Master Mode	(Notes 7 and 8)	t_{sfdm}	-20	-	20	ns
SCK Pulse Width Low	Slave Mode	(Note 7)	t_{sckl}	40	-	-	ns
SCK Pulse Width High	Slave Mode	(Note 7)	t_{sckh}	40	-	-	ns
SCK rising to FSYNC edge delay	Slave Mode	(Notes 7 and 8)	t_{sfds}	20	-	-	ns
FSYNC edge to SCK rising setup	Slave Mode	(Notes 7 and 8)	t_{fss}	20	-	-	ns
SCK falling (rising) to SDATA valid		(Note 8)	t_{ssv}	-	-	20	ns
C, U, CBL valid to FSYNC edge	CS8414	(Note 8)	t_{cuvf}	-	$1/f_{sck}$	-	s
MCK to FSYNC edge delay	FSYNC from RXN/RXP		t_{mfd}	-	15	-	ns

Notes:

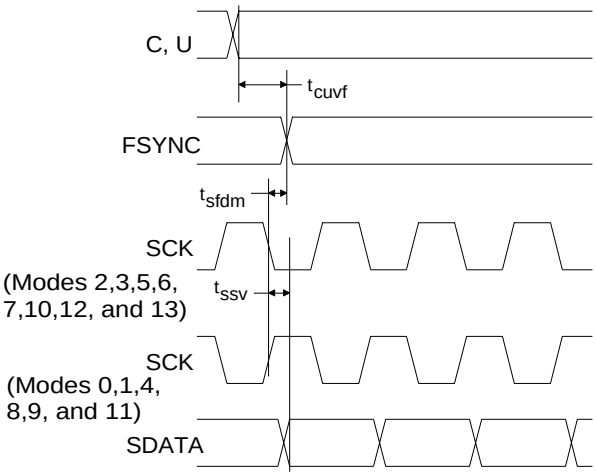
6. The output word rate, OWR, refers to the frequency at which an audio sample is output from the part. (A stereo pair is two audio samples.) Therefore, in Master mode, there are always 32 SCK periods in one audio sample. In Slave mode, exactly 32 SCK periods per audio sample must be provided in most serial port formats. Therefor, if SCK is 128 x Fs, then SCK must be gated to provide exactly 32 periods per audio sample.
7. In Master mode, SCK and FSYNC are outputs. In Slave mode, they are inputs. In the CS8413, control reg. 2 bit 1, MSTR, selects master. In the CS8414, formats 1, 3 and 9 are slaves.
8. The table above assumes data is output on the falling edge and latched on the rising edge. With the CS8413 the edge is selectable. The table is defined for the CS8413 with control reg. 2 bit 0, SCED, set to one, and for the CS8414 in formats 2, 3, 5, 6 and 7. For the other formats, the table and figure edges must be reversed (i.e. “rising” to “falling” and vice versa.)



Serial Output Timing - Slave Mode



FSYNC Generated From Received Data



Serial Output Timing - Master Mode & C, U Port

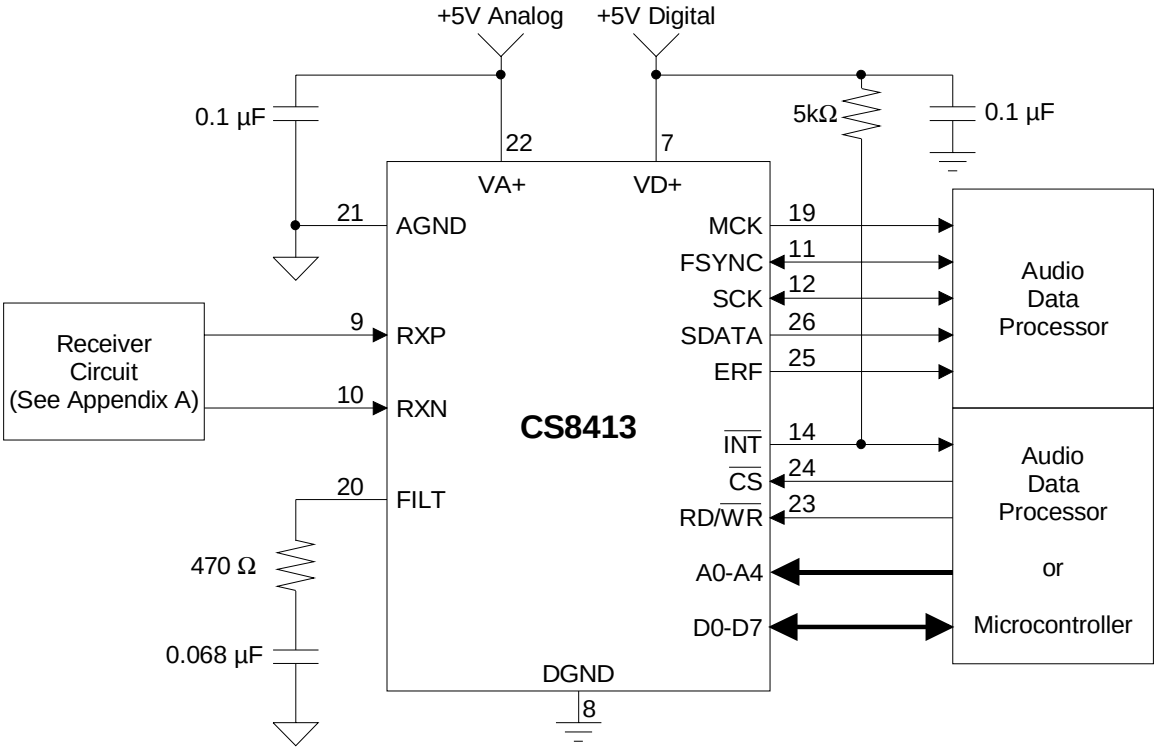


Figure 1. CS8413 Typical Connection Diagram

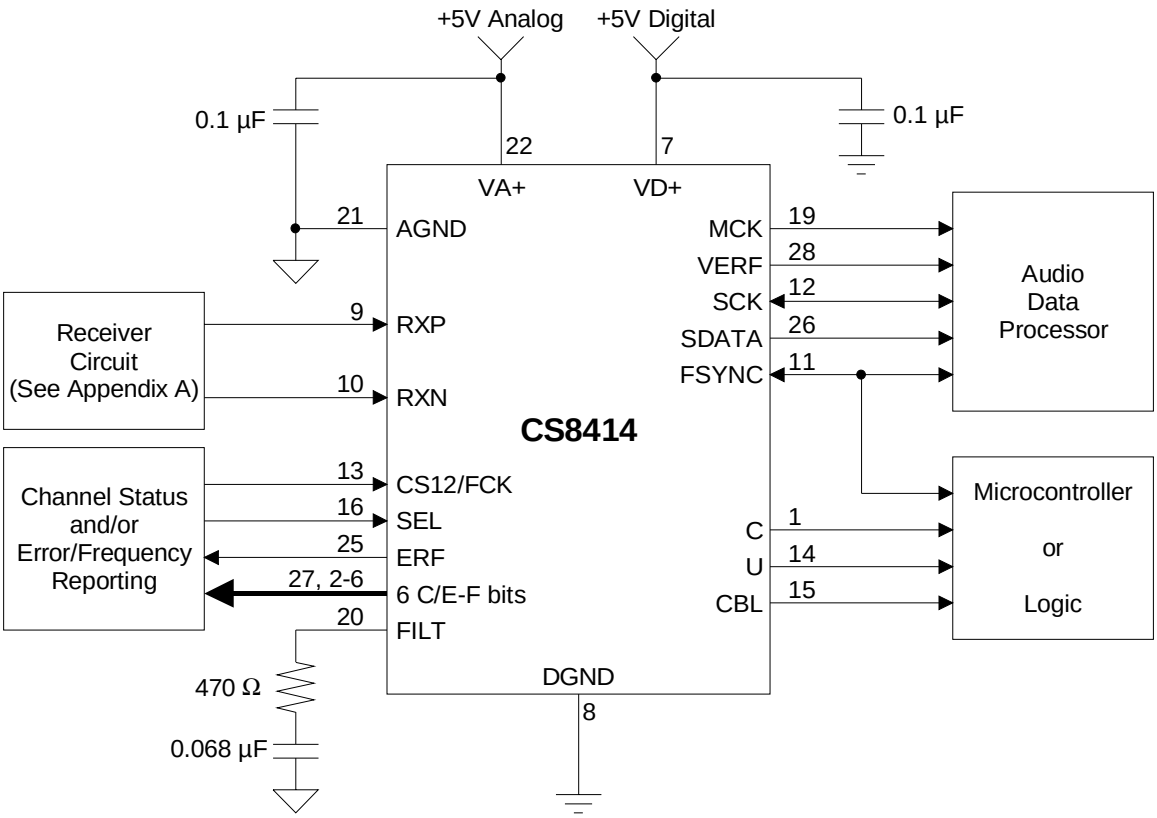


Figure 2. CS8414 Typical Connection Diagram

GENERAL DESCRIPTION

The CS8413/14 are monolithic CMOS circuits that receive and decode audio and digital data according to the AES/EBU, IEC 958, S/PDIF, and EIAJ CP340/1201 interface standards. Both chips contain RS422 line receivers and Phase-Locked Loops (PLL) that recover the clock and synchronization signals, and de-multiplex the audio and digital data. The CS8413 contains a configurable internal buffer memory, read via a parallel port, which can buffer channel status, user, and optionally auxiliary data. The CS8414 de-multiplexes the channel status, user, and validity information directly to serial output pins with dedicated pins for the most important channel status bits. Both chips also contain extensive error reporting as well as incoming sample frequency indication for auto-set applications.

The CS8413/14 are pin-compatible with the CS8411/12 digital audio receiver parts. The functionality of the CS8413/14 is the same as the CS8411/12 with two exceptions: first, the operating frequency (sample rate) of the CS8413/14 is extended to include 96 kHz, and second, the frequency reporting bits are modified to delete the ±400 ppm ranges, and include 88.2 kHz and 96 kHz ranges.

Familiarity with the AES/EBU and IEC 958 specifications are assumed throughout this document. The App Note, Overview of Digital Audio Interface Data Structures, contains information on digital audio specifications; however, it is not meant to be a complete reference. To guarantee compliance, the proper standards documents should be obtained. The AES/EBU standard, AES3-1985, should be obtained from the Audio Engineering Society or ANSI (ANSI document # ANSI S4.40-1985); the IEC 958 standard from the International Electrotechnical Commission; and the EIAJ CP340/1201 standard from the Japanese Electronics Bureau.

Line Receiver

The RS422 line receiver can decode differential as well as single ended inputs. The receiver consists of a differential input Schmitt trigger with 50mV of hysteresis. The hysteresis prevents noisy signals from corrupting the phase detector. Appendix A contains more information on how to configure the line receivers for differential and single ended signals.

Clocks and Jitter Attenuation

The primary function of these chips is to recover audio data and low jitter clocks from a digital audio transmission line. The clocks that can be generated are MCK ($256xF_S$), SCK ($64xF_S$), and FSYNC (F_S or $2xF_S$). MCK is the output of the voltage controlled oscillator which is a component of the PLL. The PLL consists of phase and frequency detectors, a second-order loop filter, and a voltage controlled oscillator. All components of the PLL are on chip with the exception of a resistor and capacitor used in the loop filter. This filter is connected between the FILT pin and AGND. The typical closed-loop transfer function, which specifies the PLL's jitter attenuation characteristics, is shown in Figure 3. Most jitter introduced by the transmission line is high in frequency and will be strongly attenuated.

Multiple frequency detectors are used to minimize the time it takes the PLL to lock to the incoming data stream and to prevent false lock conditions. When the PLL is not locked to the incoming data stream, the frequency detectors pull the VCO frequency within the lock range of the PLL. When no digital audio data is present, the VCO frequency is pulled to its minimum value.

As a master, SCK is always MCK divided by four, producing a frequency of $64xF_S$. In the CS8413, FSYNC can be programmed to be a divided version of MCK or it can be generated directly from the incoming data stream. In the CS8414, FSYNC is always generated from the incoming data stream. When FSYNC is generated from the data, its edges

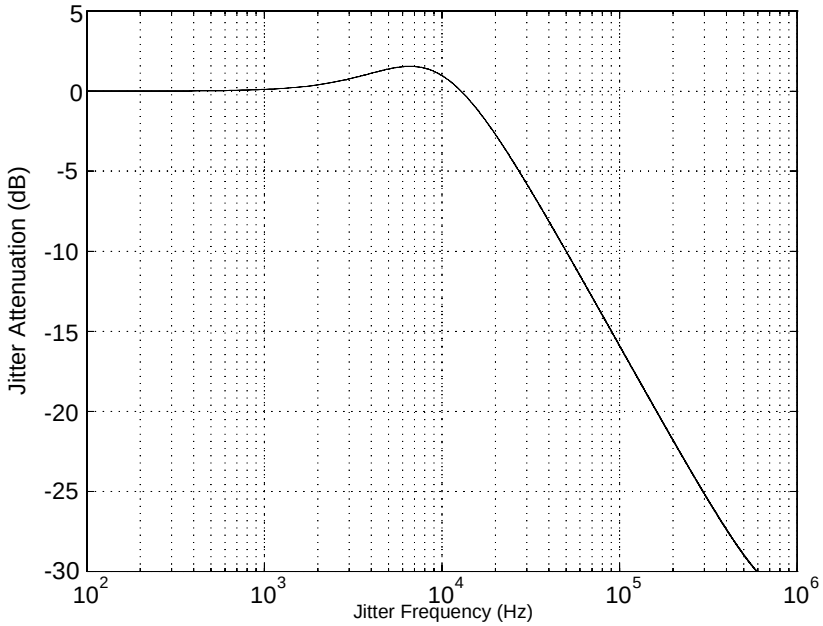


Figure 3. Typical Jitter Attenuation Characteristics

are extracted at times when intersymbol interference is at a minimum. This provides a sample frequency clock that is as spectrally pure as the digital audio source clock for moderate length transmission lines. For long transmission lines, the CS8413 can be programmed to generate FSYNC from MCK instead of from the incoming data.

CS8413 DESCRIPTION

The CS8413 is more flexible than the CS8414 but requires a microcontroller or DSP to load internal registers. The CS8414 does not have internal registers so it may be used in a stand-alone mode where a microprocessor or DSP is not available.

The CS8413 accepts data from a transmission line coded according to the digital audio interface standards. The I.C. recovers clocks and data, and separates the audio data from control information. The audio data is output through a configurable serial port and the control information is stored in internal dual-port RAM. Extensive error reporting is available via internal registers with the option of repeating the last sample when an error occurs. A block diagram of the CS8413 is shown in Figure 4

Parallel Port

The parallel port accesses two status registers, two interrupt enable registers, two control registers, and 28 bytes of dual-port buffer memory. The status registers and interrupt enable registers occupy the same address space. A bit in control register 1 selects the two registers, either status or interrupt enable, that occupy addresses 0 and 1 in the memory map. The address bus and the RD/$\overline{WR}$ line should be valid when $\overline{CS}$ goes low. If RD/$\overline{WR}$ is low, the value on the data bus will be written into the buffer memory at the specified address. If RD/$\overline{WR}$ is high, the value in the buffer memory, at the specified address, is placed on the data bus. Detailed timing for the parallel port can be found in the *Switching Characteristics - Parallel Port table*.

The memory space on the CS8413 is allocated as shown in Figure 5. There are three defined buffer modes selectable by two bits in control register 1. Further information on the buffer modes can be found in the *Control Registers section.*

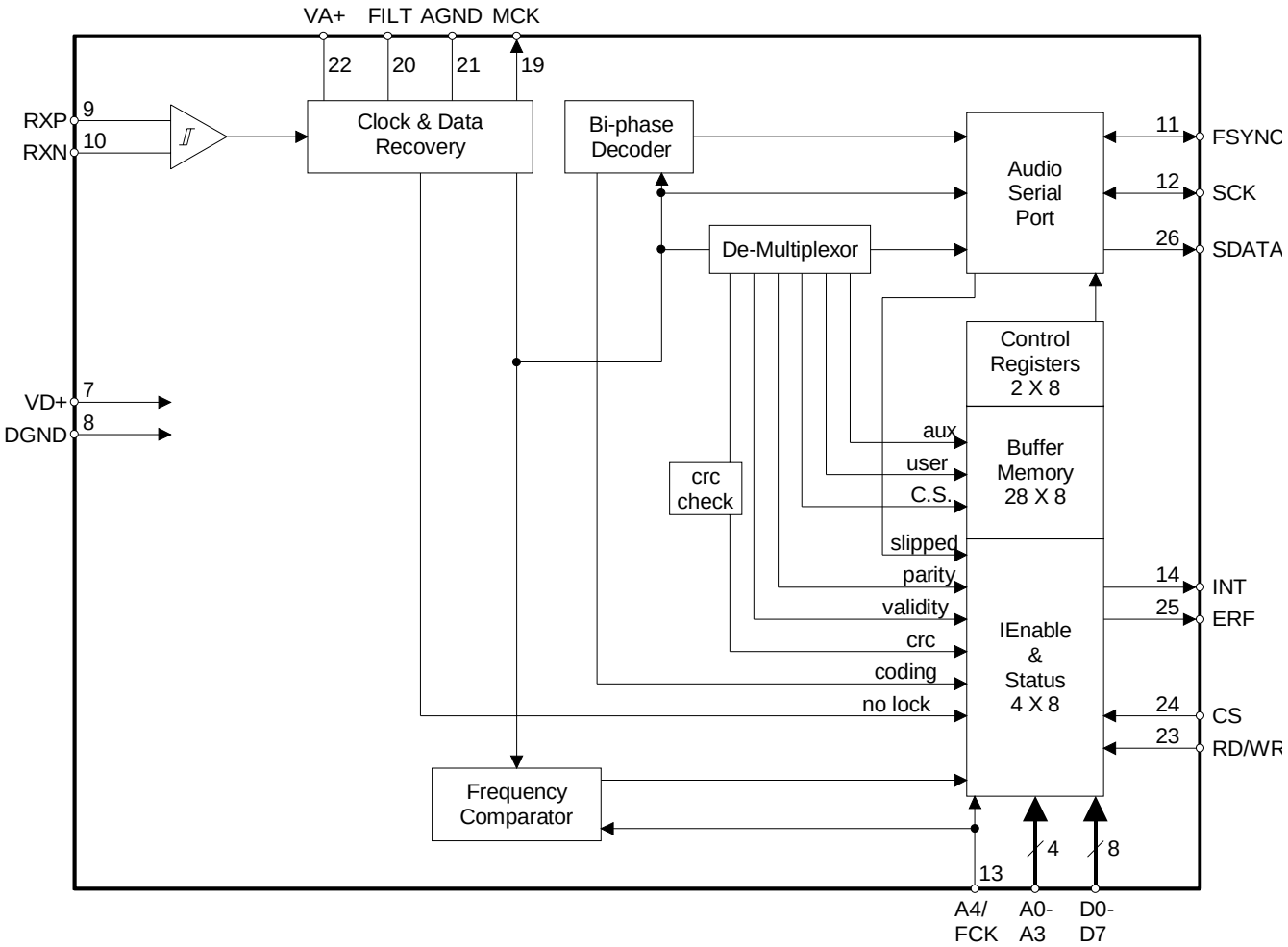


Figure 4. CS8413 Block Diagram

Status and IEnable Registers

The status and interrupt enable registers occupy the same address space. The IER/$\overline{SR}$ bit in control register 1 selects whether the status registers (IER/$\overline{SR}$ = 0) or the IEnable registers (IER/$\overline{SR}$ = 1) occupy addresses 0 and 1. Upon power-up, the control and IEnable registers contain all zeros; therefore, the status registers are visible and all interrupts are disabled. The IER/$\overline{SR}$ bit must be set to make the IEnable registers visible.

Status register 1 (SR1), shown in Figure 6, reports all the conditions that can generate a low pulse four SCLK cycles wide on the interrupt pin ($\overline{INT}$). The three least significant bits, FLAG2-FLAG0, are used to monitor the ram buffer. These bits continually change and indicate the position of the buffer pointer which points to the buffer memory location currently being written. Each flag has a corresponding interrupt enable bit in IEnable register 1 which, when set, allows a transition on the flag to generate a pulse on the interrupt pin. FLAG0 and FLAG1 cause interrupts on both edges whereas FLAG2 causes an interrupt on the rising edge only. Further information, including timing, on the flags can be found in the *Buffer Memory* section.

The next five bits; ERF, SLIP, CCHG, CRCE/CRC1, and CSDIF/CRC2, are latches which are set when their corresponding conditions occur, and are reset when SR1 is read. Interrupt

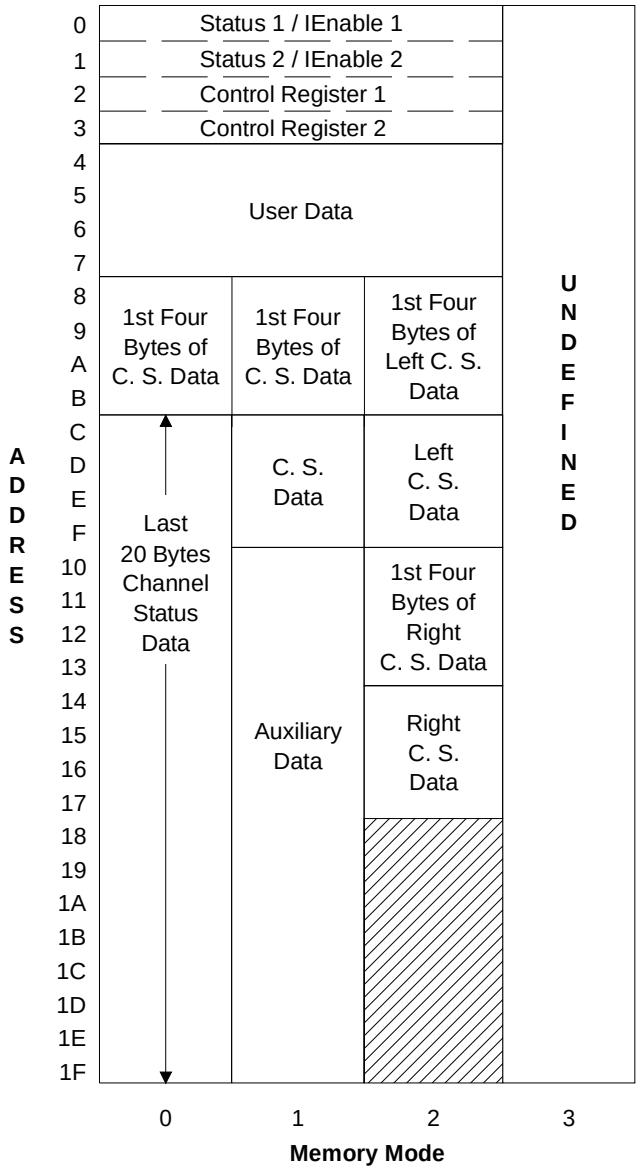


Figure 5. CS8413 Buffer Memory Map

pulses are generated the first time that condition occurs. If the status register is not read, further instances of that same condition will not generate another interrupt. ERF is the error flag bit and is set when the ERF pin goes high. It is an OR'ing of the errors listed in status register 2, bits 0 through 4, AND'ed with their associated interrupt enable bits in IEnable register 2.

SLIP is only valid when the audio port is in slave mode (FSYNC and SCK are inputs to the CS8413). This flag is set when an audio sample is dropped or

X:00	7	6	5	4	3	2	1	0
SR1.	CSDIF/ CRC2	CRCE/ CRC1	CCHG	SLIP	ERF	FLAG2	FLAG1	FLAG0
IER1.	← INTERRUPT ENABLE BITS FOR ABOVE →							

SR1: CSDIF: CS different between sub-frames. Buffer modes 0 & 1
CRC2: CRC Error - sub-frame 2. Buffer mode 2 only.
CRCE: CRC Error - selected sub-frame. Buffer modes 0 & 1
CRC1: CRC Error - sub-frame 1. Buffer mode 2 only.
CCHG: Channel Status changed
SLIP: Slipped an audio sample
ERF: Error Flag. ORing of all errors in SR2.
FLAG2: High for first four bytes of channel status
FLAG1: Memory mode dependent - See Figure 11.
FLAG0: High for last two bytes of user data.

IER1: Enables the corresponding bit in SR1.
A "1" enables the interrupt. A "0" masks the interrupt.

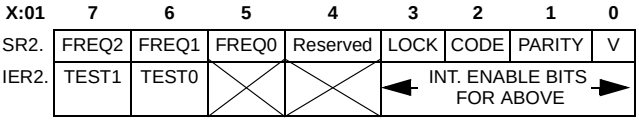
Figure 6. Status/IEnable Register 1

reread because the audio data output from the part is at a different frequency than the data received from the transmission line. CCHG is set when any bit in channel status bytes 0 through 3, stored in the buffer, changes from one block to the next. In buffer modes 0 and 1, only one channel of channel status data is buffered, so CCHG is only affected by that channel. (CS2/$\overline{CS1}$ in CR1 selects which channel is buffered.) In buffer mode 2 both channels are buffered, so both channels affect CCHG. This bit is updated after each byte (0 to 3) is written to the buffer. The two most significant bits in SR1, CRCE/CRC1 and CSDIF/CRC2, are dual function flags. In buffer modes 0 and 1, they are CRCE and CSDIF, and in buffer mode 2, they are CRC1 and CRC2. In buffer modes 0 and 1, the channel selected by the CS2/$\overline{CS1}$ bit is stored in RAM and CRCE indicates that a CRC error occurred in that channel. CSDIF is set if there is any difference between the channel status bits of each channel. In buffer mode 2 channel status from both channels is buffered, with CRC1 indicating a CRC error in channel 1 and CRC2 indicating a CRC error in channel 2. CRCE, CRC1, and CRC2 are updated at the block boundary. Block boundary violations also cause CRC1,2 or CRCE to be set.

IEnable register 1, which occupies the same address space as status register 1, contains interrupt enable bits for all conditions in status register 1. A "1" in a bit location enables the same bit location in

status register 1 to generate an interrupt pulse. A "0" masks that particular status bit from causing an interrupt.

Status register 2 (SR2) reports all the conditions that can affect the error flag bit in SR1 and the error pin (ERF), and can specify the received clock frequency. As previously mentioned, the first five bits of SR2 are AND'ed with their interrupt enable bits (in IER2) and then OR'ed to create ERF. The V, PARITY, CODE and LOCK bits are latches which are set when their corresponding conditions occur, and are reset when SR2 is read. The ERF pin is asserted each time the error occurs assuming the interrupt enable bit in IER2 is set for that particular error. When the ERF pin is asserted, the ERF bit in SR1 is set. If the ERF bit was not set prior to the ERF pin assertion, an interrupt will be generated (assuming bit 3 in IER1 is set). Although the ERF pin is asserted for each occurrence of an enabled error condition, the ERF bit will only cause an interrupt once if SR1 is not read.



SR2: FREQ2: The 3 FREQ bits indicate incoming sample frequency.
FREQ1: (must have 6.144 MHz clock on FCK pin and FCEN
FREQ0: must be "1")
LOCK: Out-of-Lock error
CODE: Coding violation
PARITY: Parity error
V: Validity bit high

IER2: TEST1,0: (0 on power-up) Must stay at "0".
INT. ENABLES: Enables the corresponding bit in SR2.
A "1" enables the interrupt. A "0" masks the interrupt.

Figure 7. Status/IEnable Register 2

V is the validity status bit which is set any time the received validity bit is high. PARITY is set when a parity error is detected. CODE is set when a biphase coding error is detected. LOCK is asserted when the receiver PLL is not locked and occurs when there is no input on RXP/RXN, or if the received frequency is out of the receiver lock range (28.4 kHz to 100 kHz).

The upper three bits in SR2, FREQ2-FREQ0, can report the receiver frequency when the receiver is locked. These bits are only valid when FCEN in control register 1 is set, and a 6.144 MHz clock is applied to the FCK pin. When FCEN is set, the A4/FCK pin is used as FCK and A4 is internally set to zero; therefore, only the lower half of the buffer can be accessed. Table 1 lists the frequency ranges reported. The FREQ bits are updated three times per block and the clock on the FCK pin must be valid for two thirds of a block for the FREQ bits to be accurate. The FREQ bits are invalid when the PLL is out of lock.

FREQ2	FREQ1	FREQ0	Sample Frequency
0	0	0	Out of Range
0	0	1	reserved
0	1	0	reserved
0	1	1	96 kHz ± 4%
1	0	0	88.2 kHz ± 4%
1	0	1	48 kHz ± 4%
1	1	0	44.1 kHz ± 4%
1	1	1	32 kHz ± 4%

Table 1. Incoming Sample Frequency Bits

IEnable register 2 has corresponding interrupt enable bits for the first five bits in SR2. A "1" enables the condition in SR2 to cause ERF to go high, while a "0" masks that condition. Bit 5 is unused and bits 6 and 7, the two most significant bits, are factory test bits and must be set to zero when writing to this register. The CS8413 sets these bits to zero on power-up.

Control Registers

The CS8413 contains two control registers. Control register 1 (CR1), at address 2, selects system level features, while control register 2 (CR2), at address 3, configures the audio serial port.

In control register 1, when $\overline{\text{RST}}$ is low, all outputs are reset except MCK (FSYNC and SCLK are high impedance). The CS8413 should be reset imediately after power-up and any time the user performs a

system-wide reset. After the user sets $\overline{RST}$ high, the CS8413 comes fully out of reset when the block boundary is found. The serial port, in master mode, will begin to operate as soon as $\overline{RST}$ goes high. B0 and B1 select one of three buffer modes listed in Table and illustrated in Figure 5. In all modes four bytes of user data are stored. In mode 0, one entire block of channel status is stored. In mode 1 eight bytes of channel status and sixteen bytes of auxiliary data are stored. In mode 2, eight bytes of channel status from each sub-frame are stored. The buffer modes are discussed in more detail in the *Buffer Memory* section. The next bit, CS2/$\overline{CS1}$, selects the particular sub-frame of channel status to buffer in modes 0 and 1, and has no effect in mode 2. When CS2/$\overline{CS1}$ is low, sub-frame 1 is buffered, and when CS2/$\overline{CS1}$ is high, sub-frame 2 is buffered. IER/$\overline{SR}$ selects which set of registers, either IEnable or status, occupy addresses 0 and 1. When IER/$\overline{SR}$ is low, the status registers occupy the first two addresses, and when IER/$\overline{SR}$ is high, the IEnable registers occupy those addresses. FCEN enables the internal frequency counter. A 6.144 MHz clock must be connected to the FCK pin as a reference. The value of the FREQ bits in SR2 are not valid until two thirds of a block of data is received. Since FCK and A4, the most significant address bit, occupy the same pin, A4 is internally set to zero when FCEN is high. Since A4 is forced to zero, the upper half of the buffer is not accessible while using the frequency compare feature. FPLL determines how FSYNC is derived. When FPLL is low, FSYNC is derived from the incoming data, and when FPLL is high, it is derived from the internal phase-locked loop.

Control Register 2 configures the serial port which consists of three pins: SCK, SDATA, and FSYNC. SDATA is always an output, but SCK and FSYNC can be configured as inputs or outputs. FSYNC and SDATA can have a variety of relationships to each other, and the polarity of SCK can be controlled. The large variety of audio data formats provides an easy interface to most DSPs and other audio processors. SDATA is normally just audio data, but special modes are provided that output received biphase data, or received NRZ data with zeros substituted for preamble. Another special mode allows an asynchronous SCK input to read audio data from the serial port without slipping samples. In this mode FSYNC and SDATA are outputs synchronized to the SCK input. Since SCK is asynchronous to the received clock, the number of SCK cycles between FSYNC edges will vary.

B1	B0	Mode	Buffer Memory Contents
0	0	0	Channel Status
0	1	1	Auxiliary Data
1	0	2	Independent Channel Status
1	1	3	Reserved

Table 2. Buffer Memory Modes

X:02	7	6	5	4	3	2	1	0
CR1.	FPLL	FCEN	IER/$\overline{SR}$	CS2/$\overline{CS1}$	B1	B0		$\overline{RST}$

CR1:
- FPLL: 0 - FSYNC from RXP/RXN, 1 - FSYNC from PLL
- FCEN: enables freq. comparator (FCK must be 6.144 MHz).
- IER/$\overline{SR}$: [X:00,01] 0 - status, 1 - interrupt enable registers.
- CS2/$\overline{CS1}$: ch. status to buffer; 0 - sub-frame 1, 1 - sub-frame 2.
- B1: with B0, selects the buffer memory mode.
- B0: with B1, selects the buffer memory mode.
- $\overline{RST}$: Resets internal counters. Set to "1" for normal operation.

Figure 8. Control Register 1

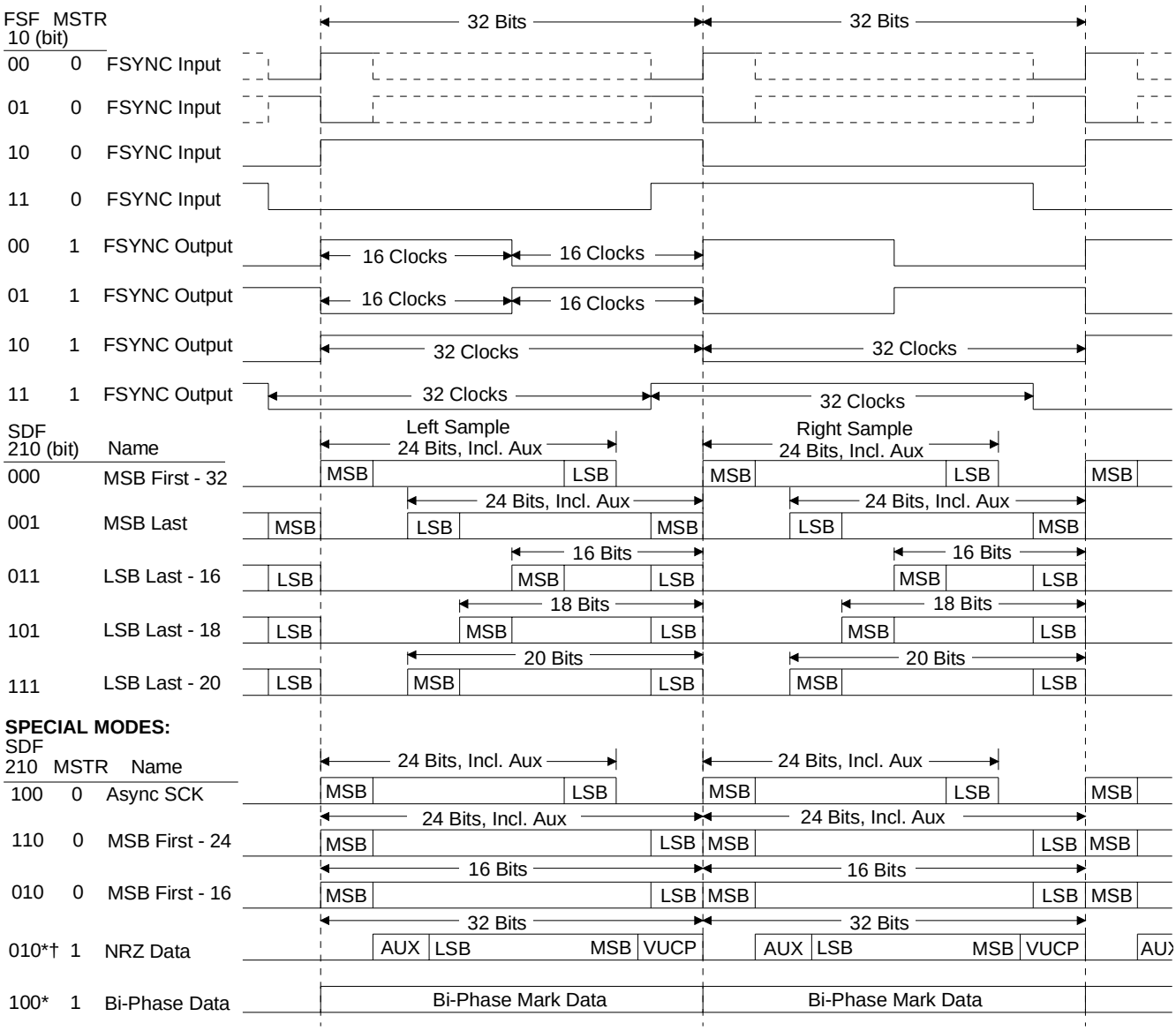
X:03	7	6	5	4	3	2	1	0
CR2.	ROER	SDF2	SDF1	SDF0	FSF1	FSF0	MSTR	SCED

CR2:
- ROER: Repeat previous value on error (audio data)
- SDF2: with SDF0 & SDF1, select serial data format.
- SDF1: with SDF0 & SDF2, select serial data format.
- SDF0: with SDF1 & SDF2, select serial data format.
- FSF1: with FSF0, select FSYNC format.
- FSF0: with FSF1, select FSYNC format.
- MSTR: When set, SCK and FSYNC are output
- SCED: When set, falling edge of SCK outputs data. When clear, rising edge of SCK outputs data.

Figure 9. Control Register 2

ROER, when set, causes the last audio sample to be reread if the error pin, ERF, is active. When out of lock, the CS8413 will output zeros if ROER is set

and output random data if ROER is not set. The conditions that activate ERF are those reported in SR2 and enabled in IER2. Figure 10 illustrates the modes selectable by SDF2-SDF0 and FSF1-FSF0. MSTR, which in most applications will be set to one, determines whether FSYNC and SCK are outputs (MSTR = 1) or inputs (MSTR = 0). When FSYNC and SCK are inputs (slave mode) the audio data can be read twice or missed if the device controlling FSYNC and SCK is on a different timebase than the CS8413. If the audio data is read twice or missed, the SLIP bit in SR1 is set. SCED selects the SCK edge to output data on. SCED high causes data to be output on the falling edge, and SCED low causes data to be output on the rising edge.



* Error flags are not accurate in these modes

† FSYNC is inverted FSF = 11

Figure 10. CS8413 Serial Port SDATA and FSYNC Timing

Audio Serial Port

The audio serial port outputs the audio data portion from the received data and consists of three pins: SCK, SDATA, and FSYNC. SCK clocks the data out on the SDATA line. The edge that SCK uses to output data is programmable from CR2. FSYNC delineates the audio samples and may indicate the particular channel, left or right. Figure 10 illustrates the multitude of formats that SDATA and FSYNC can take.

Normal Modes

SCK and FSYNC can be inputs (MSTR = 0) or outputs (MSTR = 1), and are usually programmed as outputs. As outputs, SCK contains 32 periods for each sample and FSYNC has four formats. The first two output formats of FSYNC (shown in Figure 10) delineate each word and the identification of the particular channel must be kept track of externally. This may be done using the rising edge of FLAG2 to indicate the next data word is left channel data. The last two output formats of FSYNC also delineate each channel with the polarity of FSYNC indicating the particular channel. The last format has FSYNC change one SCK cycle before the frame containing the data and may be used to generate an I^2S compatible interface.

When SCK is programmed as an input, 32 SCK cycles per sample must be provided. (There are two formats in the *Special Modes* section where SCK can have 16 or 24 clocks per sample.) The four modes where FSYNC is an input are similar to the FSYNC output modes. The first two require a transition of FSYNC to start the sample frame, whereas the last two are identical to the corresponding FSYNC output modes. If the circuit generating SCK and FSYNC is not locked to the master clock of the CS8413, the serial port will eventually be reread or a sample will be missed. When this occurs, the SLIP bit in SR1 will be set.

SDATA can take on five formats in the normal serial port modes. The first format (see Figure 10), MSB First, has the MSB aligned with the start of a sample frame. Twenty-four audio bits are output including the auxiliary bits. This mode is compatible with many DSPs. If the auxiliary bits are used for something other than audio data, they must be masked off. The second format, MSB Last, outputs data LSB first with the MSB aligned to the end of the sample frame. This format is conducive to serial arithmetic. Both of the above formats output all audio bits from the received data. The last three formats are LSB Last formats that output the most significant 16, 18, and 20 bits respectively, with the LSB aligned to the end of the sample frame. These formats are used by many interpolation filters.

Special Modes

Five special modes are included for unique applications. In these modes, the master bit, MSTR, must be defined as shown in Figure 10. In the first mode, Asynchronous SCK, FSYNC (which is an output in this mode) is aligned to the incoming SCK. This mode is useful when the SCK is locked to an external event and cannot be derived from MCK. Since SCK is asynchronous, the number of SCK cycles per sample frame will vary. The data output will be MSB first, 24 bits, and aligned to the beginning of a sample frame. The second and third special modes are unique in that they contain 24 and 16 SCK cycles respectively per sample frame, whereas all normal modes contain 32 SCK cycles. In these two modes, the data is MSB first and fills the entire frame. The fourth special mode outputs NRZ data including the V, U, C, and P bits and the preamble replaced with zeros. SCK is an output with 32 SCK cycles per sample frame. The fifth mode outputs the biphase data recovered from the transmission line with 64 SCK cycles output per sample frame, with data changing on the rising edge.

Normally, data recovered by the CS8413 is delayed by two frames in propagating through the part, but

in the fourth and fifth special modes, the data is delayed only a few bit periods before being output. However, error codes, and the C, U and V bits follow the normal pathway with a two frame delay (so that the error code would be output with the offending data in the other modes). As a result, in special modes four and five, the error codes are nearly two frames behind the data output on SDATA.

Buffer Memory

In all buffer modes, the status, mask, and control registers are located at addresses 0-3, and the user data is buffered at locations 4 through 7. The parallel port can access any location in the user data buffer at any time; however, care should be taken not to read a location when that location is being updated internally. This internal writing is done through a second port of the buffer and is done in a cyclic manner. As data is received, the bits are assembled in an internal 8-bit shift register which, when full, is loaded into the buffer memory. The first bit received is stored in D0 and, after D7 is received, the byte is written into the proper buffer memory location.

The user data is received one bit per sub-frame. At the channel status block boundary, the internal pointer for writing user data is initialized to 04H (Hex). After receiving eight user bits, the byte is written to the address indicated by the user pointer which is then incremented to point to the next address. After receiving all four bytes of user data, 32 audio samples, the user pointer is set to 04H again and the cycle repeats. FLAG0, in SR1 can be used to monitor the user data buffer. When the last byte of the user buffer, location 07H, is written, FLAG0 is set low and when the second byte, location 05H, is written, FLAG0 is set high. If the corresponding bit in the interrupt enable register (IER1, bit 0) is set, a transition of FLAG0 will generate a low pulse on the interrupt pin. The level of FLAG0 indicates which two bytes the part will write next, thereby indicating which two bytes are free to be read.

FLAG1 is buffer mode dependent and is discussed in the individual buffer mode sections. A transition of FLAG1 will generate an interrupt if the appropriate interrupt enable bit is set.

FLAG2 is set high after channel status byte 23, the last byte of the block, is written and set low after channel status byte 3 is written to the buffer memory. FLAG2 is unique in that only the rising edge can cause an interrupt if the appropriate interrupt enable bit in IER1 is set.

Figure 11 illustrates the flag timing for an entire channel status block which includes 24 bytes of channel status data per channel and 384 audio samples. The lower portion of Figure 11 expands the first byte of channel status showing eight pairs of data, with a pair defined as a frame. This is further expanded showing the first sub-frame (A0) to contain 32 bits defined as per the digital audio standards. When receiving stereo, channel A is left and channel B is right.

For all three buffer modes, the three most significant bits in SR1, shown in Figure 6, can be used to monitor the channel status data. In buffer mode 2, bits 7 and 6 change definition and are described in that section. Channel status data, as described in the standards, is independent for each channel. Each channel contains its own block of channel status data, and in most systems, both channels will contain the same channel status data. Buffer modes 0 and 1 operate on one block of channel status with the particular block selected by the CS2/$\overline{CS1}$ bit in CR1. CSDIF, bit 7 in SR1, indicates when the channel status data for each channel is not the same even though only one channel is being buffered. CRCE, bit 6 in SR1, indicates a CRC error occurred in the buffered channel. CCHG, bit 5 in SR1, is set when any bit in the buffered channel status bytes 0 to 3, change from one block to the next.

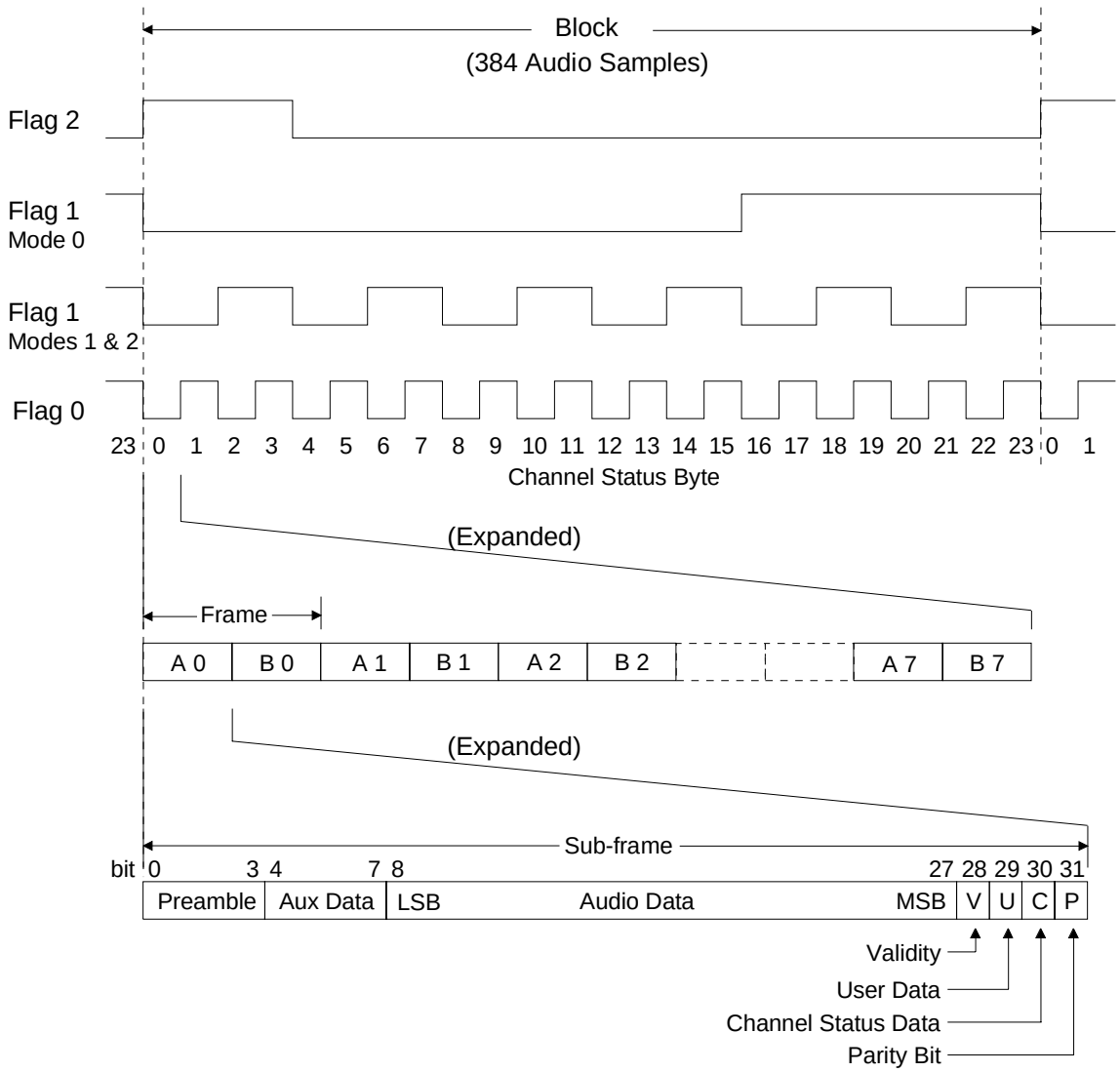


Figure 11. CS8413 Status Register Flag Timing

Buffer Mode 0

The user data buffer previously described is identical for all modes. Buffer mode 0 allocates the rest of the buffer to channel status data. This mode stores an entire block of channel status in 24 memory locations from address 08H to 1FH. Channel status (CS) data is different from user data in that channel status data is independent for each channel. A block of CS data is defined as one bit per frame, not one bit per sub-frame; therefore, there are two blocks of channel status. The CS2/$\overline{CS1}$ bit in CR1 selects which channel is stored in the buffer. In a typical system sending stereo data, the channel status data for each channel would be identical.

FLAG1 in status register 1, SR1, can be used to monitor the channel status buffer. In mode 0, FLAG1 is set low after channel status byte 23 (the last byte) is written, and is set high when channel status byte 15, location 17H is written. If the corresponding interrupt enable bit in IER1 is set, a transition of FLAG1 will generate a pulse on the interrupt pin. Figure 12 illustrates the memory write sequence for buffer mode 0 along with flag timing. The arrows on the flag timing indicate when an interrupt will occur if the appropriate interrupt enable bit is set. FLAG0 can cause an interrupt on either edge, which is only shown in the expanded portion of the figure for clarity.

Buffer Mode 1

In buffer mode 1, eight bytes are allocated for channel status data and sixteen bytes for auxiliary data as shown in Figure 5. The user data buffer is the same for all modes. The channel status buffer, locations 08H to 0FH, is divided into two sections. The first four locations always contain the first four bytes of channel status, identical to mode 0, and are written once per channel status block. The second four locations, addresses 0CH to 0FH, provide a cyclic buffer for the last 20 bytes of channel status data. The channel status buffer is divided in this fashion because the first four bytes are the most important ones; whereas, the last 20 bytes are often not used (except for byte 23, CRC).

FLAG1 and FLAG2 can be used to monitor this buffer as shown in Figure 13. FLAG1 is set high when CS byte 1, location 09H, is written and is toggled when every other byte is written. FLAG2 is set high after CS byte 23 is written and set low after CS byte 3, location 0BH, is written. FLAG2 determines whether the channel status pointer is writing to the first four-byte section of the channel status buffer or the second four-byte section, while FLAG1 indicates which two bytes of the section are free to update.

The auxiliary data buffer, locations 10H to 1FH, is written to in a cyclic manner similar to the other buffers. Four auxiliary data bits are received per audio sample (sub-frame) and, since the auxiliary data is four times larger than the user data, the auxiliary data buffer on the CS8413 is four times larger allowing FLAG0 to be used to monitor both.

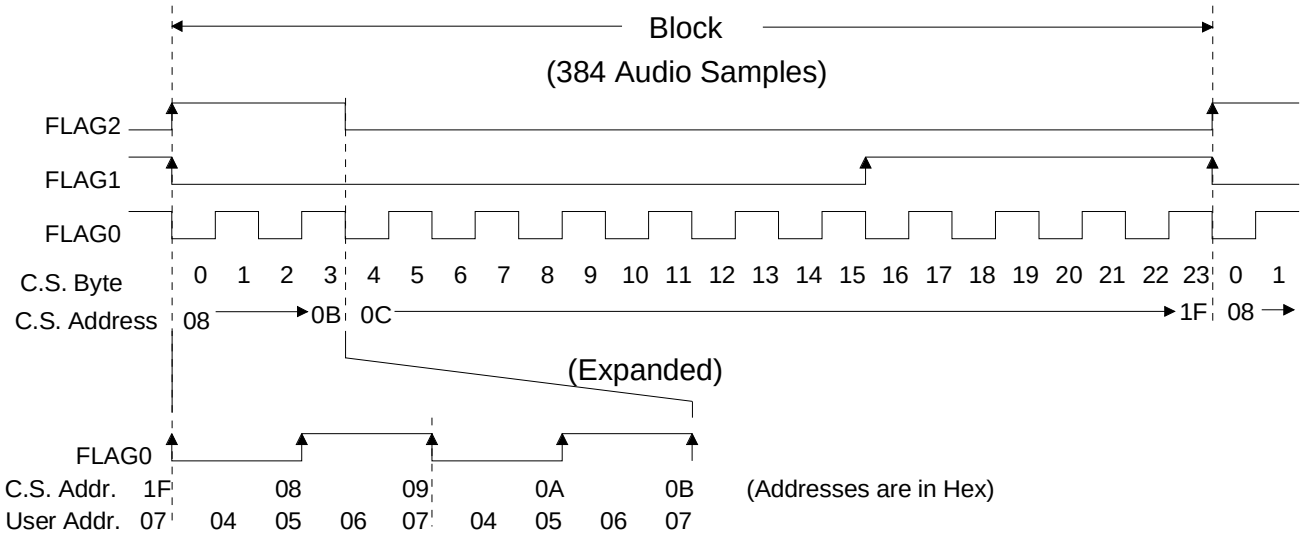


Figure 12. CS8413 Buffer Memory Write Sequence - MODE 0

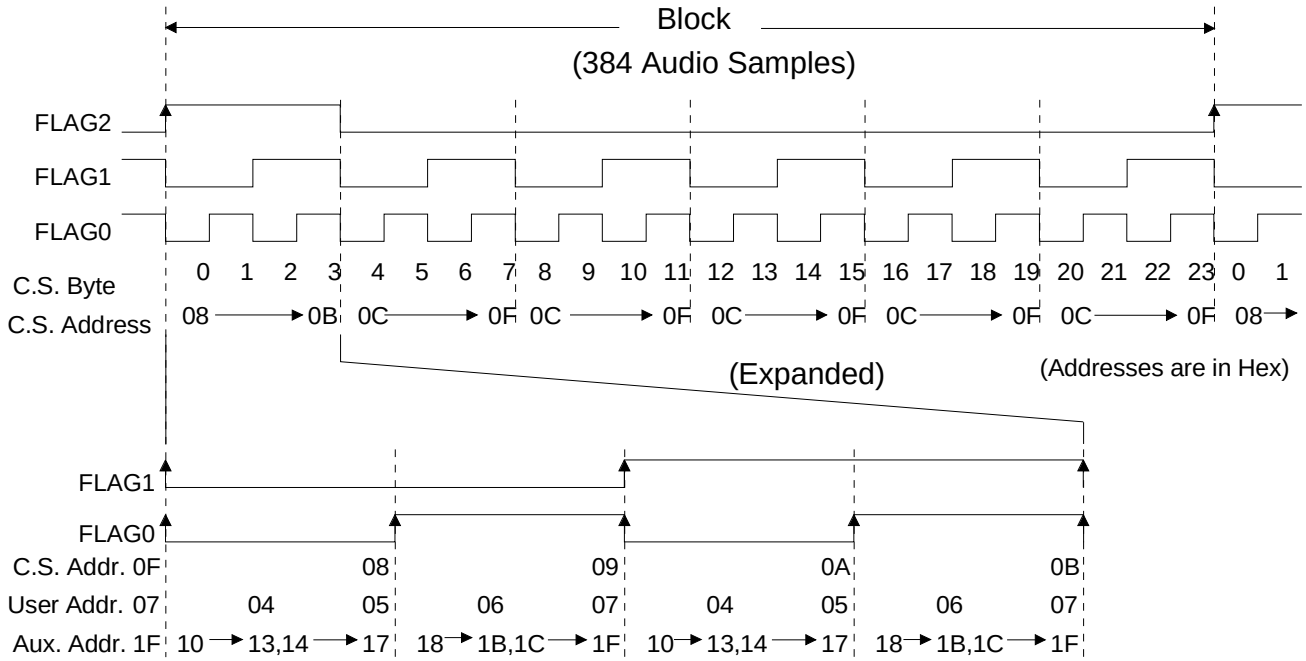


Figure 13. CS8413 Buffer Memory Write Sequence - MODE 1

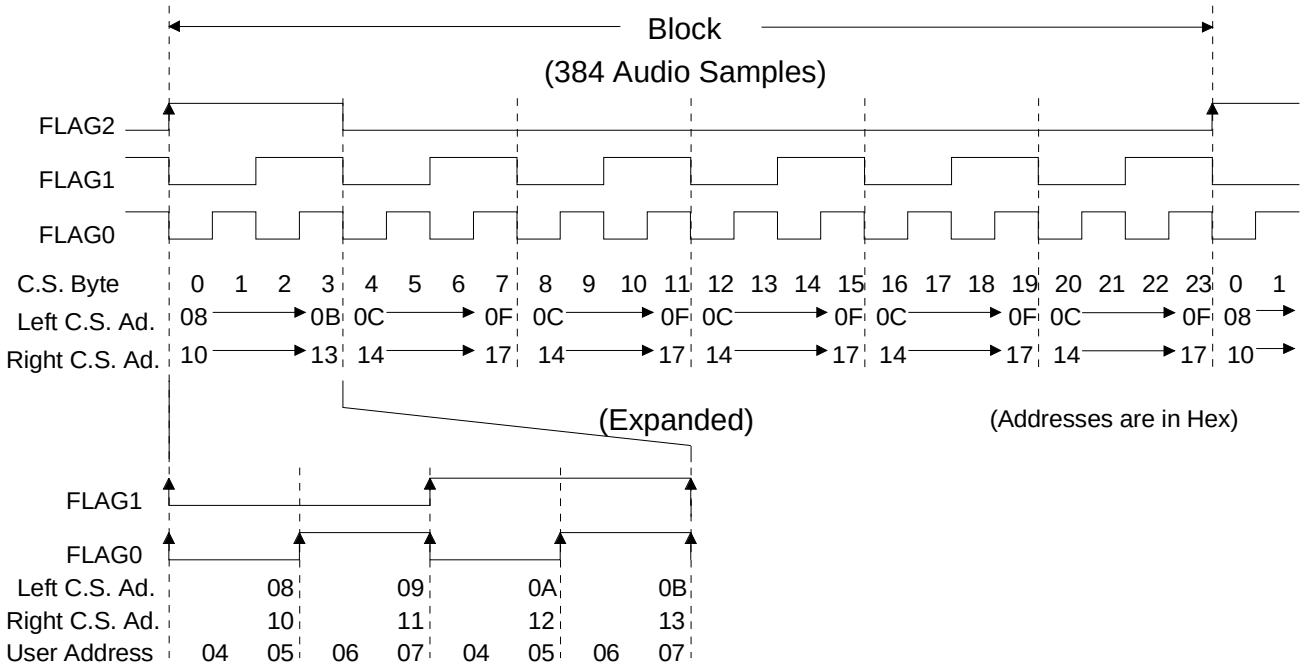


Figure 14. CS8413 Buffer Memory Write Sequence - MODE 2

Buffer Mode 2

In buffer mode 2, two 8-byte buffers are available to independently buffer each channel of channel status data. Both buffers are identical to the channel status buffer in mode 1 and are written to simultaneously, with locations 08H to 0FH containing CS data for channel A and locations 10H to 17H containing CS data for channel B. Both CS buffers can be monitored using FLAG1 and FLAG2 as described in the *BUFFER MODE 1* section.

The two most significant bits in SR1 change definition for buffer mode 2. These two bits, when set, indicate CRC errors for their respective channels. A CRC error occurs when the internal calculated CRC for channel status bytes 0 through 22 does not match channel status byte 23. CCHG, bit 5 in SR1, is set when any bit in the first four channel status bytes of either channel changes from one block to the next. Since channel status doesn't change very often, this bit may be monitored rather than checking all the bits in the first four bytes. These bits are illustrated in Figure 6.

Buffer Updates and Interrupt Timing

As mentioned previously in the buffer mode sections, conflicts between externally reading the buffer RAM and the CS8413 internally writing to it may be averted by using the flag levels to avoid the section currently being addressed by the part. However, if the interrupt line, along with the flags, is utilized, the actual byte that was just updated can be determined. In this way, the entire buffer can be read without concern for internal updates. Figure 15 shows the detailed timing for the interrupt line, flags, and the RAM write line. SCK is 64 times the incoming sample frequency, and is the same SCK output in master mode. The FSYNC shown is valid for all master modes except the I^2S compatible mode. The interrupt pulse is shown to be 4 SCK periods wide and goes low 5 SCK periods after the RAM is written. Using the above information, the entire data buffer may be read starting with the next byte to be updated by the internal pointer.

ERF Pin Timing

ERF signals that an error occurred while receiving the audio sample that is currently being read from the serial port. ERF changes with the active edge of FSYNC and is high during the erroneous sample. ERF is affected by the error conditions reported in SR2: LOCK, CODE, PARITY, and V. Any of these conditions may be masked off using the corresponding bits in IER2. The ERF pin will go high for each error that occurs. The ERF bit in SR1 is different from the ERF pin in that it only causes an interrupt the first time an error occurs until SR1 is read. More information on the ERF pin and bit is

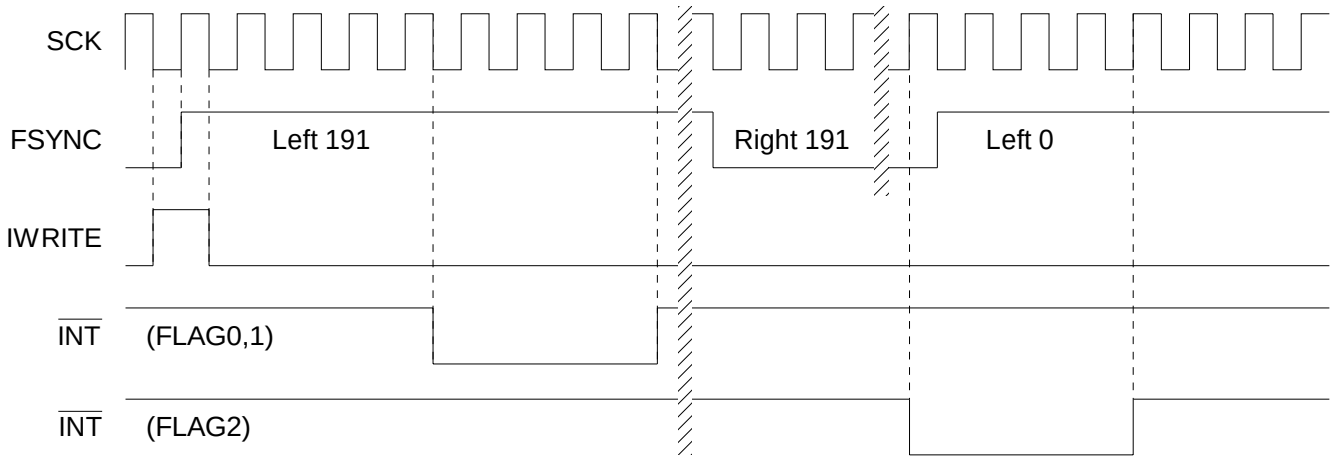


Figure 15. RAM/Buffer - Write and Interrupt Timing

contained at the end of the *Status and IEnable Registers* section.

CS8414 DESCRIPTION

The CS8414 does not need a microprocessor to handle the non-audio data (although a micro may be used with the C and U serial ports). Instead, dedicated pins are available for the most important channel status bits. The CS8414 is a monolithic CMOS circuit that receives and decodes digital audio data which was encoded according to the digital audio interface standards. It contains an RS422 line receiver and clock and data recovery utilizing an on-chip phase-locked loop. The audio data is output through a configurable serial port that supports 14 formats. The channel status and user data have their own serial pins and the validity flag is OR'ed with the ERF flag to provide a single pin, VERF, indicating that the audio output may not be valid. This pin may be used by interpolation filters that provide error correction. A block diagram of the CS8414 is illustrated in Figure 16.

The line receiver and jitter performance are described in the sections directly preceding the CS8413 sections in the beginning of this data sheet.

Audio Serial Port

The audio serial port is used primarily to output audio data and consists of three pins: SCK, FSYNC, and SDATA. These pins are configured via four control pins: M0, M1, M2, and M3. M3 selects between eight normal serial formats (M3 = 0), and six special formats (M3 = 1).

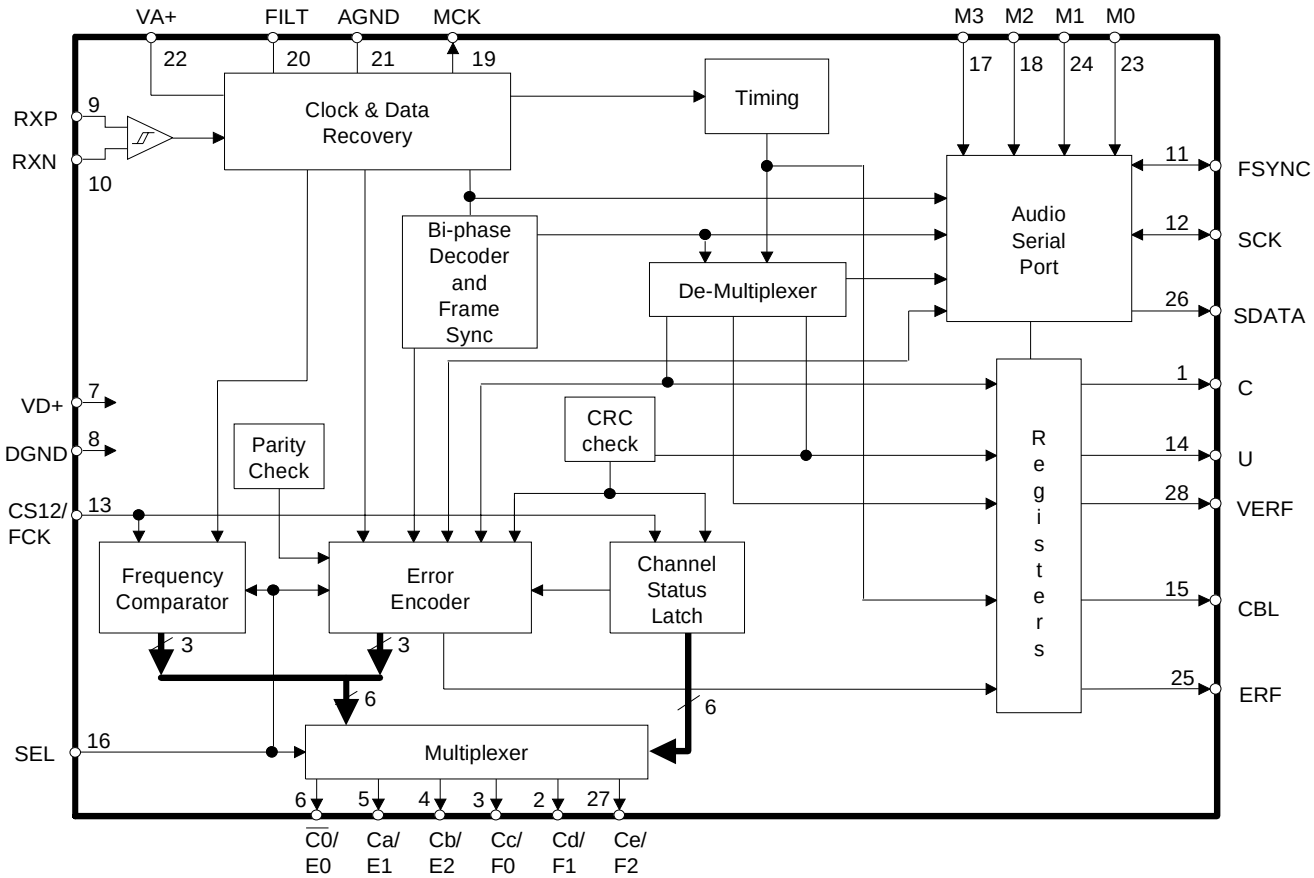


Figure 16. CS8414 Block Diagram

Normal Modes (M3 = 0)

When M3 is low, the normal serial port formats shown in Figure 17 are selected using M2, M1, and M0. These formats are also listed in Table 3, wherein the first word past the format number (Out-In) indicates whether FSYNC and SCK are outputs from the CS8414 or are inputs. The next word (L/R-WSYNC) indicates whether FSYNC indicates the particular channel or just delineates each word. If an error occurs (ERF = 1) while using one of these formats, the previous valid audio data for that channel will be output. As long as ERF is high, that same data word will be output. If the CS8414 is not locked, it will output all zeroes. In some modes FSYNC and SCK are outputs and in others they are inputs. In Table 3, LSBJ is short for *LSB justified* where the LSB is justified to the end of the audio frame and the MSB varies with word length. As outputs the CS8414 generates 32 SCK periods per audio sample (64 per stereo sample) and, as inputs, 32 SCK periods must be provided per audio sample. When FSYNC and SCK are inputs, one stereo sample is double buffered. For those modes which output 24 bits of audio data, the auxiliary bits will be included. If the auxiliary bits are not used for audio data, they must be masked off.

M2	M1	M0	Format
0	0	0	0 - Out, L/R, 16-24 Bits
0	0	1	1 - In, L/R, 16-24 Bits
0	1	0	2 - Out, L/R, I^2S Compatible
0	1	1	3 - In, L/R, I^2S Compatible
1	0	0	4 - Out, WSYNC, 16-24 Bits
1	0	1	5 - Out, L/R, 16 Bits LSBJ
1	1	0	6 - Out, L/R, 18 Bits LSBJ
1	1	1	7 - Out, L/R, MSB Last

Table 3. Normal Audio Port Modes (M3 = 0)

Special Modes (M3 = 1)

When M3 is high, the special audio modes described in Table 4 are selected via M2, M1, and M0. In formats 8, 9, and 10, SCK, FSYNC, and SDATA are the same as in formats 0, 1, and 2 respectively; however, the recovered data is output as is even if ERF is high, indicating an error. (In modes 0-2 the previous valid sample is output.) Similarly, when out of lock, the CS8414 will still output all the recovered data, which should be zeros if there is no input to the RXP, RXN pins. Format 11 is similar to format 0 except that SCK is an input and FSYNC is an output. In this mode FSYNC and SDATA are synchronized to the incoming SCK, and the number of SCK periods between FSYNC edges will vary since SCK is not synchronous to received data stream. This mode may be useful when writing data to storage.

M2	M1	M0	Format
0	0	0	8 - Format 0 - No repeat on error
0	0	1	9 - Format 1 - No repeat on error
0	1	0	10 - Format 2 - No repeat on error
0	1	1	11 - Format 0 - Async. SCK input
1	0	0	12 - Received NRZ Data
1	0	1	13 - Received Bi-phase Data
1	1	0	14 - Reserved
1	1	1	15 - CS8414 Reset

Table 4. Special Audio Port Modes (M3 = 1)

Format 12 is similar to format 7 except that SDATA is the entire data word received from the transmission line including the C, U, V, and P bits, with zeros in place of the preamble. In format 13 SDATA contains the entire biphase encoded data from the transmission line including the preamble, and SCK is twice the normal frequency. The normal two frame delay of data from input to output is reduced to only a few bit periods in formats 12 and 13. However, the C, U, V bits and error codes follow their normal pathways and therefore follow the output data by nearly two frames. Figure 18 illustrates formats 12 and 13. Format 14 is reserved and not presently used, and format 15 causes the CS8414 to go into a reset state. While in reset all outputs will be inactive except MCK. The CS8414 comes out of reset at the first block boundary after

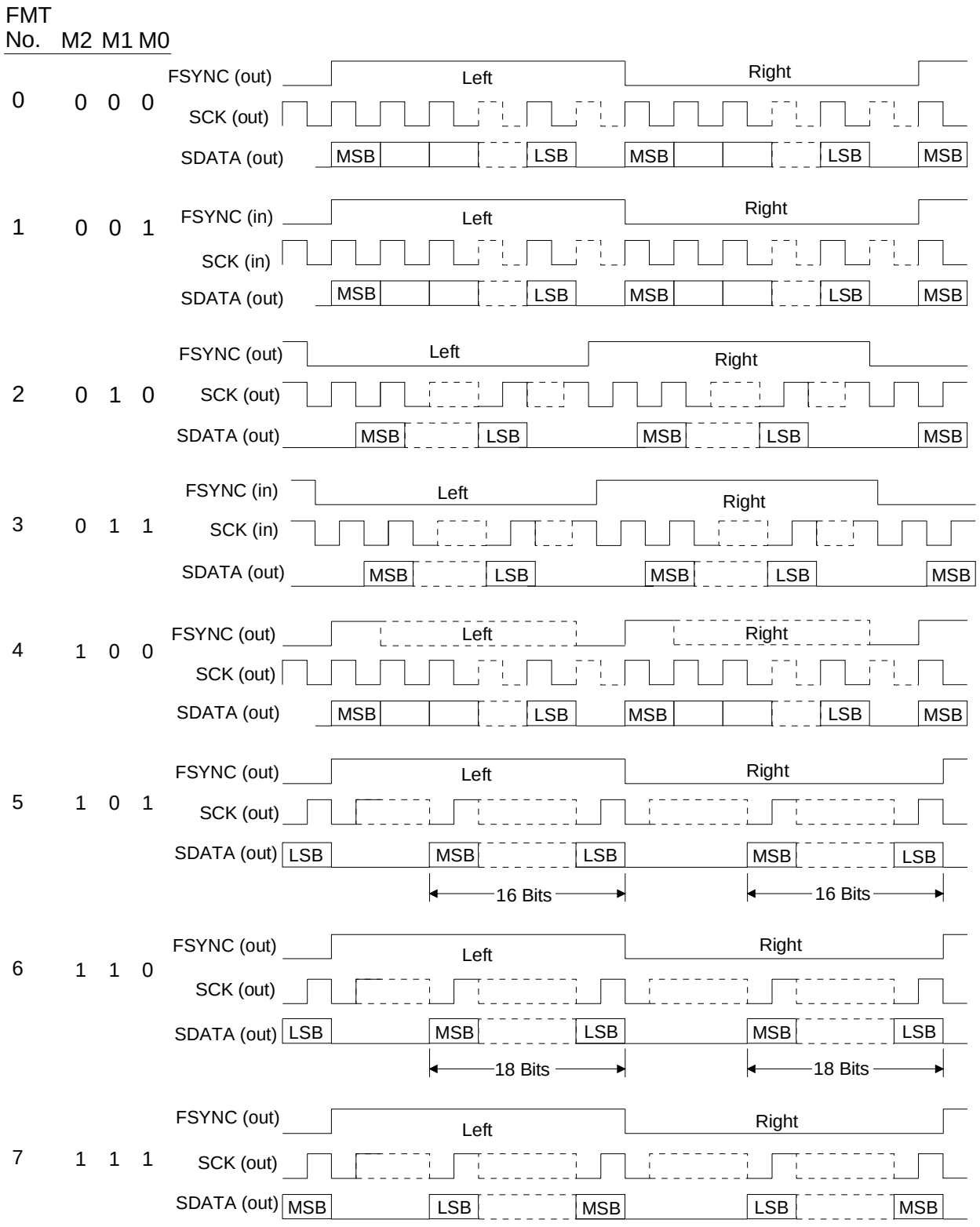


Figure 17. CS8414 Audio Serial Port Formats

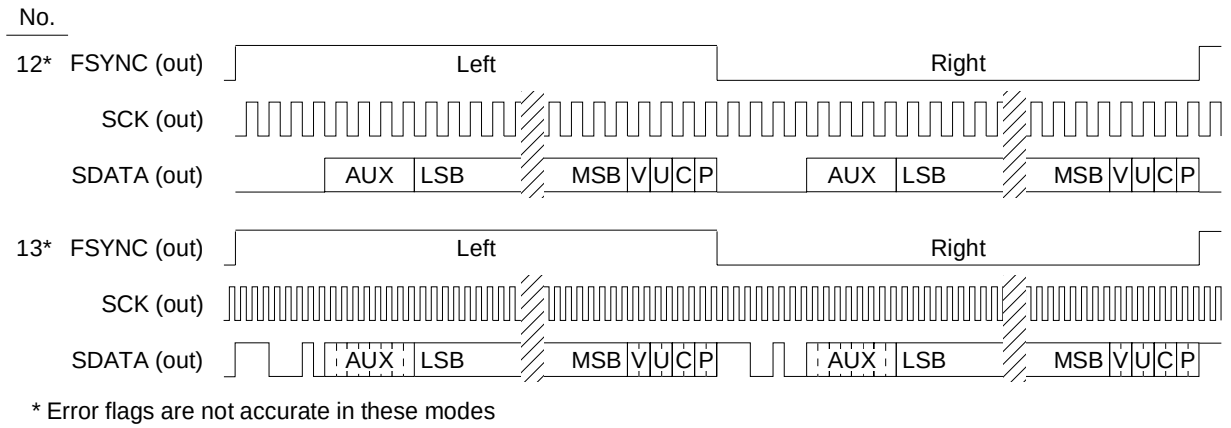


Figure 18. Special Audio Port Formats 12 and 13

leaving the reset state. The CS8414 should be reset immediately after power-up and any time the user performs a system-wide reset. See Appendix B for a suggested reset circuit.

C, U, VERF, ERF, and CBL Serial Outputs

The C and U bits and CBL are output one SCK period prior to the active edge of FSYNC in all serial port formats except 2 and 3 (I^2S modes). The active edge of FSYNC may be used to latch C, U, and CBL externally. In formats 2 and 3, the C and U bits and CBL are updated with the active edge of FSYNC. The validity + error flag (VERF) and the error flag (ERF) are always updated at the active edge of FSYNC. This timing is illustrated in Figure 19.

The C output contains the channel status bits with CBL rising indicating the start of a new channel status block. CBL is high for the first four bytes of channel status (32 frames or 64 samples) and low for the last 20 bytes of channel status (160 frames or 320 samples). The U output contains the User Channel data. The V bit is OR'ed with the ERF flag and output on the VERF pin. This indicates that the audio sample may be in error and can be used by interpolation filters to interpolate through the error. ERF being high indicates a serious error occurred on the transmission line. There are three errors that cause ERF to go high: a parity error or biphase coding violation during that sample, or an out of lock PLL receiver. Timing for the above pins is illustrated in Figure 19.

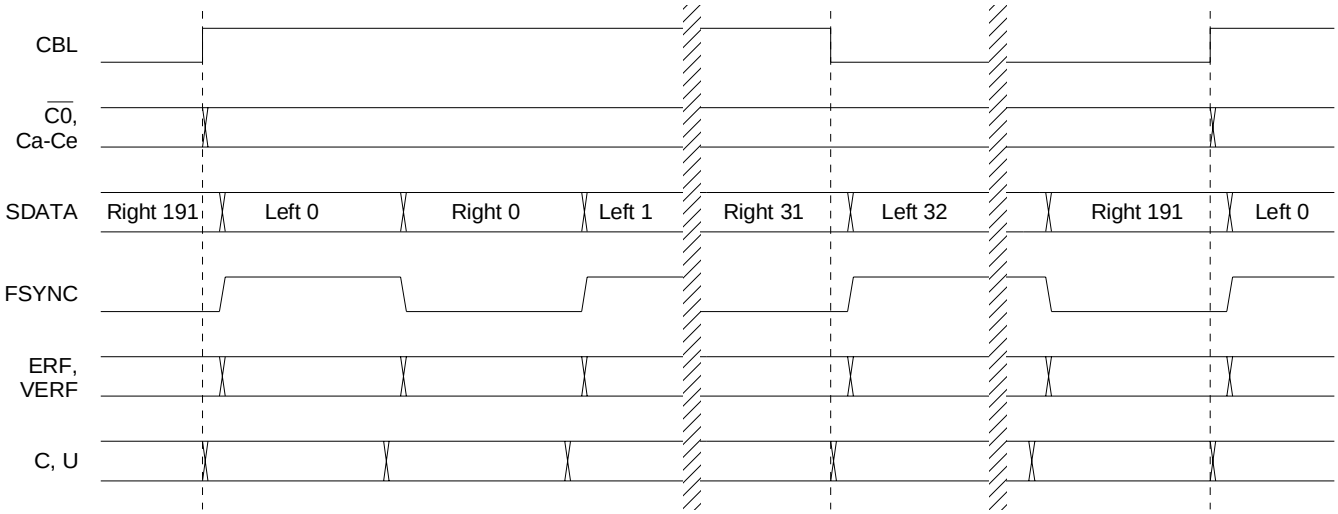


Figure 19. CBL Timing

Multifunction Pins

There are seven multifunction pins which contain either error and received frequency information, or channel status information, selectable by SEL.

Error and Frequency Reporting

When SEL is low, error and received frequency information are selected. The error information is encoded on pins E2, E1, and E0, and is decoded as shown in Table 5. When an error occurs, the corresponding error code is latched. Clearing is then accomplished by bringing SEL high for more than eight MCK cycles. The errors have a priority associated with their error code, with validity having the lowest priority and no lock having the highest priority. Since only one code can be displayed, the error with the highest priority that occurred since the last clearing will be selected.

E2	E1	E0	Error
0	0	0	No Error
0	0	1	Validity Bit High
0	1	0	Reserved
0	1	1	Slipped Sample
1	0	0	CRC Error (PRO only)
1	0	1	Parity Error
1	1	0	Bi-phase Coding Error
1	1	1	No Lock

Table 5. Error Decoding

The validity flag indicates that the validity bit for a previous sample was high since the last clearing of the error codes. The slipped sample error can only occur when FSYNC and SCK of the audio serial port are inputs. In this case, if FSYNC is asynchronous to the received data rate, periodically a stereo sample will be dropped or reread depending on whether the read rate is slower or faster than the received data rate. When this occurs, the slipped sample error code will appear on the 'E' pins. The CRC error is updated at the beginning of a channel status block, and is only valid when the professional format of channel status data is received. This error is indicated when the CS8414 calculated CRC value does not match the CRC byte of the channel status block or when a block boundary changes (as in removing samples while editing). The parity error occurs when the incoming sub-frame does not have even parity as specified by the standards. The biphase coding error indicates a biphase coding violation occurred. The no lock error indicates that the PLL is not locked onto the incoming data stream.

The received frequency information is encoded on pins F2, F1, and F0, and is decoded as shown in Table 6. The on-chip frequency comparator compares the received clock frequency to an externally supplied 6.144 MHz clock which is input on the FCK pin. The 'F' pins are updated three times during a channel status block including prior to the rising edge of CBL. CBL may be used to externally latch the 'F' pins. The clock on FCK must be valid for two thirds of a block for the 'F' pins to be accurate. The 'F' pins are invalid when the PLL is out of lock.

F2	F1	F0	Sample Frequency
0	0	0	Out of Range
0	0	1	reserved
0	1	0	reserved
0	1	1	96 kHz ±4%
1	0	0	88.2 kHz ±4%
1	0	1	48 kHz ±4%
1	1	0	44.1 kHz ±4%
1	1	1	32 kHz ±4%

Table 6. Sample Frequency Decoding

Channel Status Reporting

When SEL is high, channel status is displayed on $\overline{C0}$, and Ca-Ce for the channel selected by CS12. If CS12 is low, channel status for sub-frame 1 is displayed, and if CS12 is high, channel status for sub-frame 2 is displayed. The contents of Ca-Ce depend

upon the $\overline{C0}$ professional/consumer bit. The information reported is shown in Table 7.

Pin	Professional	Consumer
$\overline{C0}$	0 (low)	1 (high)
Ca	$\overline{C1}$	$\overline{C1}$
Cb	EM0	$\overline{C2}$
Cc	EM1	$\overline{C3}$
Cd	$\overline{C9}$	$\overline{ORIG}$
Ce	$\overline{CRCE}$	$\overline{IGCAT}$

Table 7. Channel Status Pins

Professional Channel Status ($\overline{C0}$ = 0)

When $\overline{C0}$ is low, the received channel status block is encoded according to the professional/broadcast format. The Ca through Ce pins are defined for some of the more important professional bits. As listed in Table 7, Ca is the inverse of channel status bit 1. Therefore, if the incoming channel status bit 1 is 1, Ca, defined as $\overline{C1}$, will be 0. $\overline{C1}$ indicates whether audio ($\overline{C1}$ = 1) or non-audio ($\overline{C1}$ = 0) data is being received. Cb and Cc, defined as EM0 and EM1 respectively, indicate emphasis and are encoded versions of channel status bits 2, 3, and 4. The decoding is listed in Table 8. Cd, defined as $\overline{C9}$, is the inverse of channel status bit 9, which gives some indication of channel mode. (Bit 9 is also defined as bit 1 of byte 1.) When Ce, defined as $\overline{CRCE}$, is low, the CS8414 calculated CRC value does not match the received CRC value. This signal may be used to qualify Ca through Cd. If Ca through Ce are being displayed, Ce going low can indicate not to update the display.

EM1	EM0	C2	C3	C4	Emphasis
0	0	1	1	1	CCITT J.17 emphasis
0	1	1	1	0	50/15 μs emphasis
1	0	1	0	0	No Emphasis
1	1	0	0	0	Not Indicated

Table 8. Emphasis Encoding

Consumer Channel Status ($\overline{C0}$ = 1)

When $\overline{C0}$ is high, the received channel status block is encoded according to the consumer format. In this case Ca through Ce are defined differently as shown in Table 7. Ca is the inverse of channel status bit 1, $\overline{C1}$, indicating audio ($\overline{C1}$ = 1) or non-audio ($\overline{C1}$ = 0). Cb is defined as the inverse of channel status bit 2, $\overline{C2}$, which indicates copy inhibit/copyright information. Cc, defined as $\overline{C3}$, is the emphasis bit of channel status, with $\overline{C3}$ low indicating the data has had pre-emphasis added.

The audio standards, in consumer mode, describe bit 15, L, as the generation status which indicates whether the audio data is an original work or a copy (1st generation or higher). The definition of the L bit is reversed for three category codes: two broadcast codes, and laser-optical (CD's). Therefore, to interpret the L bit properly, the category code must be decoded. The CS8414 does this decoding internally and provides the $\overline{ORIG}$ signal that, when low, indicates that the audio data is original over all category codes.

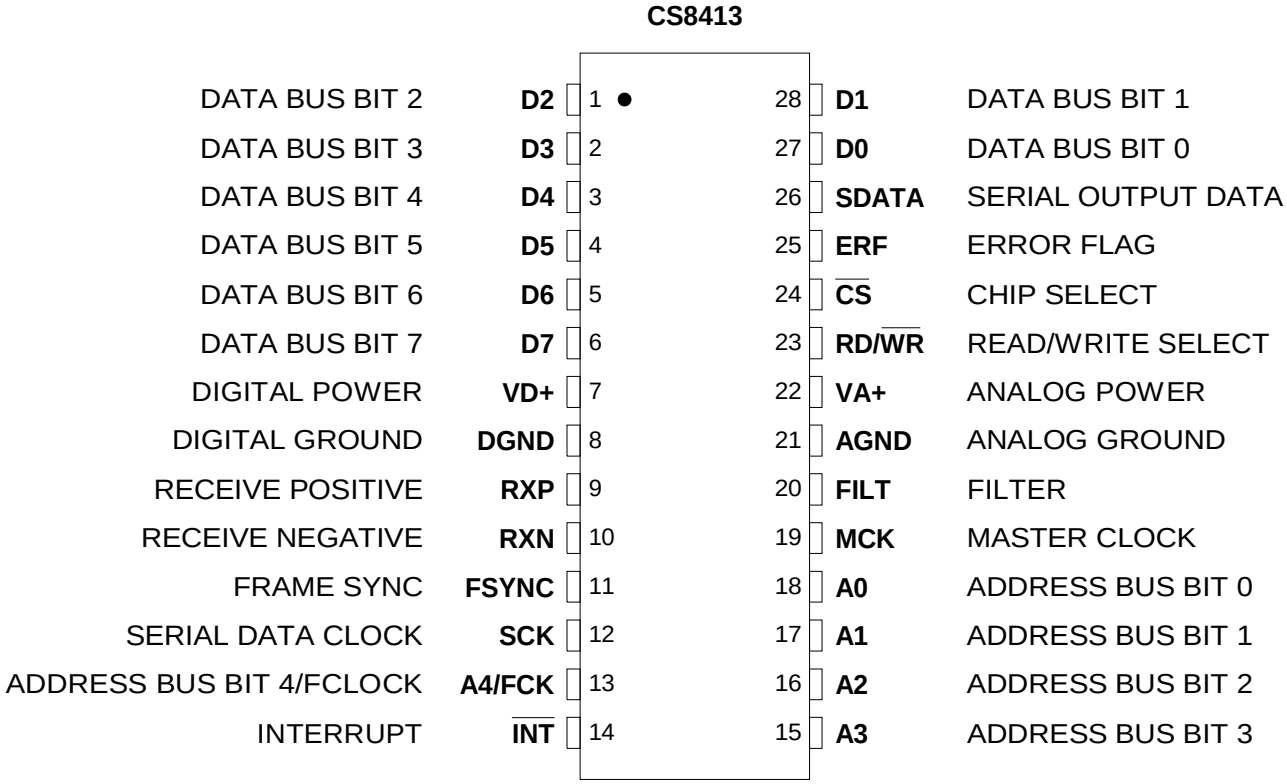
SCMS

The consumer audio standards also mention a serial copy management system, SCMS, for dealing with copy protection of copyrighted works. SCMS is designed to allow unlimited duplication of the original work, but no duplication of any copies of the original. This system utilizes the channel status bit 2, Copy, and channel status bit 15, L or generation status, along with the category codes. If the Copy bit is 0, copyright protection is asserted over the material. Then, the L bit is used to determine if the material is an original or a duplication. (As mentioned in the previous paragraph, the definition of the L bit can be reversed based on the category codes.) There are two category codes that get special attention: general and A/D converters without C or L bit information. For these two categories the SCMS standard requires that equipment interfacing to these categories set the C bit to 0 (copyright pro-

tection asserted) and the L bit to 1 (original). To support this feature, Ce, in the consumer mode, is defined as $\overline{\text{IGCAT}}$ (ignorant category) which is low for the “general” (0000000) and “A/D converter without copyright information” (01100xx) categories.



PIN DESCRIPTIONS: CS8413



Power Supply Connections

VD+ - Positive Digital Power, PIN 7.

Positive supply for the digital section. Nominally +5 volts.

VA+ - Positive Analog Power, PIN 22.

Positive supply for the analog section. Nominally +5 volts. This supply should be as quiet as possible since noise on this pin will directly affect the jitter performance of the recovered clock.

DGND - Digital Ground, PIN 8.

Ground for the digital section. DGND should be connected to same ground as AGND.

AGND - Analog Ground, PIN 21.

Ground for the analog section. AGND should be connected to same ground as DGND.

Audio Output Interface

SCK - Serial Clock, PIN 12.

Serial clock for SDATA pin which can be configured (via control register 2) as an input or output, and can sample data on the rising or falling edge. As an input, SCK must contain 32 clocks for every audio sample in all normal audio serial port formats.

FSYNC - Frame Sync, PIN 11.

Delineates the serial data and may indicate the particular channel, left or right. Also, FSYNC may be configured as an input or output. The format is based on bits in control register 2.

SDATA - Serial Data, PIN 26.

Audio data serial output pin.

ERF - Error Flag, PIN 25.

Signals that an error has occurred while receiving the audio sample currently being read from the serial port. The errors that cause ERF to go high are enumerated in status register 2 and enabled by setting the corresponding bit in IEnable register 2.

A4/FCK - Address Bus Bit 4/Frequency Clock, PIN 13.

This pin has a dual function and is controlled by the FCEN bit in control register 1. A4 is the address bus pin as defined below. When used as FCK, an internal frequency comparator compares a 6.144 MHz clock input on this pin to the received clock frequency and stores the value in status register 1 as three FREQ bits. These bits indicate the incoming frequency. When defined as FCK, A4 is internally set to 0.

Parallel Interface

$\overline{\text{CS}}$ - Chip Select, PIN 24.

This input is active low and allows access to the 32 bytes of internal memory. The address bus and RD/$\overline{\text{WR}}$ must be valid while $\overline{\text{CS}}$ is low.

RD/$\overline{\text{WR}}$ - Read/Write, PIN 23.

If RD/$\overline{\text{WR}}$ is low when $\overline{\text{CS}}$ goes active (low), the data on the data bus is written to internal memory. If RD/$\overline{\text{WR}}$ is high when $\overline{\text{CS}}$ goes active, the data in the internal memory is placed on the data bus.

A4-A0 - Address Bus, PINS 13, 15-18.

Parallel port address bus that selects the internal memory location to be read from or written to. Note that A4 is the dual function pin A4/FCK as described above.

D0-D7 - Data Bus, PINS 27-28, 1-6.

Parallel port data bus used to check status, read or write control words, or read internal buffer memory.

$\overline{\text{INT}}$ - Interrupt, PIN 14.

Open drain output that can signal the state of the internal buffer memory as well as error information. A 5kΩ resistor to VD+ is typically used to support logic gates. All bits affecting $\overline{\text{INT}}$ are maskable to allow total control over the interrupt mechanism.

Receiver Interface

RXP, RXN - Differential Line Receivers, PINS 9, 10.

RS422 compatible line receivers. Described in detail in Appendix A.

Phase Locked Loop

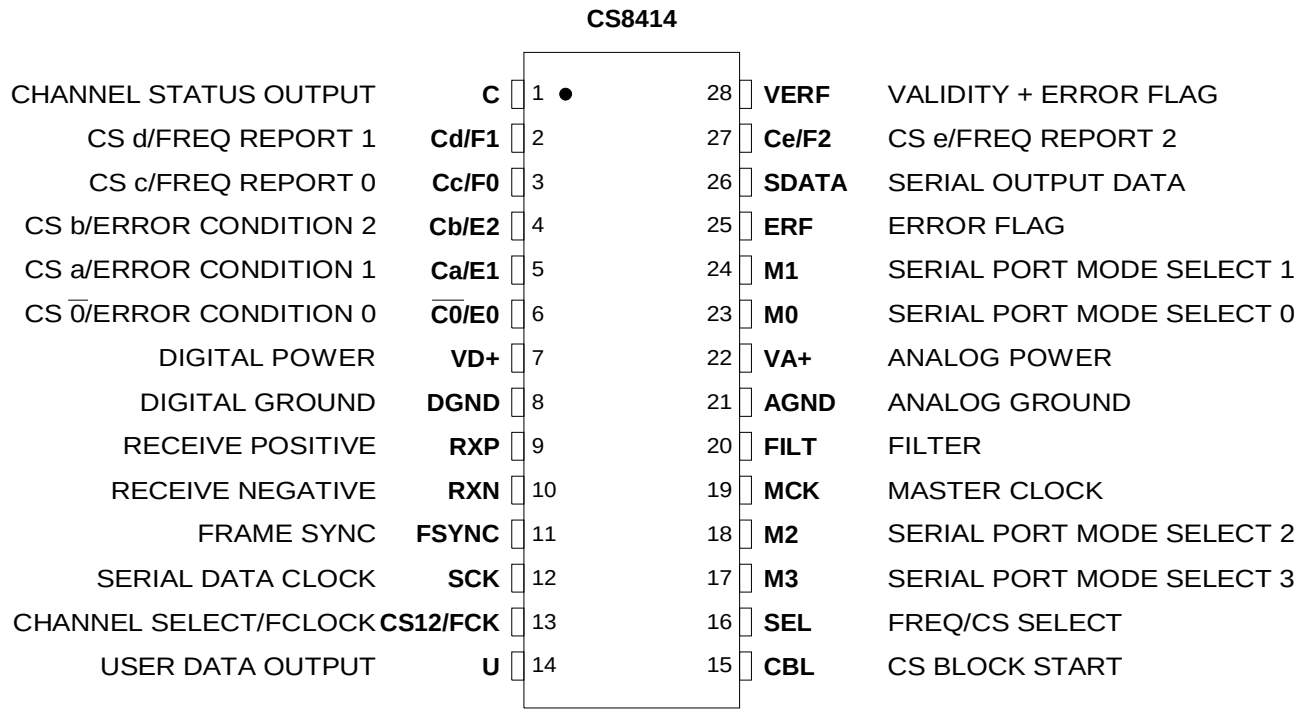
MCK - Master Clock, PIN 19.

Low jitter clock output of 256 times the received sample frequency.

FILT - Filter, PIN 20.

An external 470Ω resistor and 0.068µF capacitor are required from the FILT pin to analog ground.

PIN DESCRIPTIONS: CS8414



Power Supply Connections

VD+ - Positive Digital Power, PIN 7.

Positive supply for the digital section. Nominally +5 volts.

VA+ - Positive Analog Power, PIN 22.

Positive supply for the analog section. Nominally +5 volts.

DGND - Digital Ground, PIN 8.

Ground for the digital section. DGND should be connected to same ground as AGND.

AGND - Analog Ground, PIN 21.

Ground for the analog section. AGND should be connected to same ground as DGND.

Audio Output Interface

SCK - Serial Clock, PIN 12.

Serial clock for SDATA pin which can be configured (via the M0, M1, M2, and M3 pins) as an input or output, and can sample data on the rising or falling edge. As an output, SCK will generate 32 clocks for every audio sample. As an input, 32 SCK periods per audio sample must be provided in all normal modes.

FSYNC - Frame Sync, PIN 11.

Delineates the serial data and may indicate the particular channel, left or right, and may be an input or output. The format is based on M0, M1, M2, and M3 pins.

SDATA - Serial Data, PIN 26.

Audio data serial output pin.

M0, M1, M2, M3 - Serial Port Mode Select, PINS 23, 24, 18, 17.

Selects the format of FSYNC and the sample edge of SCK with respect to SDATA. M3 selects between eight normal modes (M3 = 0), and six special modes (M3 = 1).

Control Pins

VERF - Validity + Error Flag, PIN 28.

A logical OR'ing of the validity bit from the received data and the error flag. May be used by interpolation filters to interpolate through errors.

U - User Bit, PIN 14.

Received user bit serial output port. FSYNC may be used to latch this bit externally. (Except in I^2S modes when this pin is updated on the active edge of FSYNC.)

C - Channel Status Output, PIN 1.

Received channel status bit serial output port. FSYNC may be used to latch this bit externally. (Except in I^2S modes when this pin is updated on the active edge of FSYNC.)

CBL - Channel Status Block Start, PIN 15.

The channel status block output is high for the first four bytes of channel status and low for the last 20 bytes.

SEL - Select, PIN 16.

Control pin that selects either channel status information (SEL = 1) or error and frequency information (SEL = 0) to be displayed on six of the following pins.

$\overline{C0}$, Ca, Cb, Cc, Cd, Ce - Channel Status Output Bits, PINS 2-6, 27.

These pins are dual function with the 'C' bits selected when SEL is high. Channel status information is displayed for the channel selected by CS12. $\overline{C0}$, which is channel status bit 0, defines professional ($\overline{C0}$ = 0) or consumer ($\overline{C0}$ = 1) mode and further controls the definition of the Ca-Ce pins. These pins are updated with the rising edge of CBL.

CS12 - Channel Select, PIN 13.

This pin is also dual function and is selected by bringing SEL high. CS12 selects sub-frame 1 (when low) or sub-frame 2 (when high) to be displayed by channel status pins $\overline{C0}$ and Ca through Ce.

FCK - Frequency Clock, PIN 13.

Frequency Clock input that is enabled by bringing SEL low. FCK is compared to the received clock frequency with the value displayed on F2 through F0. Nominal input value is 6.144 MHz.

E0, E1, E2 - Error Condition, PINS 4-6.

Encoded error information that is enabled by bringing SEL low. The error codes are prioritized and latched so that the error code displayed is the highest level of error since the last clearing of the error pins. Clearing is accomplished by bring SEL high for more than 8 MCK cycles.

F0, F1, F2 - Frequency Reporting Bits, PINS 2-3, 27.

Encoded sample frequency information that is enabled by bringing SEL low. A proper clock on FCK must be input for at least two thirds of a channel status block for these pins to be valid. They are updated three times per block, starting at the block boundary. These pins are invalid when the PLL is out of lock.

ERF - Error Flag, PIN 25.

Signals that an error has occurred while receiving the audio sample currently being read from the serial port. Three errors cause ERF to go high: a parity or biphase coding violation during the current sample, or an out of lock PLL receiver.

Receiver Interface

RXP, RXN - Differential Line Receivers, PINS 9, 10.

RS422 compatible line receivers.

Phase Locked Loop

MCK - Master Clock, PIN 19.

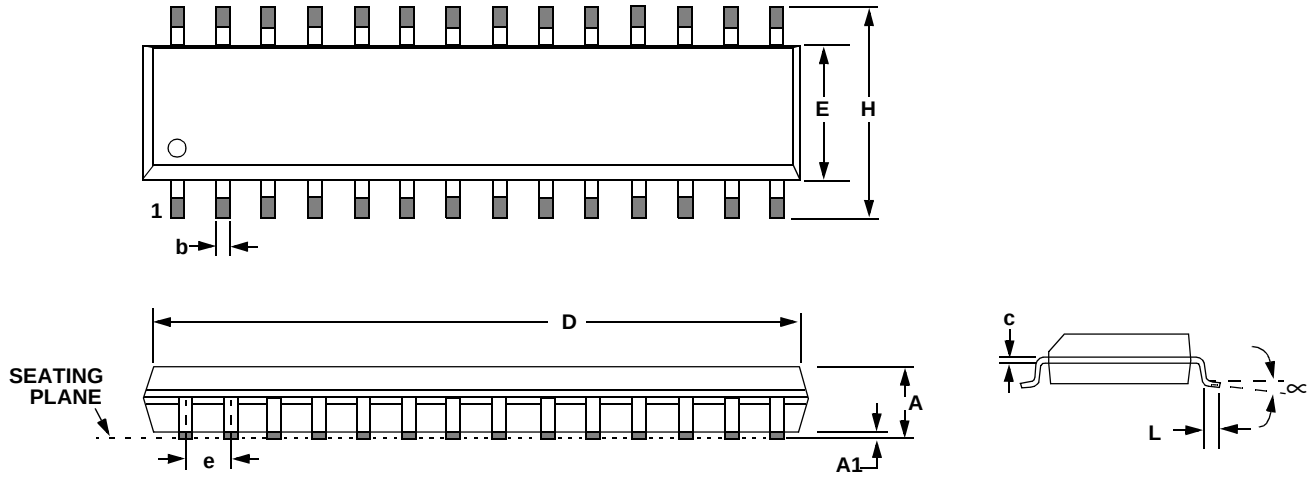
Low jitter clock output of 256 times the received sample frequency.

FILT - Filter, PIN 20.

An external 470Ω resistor and 0.068µF capacitor is required from FILT pin to analog ground.

PACKAGE DIMENSIONS

28L SOIC (300 MIL BODY) PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.697	0.713	17.70	18.10
E	0.291	0.299	7.40	7.60
e	0.040	0.060	1.02	1.52
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
∝	0°	8°	0°	8°

APPENDIX A: RS422 RECEIVER INFORMATION

The RS422 receivers on the CS8413 and CS8414 are designed to receive both the professional and consumer interfaces, and meet all specifications listed in the digital audio standards. Figure A20 illustrates the internal schematic of the receiver portion of both chips. The receiver has a differential input. A Schmitt trigger is incorporated to add hysteresis which prevents noisy signals from corrupting the phase detector.

Professional Interface

The digital audio specifications for professional use call for a balanced receiver, using XLR connectors, with 110Ω ±20% impedance. (The XLR connector on the receiver should have female pins with a male shell.) Since the receiver has a very high impedance, a 110Ω resistor should be placed across the receiver terminals to match the line impedance, as shown in Figure A21, and, since the part has internal biasing, no external biasing network is needed. If some isolation is desired without the use of transformers, a 0.01µF capacitor should be placed on the input of each pin (RXP and RXN) as shown in Figure A22. However, if transformers are not used, high frequency energy could be coupled between transmitter and receiver causing degradation in analog performance.

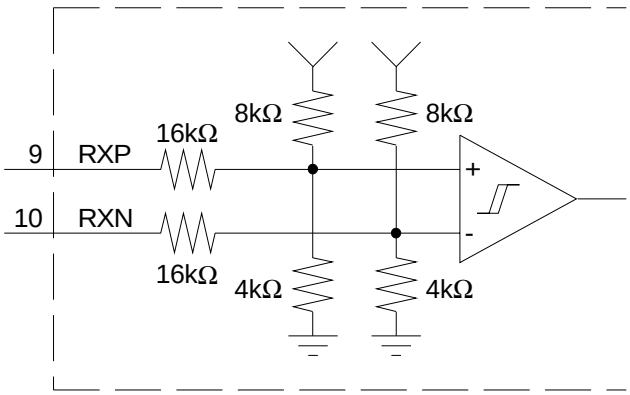


Figure 20. RS422 Receiver Internal Circuit

Although transformers are not required by AES they are strongly recommended. The EBU requires transformers. Figures A21 and A22 show an optional DC blocking capacitor on the transmission line. A 0.1 to 0.47µF ceramic capacitor may be used to block any DC voltage that is accidentally connected to the digital audio receiver. The use of this capacitor is an issue of robustness as the digital audio transmission line does not have a DC voltage component.

Grounding the shield of the cable is a tricky issue. In the configuration of systems, it is important to avoid ground loops and DC current flowing down the shield of the cable that could result when boxes with different ground potentials are connected. Generally, it is good practice to ground the shield to the chassis of the transmitting unit, and connect the shield through a capacitor to chassis ground at the receiver. However, in some cases it is advantageous to have the ground of two boxes held to the same potential, and the cable shield might be depended upon to make that electrical connection. Generally, it may be a good idea to provide the op-

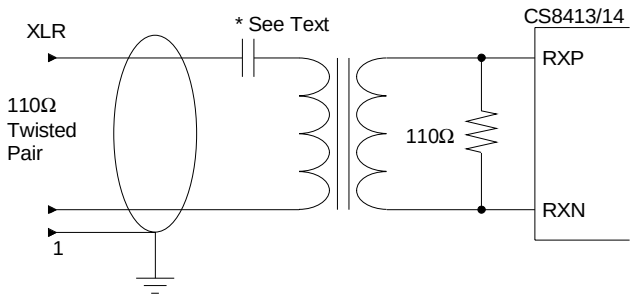


Figure 21. Professional Input Circuit

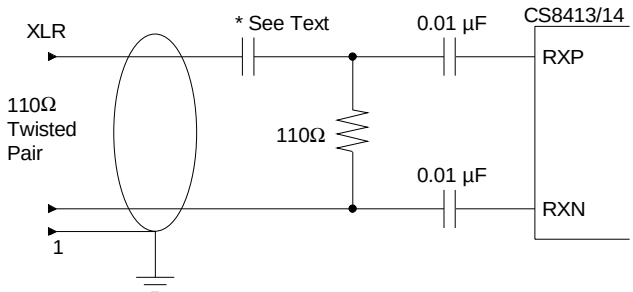


Figure 22. Transformerless Professional Circuit

tion of grounding or capacitively coupling to ground with a “ground-lift” circuit.

Consumer Interface

In the case of the consumer interface, the standards call for an unbalanced circuit having a receiver impedance of 75Ω ±5%. The connector for the consumer interface is an RCA phono plug (fixed socket described in Table IV of IEC 268-11). The receiver circuit for the consumer interface is shown in Figure A23.

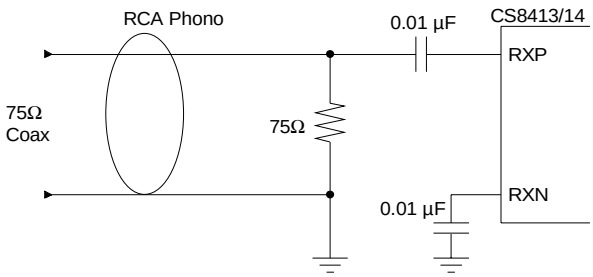


Figure 23. Consumer Input Circuit

TTL/CMOS Levels

The circuit shown in Figure A24 may be used when external RS422 receivers or TTL/CMOS logic drive the CS8413/14 receiver section.

Transformers

Please refer Application Note AN134: AES and S/PDIF Recommended Transformers for further information.

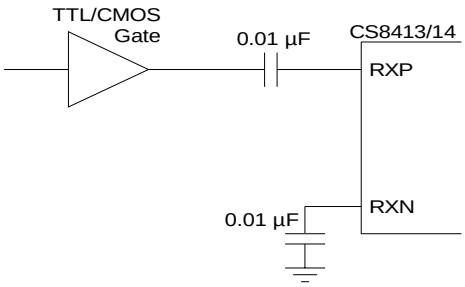


Figure 24. TTL/CMOS Interface

APPENDIX B: SUGGESTED RESET CIRCUIT FOR CS8414

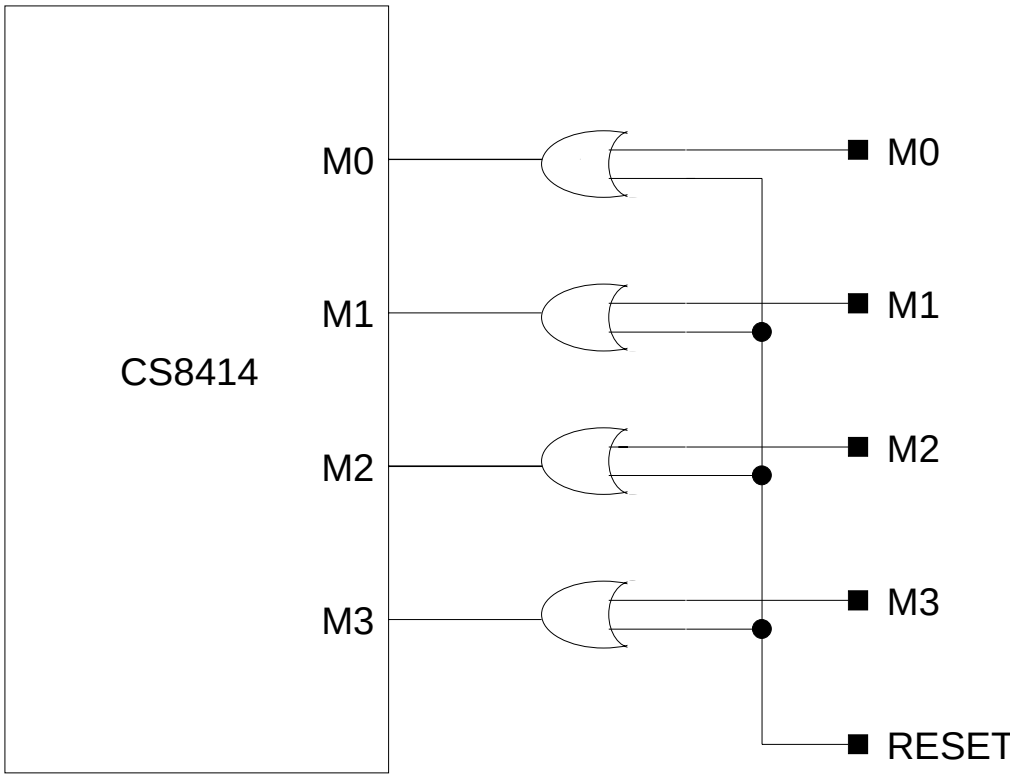


Figure 25. CS8414 Reset Circuit

The CS8414 should be reset immediately after power-up and any time the user issues a system-wide reset. This is accomplished by pulling all four Mode Select pins high. Figure 25 shows a simple circuit to implement this. The OR gates can be 74LS32 type gates.

• Notes •


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