A DIVISION OF CIRRUS LOGIC

**CS5396**
**CS5397**

# *120 dB, 96 kHz Audio A/D Converter*

## Features

- 24-Bit Conversion
- 120 dB Dynamic Range (A-Weighted)
- Low Noise and Distortion
  >105 dB THD + N
- Complete CMOS Stereo A/D System
  Delta-Sigma A/D Converters
  Digital Anti-Alias Filtering
  S/H Circuitry and Voltage Reference
- CS5396 - digital filter optimized for audio
- CS5397 - non-aliasing digital filter
- Adjustable System Sampling Rates including 32, 44.1, 48 & 96 kHz
- Differential Analog Architecture
- Linear Phase Digital Anti-Alias Filtering
- 10 Tap Programmable Psychoacoustic Noise Shaping Filter
- Single +5 V Power Supply

## General Description

The CS5396 and CS5397 are complete analog-to-digital converters for stereo digital audio systems. They perform sampling, analog-to-digital conversion and anti-alias filtering, generating 24-bit values for both left and right inputs in serial form at sample rates up to 100 kHz per channel.

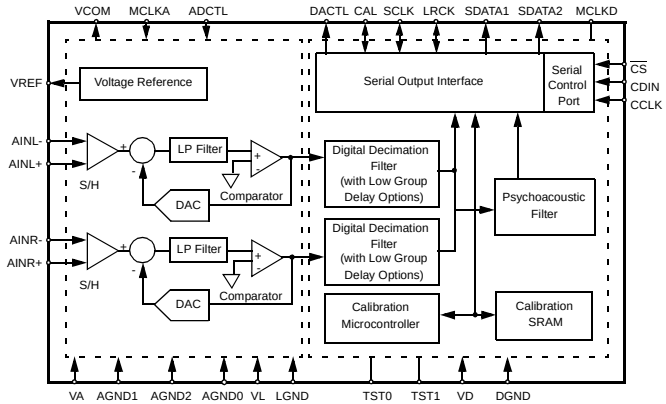
The CS5396/97 use a patented 7th-order, tri-level delta-sigma modulator followed by digital filtering and decimation, which removes the need for an external anti-alias filter. The ADCs use a differential architecture which provides excellent noise rejection.

The CS5396 has a linear phase filter optimized for audio applications with ±0.005 dB passband ripple and >117 dB stopband rejection. The CS5397 has a non-aliasing filter response with ±0.005 passband ripple and >117 dB stopband attenuation. Other features available in both the CS5396 and CS5397 are an optional low group delay filter and a unique psychoacoustic noise shaping filter which subjectively truncates the output to 16, 18 or 20 bits while 24-bit sound quality is preserved.

The CS5396/97 are targeted for the highest performance professional audio systems requiring wide dynamic range, negligible distortion and low noise.

**ORDERING INFORMATION**

| | | |
|---|---|---|
| CS5396-KS | -10° to 50° C | 28-pin SOIC |
| CS5397-KS | -10° to 50° C | 28-pin SOIC |
| CDB5396/97 | | Evaluation Board |




*Preliminary Product Information* | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.


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## ANALOG CHARACTERISTICS ($T_A$ = 25°C; VA, VL,VD = 5V; Full-scale Input Sinewave, 997 Hz; Analog connections as shown in Figure 1; Measurement Bandwidth is 20 Hz to 20 kHz unless otherwise specified; Logic 0 = 0V, Logic 1 = VD;

| Parameter | | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Dynamic Performance** | | | | | | |
| Dynamic Range | MCLK equal to 24.576 MHz | | TBD | | | |
| Fs = 48 kHz in 128x Oversampling Mode | (A-weighted) | | TBD | 120 | - | dB |
| Fs = 48 kHz in 128x mode | | | TBD | 117 | - | dB |
| Fs = 96 kHz in 64x mode | (A-weighted) | | TBD | 120 | - | dB |
| Fs = 96 kHz in 64x mode | (40 kHz Bandwidth) | | | 114 | - | dB |
| | MCLK equal to 12.288 MHz | | TBD | | | |
| Fs = 48 kHz in 64x mode | (A-weighted) | | TBD | 117 | - | dB |
| Fs = 48 kHz in 64x mode | | | | 114 | - | dB |
| Total Harmonic Distortion + Noise | | THD+N | | | | |
| Fs = 48 kHz in 128x mode | -1 dB (Note 1) | | TBD | 105 | - | dB |
| | -20 dB (Note 1) | | TBD | 97 | - | dB |
| | -60 dB (Note 1) | | TBD | 57 | - | dB |
| Fs = 96 kHz in 64x mode | -1 dB (Note 1) | | TBD | 105 | - | dB |
| (40 kHz bandwidth) | -20 dB (Note 1) | | TBD | 97 | - | dB |
| | -60 dB (Note 1) | | TBD | 57 | - | dB |
| Fs = 48 kHz in 64x mode | -1 dB (Note 1) | | TBD | 105 | - | dB |
| | -20 dB (Note 1) | | TBD | 97 | - | dB |
| | -60 dB (Note 1) | | TBD | 57 | - | dB |
| Total Harmonic Distortion | -1 dB (Note 1) | THD | TBD | 0.00056 | - | % |
| Interchannel Phase Deviation | | | - | 0.0001 | - | deg |
| Interchannel Isolation | | | - | 120 | - | dB |
| Dynamic Range Performance Drift | (following calibration) | | - | 0.05 | - | dB/°C |
| ***dc Accuracy*** | | | | | | |
| Interchannel Gain Mismatch | | | - | 0.05 | - | dB |
| Gain Error | | | - | ±5 | TBD | % |
| Gain Drift | | | - | ±100 | - | ppm/°C |
| Offset Error (With high pass filter enabled) | | | - | 0 | - | LSB |
| ***Analog Input*** | | | | | | |
| Full-scale Differential Input Voltage | (Note 2) | $V_{IN}$ | TBD | 4 | TBD | $V_{pp}$ |
| Input Impedance | Differential | $Z_{IN}$ | - | 4.5 | - | kΩ |
| | Common-mode | | - | TBD | - | kΩ |
| Common-Mode Rejection Ratio | | CMRR | - | 82 | - | dB |

Notes: 1. Referenced to typical full-scale differential input voltage (4.0 Vpp).

2. Specified for a fully differential input ±{(AINR+)-(AINR-)}.The ADC accepts input voltages up to the analog supplies (VA and AGND). Full-scale outputs will be produced for differential inputs beyond VIN.

* Refer to Parameter Definitions at the end of this data sheet.

Specifications are subject to change without notice.

## DIGITAL FILTER CHARACTERISTICS ($T_A$ = 25 °C; VA, VL,VD = 5V±5%; Fs = 48 kHz)

| Parameter | Symbol | CS5396 Min | CS5396 Typ | CS5396 Max | CS5397 Min | CS5397 Typ | CS5397 Max | Unit |
|---|---|---|---|---|---|---|---|---|
| ***High-Performance Filter*** | | | | | | | | |
| Passband(-0.01 dB) | | 0 | - | 0.4604 | 0 | - | 0.3958 | Fs |
| Passband Ripple | | - | - | ±0.005 | - | - | ±0.005 | dB |
| Stopband | | 0.5542 | - | 63.45 | 0.4979 | - | 63.50 | Fs |
| Stopband Attenuation | | 117 | - | - | 117 | - | - | dB |
| Group Delay (Fs = Output Sample Rate) | $t_{gd}$ | | | | | | | |
| 128x Oversampling Mode | | - | 34/Fs | - | - | 34/Fs | - | µs |
| 64x Oversampling Mode | | - | 34/Fs | - | - | 34/Fs | - | µs |
| Group Delay Variation vs. Frequency | $\Delta t_{gd}$ | - | - | 0.0 | - | - | 0.0 | µs |
| ***Low Group Delay Filter*** | | | | | | | | |
| Passband(-0.01 dB) | | 0 | - | 0.375 | 0 | - | 0.375 | Fs |
| 128x Oversampling Mode | | 0 | - | 0.188 | 0 | - | 0.188 | Fs |
| 64x Oversampling Mode | | | | | | | | |
| Passband Ripple | | - | - | 0.015 | - | - | 0.015 | dB |
| Stopband | | 0.646 | - | 127.35 | 0.646 | - | 127.35 | Fs |
| 128x Oversampling Mode | | 0.323 | - | 63.68 | 0.323 | - | 63.68 | Fs |
| 64x Oversampling Mode | | | | | | | | |
| Stopband Attenuation | | 86 | - | | 86 | - | | dB |
| Group Delay (Fs = Output Sample Rate) | $t_{gd}$ | - | 10/Fs | - | - | 10/Fs | - | µs |
| Group Delay Variation vs. Frequency | $\Delta t_{gd}$ | - | - | 0.0 | - | - | 0.0 | µs |
| ***High Pass Filter Characteristics*** | | | | | | | | |
| Frequency Response-3.0 dB (Note 3) | | - | 1.8 | - | - | 1.8 | - | Hz |
| -0.036 dB (Note 3) | | | 20 | - | | 20 | - | Hz |
| Phase Deviation@ 20Hz (Note 3) | | - | 5.3 | - | - | 5.3 | - | Deg |
| Passband Ripple | | - | - | 0 | - | - | 0 | dB |

Notes: 3. Response shown is for Fs equal to 48 kHz. Filter characteristics scale with Fs.

## POWER AND THERMAL CHARACTERISTICS

($T_A$ = 25 °C; VA, VL,VD = 5V±5%; Fs = 48 kHz; Master Mode)

| Parameter | | Symbol | 64X oversampling MCLK=12.288 MHz Min | Typ | Max | 128X oversampling MCLK=24.576 MHz Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Power Supply Current (Normal Operation) | VA+VL | $I_A$ | - | 150 | TBD | - | 160 | TBD | mA |
| | VD | $I_D$ | - | 65 | TBD | - | 125 | TBD | mA |
| Power Supply Current (Power-Down Mode) | VA+VL | $I_A$ | - | 2 | - | - | 3 | - | mA |
| | VD | $I_D$ | - | 2 | - | - | 3.5 | - | mA |
| Power Consumption(Normal Operation) | | | - | 1075 | TBD | - | 1425 | TBD | mW |
| (Power-Down Mode) | | | - | 20 | - | - | 33 | - | mW |
| Power Supply Rejection Ratio (1 kHz) | | PSRR | - | 65 | - | - | 65 | - | dB |
| Allowable Junction Temperature | | | - | - | 135 | - | - | 135 | °C |
| Junction to Ambient Thermal Impedance | | $T_{JA}$ | - | 45 | - | - | 45 | - | °C/W |

## DIGITAL CHARACTERISTICS ($T_A$ = 25 °C; VA, VL,VD = 5V±5%)

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| High-Level Input Voltage | $V_{IH}$ | 2.4 | - | - | V |
| Low-Level Input Voltage | $V_{IL}$ | - | - | 0.8 | V |
| High-Level Output Voltage at $I_o$ = -20 µA | $V_{OH}$ | VD - 1.0 | - | - | V |
| Low-Level Output Voltage at $I_o$ = 20 µA | $V_{OL}$ | - | - | 0.4 | V |
| Input Leakage Current | $I_{in}$ | - | - | ±10 | µA |

## ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, All voltages with respect to ground.)

| Parameter | | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| DC Power Supplies: | Analog | VA | -0.3 | - | +6.0 | V |
| | Logic | VL | -0.3 | - | +6.0 | V |
| | Digital | VD | -0.3 | - | +6.0 | V |
| | \|VA - VD\| | | - | - | 0.4 | V |
| | (Note 6) | | - | - | 0.4 | V |
| | \|VA - VL\| | | - | - | 0.4 | V |
| | (Note 6) | | | | | |
| | \|VD - VL\| | | | | | |
| | (Note 6) | | | | | |
| Input Current | (Note 4) | $I_{in}$ | - | - | ±10 | mA |
| Analog Input Voltage | (Note 5) | $V_{IN}$ | AGND-0.7 | - | VA+0.7 | V |
| Digital Input Voltage | (Note 5) | $V_{IND}$ | -0.3 | - | VD+0.7 | V |
| Ambient Operating Temperature (Power Applied) | | $T_A$ | -55 | - | +50 | °C |
| Storage Temperature | | $T_{stg}$ | -65 | - | +150 | °C |

Notes: 4. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

5. The maximum over/under voltage is limited by the input current.

6. Applies to normal operation. Greater differences during power up/down will not cause SCR latch-up.
WARNING: Operation beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

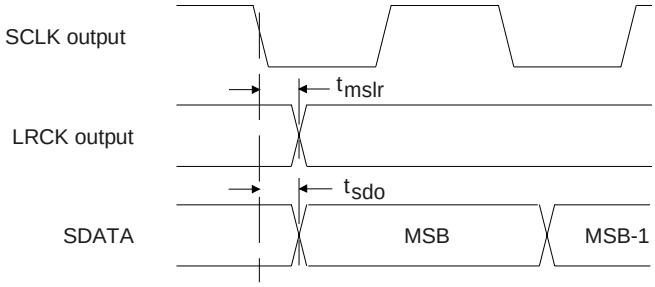
## RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, all voltages with respect to ground.)

| Parameter | | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| DC Power Supplies: | Positive Digital | VD | 4.75 | 5.0 | 5.25 | V |
| | Positive Logic | VL | 4.75 | 5.0 | 5.25 | V |
| | Positive Analog | VA | 4.75 | 5.0 | 5.25 | V |
| | \|VA - VD\| (Note 6) | | - | - | 0.4 | V |
| Ambient Operating Temperature (Power Applied) | | $T_A$ | -10 | - | +50 | °C |

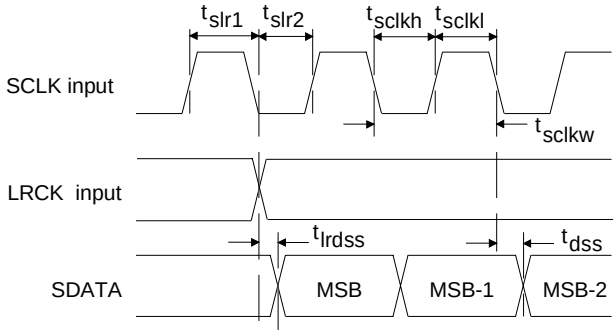
Specifications are subject to change without notice.

## SWITCHING CHARACTERISTICS ($T_A$ = 25 °C; VA = 5V±5%; Inputs: Logic 0 = 0V, Logic 1 = VA = VD; $C_L$ = 20 pF)

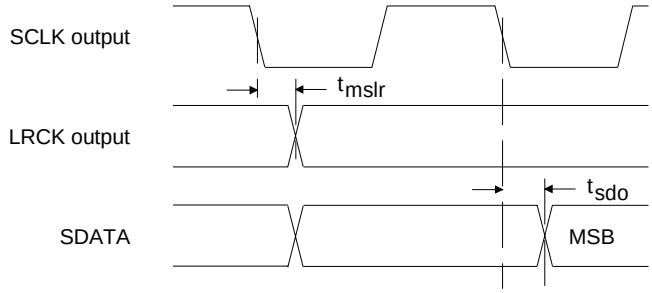
| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Output Sample Rate | Fs | 2 | - | 100 | kHz |
| MCLK Period | $t_{clkw}$ | 39.06 | - | 1950 | ns |
| MCLK Low | $t_{clkl}$ | 26 | - | - | ns |
| MCLK High | $t_{clkh}$ | 26 | - | - | ns |
| MCLK Fall Time | $t_{clkft}$ | - | - | 8 | ns |
| ***Master Mode*** | | | | | |
| SCLK falling to LRCK | $t_{mslr}$ | -20 | - | +20 | ns |
| SCLK falling to SDATA valid | $t_{sdo}$ | - | - | 20 | ns |
| SCLK duty cycle | | - | 50 | - | % |
| ***Slave Mode*** | | | | | |
| LRCK Period | 1/Fs | 10 | - | 500 | µs |
| LRCK duty cycle | | - | 50 | - | % |
| SCLK Period | $t_{sclkw}$ | 4 x $t_{clw}$ | - | - | ns |
| SCLK Pulse Width Low | $t_{sclkl}$ | 2 x $t_{clw}$ | - | - | ns |
| SCLK Pulse Width High | $t_{clkh}$ | 60 | - | - | ns |
| SCLK falling to SDATA valid | $t_{dss}$ | - | - | $t_{clw}$ + 20 ns | ns |
| LRCK edge to MSB valid | $t_{lrdss}$ | - | - | $t_{clw}$ + 20 ns | ns |
| SCLK rising to LRCK edge delay | $t_{slr1}$ | $t_{clw}$ + 20 ns | - | - | ns |
| LRCK edge to rising SCLK setup time | $t_{slr2}$ | $t_{clw}$ + 20 ns | - | - | ns |



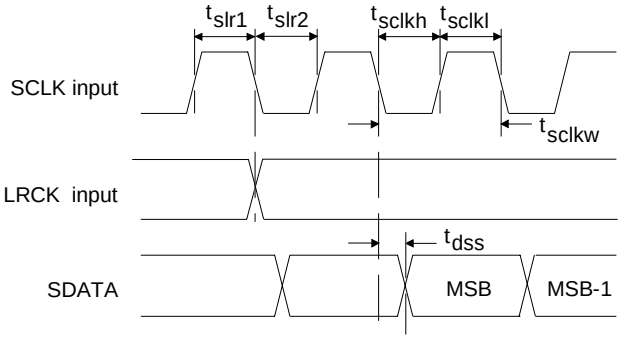

**SCLK to SDATA & LRCK - MASTER mode**
**Serial Data Format, Left Justified**




**SCLK to LRCK & SDATA - SLAVE mode**
**Serial Data Format, Left Justified**




**SCLK to SDATA & LRCK - MASTER mode**
**Serial Data Format, $I^2S$ compatible**



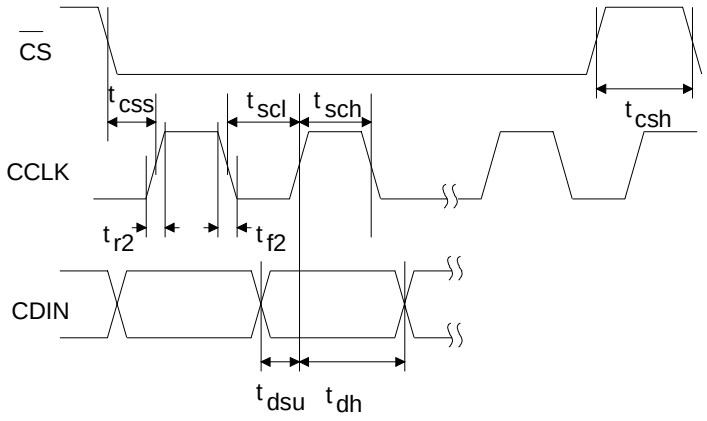

**SCLK to LRCK & SDATA - SLAVE mode**
**Serial Data Format, $I^2S$ compatible**

## SPI CONTROL PORT SWITCHING CHARACTERISTICS ($T_A$ = 25 °C; VD, VA = 5V ±5%; Inputs: Logic 0 = DGND, Logic 1 = VD; $C_L$ = 20 pF)

| Parameter | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| ***SPI Mode*** | | | | | |
| CCLK Clock Frequency | | $f_{sck}$ | - | 6 | MHz |
| $\overline{CS}$ High Time Between Transmissions | | $t_{csh}$ | 1.0 | - | µs |
| $\overline{CS}$ Falling to CCLK Edge | | $t_{css}$ | 20 | - | ns |
| CCLK Low Time | | $t_{scl}$ | 66 | - | ns |
| CCLK High Time | | $t_{sch}$ | 66 | - | ns |
| CDIN to CCLK Rising Setup Time | | $t_{dsu}$ | 40 | - | ns |
| CCLK Rising to DATA Hold Time | (Note 7) | $t_{dh}$ | 15 | - | ns |
| Rise Time of CCLK and CDIN | (Note 8) | $t_{r2}$ | - | 100 | ns |
| Fall Time of CCLK and CDIN | (Note 8) | $t_{f2}$ | - | 100 | ns |

Notes: 7. Data must be held for sufficient time to bridge the transition time of CCLK.

8. For $F_{SCK}$ < 1 MHz.

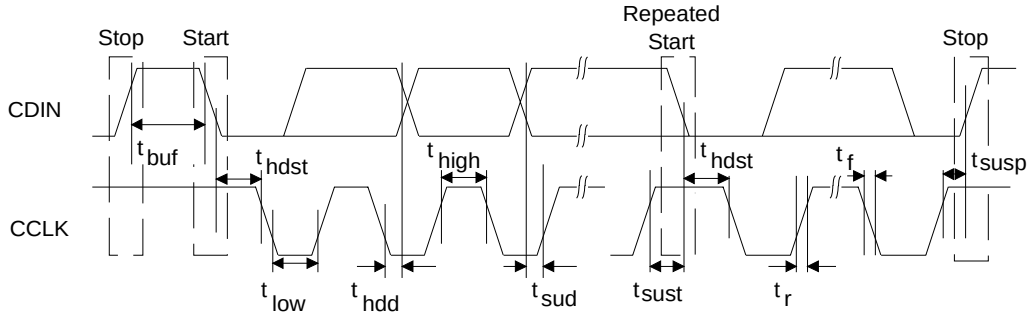


## I²C CONTROL PORT SWITCHING CHARACTERISTICS ($T_A$ = 25 °C; VD, VA = 5V ±5%; Inputs: Logic 0 = DGND, Logic 1 = VD; $C_L$ = 20 pF)

| Parameter | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| ***I²C® Mode*** | ***(Note 9)*** | | | | |
| CCLK Clock Frequency | | $f_{scl}$ | - | 100 | kHz |
| Bus Free Time Between Transmissions | | $t_{buf}$ | 4.7 | - | µs |
| Start Condition Hold Time (prior to first clock pulse) | | $t_{hdst}$ | 4.0 | - | µs |
| Clock Low Time | | $t_{low}$ | 4.7 | - | µs |
| Clock High Time | | $t_{high}$ | 4.0 | - | µs |
| Setup Time for Repeated Start Condition | | $t_{sust}$ | 4.7 | - | µs |
| CDIN Hold Time from CCLK Falling | (Note 10) | $t_{hdd}$ | 0 | - | µs |
| CDIN Setup Time to CCLK Rising | | $t_{sud}$ | 250 | - | ns |
| Rise Time of Both CDIN and CCLK Lines | | $t_r$ | - | 1 | µs |
| Fall Time of Both CDIN and CCLK Lines | | $t_f$ | - | 300 | ns |
| Setup Time for Stop Condition | | $t_{susp}$ | 4.7 | - | µs |

Notes: 9. Use of the I²C® bus interface requires a license from Philips.

10. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.



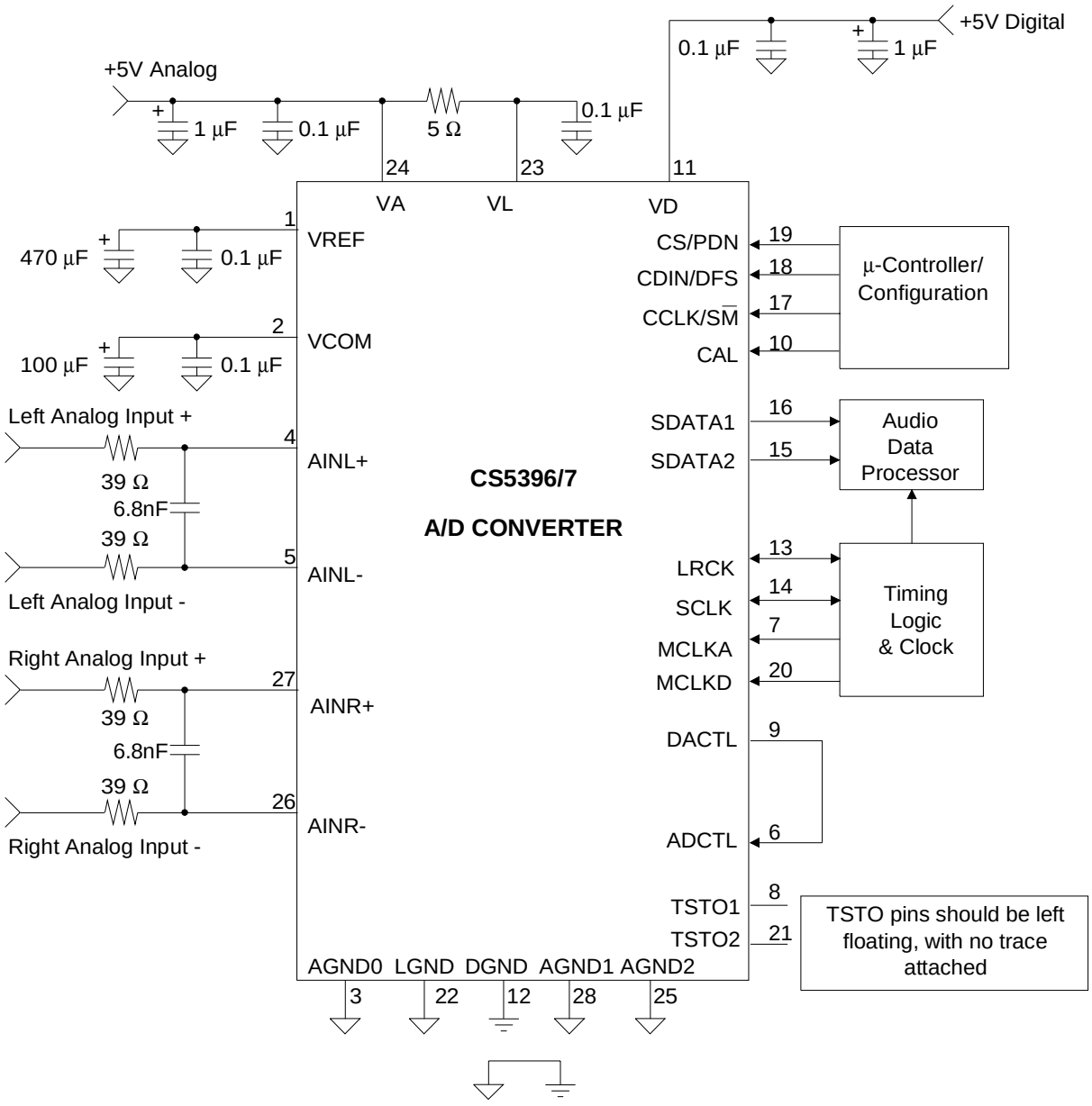



**Figure 1. Typical Connection Diagram**

## GENERAL DESCRIPTION

The CS5396/97 is a 24-bit, stereo A/D converter designed for stereo digital audio applications. The analog input channels are simultaneously sampled by separate, patented, 7th-order tri-level delta-sigma modulators at either 128 or 64 times the output sample rate (64× Fs or 128× Fs) of the device. The resulting serial bit streams are digitally filtered, yielding pairs of 24-bit values at output sample rates (Fs) of up to 100 kHz. This technique yields nearly ideal conversion performance independent of input frequency and amplitude. The converter does not require difficult-to-design or expensive anti-alias filters, and it does not require external sample-and-hold amplifiers or voltage references. Only normal power supply decoupling components, voltage reference bypass capacitors and a single resistor and capacitor on each input for anti-aliasing are required, as shown in Figure 1. An on-chip voltage reference provides for a differential input signal range of 4.0 Vpp. The device also contains a high pass filter, implemented digitally after the decimation filter, to completely eliminate any internal offsets in the converter or any offsets present at the input circuitry to the device. Output data is available in serial form, coded as 2's complement 24-bit numbers. For more information on delta-sigma modulation techniques see the references at the end of this data sheet.

### Stand-Alone vs. Control Port Mode

The CS5396/97 can operate in either Stand-Alone or Control Port Mode. The functionality of pins 17, 18 and 19 is established upon entering either the Stand-Alone or Control Port mode, as described in the Pin Description section.

The Control Port Mode requires a micro-controller and allows access to many additional features, which include:

- 128× Oversampling Mode
- Reduction of 24-bit data to 20, 18 or 16-bit data with psychoacoustically optimized dither
- Programmability of psychoacoustic filter coefficients
- Peak Input Signal Level Monitor with either High Resolution or Bar Graph mode selection
- Signal inversion
- High pass filter defeat
- Mute
- Access to the digital filter to allow the input of external digital audio data to produce a two-to-one decimated output and/or psychoacoustic bit reduction.

## STAND-ALONE MODE

### Master Clock - Stand-Alone Mode

The master clock is the clock source for the delta-sigma modulator sampling (MCLKA) and digital filters (MCLKD). The required MCLKA/D frequency is determined by the desired Fs and must be 256× Fs. Table 1 shows some common master clock frequencies.

| LRCK (kHz) | MCLKA/D (MHz) | SCLK (MHz) |
|---|---|---|
| 32 | 8.192 | 2.048 |
| 44.1 | 11.2896 | 2.822 |
| 48 | 12.288 | 3.072 |
| 64 | 16.384 | 4.096 |
| 88.2 | 22.5792 | 5.6448 |
| 96 | 24.576 | 6.144 |

**Table 1. Common Clock Frequencies for Stand-Alone Mode**

### Serial Data Interface - Stand-Alone Mode

The CS5396/97 supports two serial data formats which are selected via the digital format select pin, DFS. The digital output format determines the relationship between the serial data, left/right clock and serial clock. Figures 2 and 3 detail the interface for-

mats. The serial data interface is accomplished via the serial data outputs; SDATA1 and SDATA2; serial data clock, SCLK, and the left/right clock, LRCK. The serial nature of the output data results in the left and right data words being read at different times. However, the samples within an LRCK cycle represent simultaneously sampled analog inputs.

### *Serial Data- Stand-Alone Mode*

The serial data block consists of 24 bits of audio data presented in 2's-complement format with the MSB-first. The data is clocked from SDATA1 and SDATA2 by the serial clock and the channel is determined by the Left/Right clock. The full precision 24-bit data is available on SDATA1 and the output from the low group delay filter is available on SDATA2.

### *Serial Clock - Stand-Alone Mode*

The serial clock shifts the digitized audio data from the internal data registers via the SDATA1 and SDATA2 pins. SCLK is an output in Master Mode where internal dividers will divide the master clock by 4 to generate a serial clock which is 64× Fs. In Slave Mode, SCLK is an input with a serial clock typically between 48× and 128× Fs. However, it is recommended that SCLK be equal to 64×, though other frequencies are possible, to avoid potential interference effects which may degrade system performance.

### *Left/Right Clock - Stand-Alone Mode*

The Left/Right clock, LRCK, determines which channel, left or right, is to be output on SDATA1 and SDATA2. In Master Mode, LRCK is an output whose frequency is equal to Fs. In Slave Mode, LRCK is an input whose frequency must be equal to Fs and synchronous to MCLKA/D.

### Master Mode - Stand-Alone Mode

In Master mode, SCLK and LRCK are outputs which are internally derived from the master clock. Internal dividers will divide MCLKA/D by 4 to generate a SCLK which is 64× Fs and by 256 to generate a LRCK which is equal to Fs. The CS5396/97 is placed in the Master mode with the slave/master pin, S/$\overline{M}$, low.

### Slave Mode - Stand-Alone Mode

LRCK and SCLK become inputs in SLAVE mode. LRCK must be externally derived from MCLKA/D and be equal to Fs. It is recommended that SCLK be equal to 64×. Other frequencies between 48× and 128× Fs are possible but may degrade system performance due to interference effects. The master clock frequency must be 256× Fs. The CS5396/97 is placed in the Slave mode with the slave/master pin, S/$\overline{M}$, high.

### High Pass Filter - Stand-Alone Mode

The CS5396/97 includes a high pass filter after the decimator to remove the DC offsets introduced by the analog buffer stage and the CS5396/97 analog modulator. The characteristics of this first-order high pass filter are outlined below, for Fs equal to 48 kHz. This filter response scales linearly with sample rate.

| | |
|---|---|
| Frequency response: | -3 dB @ 1.8 Hz |
| | -0.036 dB @ 20 Hz |
| Phase deviation: | 5.3 degrees @ 20 Hz |
| Passband ripple: | None |

### Power-up and Calibration - Stand-Alone Mode

The delta-sigma modulators settle in a matter of microseconds after the analog section is powered, either through the application of power or by exiting the power-down mode. However, the voltage reference will take a much longer time to reach a final value due to the presence of external capacitance on the VREF pin. A time delay of approximately 10ms/µF is required after applying power to the device or after exiting a power down state.

A calibration of the tri-level delta-sigma modulator should always be initiated following power-up and after allowing sufficient time for the voltage on the external VREF capacitor to settle. This is required to minimize noise and distortion. It is also advised that the CS5396/97 be calibrated after the device has reached thermal equilibrium, approximately 10 seconds, to maximize performance.

### Synchronization of Multiple Devices - Stand Alone Mode

In systems where multiple ADCs are required, care must be taken to achieve simultaneous sampling. It is recommended that the rising edge of the CAL signal be timed with a falling edge of MCLK to ensure that all devices will initiate a calibration and synchronization sequence on the same rising edge of MCLK. The absence of re-timing of the CAL signal can result in a sampling difference of one MCLK period.

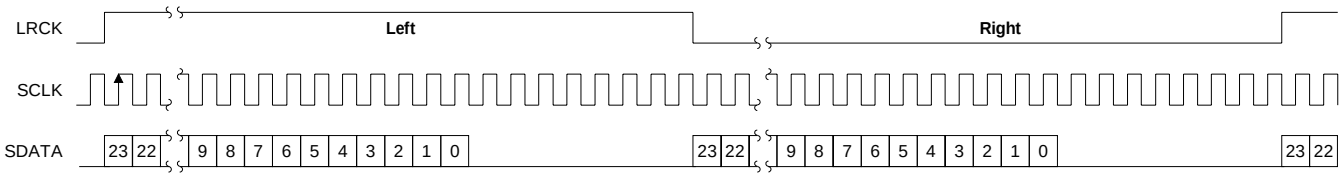
## CONTROL PORT MODE

### Access to Control Port Mode

The mode selection between Stand-Alone and Control Port Mode is determined by the state of the SDATA1 pin 250 MCLK cycles following the internal power-on reset. A 47 kΩ pull-up resistor on SDATA1 will select the Control Port Mode. However, the control port will not respond to CCLK and CDIN until the pull-up on the SDATA1 pin is released.

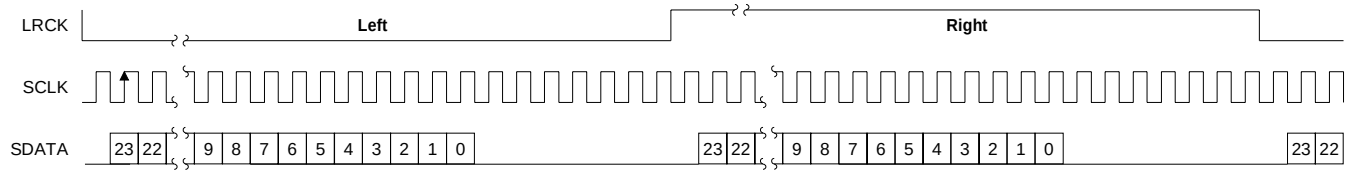
#### *Internal Power-On Reset*

The timing required to determine Control port mode and $I^2S$/SPI mode is based on an internal power-on reset. The internal power-on reset requires the power supply to exceed a threshold voltage. However, there is no external indication of when the internal reset is activated. If precise timing of the Control port and $I^2S$/SPI decisions is required, MCLK should not be applied until the power supply has stabilized.




| MASTER | SLAVE |
|---|---|
| 24-Bit Left Justified Data | 24-Bit Left Justified Data |
| Data Valid on Rising Edge of 64x SCLK | Data Valid on Rising Edge of SCLK |
| MCLK equal to 256x Fs | MCLK equal to 256x Fs |

**Figure 2. Serial Data Format 0, Stand-Alone Mode, DFS low. Left Justified.**




| MASTER | SLAVE |
|---|---|
| $I^2S$ 24-Bit Data | $I^2S$ 24-Bit Data |
| Data Valid on Rising Edge of 64x SCLK | Data Valid on Rising Edge of SCLK |
| MCLK equal to 256x Fs | MCLK equal to 256x Fs |

**Figure 3. Serial Data Format 1, Stand-Alone Mode, DFS High. $I^2S$ compatible**

## Master Clock - Control Port Mode

The master clock is the clock source for the delta-sigma modulator sampling (MCLKA) and digital filters (MCLKD). The required MCLKA/D frequency is determined by the desired Fs and the chosen Oversampling Mode. Table 2 shows some common master clock frequencies.

## 64× vs. 128× Oversampling Modes

The CS5396/97 can operate in a 64× Oversampling Mode with a 256× master clock (MCLKA/D) at a maximum sample rate of 100 kHz. The device can also operate in a 128× Oversampling Mode with a 512× master clock (MCLKA/D) where the maximum Fs is 50 kHz. Notice that the required master clock is 24.576 MHz for Fs equal to either 48 kHz in the 128× Oversampling Mode or 96 kHz in the 64× Oversampling Mode. The sampling mode is set via the control register which alters the decimation ratio of the digital filter. The 64× Oversampling Mode is the default mode. Table 2 shows some common clock frequencies for both modes. Refer to Appendix A for additional discussion of 64× vs. 128× Oversampling Modes.

| LRCK (kHz) | Over-sampling | MCLKA/D (MHz) | SCLK (MHz) |
|---|---|---|---|
| 32 | 64 | 8.192 | 2.048 |
| 44.1 | 64 | 11.2896 | 2.822 |
| 48 | 64 | 12.288 | 3.072 |
| 32 | 128 | 16.384 | 4.096 |
| 44.1 | 128 | 22.5792 | 5.6448 |
| 48 | 128 | 24.576 | 6.144 |
| 64 | 64 | 16.384 | 4.096 |
| 88.2 | 64 | 22.5792 | 5.6448 |
| 96 | 64 | 24.576 | 6.144 |

**Table 2. Common Clock Frequencies**

## Serial Data Interface - Control Port Mode

The CS5396/97 supports two serial data formats which are selected via the control register. The digital output format determines the relationship between the serial data, left/right clock and serial clock. Figures 4 - 7 detail the interface formats. The serial data interface is accomplished via the serial data outputs; SDATA1 and SDATA2, serial data clock, SCLK, and the left/right clock, LRCK. The serial nature of the output data results in the left and right data words being read at different times. However, the samples within an LRCK cycle represent simultaneously sampled analog inputs.

### *Serial Data - Control Port Mode*

The serial data block is presented in 2's-complement format with the MSB-first. The data is clocked from SDATA1 and SDATA2 by the serial clock and the channel is determined by the Left/Right clock. The full precision 24 bit data is available on SDATA1 and the output from the low group delay is available on SDATA2.

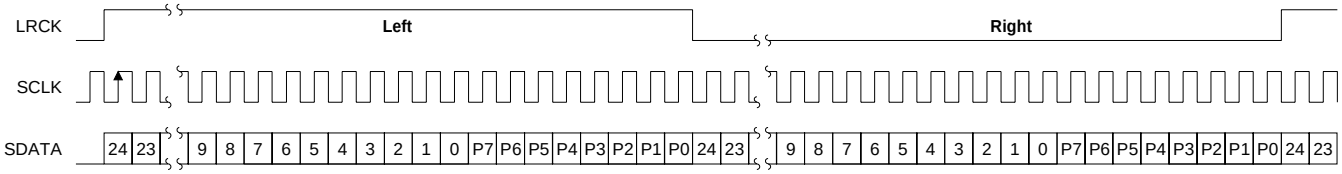
The serial data can be followed by 8 Peak Signal Level, PSL, bits as shown in Figures 4 - 7 if the PKEN bit is set. Refer to the Dual Audio Output section of this data sheet for further discussion of SDATA1 and SDATA2 options.

### *Serial Clock - Control Port Mode*

The serial clock shifts the digitized audio data from the internal data registers via SDATA1 and SDATA2. SCLK is an output in Master Mode where internal dividers will divide the master clock by 4 to generate a serial clock which is 64× Fs in the 64× Oversampling Mode. In the 128× Oversampling Mode, internal dividers will divide MCLKA/D by 4 to generate a SCLK which is 128× Fs. In Slave Mode, SCLK is an input with a serial clock typically between 48× and 128× Fs. It is recommended that SCLK be equal to 64× in the 64× Oversampling Mode and equal to 128× in the 128× Oversampling Mode to avoid possible system performance degradation due to interference effects.

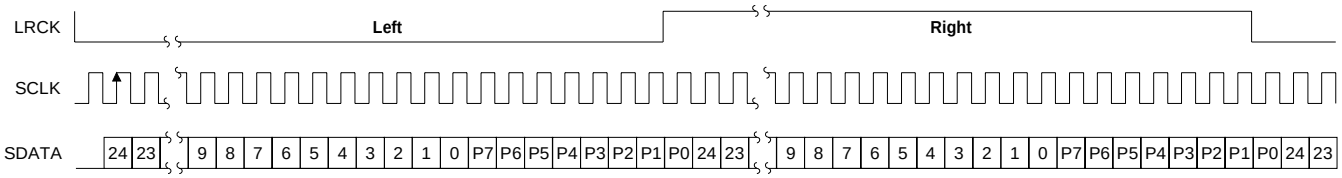
### *Left/Right Clock -Control Port Mode*

The Left/Right clock, LRCK, determines which channel, left or right, is to be output on SDATA1



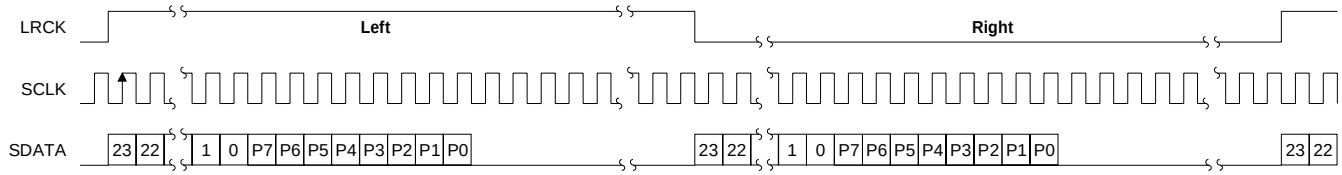

| MASTER | SLAVE |
|---|---|
| 24-Bit Left Justified Data | 24-Bit Left Justified Data |
| Data Valid on Rising Edge of 64x SCLK | Data Valid on Rising Edge of SCLK |
| MCLK equal to 256x Fs | MCLK equal to 256x Fs |

**Figure 4. Control Port Mode, Serial Data. Left Justified. 64x Oversampling Mode**
The peak signal level bits are available only if Bit 6 of Byte 7 is set.



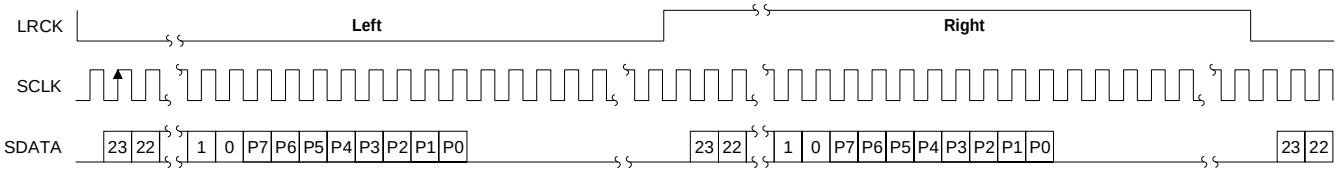

| MASTER | SLAVE |
|---|---|
| $I^2S$ 24-Bit Data | $I^2S$ 24-Bit Data |
| Data Valid on Rising Edge of 64x SCLK | Data Valid on Rising Edge of SCLK |
| MCLK equal to 256x Fs | MCLK equal to 256x Fs |

**Figure 5. Control Port Mode, Serial Data. $I^2S$ Compatible. 64x Oversampling Mode.**
The peak signal level bits are available only if Bit 6 of Byte 7 is set.




| MASTER | SLAVE |
|---|---|
| 24-Bit Left Justified Data | 24-Bit Left Justified Data |
| Data Valid on Rising Edge of 128x SCLK | Data Valid on Rising Edge of SCLK |
| MCLK equal to 512x Fs | MCLK equal to 512x Fs |

**Figure 6. Control Port Mode, Serial Data. Left Justified. 128x Oversampling Mode**
The peak signal level bits are available only if Bit 6 of Byte 7 is set.




| MASTER | SLAVE |
|---|---|
| $I^2S$ 24-Bit Data | $I^2S$ 24-Bit Data |
| Data Valid on Rising Edge of 128x SCLK | Data Valid on Rising Edge of SCLK |
| MCLK equal to 512x Fs | MCLK equal to 512x Fs |

**Figure 7. Control Port Mode, Serial Data. $I^2S$ Compatible. 128x Oversampling Mode.**
The peak signal level bits are available only if Bit 6 of Byte 7 is set.

and SDATA2. In Master Mode, LRCK is an output whose frequency is equal to Fs. In Slave Mode, LRCK is an input whose frequency must be equal to Fs and synchronous to MCLKA/D.

### Master Mode- Control Port Mode

In Master mode, SCLK and LRCK are outputs which are internally derived from the master clock. In the 64× Oversampling Mode, internal dividers will divide MCLKA/D by 4 to generate a SCLK which is 64× Fs and by 256 to generate a LRCK which is equal to Fs. In the 128× Oversampling Mode, internal dividers will divide MCLKA/D by 4 to generate a SCLK which is 128× Fs and by 512 to generate a LRCK which is equal to Fs. The CS5396/97 is placed in the Master mode via the control register.

### Slave Mode - Control Port Mode

LRCK and SCLK become inputs in SLAVE mode. LRCK must be externally derived from MCLKA/D and be equal to Fs. It is recommended that SCLK be equal to 64× in the 64× Oversampling Mode and equal to 128× in the 128× Oversampling Mode. Other frequencies are possible but may degrade system performance due to interference effects. The CS5396/97 is placed in the Slave mode via the control register.

### Synchronization of Multiple Devices - Control Port Mode

In systems where multiple ADCs are required, care must be taken to achieve simultaneous sampling. The FSTART bit in register 1 controls the synchronization of the internal clocks and sampling process between the analog modulator and the digital filter. Multiple ADCs can be synchronized if the FSTART command is initiated on the same edge of MCLK. This can be accomplished by re-timing the CCLK clock with the falling edge of MCLK. This is a relatively simple matter if the ADCs have the same address. However, if the system requires the devices to have individual addresses, synchronization can be accomplished by;

1) Disable the address enable bit (ADDREN) in register 7

2) Issue a system broadcast FSTART command synchronized with CCLK.

3) Reset the ADDREN bit.

### Power-up and Calibration - Control Port Mode

The delta-sigma modulators settle in a matter of microseconds after the analog section is powered, either through the application of power or by exiting the power-down mode. However, the voltage reference will take a much longer time to reach a final value due to the presence of external capacitance on the VREF pin. A time delay of approximately 10ms/µF is required after applying power to the device or after exiting a power down state.

A calibration of the tri-level delta-sigma modulator should always be initiated following power-up and after allowing sufficient time for the voltage on the external VREF capacitor to settle. This is required to minimize noise and distortion. It is also advised that the CS5396/97 be calibrated after the device has reached thermal equilibrium to maximize performance. A calibration sequence requires the following commands;

1) set the FSTART bit

2) set the GND CAL bit

3) set the CAL bit

4) Wait a minimum of 2050 LRCK periods in the 128x mode or 4100 LRCK periods in the 64x mode.

5) Remove GND CAL

### High Pass Filter -Control Port Mode

The CS5396/97 includes a high pass filter after the decimator to remove the DC offsets introduced by

the analog buffer stage and the CS5396/97 analog modulator. The high pass filter can be defeated with the control register. It is also possible to write to the left/right offset registers to establish a predetermined offset.

The characteristics of this first-order high pass filter are outlined below for Fs equal to 48 kHz. The filter response scales linearly with sample rate.

| | |
|---|---|
| Frequency response: | -3 dB @ 1.8 Hz |
| | -0.036 dB @ 20 Hz |
| Phase deviation: | 5.3 degrees @ 20 Hz |
| Passband ripple: | None |

## Input Level Monitoring - Control Port Mode

The CS5396/97 includes independent Peak Input Level Monitoring for each channel. The analog-to-digital converter continually monitors the peak digital signal for both channels and records these values in the Active registers. This information can be transferred to the Output registers by writing the PU (Peak Update) bit which will also reset the Active register. The Active register contains the peak signal level since the previous peak update request. The 8-bit contents of the output registers are available in both interface modes. The peak signal level information is available in two formats - High Resolution Mode and Bar Graph Mode. The output format is controlled via the control register.

### *High Resolution Mode*

Bits P7-P0 indicate the Peak Signal Level (PSL) since the previous peak update (or previous write of the PU bit). If the ADC input level is less than full-scale, bits P5-P0 represent the peak value from -60 dB to 0 dB of full scale in 1 dB steps. The PSL outputs are accurate to within 0.25 dB. Bit P6 provides a coarse means of determining an ADC input idle condition. Bit P7 indicates an ADC overflow condition if the ADC input level is greater than full-scale.

P7 - Overrange
0 - Analog input less than full-scale level
1 - Analog input greater than full-scale

P6 - Idle channel
0 - Analog input >-60 dB from full-scale
1 - Analog input <-60 dB from full-scale

P5 to P0 - Input Level Bits (1 dB steps)

| Inputs <0 dB | P5 - P0 |
|---|---|
| 0 dB | 000000 |
| -1 dB | 000001 |
| -2 dB | 000010 |
| -60 dB | 111100 |

### *Bar Graph Mode*

This mode provides a decoded output format which indicates the peak input signal level in a “Bar Graph” format which can be used to drive front panel LEDs. This decoded output can be used to drive front panel LEDs.

| Input Level | T7 - T0 |
|---|---|
| Overflow | 11111111 |
| 0 dB to -3 dB | 01111111 |
| -3 dB to -6 dB | 00111111 |
| -6 dB to -10 dB | 00011111 |
| -10 dB to -20 dB | 00001111 |
| -20 dB to -30 dB | 00000111 |
| -30 dB to -40 dB | 00000011 |
| -40 dB to -60 dB | 00000001 |
| < - 60 dB | 00000000 |

## Dual Digital Audio Outputs

The CS5396/97 contains two stereo digital audio output channels - SDATA1 and SDATA2. These audio output channels are completely independent, as SDATA1 can contain 24-bit audio data simultaneous with psychoacoustic audio data on SDATA2. Another example of this independence is 24-bit audio data output on SDATA1 simultaneously with a low group delay output on SDATA2.

The audio output formats are completely programmable through the $I^2C$/SPI µC interface. The output

formats include: inverted output, psychoacoustic output (16-bit, 18-bit, 20-bit), and low group delay output.

### Psychoacoustic Filter

The CS5396/97 includes a programmable 10 tap digital filter which can be used to perform psychoacoustic noise-shaping of the audio spectrum if desired. The filter can implement a variety of 16-bit, 18-bit, or 20-bit noise-shaped responses by setting the digital filter coefficients. Further discussion of the psychoacoustic filter can be found in Appendix C.

Appendix B discusses an application using the psychoacoustic filter independently of the A/D converter function. In this mode, SDATA2 becomes an input to the psychoacoustic filter stage and SDATA1 is the digital audio output.

### Low Group Delay Filter

The characteristics of the low group delay filter are shown in Figures 17 - 24.

### µC Interface Formats

The device supports either SPI or $I^2C$ interface formats. The CS5396/97 monitors the state of $\overline{CS}$ during power-up and will configure to an SPI interface if the pin is held low. Conversely, if the pin is held high, the port will configure to a $I^2C$ interface.

#### *SPI Mode*

In SPI mode, $\overline{CS}$ is the chip select signal, CCLK is the µC bit clock and CDIN is the input data line from the microcontroller. Notice that it is not possible to read the CS5396/97 registers in SPI mode due to the lack of a data output pin.

To write to a register, bring $\overline{CS}$ low. The first 7 bits on CDIN are the chip address, and must be zero. The eighth bit is a read/write indicator ($R/\overline{W}$) which must be low.

The next 8 bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next 8 bits are the data which will be placed into the register designated by the MAP.

The CS5396/97 has a MAP auto increment, which will increment the MAP after each byte is written, allowing block writes of successive registers.

#### *$I^2C$ Mode*

In $I^2C$ mode, CDIN is a bidirectional data line. Data is clocked into and out of the part by CCLK.

The eighth bit of the address byte is the $R/\overline{W}$ bit (high for a read, low for a write). If the operation is a write, the next byte is the Memory Address Pointer which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the Memory Address Pointer will be output. MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. Use of the $I^2C$ bus compatible interface requires a license from Philips. $I^2C$ bus in a registered trademark of Philips Semiconductors.

#### *Establishing the Chip Address in $I^2C$ Mode*

Connecting SDATA1 pin and $\overline{CS}$ to 5 volts during power-up will set the device to the Control Port and $I^2C$ mode. However, the control port will not respond to CCLK and CDATA until the hold on the SDATA1 pin is released. The chip address can be set by:

1) Release the hold on the SDATA1 pin of the device to be addressed.
2) Program the chip address and set the Address Enable bit, addren, which will prevent further communication to this device without the correct address.
3) Repeat steps 1 and 2 for the remaining devices on the bus.

## ANALOG CONNECTIONS - ALL MODES

Figure 1 shows the analog input connections. The analog inputs are presented differentially to the

modulators via the AINR+/- and AINL+/- pins. Each analog input will accept a maximum of 2.0 Vpp. The + and - input signals are 180° out of phase resulting in a differential input voltage of 4.0 Vpp. Figure 8 shows the input signal levels for full scale.

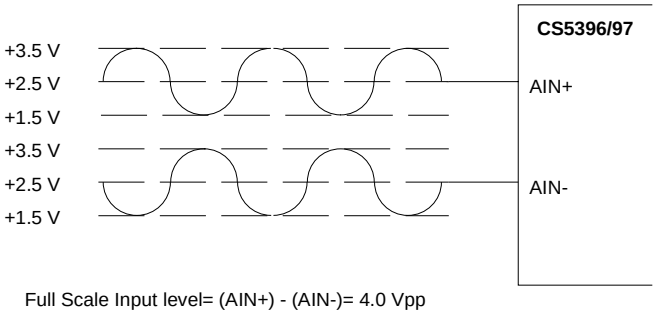



**Figure 8. Full scale input voltage**

The analog modulator samples the input at 6.144 MHz (MCLK=24.576 MHz) corresponding to Fs equal to 48 kHz in the 128× Oversampling Mode and Fs equal to 96 kHz in the 64× Oversampling Mode. The digital filter will reject signals within the stopband of the filter. However, there is no rejection for input signals which are ($n \times 6.144$ MHz) ± the digital passband frequency, where n=0,1,2,...A 39 Ω resistor in series with the analog input and a 6.8 nF COG capacitor between the inputs will attenuate any noise energy at 6.144 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these can degrade signal linearity. If active circuitry precedes the ADC, it is recommended that the above RC filter is placed between the active circuitry and the AINR and AINL pins. The above example frequencies scale linearly with output sample rate.

The on-chip voltage reference and the common mode voltage are available at VREF and VCOM for the purpose of decoupling only. However, due to the sensitivity of this node, the circuit traces attached to these pins must be minimal in length and no load current may be taken from VREF. It is possible to use VCOM as a reference voltage to bias the input buffer circuits, if the circuit trace is very short and VCOM is buffered at the converter (refer to the CDB53965/97). The recommended decoupling scheme for VREF, Figure 1, is a 470 µF electrolytic capacitor and a 0.1 µF ceramic capacitor connected from VREF to AGND. The recommended decoupling scheme for VCOM, Figure 1, is a 100 µF electrolytic capacitor and a 0.1 µF ceramic capacitor connected from VCOM to AGND.

## GROUNDING AND POWER SUPPLY DECOUPLING - ALL MODES

As with any high resolution converter, the ADC requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA and VL connected to a clean +5 V supply. VD, which powers the digital filter, should be run from the system +5 V logic supply, provided that it is not excessively noisy (< ±50 mV pk-to-pk). Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest.

The printed circuit board layout should have separate analog and digital regions and ground planes, with the ADC straddling the boundary. All signals, especially clocks, should be kept away from the VREF pin in order to avoid unwanted coupling into the modulators. The VREF decoupling capacitors, particularly the 0.01 µF, must be positioned to minimize the electrical path from VREF and pin 3, AGND. The CDB5396/97 evaluation board demonstrates the optimum layout and power supply arrangements, as well as allowing fast evaluation of the ADC.

To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

## DIGITAL FILTER PLOTS

Figures 9-24 show the performance of the digital filters included in the ADC. All plots are normalized to Fs. Assuming a sample rate of 48 kHz, the 0.5 frequency point on the plot refers to 24 kHz. The filter frequency response scales precisely with Fs.

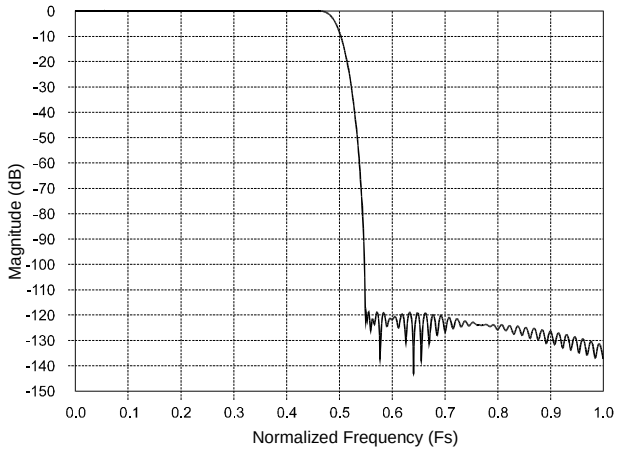



**Figure 9. CS5396 Stop Band Attenuation**

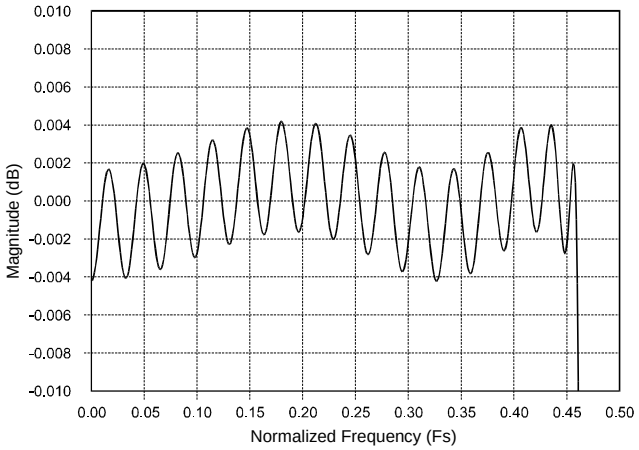



**Figure 10. CS5396 Passband Ripple**

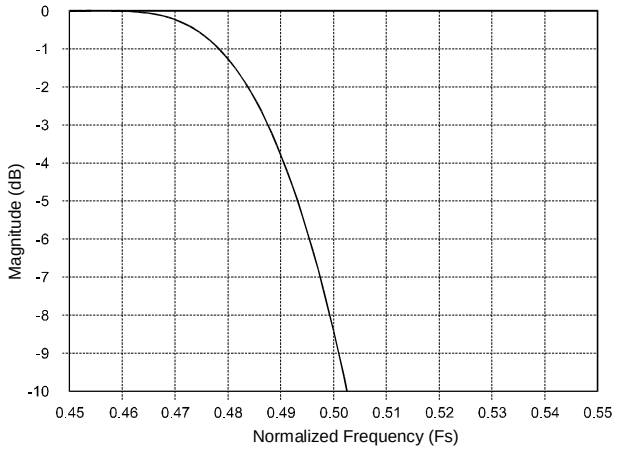



**Figure 11. CS5396 Transition Band**

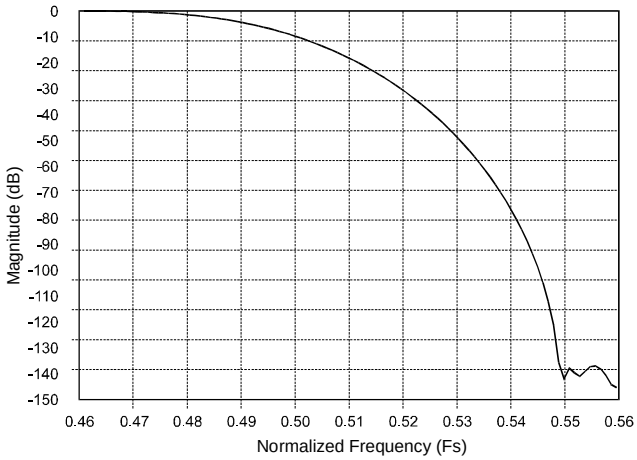



**Figure 12. CS5396 Transition Band**

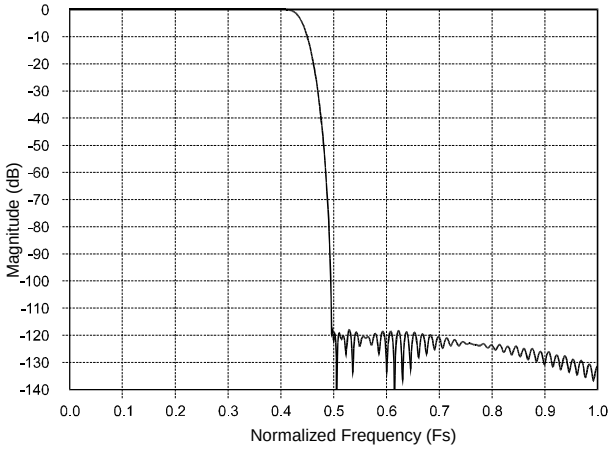



**Figure 13. CS5397 Stop Band Attenuation**

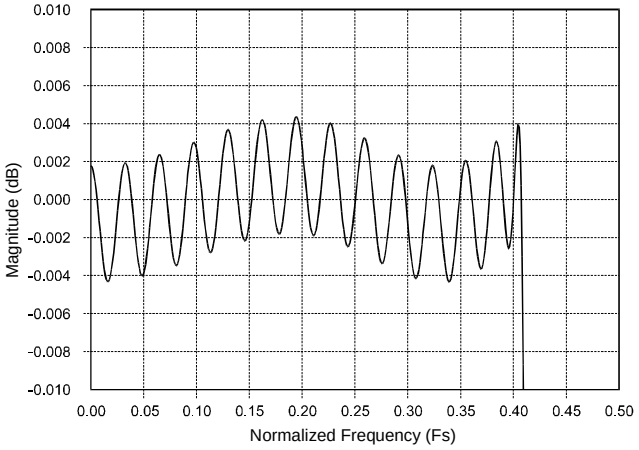



**Figure 14. CS5397 Passband Ripple**

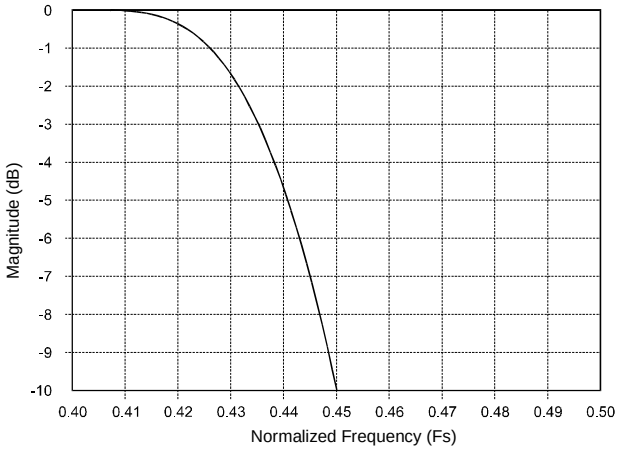



**Figure 15. CS5397 Transition Band**

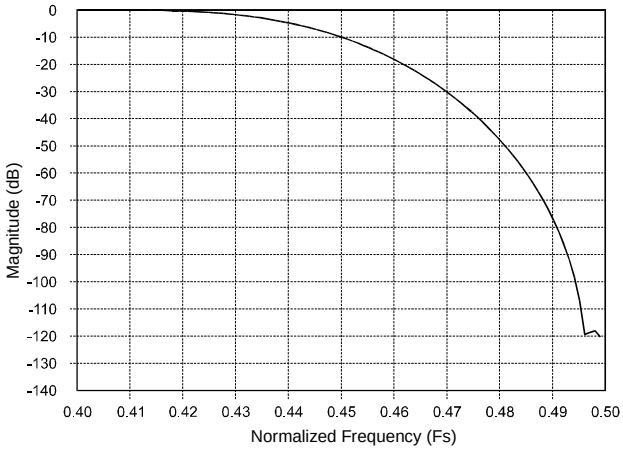



**Figure 16. CS5397 Transition Band**

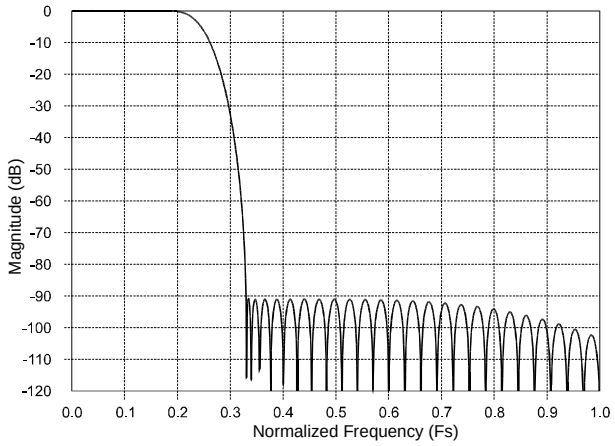



**Figure 17. Low Group Delay Filter Stop Band Attenuation 64x Oversampling Mode**

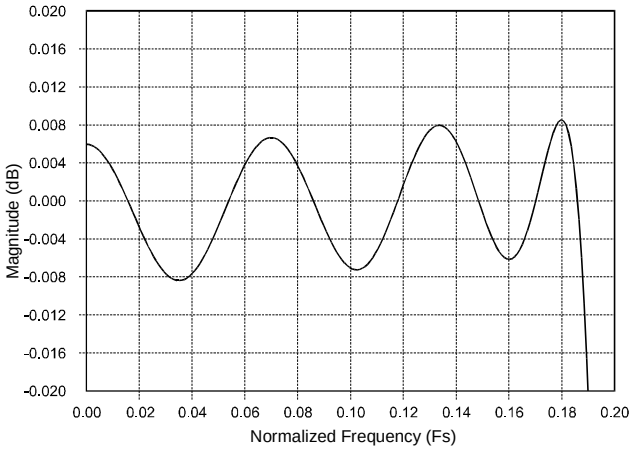



**Figure 18. Low Group Delay Filter Passband Ripple 64x Oversampling Mode**

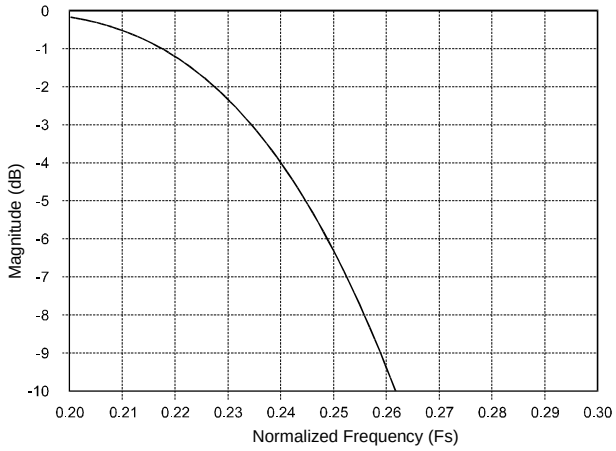



**Figure 19. Low Group Delay Filter Transition Band 64x Oversampling Mode**

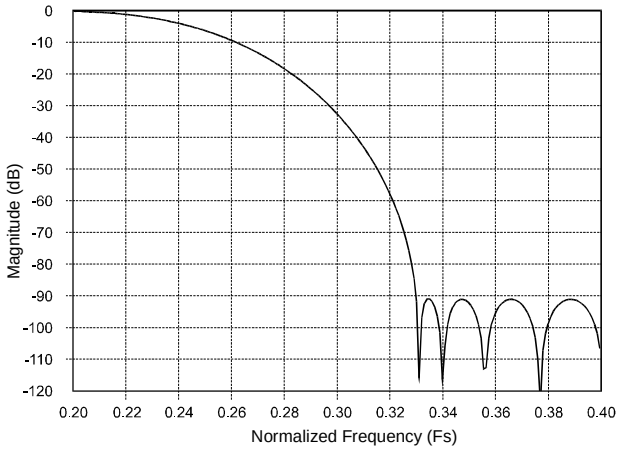



**Figure 20. Low Group Delay Filter Transition Band 64x Oversampling Mode**

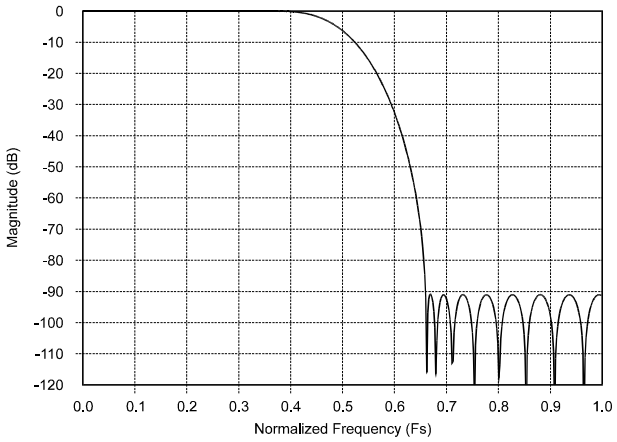



**Figure 21. Low Group Delay Filter Stop Band Attenuation 128x Oversampling Mode**

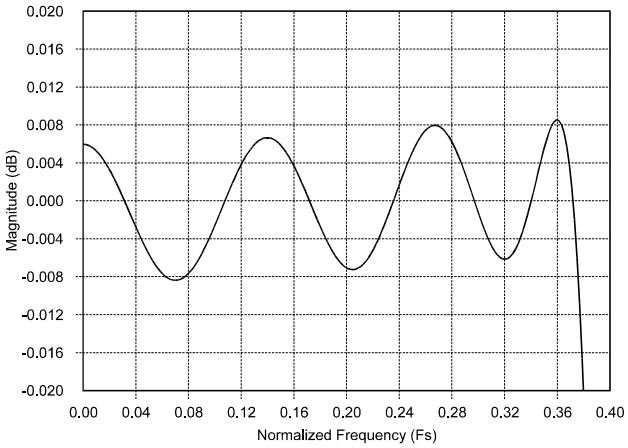



**Figure 22. Low Group Delay Filter Passband Ripple 128x Oversampling Mode**

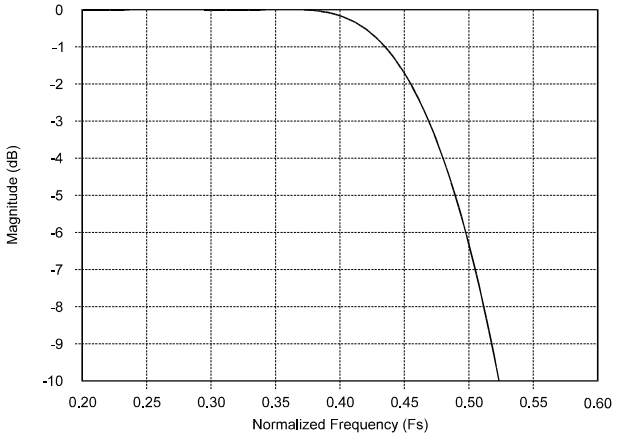



**Figure 23. Low Group Delay Filter Transition Band 128x Oversampling Mode**

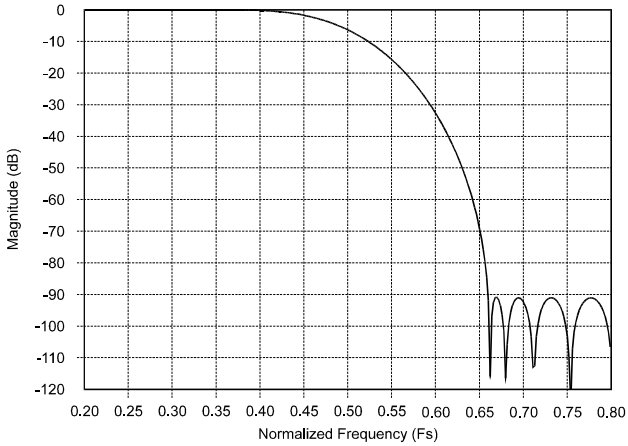



**Figure 24. Low Group Delay Filter Transition Band 128x Oversampling Mode**

## REGISTER DESCRIPTION

** “default” ==> bit status after power-up-sequence

*Analog control (address 00000001)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| fstart | gndcal | aapd | adpd | 1bit | | | |
| 0 | 0 | 0 | 0 | 0 | | | |

FSTART (Frame start)Default = ‘0’.

This bit must be set to ‘1’ to synchronize the modulator output and the decimation filter input and is automatically reset to ‘0’ after a “fstart” pulse is sent to the analog and digital block.

GNDCAL (Ground calibration enable)

Default = ‘0’.

Modulator input is tied to internal “Vcom” when this bit is ‘1’.

AAPD (Analog Section of modulator in power down)

Default = ‘0’.

The analog section of the modulator is in power down mode when aapd = ‘1’.

ADPD (Digital Section of modulator in power down)

Default = ‘0’.

The digital section on the modulator is in power down mode when adpd = ‘1’.

TEST BIT Default =’0’.

Must remain at 0.

*Mode (address 00000010)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 128x/$\overline{64x}$ | cal | change_sign | _LR/LL | _hpen | s/_m | DFS | mute |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

128x/$\overline{64x}$ Default = ‘0’.

Oversampling ratio is 128 when this bit is ‘1’ and 64 when this bit is ‘0’.

CAL (System calibration enable)

Default = ‘0’.

Setting this bit to ‘1’ will initiate calibration.

This bit is automatically reset to ‘0’ following calibration.

Change_sign (Change Sign enable)

Default = ‘0’.

A ‘1’ will interchange the analog input paths within each channel resulting in a phase inversion of the analog signal. This bit applies to both channels.

_LR/LL (Left-Right output disable) Default = ‘0’.

If this bit is ‘0’, SDATA1 will output the Left and Right channel data from the sdata1 source and SDATA2 will output the Left and Right channel data from the sdata2 source as described elsewhere in the data sheet.

If this bit is set to ‘1’, the Left channel data from sdata1 source and sdata2 source (stored in Audio port register) will be sent out in SDATA1. SDATA2 will output all the Right channel data.

HPEN (HP enable) Default = '0'.
The highpass filter will be disabled when _HPEN = '1'. The highpass filter will be automatically enabled following calibration.

S/_M (Slave / Master mode) Default = '0'.
In master mode, LRCK, and SCLK are outputs. In slave mode, LRCK and SCLK are inputs. This bit is ignored when sdata1 is used as input port in "fir2in" or "psychoin" mode (refer to Digital control & Tag register and Appendix B).

DFS (Digital Format Select)Default = '0'.
Output of serial data complies with $I^2S$ standard when DFS is 1. Output of serial data is Left Justified when DFS is 0.

MUTE Default = '0'.
Data at SDATA1 and SDATA2 is always '0' when this set to '1'.

*Audio port (address 00000011)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 24bit (sdata1) | 24bit (sdata2) | psycho (sdata1) | psycho (sdata2) | psel18/_16 | psel20/_16 | lgd (sdata1) | lgd (sdata2) |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

24bit(SDATA1) Default = '1'.
A '1' enables the serial audio port 1 to transmit the 24-bit high precision output.
This bit must be set to '0' to enable other SDATA1 output options.

24bit(SDATA2) Default = '0'.
A '1' enables the serial audio port 2 to transmit 24-bit high precision output. This bit must be set to '0' to enable other SDATA2 output options.

psycho(SDATA1) Default = '0'.
psychoacoustic output will be the data at the serial audio port 1 if this bit is '1' and all other bits of the port are set to '0'.

psycho(SDATA2) Default = '0'.
psychoacoustic output will be the data at the serial audio port 2 if this bit is '1' and all other bits of the port are set to '0'.

psel18/_16(Psycho 18bit or 16bit)
Default = '0'.
This bit indicates the number of output bit if the psychoacoustic filter is chosen as output. A '0' here allows 16 bits output whereas a '1' allows 18 bits output as long as "psel20/_16" is '0'.

psel20/_16(Psycho 20bit)
Default = '0'.
This bit has the highest priority when setting the number of output bit of psychoacoustic filter. If this bit is '1', the output is set to 20-bit regardless of the status of "psel18/_16".

LGD(sdata1) Default = '0'.
24-bit low-group-delay filter output will go through a highpass filter if "_hpen" bit in the Mode register is '0'. The LGD output will be the data at the serial audio port 1 if this bit is '1' and all other bits of the port set to '0'.

LGD(sdata2) Default = '1'.

24-bit low-group-delay filter output will go through a high passfilter if "_hpen" bit in the Mode register is '0'. If "_hpen" is '1', data at the serial audio port will derive directly from the LGD filter output.
If more than 1 bit is set for sdata2, low-group-delay filter output will be selected for output at the port.

*Test Mode 0(address 00000100)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| aoverflow | doverflow | fir1_en | fir1(LRCK) | _psydither | dstart1 | dstart0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

aoverflow — A '1' indicates an overflow condition occurs in the modulator. This bit is reset by reading the register.

doverflow — A '1' indicates an overflow condition occurs in the decimation filter. This bit is reset by reading the register.

fir1_en(sdata) — Default = '0'.
Test purpose only.

fir1L_R(fir1 L channel enable)
Default = '0'.
Test purpose only.

_psydither(psychoacoustic filter dither disable)
Default = '0'.
A '0' means adding dither in the psychoacoustic filter.

dstart1, dstart2(dstart control bits)
Default = '00'.
Test purpose only.

*Test Mode 1(add 00000101)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| test mode. reserved for factory use only | | | | | | | |

FOR FACTORY USE ONLY

*Chip Address (address 00000110)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | caddr6 | caddr5 | caddr4 | caddr3 | caddr2 | caddr1 | caddr0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

caddr(6-0) (chip address (bit6 to bit0))
Default = '0000000'.
This is used to store the programmable chip address for $I^2C$ and SPI mode.
When more than 1 device are connected to the $I^2C$ or SPI buses and using chip address is necessary, chip address set up is done by:
1) Hold the SDATA1 pin of every chip to '1' during power up.

2) Release the SDATA1 pin of the chip that is going to be programmed with chip address.
3) Send chip address and “addren”=’1’ (in Register 7) through the serial control port. (The remaining devices will not repond to this request.)
4) Repeat step 2) and step 3) for to other chips one-by-one. (SDATA1 output is tri-stated until it is released from pull up.)

*Digital Control & Peak Signal Level (address 00000111)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADDREN | pken | pkupdate | hr/_bg | | ddpd | fir2in | psychoin |
| 0 | 0 | 0 | 0 | | 0 | 0 | 0 |

addren(chip address enable)
Default = ‘0’.
When this bit is ‘0’, no chip address comparison is done. The chip will response to all the request from Control Port.
When this bit is ‘1’, the chip responds to the µC only if the chip address from the µC matches the chip address stored in “caddr(6-0)”.

pken(PEAK enable) Default = ‘0’.
PSL bits calculation is based on the high precision 24-bit output.
PSL bits output follows the serial audio port that sends out 24-bit data.
If this bit is disabled, the PSL bits location on the output stream will be replaced by zeros.

pkupdate(PEAK update)
Default = ‘0’.
A ‘0’ to ‘1’ transition will load the peak value (since the last update) to the appropriate serial audio port. The internal peak register will then reset to ‘0’.

hr/_bg(PEAK display format)
Default = ‘0’.
High resolution tag format (hr/_bg=’1’) converts the 24-bit decimation filter output into 1 dB step.
Bar Graph tag format (hr/_bg=’0’) allows LCD display format of the 24-bit output with 8 discrete values.

ddpd(digital filter power down enable)
Default = ‘0’.
The digital filter and serial audio port is in power down mode when ddpd = ‘1’.

fir2in(external fir2 input enable)
Default = ‘0’.
Input of 2nd stage decimation filter is taken from the sdata2 port. The input data will be decimated by 2 and then output to sdata1 of serial audio port.

psychoin (external psychoacoustic filter input enable)
Default = ‘0’.
Input of psychoacoustic filter is taken from the sdata2 port. The 24-bit input data will be truncated in psychoacoustic filter to the chosen output word length and then output to sdata1 of serial audio port.

*R_cal_coeff (address 00001000 - 00001010)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ralpha (bit7) | ralpha (bit6) | ralpha (bit5) | ralpha (bit4) | ralpha (bit3) | ralpha (bit2) | ralpha (bit1) | ralpha (bit0) |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ralpha (bit15) | ralpha (bit14) | ralpha (bit13) | ralpha (bit12) | ralpha (bit11) | ralpha (bit10) | ralpha (bit9) | ralpha (bit8) |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ralpha (bit23) | ralpha (bit22) | ralpha (bit21) | ralpha (bit20) | ralpha (bit19) | ralpha (bit18) | ralpha (bit17) | ralpha (bit16) |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

Default = '0000 0000 0000 0000 0100 0000'. (represents 1)
The right channel calibration factor is stored in these registers with MSB in bit 7 of register address 00001010.
This value is updated after every calibration cycle.
User can read from or write to this calibration factor through the serial control port.

*L_cal_coeff (address 00001011 - 00001101)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| lalpha (bit7) | lalpha (bit6) | lalpha (bit5) | lalpha (bit4) | lalpha (bit3) | lalpha (bit2) | lalpha (bit1) | lalpha (bit0) |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| lalpha (bit15) | lalpha (bit14) | lalpha (bit13) | lalpha (bit12) | lalpha (bit11) | lalpha (bit10) | lalpha (bit9) | lalpha (bit8) |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| lalpha (bit23) | lalpha (bit22) | lalpha (bit21) | lalpha (bit20) | lalpha (bit19) | lalpha (bit18) | lalpha (bit17) | lalpha (bit16) |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

Default = '0000 0000 0000 0000 0100 0000'. (represents 1)
The left channel calibration factor is stored in these registers with MSB in bit 7 of register address 00001101.
This value is updated after every calibration cycle.
User can read from or write to this calibration factor through the serial control port.

*L_offset (address 00001110)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| los(bit13) | los(bit12) | los(bit11) | los(bit10) | los(bit9) | los(bit8) | los(bit7) | los(bit6) |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Default = '0000 0000'.
User can read or write this offset through the serial control port.

*R_offset (address 00001111)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ros(bit13) | ros(bit12) | ros(bit11) | ros(bit10) | ros(bit9) | ros(bit8) | ros(bit7) | ros(bit6) |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Default = '0000 0000'.
User can read or write this offset through the serial control port.

*Psycho coeff (address 00010000 - 00011000)*

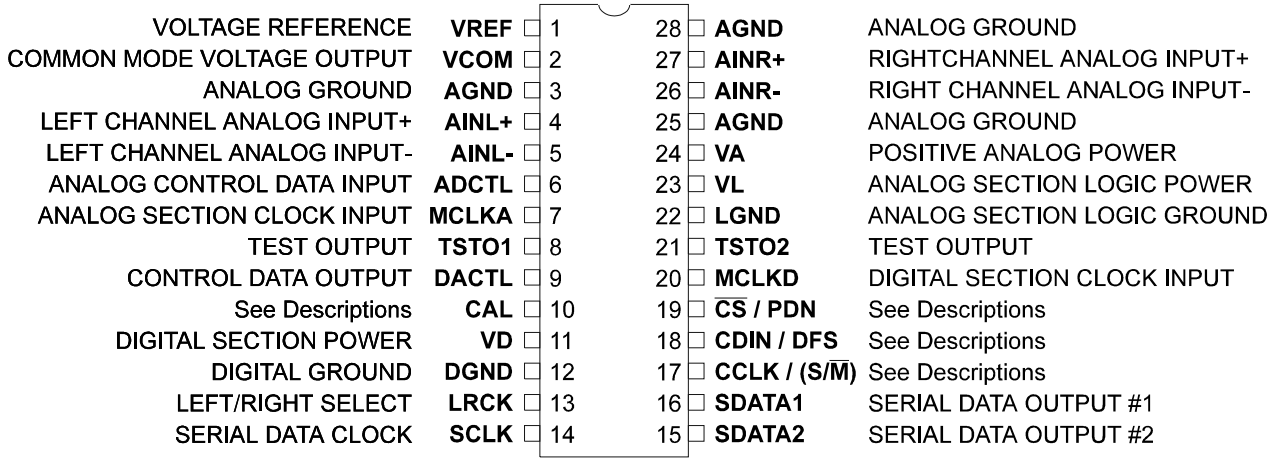
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| pc8(bit8) | pc8(bit7) | pc0(bit5) | pc8(bit4) | pc8(bit3) | pc8(bit2) | pc8(bit1) | pc8(bit0) |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| pc7(bit8) | pc7(bit7) | pc1(bit5) | pc7(bit4) | pc7(bit3) | pc7(bit2) | pc7(bit1) | pc7(bit0) |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| pc6(bit8) | pc6(bit7) | pc2(bit5) | pc6(bit4) | pc6(bit3) | pc6(bit2) | pc6(bit1) | pc6(bit0) |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| pc5(bit8) | pc5(bit7) | pc3(bit5) | pc5(bit4) | pc5(bit3) | pc5(bit2) | pc5(bit1) | pc5(bit0) |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| pc4(bit8) | pc4(bit7) | pc4(bit5) | pc4(bit4) | pc4(bit3) | pc4(bit2) | pc4(bit1) | pc4(bit0) |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| pc3(bit8) | pc3(bit7) | pc5(bit5) | pc3(bit4) | pc3(bit3) | pc3(bit2) | pc3(bit1) | pc3(bit0) |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| pc2(bit8) | pc2(bit7) | pc6(bit5) | pc2(bit4) | pc2(bit3) | pc2(bit2) | pc2(bit1) | pc2(bit0) |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| pc1(bit8) | pc1(bit7) | pc7(bit5) | pc1(bit4) | pc1(bit3) | pc1(bit2) | pc1(bit1) | pc1(bit0) |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| pc0(bit8) | pc0(bit7) | pc8(bit5) | pc0(bit4) | pc0(bit3) | pc0(bit2) | pc0(bit1) | pc0(bit0) |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

H1 Default = ‘1101 1010’.
H2 Default = ‘0011 0101’.
H3 Default = ‘1100 0010’.
H4 Default = ‘0100 0011’.
H5 Default = ‘1100 1011’.

Please see Appendix C at the end of this document

of binary point. User can read or write one or all of the coefficients through the serial control port.

## PIN DESCRIPTIONS




### *Power Supply Connections*

**VA - Positive Analog Power, Pin 24.**

Positive analog supply. Nominally +5 volts.

**VL - Positive Logic Power, Pin 23.**

Positive logic supply for the analog section. Nominally +5 volts.

**AGND - Analog Ground, Pin 3, 25 and 28.**

Analog ground reference.

**LGND - Logic Ground, Pin 22**

Ground for the logic portions of the analog section.

**VD - Positive Digital Power, Pin 11.**

Positive supply for the digital section. Nominally +5 volts.

**DGND - Digital Ground, Pin 12.**

Digital ground for the digital section.

### *Analog Inputs*

**AINR-, AINR+ - Differential Right Channel Analog Inputs, Pin 26, 27.**

Analog input connections for the right channel differential inputs. Nominally 4.0 Vpp differential for full-scale digital output.

**AINL-, AINL+ - Differential Left Channel Analog Inputs, Pin 4,5.**

Analog input connections for the left channel differential inputs. Nominally 4.0 Vpp differential for full-scale digital output.

## *Analog Outputs*

**VCOM - Common Mode Voltage Output, Pin 2.**

Nominally +2.5 volts. Requires a 100 µF electrolytic capacitor in parallel with 0.1 µF ceramic capacitor for decoupling to AGND. Caution is required if this output is to be used to bias the analog input buffer circuits. Refer to text.

**VREF - Voltage Reference Output, Pin 1.**

Nominally +4.0 volts. Requires a 470 µF electrolytic capacitor in parallel with 0.1 µF ceramic capacitor for decoupling to AGND.

## *Digital Inputs*

**ADCTL - Analog Control Input, Pin 6.**

Must be connected to DACTL. This signal enables communication between the analog and digital circuits.

**MCLKA - Analog Section Input Clock, Pin 7.**

This clock is internally divided and controls the delta-sigma modulators. The required MCLKA frequency is determined by the desired output sample rate (Fs). MCLKA of 24.576 MHz corresponds to an Fs of 96 kHz in 64x Oversampling Mode and 48 kHz in 128x Oversampling Mode.

**MCLKD - Digital Section Input Clock, Pin 20.**

MCLKD clocks the digital filter and must be connected to MCLKA. The required MCLKD frequency is determined by the desired output sample rate (Fs). MCLKD of 24.576 MHz corresponds to an Fs of 96 kHz in 64x Oversampling Mode and 48 kHz in 128x Oversampling Mode.

## *Digital Input Pin Definitions for Stand-Alone MODE*

**DFS - Digital Format Select, Pin 18.**

The relationship between LRCK, SCLK and SDATA is controlled by the DFS pin. When high, the serial output data format is $I^2S$ compatible. The serial data format is left-justified when low.

**PDN - Power-Down, Pin 19.**

When high, the device enters power-down. Upon returning low, the device enters normal operation. Calibration of the device is required following release of power-down.

**S/$\overline{M}$ - Slave or Master Mode, Pin 17.**

When high, the device is configured for Slave mode where LRCK and SCLK are inputs. The device is configured for Master mode where LRCK and SCLK are outputs when S/$\overline{M}$ is low.

**CAL - Calibration, Pin 10.**

Activates the calibration of the tri-level delta-sigma modulator.

## *Digital Pin Definitions for CONTROL-PORT MODE*

**CDIN - Control Port Data Input, Pin 18.**

Control port data input for SPI mode.
Control port data input and output for $I^2C$ mode.

**CS - Chip Select Input, Pin 19.**

Control port chip select for SPI mode. The CS5396/97 monitors the state of $\overline{CS}$ during power-up and will configure to an SPI interface if this pin is held low. Conversely, if held high, the port will configure to a $I^2C$ interface.

**CCLK - Control Port Clock Input, Pin 17.**

Control port clock input pin for both $I^2C$ and SPI modes.

**CAL - Calibration, Pin 10.**

CAL pin is not functional in Control Port Mode and should be connected to ground.

## *Digital Outputs*

**DACTL- Digital to Analog Control Output, Pin 9.**

Must be connected to ADCTL. This signal enables communication from the digital circuits to the analog circuits.

**SDATA1 - Digital Audio Data Output #1, Pin 16.**

*Stand-Alone Mode* - The 24-bit audio data is presented MSB first, in 2's complement format.
*Control Port Mode* - The 24 audio data bits are presented MSB first, in 2's complement format. The audio data can be followed by 8 Peak Signal Level bits which indicate the peak signal level. The additional audio data options include; 16, 18, or 20-bit data with or without psychoacoustically optimized dither; or the output of the Low Group Delay filter. The SDATA1 output is completely independent from SDATA2. The mode selection between Stand-Alone and Control Port mode is determined by the state of the SDATA1 pin during power-up. A 47 kΩ pull-up resistor on SDATA1 will select the Control Port mode. However, the control port will not response to CCLK and CDIN until the pull-up on the SDATA1 pin is released.

**SDATA2 - Digital Audio Data Output #2, Pin 15.**

*Stand-Alone Mode* - The 24-bit low group delay audio data is presented MSB first, in 2's complement format.

*Control Port Mode* - The 24-bit low group delay audio data is presented MSB first, in 2's complement format. The audio data can be followed by 8 peak detect bits which indicate the peak signal level. The additional audio data options include; the standard 24-bit word; 16, 18, or 20-bit data with or without psychoacoustically optimized dither. The SDATA2 output is completely independent from SDATA1.

## ***Digital Inputs or Outputs***

**LRCK - Left/Right Clock, Pin 13.**

LRCK determines which channel, left or right, is to be output on SDATA1 and SDATA2. In master mode, LRCK is an output whose frequency is equal to Fs. In Slave Mode, LRCK is an input whose frequency must be equal to Fs. Although the outputs for each channel are transmitted at different times, Left/Right pairs represent simultaneously sampled analog inputs.

*Stand-Alone Mode* - The relationship between LRCK, SCLK and SDATA is controlled by the Digital Format Select (DFS) pin.

*Control Port Mode* - The relationship between LRCK, SCLK and SDATA is controlled by the control register.

**SCLK - Serial Data Clock, Pin 14.**

*Stand-Alone Mode*- Clocks the individual bits of the serial data from SDATA1 and SDATA2. In master mode, SCLK is an output clock at 64x Fs. In slave mode, SCLK is an input which requires a continuously supplied clock at any frequency from 48x to 128x Fs (64x is recommended). The relationship between LRCK, SCLK and SDATA is controlled by the Digital Format Select (DFS) pin.

*Control Port Mode* - Clocks the individual bits of the serial data from SDATA1 and SDATA2. In master mode, SCLK is an output clock at 128x the output sample rate in the 128x Oversampling Mode and 64x the output sample rate in the 64x Oversampling Mode.

In slave mode, SCLK is an input, which requires a continuously supplied clock at any frequency from 32x to 128x the output sample rate. A 128x SCLK is preferred in the 128x Oversampling Mode and 64x SCLK is preferred in the 64x Oversampling Mode. The relationship between LRCK, SCLK and SDATA is controlled by the control register.

## ***Miscellaneous***

**TSTO1, TSTO2 - Test Outputs, Pins 8 and 21.**

These pins are intended for factory test outputs. They must not be connected to any external component or any length of circuit trace.

## PARAMETER DEFINITIONS

### Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

### Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

### Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

### Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

### Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

### Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

### Gain Drift

The change in gain value with temperature. Units in ppm/°C.

### Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

## ADDITIONAL INFORMATION


1) "Techniques to Measure and Maximize the Performance of a 120 dB, 24-bit, 96 kHz A/D Integrated Circuit" by Steven Harris, Steven Green and Ka Leung. Paper presented at the 103rd Convention of the Audio Engineering Society, September 1997.

2) "A 120 dB Dynamic Range, 96 kHz, 24-bit Analog-to-Digital Converter" by Kafai Leung, Sarah Zhu, Ka Leung and Eric Swanson. Paper presented at the 102nd Convention of the Audio Engineering Society, March 1997.

3) A 5 V, 118 dB Delta Sigma Analog-to-Digital Converter for Wideband Digital Audio by Ka Y. Leung, Eric J. Swanson, Kafai Leung, Sarah S. Zhu. Presented at ISSCC February, 1997, paper FP 13.6

4) "How to Achieve Optimum Performance from Delta-Sigma A/D and D/A Converters" by Steven Harris. Presented at the 93rd Convention of the Audio Engineering Society, October 1992.

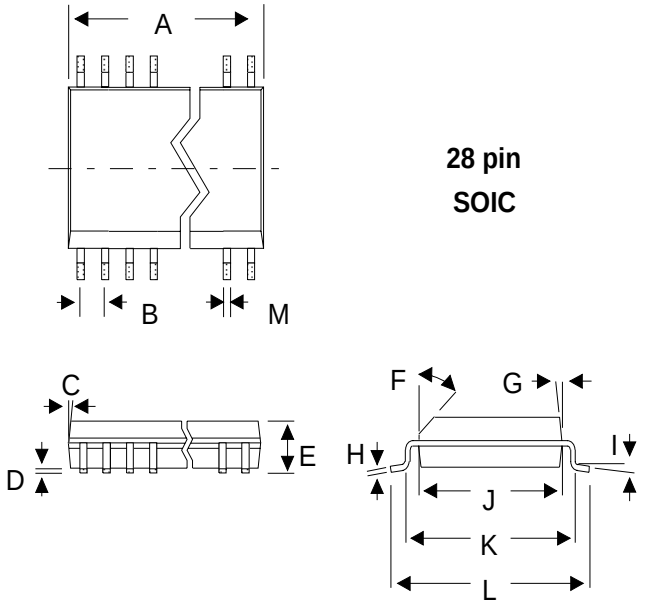
5) "The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADCs" by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

6) "A Fifth-Order Delta-Sigma Modulator with 110 dB Audio Dynamic Range" by I. Fujimori, K. Hamashita and E.J. Swanson. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.

7) "An 18-Bit Dual-Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example" by Clif Sanchez. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

8) "A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio" by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988.

## PACKAGE DIMENSIONS




**28 pin**
**SOIC**

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 17.53 | 18.03 | 0.690 | 0.710 |
| B | 1.27 BSC | | 0.050 BSC | |
| C | 7° NOM | | 7° NOM | |
| D | 0.127 | 0.330 | 0.005 | 0.013 |
| E | 2.41 | 2.67 | 0.095 | 0.105 |
| F | 45° NOM | | 45° NOM | |
| G | 7° NOM | | 7° NOM | |
| H | 0.203 | 0.381 | 0.008 | 0.015 |
| I | 2° | 8° | 2° | 8° |
| J | 7.42 | 7.59 | 0.292 | 0.298 |
| K | 8.76 | 9.02 | 0.345 | 0.355 |
| L | 10.16 | 10.67 | 0.400 | 0.420 |
| M | 0.33 | 0.51 | 0.013 | 0.020 |

## APPENDIX C: PSYCHOACOUSTIC FILTER

The psychoacoustic filter in the CS5396 is based on the paper: "Robert A. Wannamaker, Psychoacoustically Optimal Noise Shaping, Journal of the Audio Engineering Society, Vol 40, No 7/8, 1992 July/August." The default coefficients in the CS5396 are the FIR 9-tap filter coefficients described in Table 3 of the paper. Since the effective noise shaping function is (1-H), the CS5396 registers save the (1-H) function coefficients. Therefore, the negative of each filter coefficient is stored in the registers. Each coefficient is represented as a binary 2's complement number where the 4 MSB's represent the whole number of the coefficient and the 4 LSB's represent the fractional portion truncated to 4 binary bits.

Default Coefficients as listed in "Robert A. Wannamaker, Psychoacoustically Optimal Noise Shaping"

a1 = 2.412
a2 = -3.370
a3 = 3.937
a4 = -4.174
a5 = 3.353
a6 = -2.205
a7 = 1.281
a8 = -0.569
a9 = 0.0847

Coefficient conversion example 1:

a1 = 2.412

a1 = (0010.0110) binary repesentation with the fractional portion truncated to 4 bits.

-a1 = -(0010.0110) binary representation

-a1 = 1101.1010 in two's complement

this value is stored in register 10h.

Coefficient conversion example 2:

a2 = -3.370

-a2 = 3.370

-a2 = 0011.0101 binary repesentation with the fractional portion truncated to 4 bits.

-a2 = 0011.0101 in 2's complement

this value is stored in register 11h.

**PSYCHO-ACOUSTIC FILTER COEFFICIENTS**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MSB | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | LSB |

*Access:*

R/W in I2C and write only in SPI

*Filter coefficient a1 (address 10h)*

*Filter coefficient a2 (address 11h)*

*Filter coefficient a3 (address 12h)*

*Filter coefficient a4 (address 13h)*

*Filter coefficient a5 (address 14h)*

*Filter coefficient a6 (address 15h)*

*Filter coefficient a7 (address 16h)*

*Filter coefficient a8 (address 17h)*

*Filter coefficient a9 (address 18h)*

*Default:*

a1 - 1101 1010
a2 - 0011 0101
a3 - 1100 0010
a4 - 0100 0011
a5 - 1100 1011
a6 - 0010 0011
a7 - 1110 1100
a8 - 0000 1001
a9 - 1111 1111




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