CS5155H

CPU 5-Bit Synchronous Buck Controller

Description

The CS5155H is a 5-bit synchronous dual N-Channel buck controller. It is designed to provide unprecedented transient response for today's demanding high-density, high-speed logic. The regulator operates using a proprietary control method, which allows a 100ns response time to load transients. The CS5155H is designed to operate over a 4.25-20V range (V_{CC}) using 12V to power the IC and 5V or 12V as the main supply for conversion.

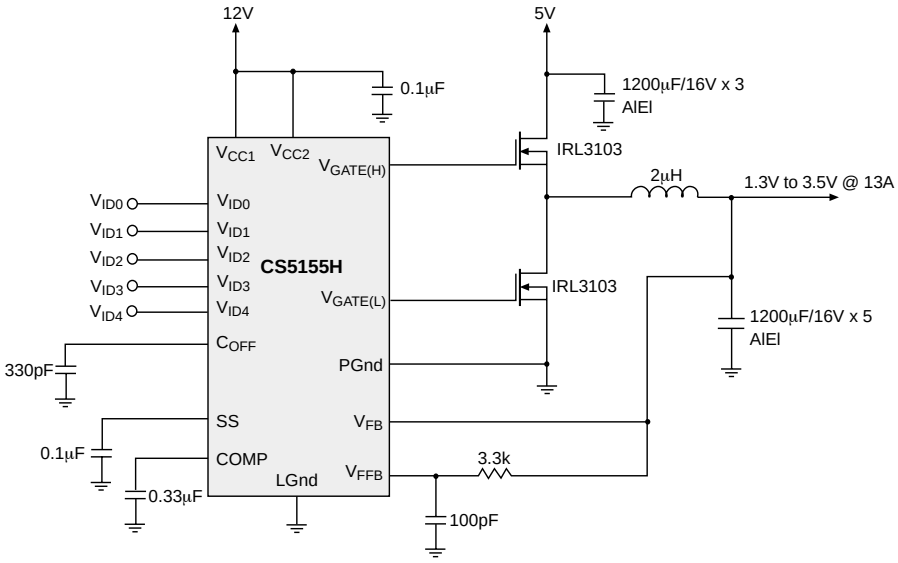
The CS5155H is specifically designed to power Pentium® II processors and other high performance core logic. It includes the following features: on board, 5-bit DAC, short circuit protection, 1.0% output tolerance, V_{CC} monitor, and programmable soft start capability. The CS5155H is backwards compatible with the 4 bit CS5150, allowing the mother board designer the capability of using either the CS5150 or the CS5155H with no change in layout. The CS5155H is available in 16 pin surface mount.

Features

- **Dual N-Channel Design**
- **Excess of 1MHz Operation**
- **100ns Transient Response**
- **5-Bit DAC**
- **Backward Compatible with 4 Bit CS5150H/5151H and Adjustable CS5120/5121**
- **30ns Gate Rise/Fall Times**
- **1% DAC Accuracy**
- **5V & 12V Operation**
- **Remote Sense**
- **Programmable Soft Start**
- **Lossless Short Circuit Protection**
- **V_{CC} Monitor**
- **25ns FET Nonoverlap Time**
- **Adaptive Voltage Positioning**
- **V^{2TM} Control Topology**
- **Current Sharing**
- **Overvoltage Protection**

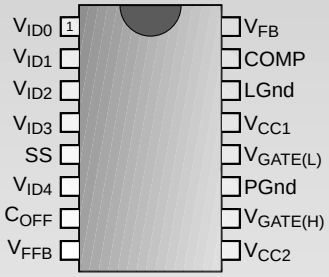
Application Diagram

Switching Power Supply for core logic - Pentium® II processor



Package Options

16 Lead SO Narrow



V^2 is a trademark of Switch Power, Inc.
Pentium is a registered trademark of Intel Corporation.

Cherry Semiconductor Corporation
2000 South County Trail, East Greenwich, RI 02818
Tel: (401)885-3600 Fax: (401)885-5786
Email: info@cherry-semi.com
Web Site: www.cherry-semi.com

Absolute Maximum Ratings

Pin Name	Max Operating Voltage	Max Current
V_{CC1}	16V / -0.3V	25mA DC / 1.5A peak
V_{CC2}	20V / -0.3V	20mA DC / 1.5A peak
SS	6V / -0.3V	-100µA
COMP	6V / -0.3V	200µA
V_{FB}	6V / -0.3V	-0.2µA
C_{OFF}	6V / -0.3V	-0.2µA
V_{FFB}	6V / -0.3V	-0.2µA
V_{ID0} - V_{ID4}	6V / -0.3V	-50µA
$V_{GATE(H)}$	20V / -0.3V	100mA DC / 1.5A peak
$V_{GATE(L)}$	16V / -0.3V	100mA DC / 1.5A peak
LGnd	0V	25mA
PGnd	0V	100mA DC / 1.5A peak

Operating Junction Temperature, T_J . . . . . 0° to 150°C

Lead Temperature Soldering

Wave Solder (through hole styles only) . . . . . 10 sec. max, 260°C peak

Reflow (SMD styles only) . . . . . 60 sec. max above 183°C, 230°C peak

Storage Temperature Range, T_S . . . . . -65° to 150°C

ESD Susceptibility 2kV

Electrical Characteristics: 0°C < T_A < +70°C; 0°C < T_J < +125°C; 8V < V_{CC1} < 14V; 5V < V_{CC2} < 20V;
DAC Code: V_{ID4} = V_{ID2} = V_{ID1} = V_{ID0} = 1; V_{ID3} = 0; $CV_{GATE(L)}$ and $CV_{GATE(H)}$ = 1nF; C_{OFF} = 330pF; C_{SS} = 0.1µF, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Error Amplifier					
V_{FB} Bias Current	V_{FB} = 0V		0.3	1.0	µA
Open Loop Gain	1.25V < V_{COMP} < 4V; Note 1	50	60		dB
Unity Gain Bandwidth	Note 1	500	3000		kH
COMP SINK Current	V_{COMP} = 1.5V; V_{FB} = 3V; V_{SS} > 2V	0.4	2.5	8.0	mA
COMP SOURCE Current	V_{COMP} = 1.2V; V_{FB} = 2.7V; V_{SS} = 5V	30	50	80	µA
COMP CLAMP Current	V_{COMP} = 0V; V_{FB} = 2.7V	0.4	1.0	1.6	mA
COMP High Voltage	V_{FB} = 2.7V; V_{SS} = 5V	4.0	4.3	5.0	V
COMP Low Voltage	V_{FB} =3V		160	600	mV
PSRR	8V < V_{CC1} < 14V @ 1kHz; Note 1	60	85		dB
■ V_{CC1} Monitor					
Start Threshold	Output switching	3.75	3.90	4.05	V
Stop Threshold	Output not switching	3.70	3.85	4.00	V
Hysteresis	Start-Stop		50		mV
■ DAC					
Input Threshold	V_{ID0}, V_{ID1}, V_{ID2}, V_{ID3}, V_{ID4}	1.00	1.25	2.40	V
Input Pull Up Resistance	V_{ID0}, V_{ID1}, V_{ID2}, V_{ID3}, V_{ID4}	25	50	100	kΩ
Pull Up Voltage		4.85	5.00	5.15	V
Accuracy (all codes except 11111)	Measure V_{FB} = V_{COMP}, 25°C ≤ T_J ≤ 125°C			1.0	%
V_{ID4} V_{ID3} V_{ID2} V_{ID1} V_{ID0}					
0 1 1 1 1		1.3266	1.3400	1.3534	V
0 1 1 1 0		1.3761	1.3900	1.4039	V
0 1 1 0 1		1.4256	1.4400	1.4544	V
0 1 1 0 0		1.4751	1.4900	1.5049	V

Electrical Characteristics: 0°C < T_A < +70°C; 0°C < T_J < +125°C; 8V < V_{CC1} < 14V; 5V < V_{CC2} < 20V; DAC Code: V_{ID4} = V_{ID2} = V_{ID1} = V_{ID0} = 1; V_{ID3} = 0; $CV_{GATE(L)}$ and $CV_{GATE(H)}$ = 1nF; C_{OFF} = 330pF; C_{SS} = 0.1µF, unless otherwise specified.

PARAMETER					TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ DAC: continued									
V_{ID4}	V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}					
0	1	0	1	1		1.5246	1.5400	1.5554	V
0	1	0	1	0		1.5741	1.5900	1.6059	V
0	1	0	0	1		1.6236	1.6400	1.6564	V
0	1	0	0	0		1.6731	1.6900	1.7069	V
0	0	1	1	1		1.7226	1.7400	1.7574	V
0	0	1	1	0		1.7721	1.7900	1.8079	V
0	0	1	0	1		1.8216	1.8400	1.8584	V
0	0	1	0	0		1.8711	1.8900	1.9089	V
0	0	0	1	1		1.9206	1.9400	1.9594	V
0	0	0	1	0		1.9701	1.9900	2.0099	V
0	0	0	0	1		2.0196	2.0400	2.0604	V
0	0	0	0	0		2.0691	2.0900	2.1109	V
1	1	1	1	1		1.2191	1.2440	1.2689	V
1	1	1	1	0		2.1186	2.1400	2.1614	V
1	1	1	0	1		2.2176	2.2400	2.2624	V
1	1	1	0	0		2.3166	2.3400	2.3634	V
1	1	0	1	1		2.4156	2.4400	2.4644	V
1	1	0	1	0		2.5146	2.5400	2.5654	V
1	1	0	0	1		2.6136	2.6400	2.6664	V
1	1	0	0	0		2.7126	2.7400	2.7674	V
1	0	1	1	1		2.8116	2.8400	2.8684	V
1	0	1	1	0		2.9106	2.9400	2.9694	V
1	0	1	0	1		3.0096	3.0400	3.0704	V
1	0	1	0	0		3.1086	3.1400	3.1714	V
1	0	0	1	1		3.2076	3.2400	3.2724	V
1	0	0	1	0		3.3066	3.3400	3.3734	V
1	0	0	0	1		3.4056	3.4400	3.4744	V
1	0	0	0	0		3.5046	3.5400	3.5754	V

■ $V_{GATE(H)}$ and $V_{GATE(L)}$					
Out SOURCE Sat at 100mA	Measure $V_{CC1} - V_{GATE(L)}$,; $V_{CC2} - V_{GATE(H)}$		1.2	2.0	V
Out SINK Sat at 100mA	Measure $V_{GATE(H)}$ – VPGnd; $V_{GATE(L)}$ – VPGnd		1.0	1.5	V
Out Rise Time	1V < $V_{GATE(H)}$ < 9V; 1V < $V_{GATE(L)}$ < 9V V_{CC1} = V_{CC2} = 12V		30	50	ns
Out Fall Time	9V > $V_{GATE(H)}$ > 1V; 9V > $V_{GATE(L)}$ > 1V V_{CC1} = V_{CC2} = 12V		30	50	ns
Shoot-Through Current	Note 1			50	mA
Delay $V_{GATE(H)}$ to $V_{GATE(L)}$	$V_{GATE(H)}$ falling to 2V; V_{CC1} = V_{CC2} = 8V $V_{GATE(L)}$ rising to 2V		25	50	ns
Delay $V_{GATE(L)}$ to $V_{GATE(H)}$	$V_{GATE(L)}$ falling to 2V; V_{CC1} = V_{CC2} = 8V $V_{GATE(H)}$ rising to 2V		25	50	ns
$V_{GATE(H)}$, $V_{GATE(L)}$ Resistance	Resistor to LGnd (Note 1)	20	50	100	kΩ
$V_{GATE(H)}$, $V_{GATE(L)}$ Schottky	LGnd to $V_{GATE(H)}$ @ 10mA LGnd to $V_{GATE(L)}$ @ 10mA		600	800	mV

Electrical Characteristics: 0°C < T_A < +70°C; 0°C < T_J < +125°C; 8V < V_{CC1} < 14V; 5V < V_{CC2} < 20V; DAC Code: V_{ID4} = V_{ID2} = V_{ID1} = V_{ID0} = 1; V_{ID3} = 0; $CV_{GATE(L)}$ and $CV_{GATE(H)}$ = 1nF; C_{OFF} = 330pF; C_{SS} = 0.1µF, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Soft Start (SS)					
Charge Time		1.6	3.3	5.0	ms
Pulse Period		25	100	200	ms
Duty Cycle	(Charge Time/Pulse Period) × 100	1.0	3.3	6.0	%
COMP Clamp Voltage	V_{FB} = 0V; V_{SS} = 0	0.50	0.95	1.10	V
V_{FFB} SS Fault Disable	$V_{GATE(H)}$ = Low; $V_{GATE(L)}$ = Low	0.9	1.0	1.1	V
High Threshold			2.5	3.0	V
■ PWM Comparator					
Transient Response	V_{FFB} = 0 to 5V to $V_{GATE(H)}$ = 9V to 1V; V_{CC1} = V_{CC2} = 12V		100	125	ns
V_{FFB} Bias Current	V_{FFB} = 0V		0.3		µA
■ Supply Current					
I_{CC1}	No Switching		8.5	13.5	mA
I_{CC2}	No Switching		1.6	3.0	mA
Operating I_{CC1}	V_{FB} = COMP = V_{FFB}		8	13	mA
Operating I_{CC2}	V_{FB} = COMP = V_{FFB}		2	5	mA
■ C_{OFF}					
Normal Charge Time	V_{FFB} = 1.5V; V_{SS} = 5V	1.0	1.6	2.2	µs
Extension Charge Time	V_{SS} = V_{FFB} = 0	5.0	8.0	11.0	µs
Discharge Current	C_{OFF} to 5V; V_{FB} >1V	5.0			mA
■ Time Out Timer					
Time Out Time	V_{FB} = V_{COMP}; V_{FFB} = 2V; Record $V_{GATE(H)}$ Pulse High Duration	10	30	65	µs
Fault Mode Duty Cycle	V_{FFB} = 0V	35	50	70	%

Note 1: Guaranteed by design, not 100% tested in production.

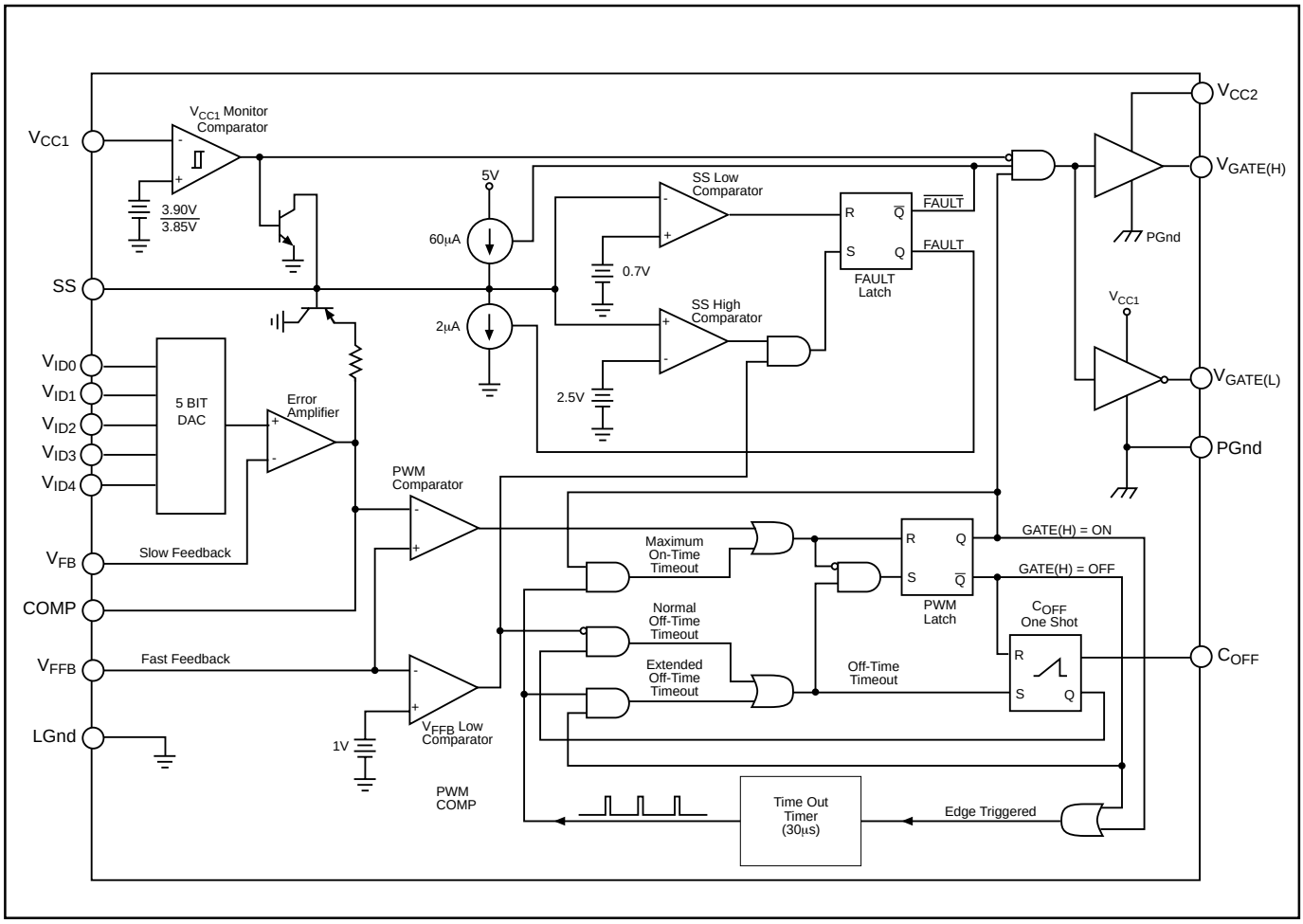
Package Pin Description

PACKAGE PIN #	PIN SYMBOL	FUNCTION
16L SO Narrow		
1,2,3,4,6	V_{ID0} – V_{ID4}	Voltage ID DAC input pins. These pins are internally pulled up to 5V providing logic ones if left open. V_{ID4} selects the DAC range. When V_{ID4} is High (logic one), the DAC range is 2.14V to 3.54V with 100mV increments. When V_{ID4} is Low (logic zero), the DAC range is 1.34V to 2.09V with 50mV increments. V_{ID0} - V_{ID4} select the desired DAC output voltage. Leaving all 5 DAC input pins open results in a DAC output voltage of 1.244V, allowing for adjustable output voltage, using a traditional resistor divider.
5	SS	Soft Start Pin. A capacitor from this pin to LGnd in conjunction with internal 60µA current source provides soft start function for the controller. This pin disables fault detect function during Soft Start. When a fault is detected, the soft start capacitor is slowly discharged by internal 2µA current source setting the time out before trying to restart the IC. Charge/discharge current ratio of 30 sets the duty cycle for the IC when the regulator output is shorted.

Package Pin Description: continued

PACKAGE PIN #	PIN SYMBOL	FUNCTION
16L SO Narrow		
7	C_{OFF}	A capacitor from this pin to ground sets the time duration for the on board one shot, which is used for the constant off time architecture.
8	V_{FFB}	Fast feedback connection to the PWM comparator. This pin is connected to the regulator output. The inner feedback loop terminates on time.
9	V_{CC2}	Boosted power for the high side gate driver.
10	$V_{GATE(H)}$	High FET driver pin capable of 1.5A peak switching current. Internal circuit prevents $V_{GATE(H)}$ and $V_{GATE(L)}$ from being in high state simultaneously.
11	PGnd	High current ground for the IC. The MOSFET drivers are referenced to this pin. Input capacitor ground and the source of lower FET should be tied to this pin.
12	$V_{GATE(L)}$	Low FET driver pin capable of 1.5A peak switching current.
13	V_{CC1}	Input power for the IC and low side gate driver.
14	LGnd	Signal ground for the IC. All control circuits are referenced to this pin.
15	COMP	Error amplifier compensation pin. A capacitor to ground should be provided externally to compensate the amplifier.
16	V_{FB}	Error amplifier DC feedback input. This is the master voltage feedback which sets the output voltage. This pin can be connected directly to the output or a remote sense trace.

Block Diagram



Applications Information

Theory of Operation

V²™ Control Method

The V²™ method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.

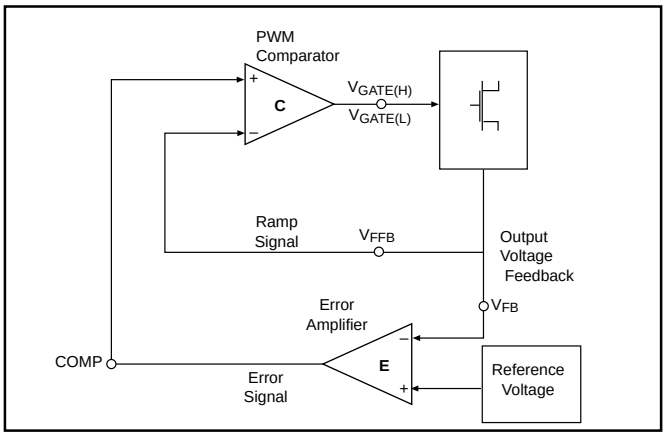


Figure 1: V²™ Control Diagram

The V²™ control method is illustrated in Figure 1. The output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to 0% or 100% duty cycle as required.

A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the V²™ control scheme to compensate the duty cycle. Since the change in inductor current modifies the ramp signal, as in current mode control, the V²™ control scheme has the same advantages in line transient response.

A change in load current will have an affect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation are drastically improved because there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The V²™ method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

Constant Off Time

To maximize transient response, the CS5155H uses a constant off time method to control the rate of output pulses. During normal operation, the off time of the high side switch is terminated after a fixed period, set by the C_{OFF} capacitor. To maintain regulation, the V²™ control loop varies switch on time. The PWM comparator monitors the output voltage ramp, and terminates the switch on time.

Constant off time provides a number of advantages. Switch duty cycle can be adjusted from 0 to 100% on a pulse by pulse basis when responding to transient conditions. Both 0% and 100% duty cycle operation can be maintained for extended periods of time in response to load or line transients. PWM slope compensation to avoid sub-harmonic oscillations at high duty cycles is avoided.

Switch on time is limited by an internal 30μs timer, minimizing stress to the power components.

Programmable Output

The CS5155H is designed to provide two methods for programming the output voltage of the power supply. A five bit on board digital to analog converter (DAC) is used to program the output voltage within two different ranges. The first range is 2.14V to 3.54V in 100mV steps, the second is 1.34V to 2.09V in 50mV steps, depending on the digital input code. If all five bits are left open, the CS5155H enters adjust mode. In adjust mode, the designer can choose any output voltage by using resistor divider feedback to the V_{FB} and V_{FFB} pins, as in traditional controllers. The CS5155H is specifically designed to be backwards compatible with the CS5150, which uses a four bit DAC code.

Start Up

Until the voltage on the V_{CC1} supply pin exceeds the 3.9V monitor threshold, the soft start and gate pins are held low. The FAULT latch is reset (no Fault condition). The output of the error amplifier (COMP) is pulled up to 1V by the comparator clamp. When the V_{CC1} pin exceeds the monitor threshold, the GateH output is activated, and the soft start capacitor begins charging. The GateH output will remain on, enabling the NFET switch, until terminated by either the PWM comparator, or the maximum on time timer.

If the maximum on time is exceeded before the regulator output voltage achieves the 1V level, the pulse is terminated. The GateH pin drives low, and the GateL pin drives high for the duration of the extended off time. This time is set by the time out timer and is approximately equal to the maximum on time, resulting in a 50% duty cycle. The GateL pin will then drive low, the GateH pin will drive high, and the cycle repeats.

When regulator output voltage achieves the 1V level present at the COMP pin, regulation has been achieved and normal off time will ensue. The PWM comparator terminates the switch on time, with off time set by the C_{OFF} capacitor. The V^{2TM} control loop will adjust switch duty cycle as required to ensure the regulator output voltage tracks the output of the error amplifier.

The soft start and COMP capacitors will charge to their final levels, providing a controlled turn on of the regulator output. Regulator turn on time is determined by the COMP capacitor charging to its final value. Its voltage is limited by the soft start COMP clamp and the voltage on the soft start pin (see Figures 2 and 3).

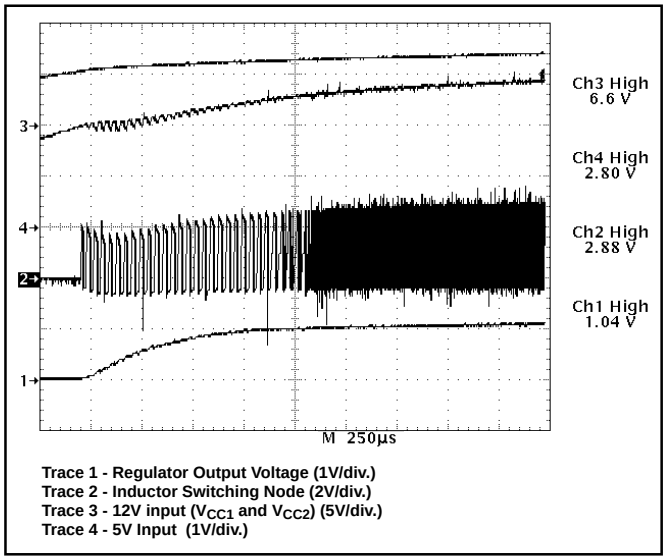


Figure 2: CS5155H demonstration board startup in response to increasing 12V and 5V input voltages. Extended off time is followed by normal off time operation when output voltage achieves regulation to the error amplifier output.

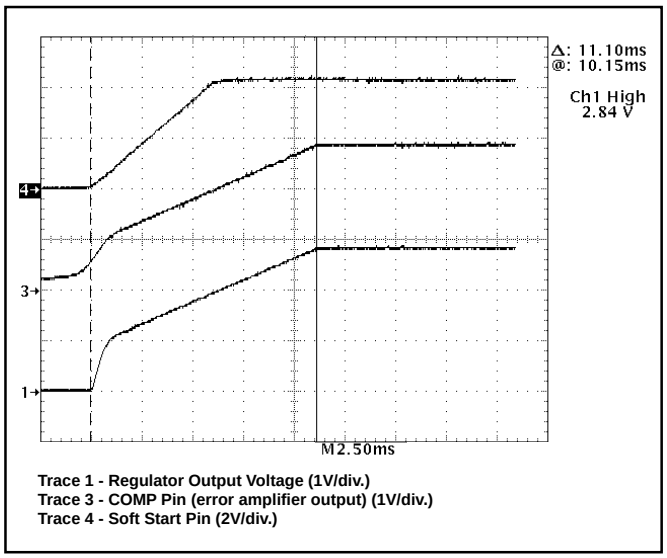


Figure 3: CS5155H demonstration board startup waveforms.

If the input voltage rises quickly, or the regulator output is enabled externally, output voltage will increase to the level set by the error amplifier output more rapidly, usually within a couple of cycles (see Figure 4).

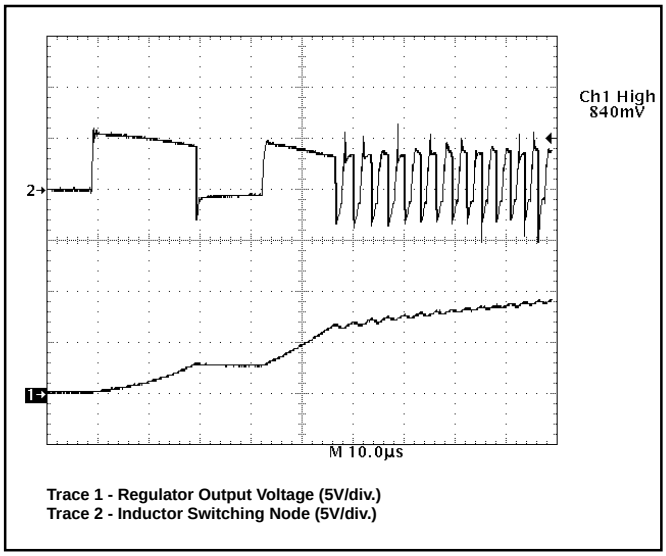


Figure 4: CS5155H demonstration board enable startup waveforms.

Normal Operation

During normal operation, switch off time is constant and set by the C_{OFF} capacitor. Switch on time is adjusted by the V^{2TM} control loop to maintain regulation. This results in changes in regulator switching frequency, duty cycle, and output ripple in response to changes in load and line. Output voltage ripple will be determined by inductor ripple current working into the ESR of the output capacitors (see Figures 5 and 6).

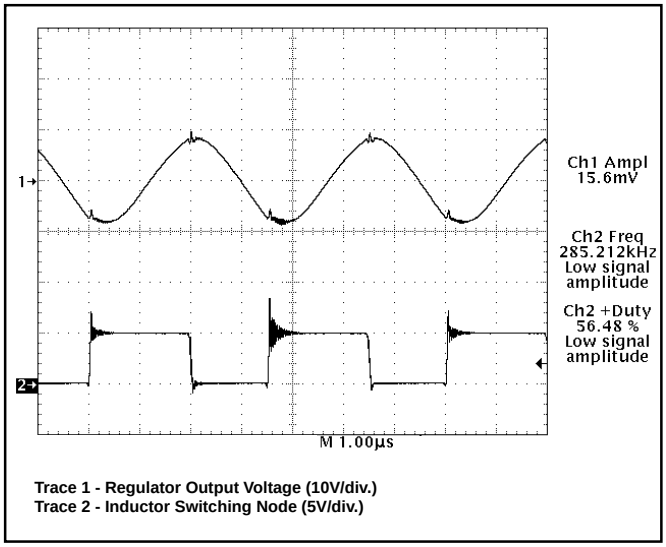


Figure 5: Peak-to-peak ripple on V_{OUT} = 2.8V, I_{OUT} = 0.5A (light load).

Applications Information: continued

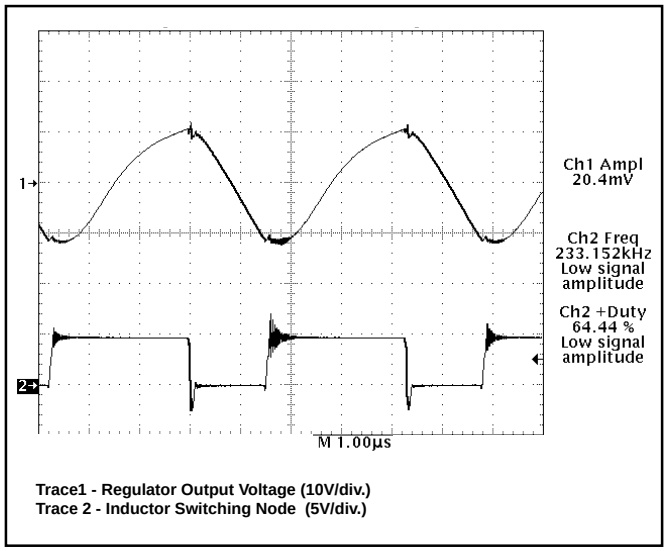


Figure 6: Peak-to-peak ripple on V_{OUT} = 2.8V, I_{OUT} = 13A (heavy load).

Transient Response

The CS5155H V^{2TM} control loop's 100ns reaction time provides unprecedented transient response to changes in input voltage or output current. Pulse by pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitor(s) during the time required to slew the inductor current.

Overall load transient response is further improved through a feature called "adaptive voltage positioning". This technique pre-positions the output capacitor's voltage to reduce total output voltage excursions during changes in load.

Holding tolerance to 1% allows the error amplifier's reference voltage to be targeted +40mV high without compromising DC accuracy. A "droop resistor", implemented through a PC board trace, connects the error amplifier's feedback pin (V_{FB}) to the output capacitors and load and carries the output current. With no load, there is no DC drop across this resistor, producing an output voltage tracking the error amplifier's, including the +40mV offset. When the full load current is delivered, an 80mV drop is developed across this resistor. This results in output voltage being offset -40mV low.

The result of adaptive voltage positioning is that additional margin is provided for a load transient before reaching the output voltage specification limits. When load current suddenly increases from it's minimum level, the output capacitor is pre-positioned +40mV. Conversely, when load current suddenly decreases from it's maximum level, the output capacitor is pre-positioned -40mV (see Figures 7, 8, and 9). For best transient response, a combination of a number of high frequency and bulk output capacitors are usually used.

If the maximum on time is exceeded while responding to a sudden increase in load current, a normal off time occurs to prevent saturation of the output inductor.

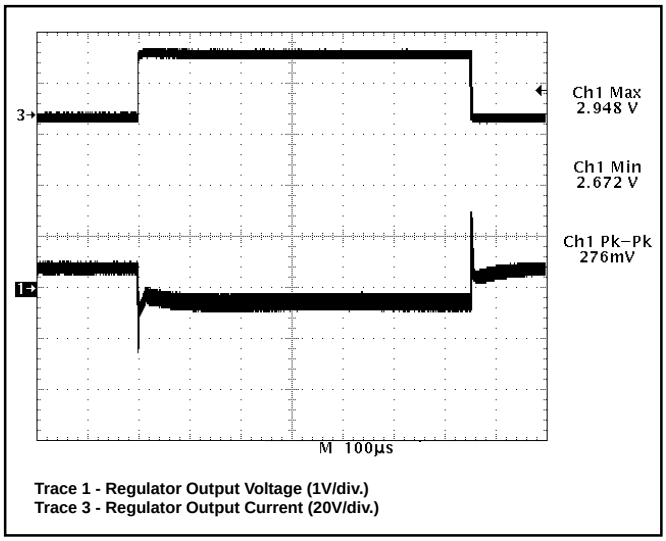


Figure 7: CS5155H demonstration board response to a 0.5 to 13A load pulse (output set for 2.8V).

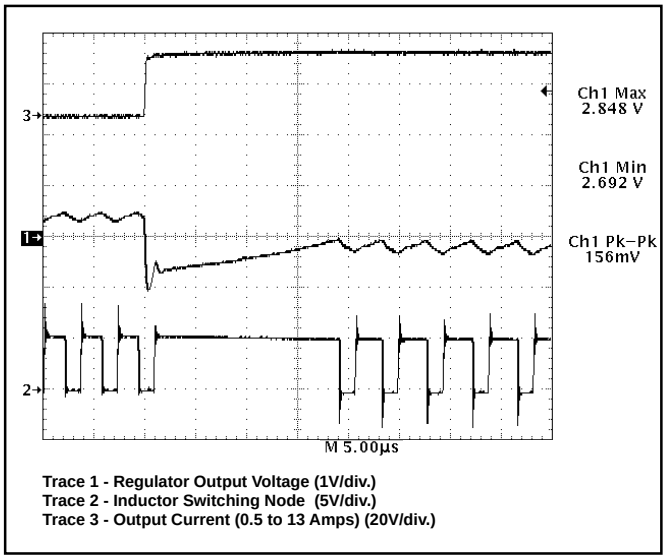


Figure 8: CS5155H demonstration board response to 13A load turn on (output set for 2.8V). Upon completing a normal off time, the V^{2TM} control loop immediately connects the inductor to the input voltage, providing 100% duty cycle. Regulation is achieved in less than 20µs.

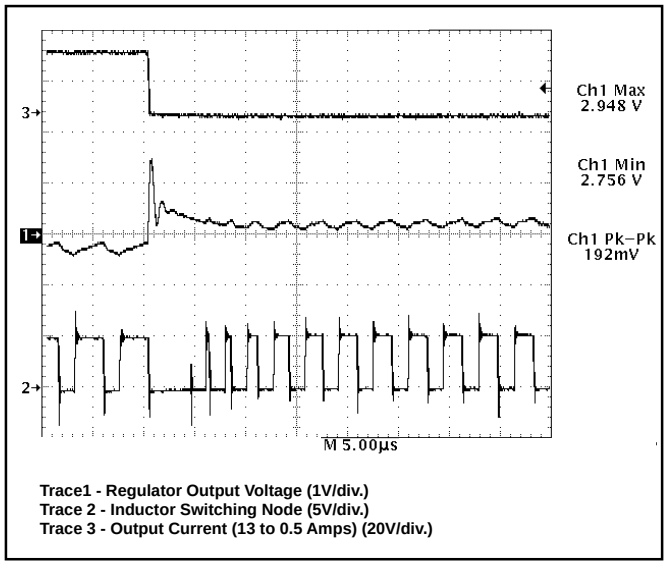


Figure 9: CS5155H demonstration board response to 13A load turn off (output set for 2.8V). V²™ control topology immediately connects inductor to ground, providing 0% duty cycle. Regulation is achieved in less than 10µs.

Protection and Monitoring Features

V_{CC1} Monitor

To maintain predictable startup and shutdown characteristics an internal V_{CC1} monitor circuit is used to prevent the part from operating below 3.75V minimum startup. The V_{CC1} monitor comparator provides hysteresis and guarantees a 3.70V minimum shutdown threshold.

Short Circuit Protection

A lossless hiccup mode short circuit protection feature is provided, requiring only the soft start capacitor to implement. If a short circuit condition occurs (V_{FFB} < 1V), the V_{FFB} low comparator sets the FAULT latch. This causes the top MOSFET to shut off, disconnecting the regulator from it's input voltage. The soft start capacitor is then slowly discharged by a 2µA current source until it reaches it's lower 0.7V threshold. The regulator will then attempt to restart normally, operating in it's extended off time mode with a 50% duty cycle, while the soft start capacitor is charged with a 60µA charge current.

If the short circuit condition persists, the regulator output will not achieve the 1V low V_{FFB} comparator threshold before the soft start capacitor is charged to it's upper 2.5V threshold. If this happens the cycle will repeat itself until the short is removed. The soft start charge/discharge current ratio sets the duty cycle for the pulses (2µA/60µA = 3.3%), while actual duty cycle is half that due to the extended off time mode (1.65%).

This protection feature results in less stress to the regulator components, input power supply, and PC board traces than occurs with constant current limit protection (see Figures 10 and 11).

If the short circuit condition is removed, output voltage will rise above the 1V level, preventing the FAULT latch from being set, allowing normal operation to resume.

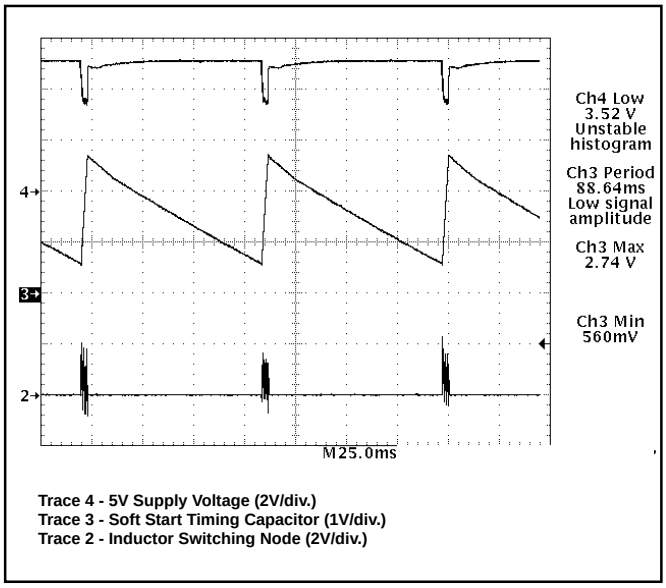


Figure 10: CS5155H demonstration board hiccup mode short circuit protection. Gate pulses are delivered while the soft start capacitor charges, and cease during discharge.

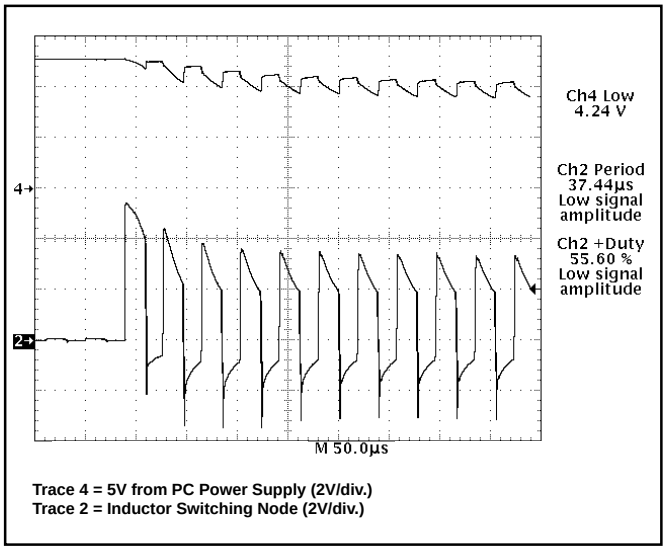


Figure 11: Startup with regulator output shorted.

Overvoltage Protection

Overvoltage protection (OVP) is provided as result of the normal operation of the V²™ control topology and requires no additional external components. The control loop responds to an overvoltage condition within 100ns, causing the top MOSFET to shut off, disconnecting the regulator from it's input voltage. The bottom MOSFET is then activated, resulting in a "crowbar" action to clamp the output voltage and prevent damage to the load (see Figures 12 and 13). The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low.

Applications Information: continued

The bottom FET and board trace must be properly designed to implement the OVP function.

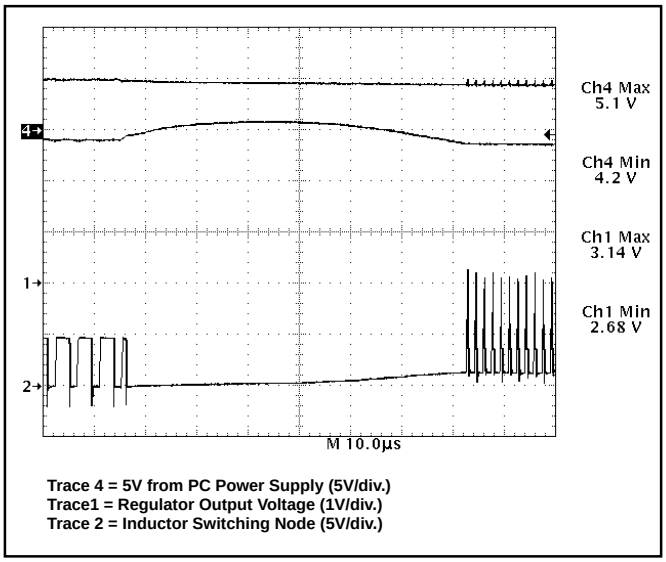


Figure 12: OVP response to an input-to-output short circuit by immediately providing 0% duty cycle, crow-barring the input voltage to ground.

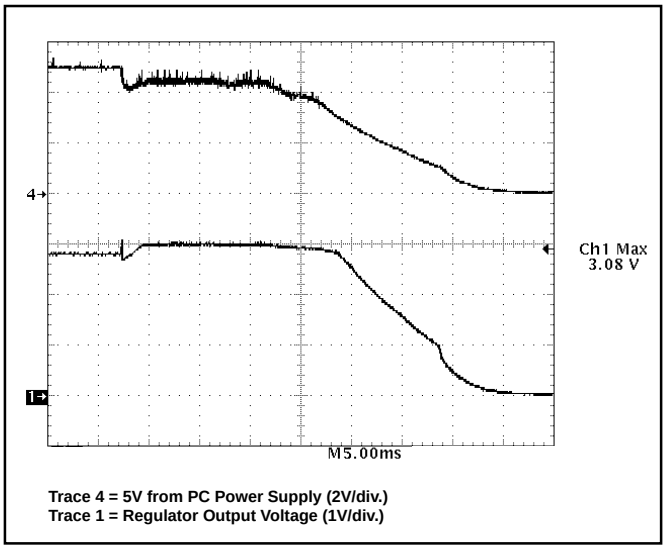


Figure 13: OVP response to an input-to-output short circuit by pulling the input voltage to ground.

External Output Enable Circuit

On/off control of the regulator can be implemented through the addition of two additional discrete components (see Figure 14). This circuit operates by pulling the soft start pin high, and the V_{FFB} pin low, emulating a short circuit condition.

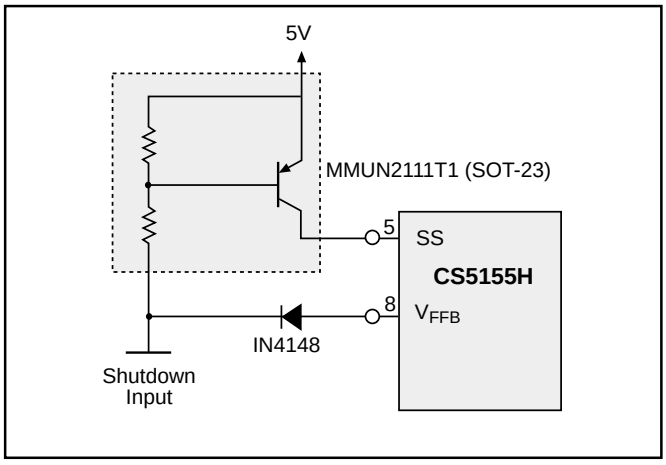


Figure 14: Implementing shutdown with the CS5155H.

External Power Good Circuit

An optional Power Good signal can be generated through the use of four additional external components (see Figure 15). The threshold voltage of the Power Good signal can be adjusted per the following equation:

$$V_{Power\ Good} = \frac{(R1 + R2) \times 0.65V}{R2}$$

This circuit provides an open collector output that drives the Power Good output to ground for regulator voltages less than $V_{Power\ Good}$.

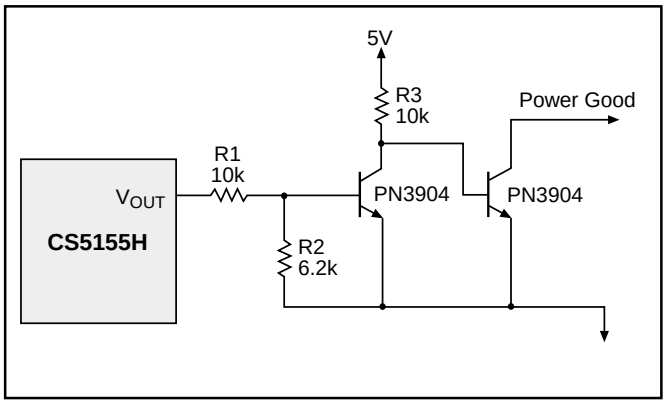


Figure 15: Implementing Power Good with the CS5155H.

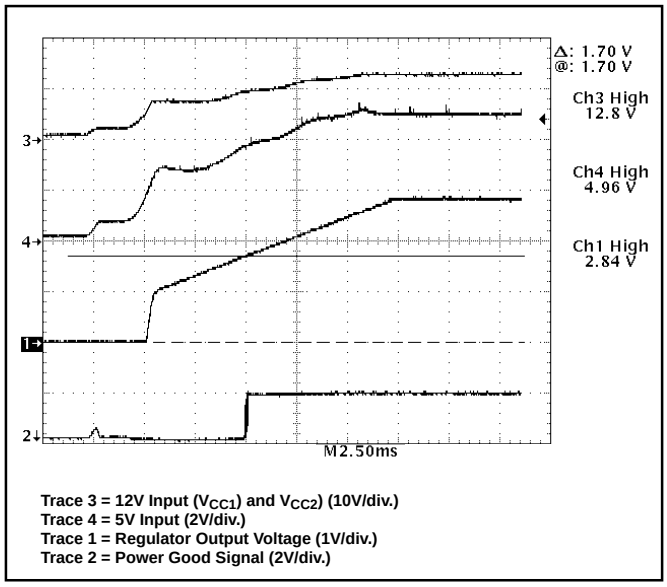


Figure 16: CS5155H demonstration board during power up. Power Good signal is activated when output voltage reaches 1.70V.

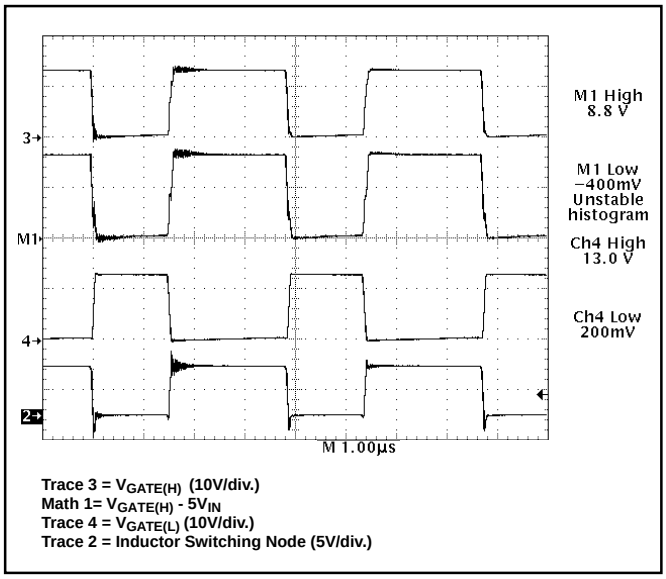


Figure 17: CS5155H gate drive waveforms depicting rail to rail swing.

Selecting External Components

The CS5155H can be used with a wide range of external power components to optimize the cost and performance of a particular design. The following information can be used as general guidelines to assist in their selection.

NFET Power Transistors

Both logic level and standard MOSFETs can be used. The reference designs derive gate drive from the 12V supply which is generally available in most computer systems and utilize logic level MOSFETs. A charge pump may be easily implemented to support 5V or 12V only systems (maximum of 20V). Multiple MOSFETs may be paralleled to reduce losses and improve efficiency and thermal management.

Voltage applied to the MOSFET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5V of ground when in the low state and to within 2V of their respective bias supplies when in the high state. In practice, the MOSFET gates will be driven rail to rail due to overshoot caused by the capacitive load they present to the controller IC. For the typical application where $V_{CC1} = V_{CC2} = 12V$ and 5V is used as the source for the regulator output current, the following gate drive is provided;

$V_{GATE(H)} = 12V - 5V = 7V$, $V_{GATE(L)} = 12V$ (see Figure 17).

The most important aspect of MOSFET performance is RDS_{ON}, which effects regulator efficiency and MOSFET thermal management requirements.

The power dissipated by the MOSFETs may be estimated as follows;

Switching MOSFET:

$$Power = I_{LOAD}^2 \times RDS_{ON} \times \text{duty cycle}$$

Synchronous MOSFET:

$$Power = I_{LOAD}^2 \times RDSON \times (1 - \text{duty cycle})$$

Duty Cycle =

$$\frac{V_{OUT} + (I_{LOAD} \times RDS_{ON\ OF\ SYNCH\ FET})}{V_{IN} + (I_{LOAD} \times RDS_{ON\ OF\ SYNCH\ FET}) - (I_{LOAD} \times RDS_{ON\ OF\ SWITCH\ FET})}$$

Off Time Capacitor (C_{OFF})

The C_{OFF} timing capacitor sets the regulator off time:

$$T_{OFF} = C_{OFF} \times 4848.5$$

When the V_{FFB} pin is less than 1V, the current charging the C_{OFF} capacitor is reduced. The extended off time can be calculated as follows:

$$T_{OFF} = C_{OFF} \times 24{,}242.5.$$

Off time will be determined by either the T_{OFF} time, or the time out timer, whichever is longer.

The preceding equations for duty cycle can also be used to calculate the regulator switching frequency and select the

Applications Information: continued

C_{OFF} timing capacitor:

$$C_{OFF} = \frac{\text{Period} \times (1 - \text{duty cycle})}{4848.5},$$

where:

$$\text{Period} = \frac{1}{\text{switching frequency}}$$

Schottky Diode for Synchronous MOSFET

A Schottky diode may be placed in parallel with the synchronous MOSFET to conduct the inductor current upon turn off of the switching MOSFET to improve efficiency. The CS5155H reference circuit does not use this device due to it's excellent design. Instead, the body diode of the synchronous MOSFET is utilized to reduce cost and conducts the inductor current. For a design operating at 200kHz or so, the low non-overlap time combined with Schottky forward recovery time may make the benefits of this device not worth the additional expense (see Figure 6, channel 2). The power dissipation in the synchronous MOSFET due to body diode conduction can be estimated by the following equation:

$$\text{Power} = V_{bd} \times I_{LOAD} \times \text{conduction time} \times \text{switching frequency}$$

Where V_{bd} = the forward drop of the MOSFET body diode. For the CS5155H demonstration board as shown in Figure 6;

$$\text{Power} = 1.6V \times 13A \times 100ns \times 233kHz = 0.48W$$

This is only 1.3% of the 36.4W being delivered to the load.

"Droop" Resistor for Adaptive Voltage Positioning

Adaptive voltage positioning is used to reduce output voltage excursions during abrupt changes in load current. Regulator output voltage is offset +40mV when the regulator is unloaded, and -40mV at full load. This results in increased margin before encountering minimum and maximum transient voltage limits, allowing use of less capacitance on the regulator output (see Figure 7).

To implement adaptive voltage positioning, a "droop" resistor must be connected between the output inductor and output capacitors and load. This is normally implemented by a PC board trace of the following value:

$$R_{DROOP} = \frac{80mV}{I_{MAX}}$$

Adaptive voltage positioning can be disabled for improved DC regulation by connecting the V_{FB} pin directly to the load using a separate, non-load current carrying circuit trace.

Input and Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the input supply lines and regulator output voltage. Key specifications for input capacitors are their ripple rating, while ESR is important for output capacitors. For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

Output Inductor

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response.

Thermal Management

Thermal Considerations for Power MOSFETs and Diodes

In order to maintain good reliability, the junction temperature of the semiconductor components should be kept to a maximum of 150°C or lower. The thermal impedance (junction to ambient) required to meet this requirement can be calculated as follows:

$$\text{Thermal Impedance} = \frac{T_{JUNCTION(MAX)} - T_{AMBIENT}}{\text{Power}}$$

A heatsink may be added to TO-220 components to reduce their thermal impedance. A number of PC board layout techniques such as thermal vias and additional copper foil area can be used to improve the power handling capability of surface mount components.

EMI Management

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.

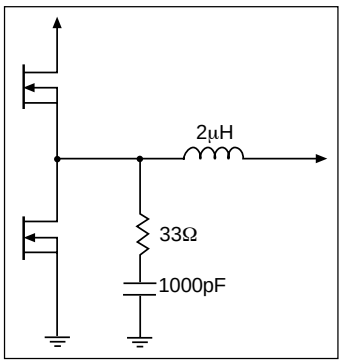


Figure 18: Filter components

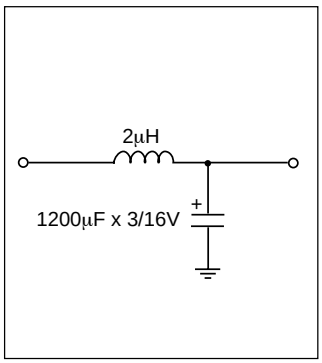


Figure 19: Input Filter

Layout Guidelines

1. Place 12V filter capacitor next to the IC and connect capacitor ground to pin 11 (PGnd).

2. Connect pin 11 (PGnd) with a separate trace to the ground terminals of the 5V input capacitors.

3. Place fast feedback filter capacitor next to pin 8 (V_{FFB}) and connect it's ground terminal with a separate, wide trace directly to pin 14 (LGnd).

Applications Information: continued

4. Connect the ground terminals of the Compensation capacitor directly to the ground of the fast feedback filter capacitor to prevent common mode noise from effecting the PWM comparator.

5. Place the output filter capacitor(s) as close to the load as possible and connect the ground terminal to pin 14 (LGnd).

6. To implement adaptive voltage positioning, connect both slow and fast feedback pins 16 (V_{FB}) and 8 (V_{FFB}) to the regulator output right at the inductor terminal. Connect inductor to the output capacitors via a trace with the following resistance:

$$R_{TRACE} = \frac{80mV}{I_{MAX}}$$

This causes the output voltage to be +40mV with no load, and -40mV with a full load, improving regulator transient response. This trace must be wide enough to carry the full output current. (Typical trace is 1.0 inch long, 0.17 inch wide). Care should be taken to minimize any additional losses after the feedback connection point to maximize regulation.

7. If DC regulation is to be optimized (at the expense of degraded transient regulation), adaptive voltage positioning can be disabled by connecting to V_{FB} pin directly to the load with a separate trace (remote sense).

8. Place 5V input capacitors close to the switching MOSFET and synchronous MOSFET.

Route gate drive signals $V_{GATE(H)}$ (pin 10) and $V_{GATE(L)}$ (pin 12 when used) with traces that are a minimum of 0.025 inches wide.

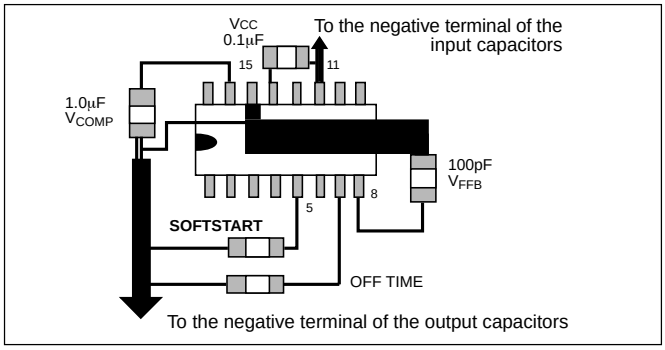


Figure 20: Layout Guidelines

Additional Application Circuits

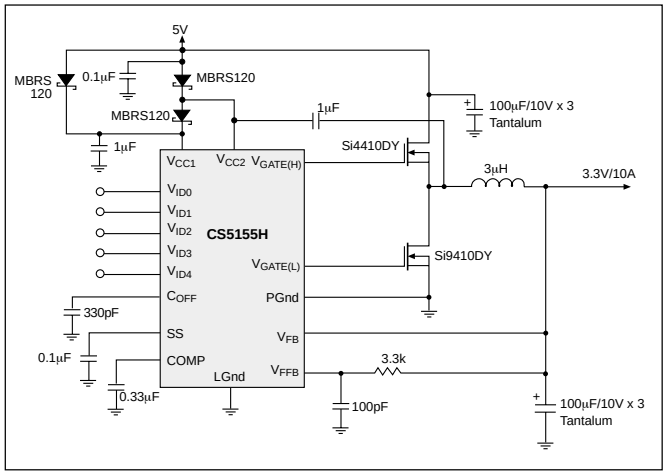


Figure 21: 5V to 3.3V/10A converter.

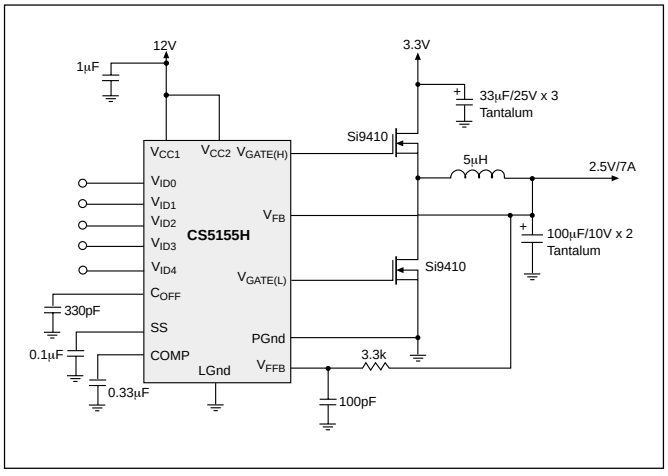


Figure 23: 3.3V to 2.5V/7A converter with 12V bias.

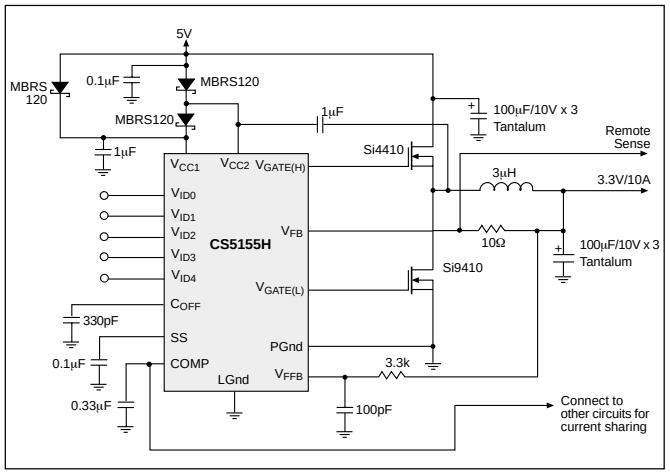


Figure 22: 5V to 3.3V/10A converter with current sharing.

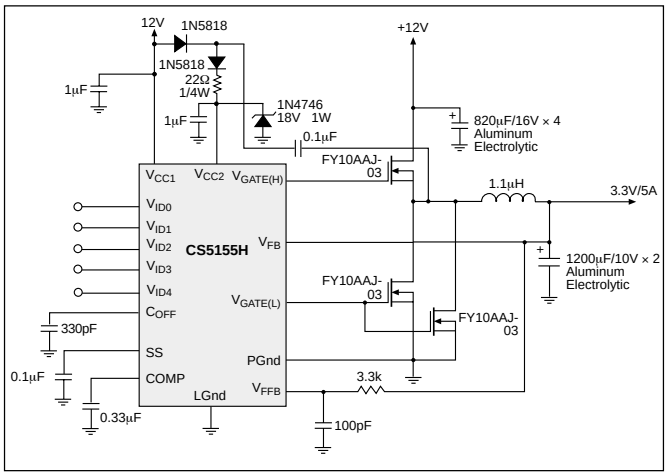


Figure 24: 12V to 3.3V/5A converter with remote sense.

Package Specification

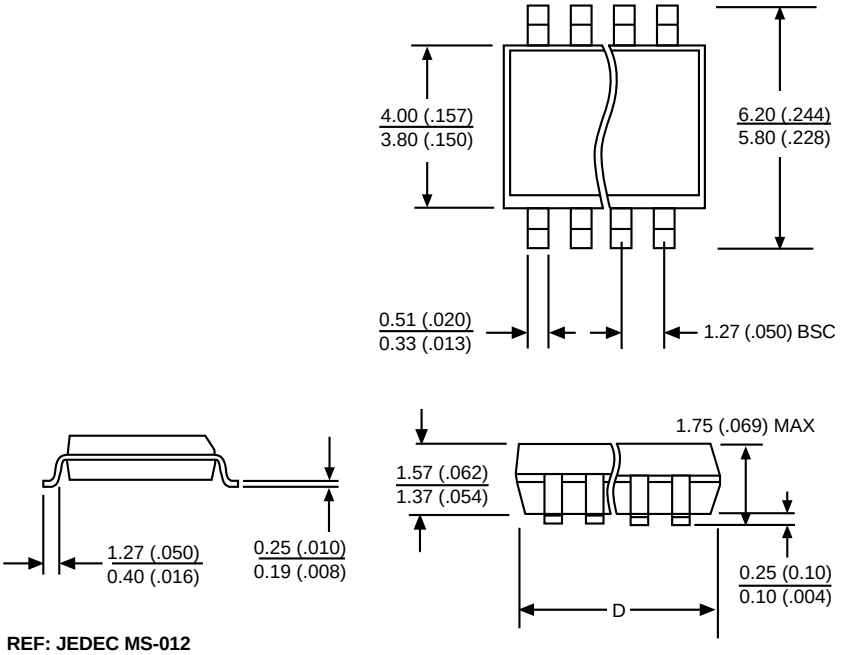
PACKAGE DIMENSIONS IN mm (INCHES)

	D			
Lead Count	**Metric**		**English**	
	Max	Min	Max	Min
16L SO Narrow	10.00	9.80	.394	.386

PACKAGE THERMAL DATA

Thermal Data		**16L SO Narrow**	
$R_{\Theta JC}$	typ	28	°C/W
$R_{\Theta JA}$	typ	115	°C/W

Surface Mount Narrow Body (D); 150 mil wide



REF: JEDEC MS-012

Ordering Information

Part Number	**Description**
CS5155HGD16	16L SO Narrow
CS5155HGDR16	16L SO Narrow *(tape & reel)*

Cherry Semiconductor Corporation reserves the right to make changes to the specifications without notice. Please contact Cherry Semiconductor Corporation for the latest available information.

© 1999 Cherry Semiconductor Corporation