CS51220

Feed Forward Voltage Mode PWM Controller with Programmable Synchronization

CS51220 is a single output PWM Controller with switching frequency up to 500 kHz. The feed forward voltage mode control provides excellent line regulation for wide input range. This PWM controller has a synchronization output allowing programmable phase delay. For overcurrent protection, the “soft hiccup” technique effectively limits the output current with maximum flexibility. In addition, this device includes such features as: soft start, pulse−by−pulse current limit, programmable foldback current limit, volt−second clamping, maximum duty cycle, overvoltage and undervoltage protection, and synchronization input. The CS51220 is available in 16 SO narrow surface mount package.

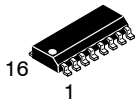
Features

- Constant Frequency Feed Forward Voltage Mode Control
- Programmable Pulse by Pulse Overcurrent Limit
- Programmable Foldback Overcurrent Limit with Delay
- Soft Hiccup Overcurrent Protection with Programmable Foldback
- Frequency Synchronization Output with Programmable Phase Delay
- Synchronization Input to Higher or Lower Frequency
- Direct Connection to External Opto Isolators
- Logic Gate Output Signal
- Accurate Volt−Second Clamping
- Programmable Soft Start
- Logic Input to Disable IC
- Line Overvoltage and Undervoltage Monitoring
- 3.3 V 3% Reference Voltage Output

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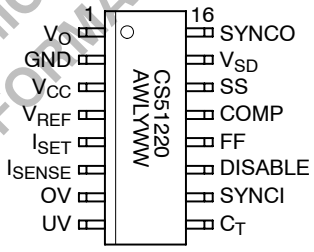
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SO−16
D SUFFIX
CASE 751B

PIN CONNECTIONS AND MARKING DIAGRAM

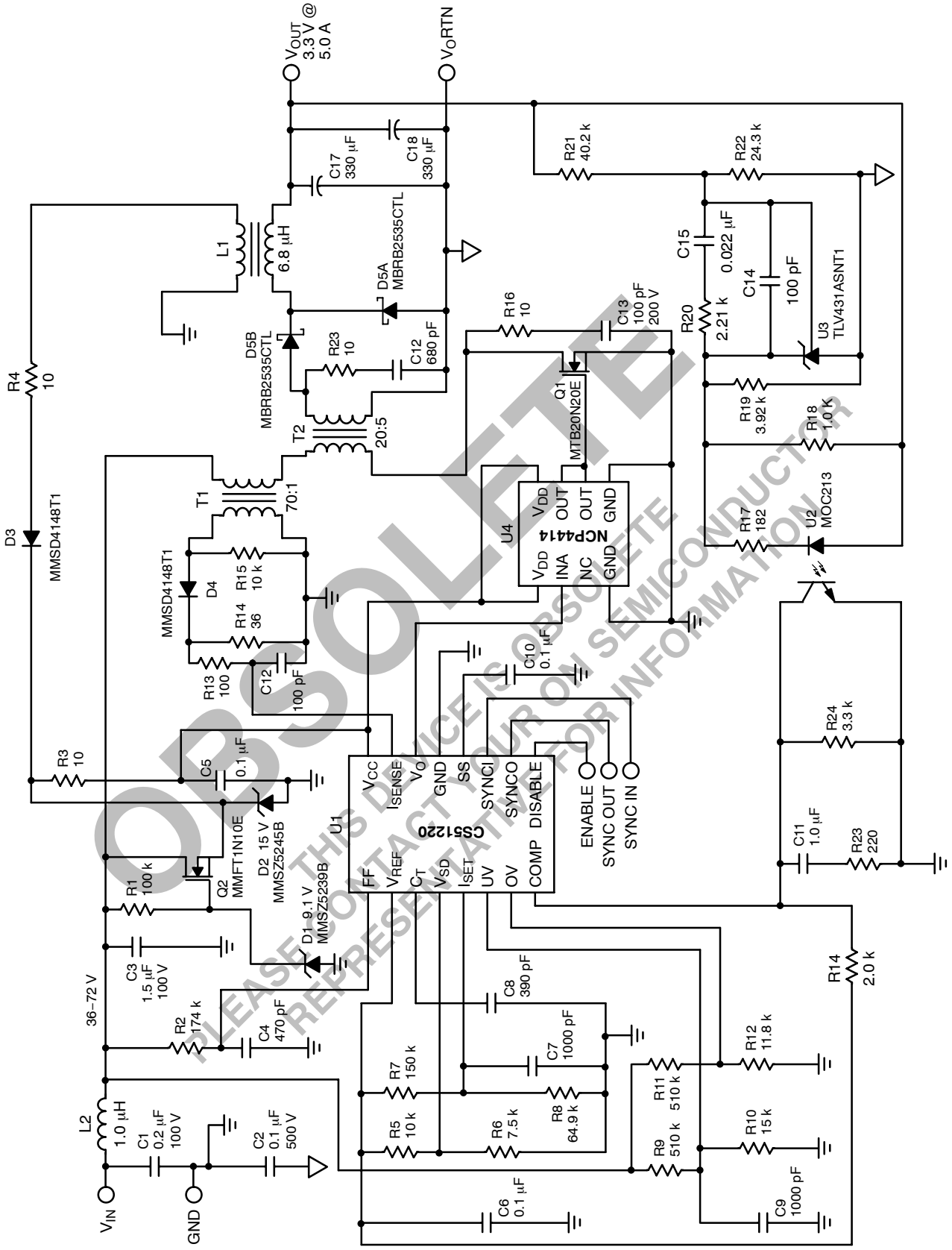


A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
CS51220ED16	SO−16	48 Units/Rail
CS51220EDR16	SO−16	2500 Tape & Reel

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Figure 1. Application Diagram, 48 V to 3.3 V Converter

MAXIMUM RATINGS*

Rating	Value	Unit
Operating Junction Temperature, T_J	150	°C
Storage Temperature Range, T_S	−65 to +150	°C
ESD Susceptibility (Human Body Model)	2.0	kV
Thermal Resistance, Junction−to−Case, $R_{\Theta JC}$	28	°C/W
Thermal Resistance, Junction−to−Ambient, $R_{\Theta JA}$	115	°C/W
Lead Temperature Soldering: Reflow: (SMD styles only) (Note 1)	230 peak	°C

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

MAXIMUM RATINGS

Pin Name	Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
Gate Logic Output	V_O	20 V	−0.3 V	100 mA	100 mA
Current Sense Input	I_{SENSE}	6.0 V	−0.3 V	10 mA	10 mA
Timing Capacitor	C_T	6.0 V	−0.3 V	10 mA	10 mA
Feed Forward	FF	6.0 V	−0.3 V	10 mA	100 mA
Error Amp Output	COMP	6.0 V	−0.3 V	10 mA	10 mA
Feedback Voltage	V_{FB}	6.0 V	−0.3 V	10 mA	10 mA
Sync Input	SYNCI	20 V	−0.3 V	10 mA	10 mA
Power Down Input	DISABLE	20 V	−0.3 V	10 mA	10 mA
Undervoltage	UV	6.0 V	−0.3 V	10 mA	10 mA
Overvoltage	OV	6.0 V	−0.3 V	10 mA	10 mA
Current Set	I_{SET}	6.0 V	−0.3 V	10 mA	10 mA
Soft Start	SS	6.0 V	−0.3 V	10 mA	10 mA
Power Supply	V_{CC}	20 V	−0.3 V	10 mA	50 mA
Sync Output	SYNCO	20 V	−0.3 V	100 mA	100 mA
Reference Voltage	V_{REF}	6.0 V	−0.3 V	Internally Limited	10 mA
Sync Delay	V_{SD}	6.0 V	−0.3 V	1.0 mA	1.0 mA
Ground	GND	N/A	N/A	50 mA	N/A

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ELECTRICAL CHARACTERISTICS (−40°C < T_A < 85°C; −40°C < T_J < 125°C; 4.7 V < V_{CC} < 16 V; C_T = 390 pF; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Supply Voltage/Current					
Start Threshold	–	4.0	4.4	4.7	V
Stop Threshold	–	3.3	3.8	4.1	V
Hysteresis	Start – Stop	400	600	1000	mV
I_{CC} @ Startup	V_{CC} < UVL Start Threshold	–	–	500	μA
I_{CC} Operating, Low V_{CC}	4.7 V < V_{CC} < 10 V	–	–	7.5	mA
I_{CC} Operating, High V_{CC}	10 V < VCC < 16 V	–	–	9.0	mA
Reference Voltage					
Total Accuracy	0 mA < I_{REF} < 2.0 mA	3.2	3.3	3.4	V
Line Regulation	I_{REF} = 2.0 mA	–	6.0	20	mV
Load Regulation	0 mA < I_{REF} < 2.0 mA, V_{CC} = 8.0 V	–	6.0	15	mV
Operating Life Shift	T = 1000 Hrs., Note 2	–	4.0	20	mV
Fault Voltage	–	2.8	2.95	3.1	V
V_{REF} OK Voltage	–	2.9	3.05	3.2	V
V_{REF} OK Hysteresis	–	50	100	150	mV
Current Limit	V_{REF} = 2.5 V	2.0	25	65	mA
Oscillator					
Frequency Accuracy	–	223	266	309	kHz
Temperature Stability	Note 2	–	8.0	–	%
Max Frequency	Note 2	500	–	–	kHz
Duty Cycle	–	80	85	90	%
Peak Voltage	Note 2	1.9	2.0	2.1	V
Valley Voltage	Note 2	0.85	0.90	0.98	V
Discharge Current	V_{CT} = 1.5 V	0.70	0.85	1.05	mA
Charge Current	V_{CT} = 1.5 V	127	150	183	μA
Synchronization					
SYNCI Input Threshold	f_{SYNC} = 500 kHz	1.0	2.0	3.0	V
SYNCI Input Resistance	V_{SYNC} = 0.5	50	150	250	kΩ
Minimum Sync Frequency	Reduction of nominal frequency.	25	–	–	%
Minimum Input Sync Pulse Width	–	–	–	200	ns
SYNCO Output High	R_{SYNCO} = 5.0 k, V_{CC} = 8.0 V	5.0	6.5	7.5	V
SYNCO Output Low	Sink 1.0 mA, V_{SD} = 2.5 V	–	0.2	0.4	V
SYNCO Delay Time	V_{CT} = 1.5 V, Toggle V_{SD}	100	200	300	ns

2. Guaranteed by design. Not tested in production.

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ELECTRICAL CHARACTERISTICS (continued) (−40°C < T_A < 85°C; −40°C < T_J < 125°C; 4.7 V < V_{CC} < 16 V; C_T = 390 pF; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Output (continued)					
High Saturation Voltage	V_{CC} − V_O, V_{CC} = 10 V, I_{SOURCE} = 100 μA	–	1.4	2.0	V
Low Saturation Voltage	V_O − GND, I_{SINK} = 100 μA	–	0.7	1.0	V
Pull Down Resistance	I_{SINK} = 100 μA	25	50	75	kΩ
Rise Time	V_{CC} = 10 V, 1.0 V < V_O < 6.0 V; 50 pF load	–	35	80	ns
Fall Time	V_{CC} = 10 V, 1.0 V < V_O < 6.0 V; 50 pF load	–	25	50	ns
Feed Forward					
Discharge Voltage	I_{FF} = 2.0 mA	0.25	0.35	0.45	V
Discharge Current	FF = 1.0 V	2.0	10	30	mA
FF to V_O Delay	Connect V_O to FF, Measure min. pulse width.	50	75	150	ns
FF Clamp Voltage	–	1.15	1.3	1.45	V
COMP Switch Off Voltage	V_{FF} = 0.2 V, Ramp down V_{COMP} V_{FF} = 0.2 V, Ramp down V_{COMP} −40°C	0.8 1.4	1.4 1.6	1.7 1.7	V V
Overcurrent Protection					
Overcurrent Comparator DC Offset	–	180	200	215	mV
I_{SENSE} Attenuation	$\Delta V_{ISET}/\Delta V_{ISENSE}$	0.9	0.94	0.98	V/V
I_{SENSE} Input Resistance	ΔV_{ISENSE} = 0 V	40	82	150	kΩ
I_{SENSE} to GATE Delay	V_{ISET} = 0.5 V	50	100	175	ns
I_{SET} Foldback Sink Current	I_{SET} = 0.5 V, SS = 1.5 V and I_{SENSE} = 0.5 V	12	15	18	μA
External Voltage Monitors					
Overvoltage Threshold	OV pin increasing	1.9	2.0	2.1	V
OV Hysteresis Current	OV = 2.15 V	10	12.5	15	μA
Undervoltage Threshold	UV pin decreasing	0.95	1.00	1.05	V
UV Hysteresis	–	25	75	125	mV
Soft Start					
Charge Current	SS = 1.5 V	35	50	65	μA
Discharge Current	SS = 1.5 V, UV = 1.5 V	4.0	5.0	7.0	μA
OC Delay Discharge Current	SS = 2.85 V, I_{SET} = 0.5, I_{SENSE} = 0.5 V	35	50	65	μA
SS Clamp Voltage	–	2.7	2.9	3.1	V
Discharge Voltage	–	0.25	0.3	0.35	V
Soft Start Fault Voltage	OV = 2.5 V or UV = 0.85 V	–	0.1	0.2	V
Hiccup Delay Discharge Voltage	–	0.08	0.1	0.12	V
Disable					
DISABLE Input Threshold	–	1.0	2.0	3.0	V
DISABLE Input Resistance	$V_{DISABLE}$ = 0.5 V	50	150	250	kΩ
DISABLE Operation Current, Low V_{CC}	4.7 V < V_{CC} < 10 V	–	–	800	μA
DISABLE Operation Current, High V_{CC}	10 V < V_{CC} < 16 V	–	–	1600	μA

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PACKAGE PIN DESCRIPTION

PACKAGE PIN #		
16 Lead SO Narrow	PIN SYMBOL	FUNCTION
1	V_O	Logic output connecting to external gate driver.
2	GND	Ground.
3	V_{CC}	Supply Voltage.
4	V_{REF}	3.3 V reference voltage output.
5	I_{SET}	Voltage at this pin sets pulse−by−pulse overcurrent threshold. When the I_{SENSE} exceeds I_{SET} for a sustained period of time, a sink current is generated at this pin. Along with external resistors, this current provides a foldback overcurrent threshold. The sink current is disabled periodically for restart.
6	I_{SENSE}	Current sense input for overcurrent protection.
7	OV	Overvoltage protection monitor.
8	UV	Undervoltage protection monitor.
9	C_T	Timing capacitor C_T determines oscillator frequency.
10	SYNCI	By applying sync pulses to this pin, the IC can be synchronized to frequencies ranging from 25% slower to several times faster than the internal oscillator frequency.
11	DISABLE	Disable mode input pin. A voltage greater than 3.0 V turns off the whole IC.
12	FF	Feed forward input for PWM ramp. This pin allows external connection to make the ramp adjustable to the input line.
13	COMP	This pin carries feedback error signal from an external amplifier. Internally, it connects to the PWM controller.
14	SS	A capacitor is connected to this pin for Soft Start and soft hiccup timing.
15	V_{SD}	The voltage at this pin programs the delay of the SYNCO output in reference to the internal oscillator.
16	SYNCO	Sync output.

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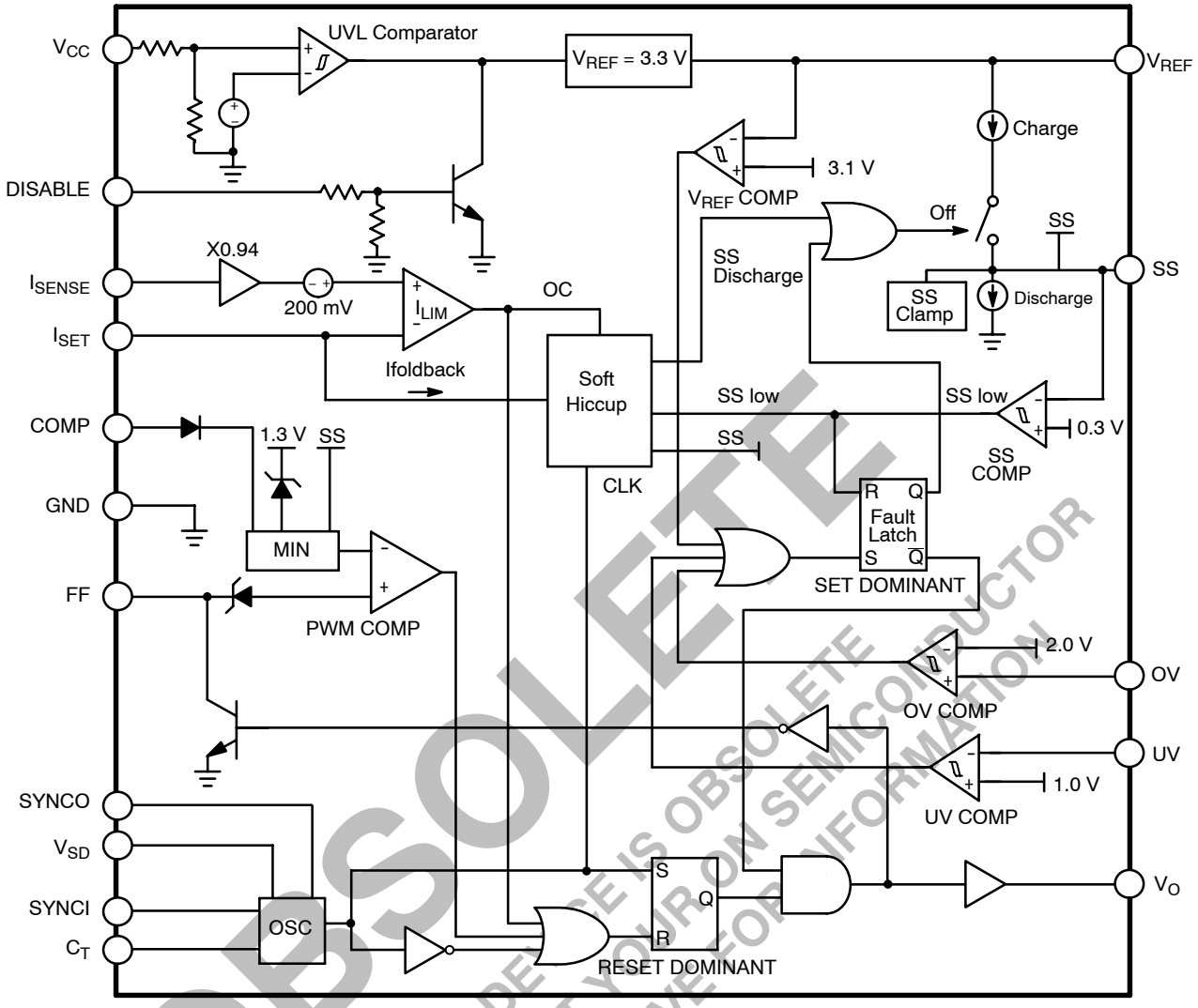


Figure 2. Block Diagram

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APPLICATIONS INFORMATION

THEORY OF OPERATION

Feed Forward Voltage Mode Control

Conventional voltage mode control uses a fixed ramp signal for pulse width modulation, typically utilizing the oscillator output as the ramp signal. Since the only feedback signal comes from the output, this results in inferior line regulation and audio susceptibility. A significant improvement in line regulation and line transient response can be achieved using Feed Forward Voltage Mode Control, implemented using the CS51220 controller.

The enhancement comes from generating the ramp signal using a pull−up resistor from the FF pin to the line voltage and a capacitor to ground. The slope of the ramp then depends on the line voltage. At the start of each switch cycle, the capacitor connected to the FF pin is charged through the resistor connected to the input voltage. Meanwhile, the V_O pin goes high to turn on a power mosfet through an external gate driver. When the rising FF pin exceeds the COMP input pin, as driven through the regulation feedback loop, V_O goes low and turns off the external switch. Simultaneously, the FF capacitor is quickly discharged and set for the next switching cycle.

Overall, both input and output voltages control the dynamics of the duty cycle. As illustrated in Figure 3, with a fixed input voltage the output voltage is regulated solely by the error amplifier. For example, an elevated output voltage pulls down the COMP pin through an external error amplifier. This in turn causes duty cycle to decrease. On the another hand, if the input voltage varies, the slope of the FF pin ramp reacts correspondingly and immediately. As an example shown in Figure 4, when the input voltage goes up, the slope of the ramp signal increases, which reduces duty cycle and counteracts the change. For line variations, feed forward control requires less response from the error amplifier, which improves the transient speed and DC regulation.

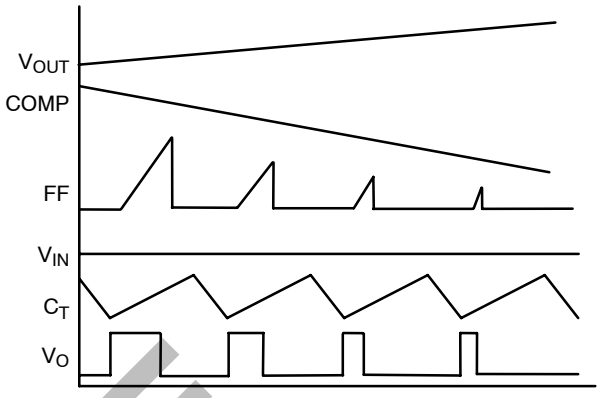


Figure 3. Pulse Width Modulated by the Output Voltage with a Constant Input Voltage

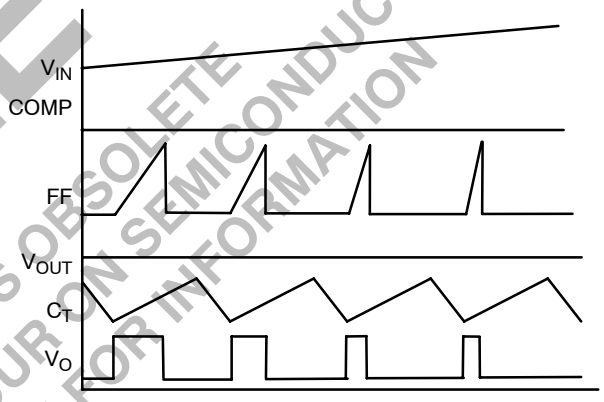


Figure 4. Pulse Width Modulated by the Input Voltage with a Constant Output Voltage

The feed forward feature can also be employed for volt−second clamp, which limits the maximum product of input voltage and switch on time. This clamp is used in circuits, such as forward and flyback converters, to prevent the transformer from saturating. Calculations used in the design of the volt−second clamp are presented in the Design Guidelines section on page 12.

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V_{CC} Power Up and Fault Conditions

During power up, an undervoltage lockout comparator monitors V_{CC} and disables V_{REF}, (which in turn disables the entire IC), until the V_{CC} voltage reaches its start threshold. Hysteresis prevents "chattering" caused by the source impedance of the V_{CC} supply. V_{REF} can also be disabled using the Disable input pin, which is active high. An internal pull−down resistor ensures the IC will start up if the Disable pin is allowed to float. In V_{CC} or Disable lockout mode, the output stage is held low by the output pull−down resistance.

After V_{REF} turns on, there are three conditions that can cause fault mode:

1. The 3.3 V V_{REF} is below regulation,
2. The OV pin rises above overvoltage threshold, or
3. The UV pin falls below undervoltage threshold.

Fault detection will cause the V_O output to go low and the SS pin to discharge. The UV and OV inputs are typically used to monitor the input line voltage. The undervoltage comparator has a built−in hysteresis voltage, while the hysteresis for the OV comparator is programmable through a current sourced from the pin when above the threshold, and the equivalent external resistance. The fault condition can only be reset after the SS pin has been completely discharged and all faults have been removed.

After a fault is removed or upon initial startup, the SS pin charges at a rate determined by an internal charge current and an external capacitor. The rising voltage on the SS pin will override the regulation feedback voltage on the COMP pin and clamp the duty cycle, helping to reduce any in−rush current during startup. The duration of the Soft Start is typically set with a capacitor from 0.01 μF to 0.1 μF.

Overcurrent Protection

The CS51220 uses the "soft hiccup" technique to provide an adjustable and predictable overcurrent limit. By choosing external component values the designer can select pulse−by−pulse current limit, soft hiccup current limit or hard hiccup limit.

Normal pulse−by−pulse current limit can be obtained by selecting the I_{SET} resistor values for a low Thevenin resistance to the I_{SET} pin. However with normal pulse−by−pulse current limit, the secondary currents during short circuits may be several times the maximum output current.

Soft hiccup limit can be obtained by setting the I_{SET} resistor values for a higher thevenin resistance. During overcurrent conditions, the I_{SET} level will fold back, after a short delay, to reduce the pulse by pulse threshold. If desired, the short circuit current can be chosen to be equal to or even less than the maximum output current. During soft hiccup the circuit will periodically disable the foldback and attempt to restart.

Hard hiccup limit can be obtained by setting the I_{SET} resistor values so that the I_{SET} pin is held below 200 mV during foldback. During overcurrent conditions, the I_{SET} level will fold back, after a short delay, preventing any gate pulses. When the SS capacitor is completely discharged, the circuit will attempt restart. This configuration provides the lowest power dissipation during short outputs.

The circuit functions can be best described by discussing the block diagram and illustrations of expected waveforms. Actual waveforms, values and circuit configurations from a design will be used. The design is from the 5.0 V supply of a dual synchronized converter.

The current is monitored with a voltage at the I_{SENSE} pin. The I_{SENSE} signal is slightly attenuated DC shifted by 200 mV, and is compared with the threshold voltage programmed by the voltage at the I_{SET} pin. If the current signal reaches the threshold voltage, the overcurrent comparator resets the V_O latch and terminates the V_O pulse. The overcurrent comparator has a maximum common mode input voltage of 1.8 V. However, an I_{SET} voltage below 1.0 V is desirable for reducing the comparator's propagation delay. During initial turnon of the power supply, normal pulse−by−pulse overcurrent control is used to protect the power supply switches. This is accomplished by comparing the voltage at the I_{SENSE} input to the voltage at the I_{SET} pin and using this to limit the duty factor of V_O, the gate drive signal. This current limit control is maintained until the SS voltage reaches 2.9 V.

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The block diagram of the soft hiccup circuit is shown in Figure 5. When overcurrent occurs and the SS is above 2.9 V, the OC pulses set the OC latch. The output of the OC latch turns on the OC delay discharge current to ramp down the SS voltage. This SS discharge ramp down is at a rate of 50 μA while the SS voltage is above 2.8 V. The level between 2.9 V and 2.8 V is called the hiccup delay discharge voltage. The time to cross this voltage creates a short delay. This delay is useful so that a quick transient overcurrent condition can be controlled and still allow the supply to return immediately to normal operation. After reaching the hiccup delay discharge voltage, the SS current is reduced to 5.0 μA and the I_{SET} foldback current is turned on at 15 μA. It is the I_{SET} foldback current that adjusts the I_{SET} level to establish a new lower I_{SENSE} current limit level. See Figure 6 for details.

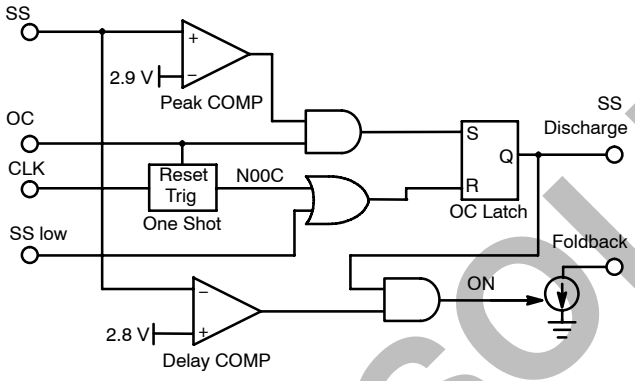


Figure 5. The Block Diagram of the Soft Hiccup Operation

A circuit monitors the OC pulses. If the OC pulses cease for 50 μs, the NOt−OverCurrent (NOOC) signal is generated. This NOOC signal resets the OC Latch and allows the SS capacitor to charge back up allowing the output to reestablish regulation.

For an equivalent circuit shown in Figure 6, the I_{SET} current reduces the overcurrent threshold and sets the new threshold at

$$V_{I(SET)} = (3.3 - I_{SET} \times R1) \times \frac{R2}{(R1 + R2)}$$

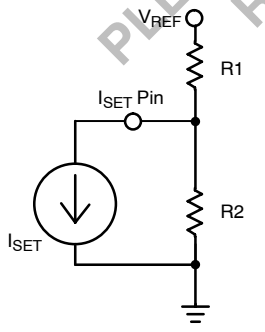


Figure 6. The Voltage Divider Used at the I_{SET} Pin Allows the I_{SET} Foldback Current to Reduce the Overcurrent Threshold

The NOOC or SS low (V_{SS} < 0.3 V) signal can reset OC latch at any time. This event turns off I_{SET} foldback and allows the recharging of the SS capacitor. Therefore, the IC allows the power supply to restart periodically or after the overcurrent condition is cleared. The OC latch can not be set until the SS capacitor is fully charged.

To implement “hard hiccup” which disables the V_O completely when the SS voltage is ramping down, select a resistor value greater than 3.3 V/I_{SET} for R1 in Figure 6, and saturate the internal I_{SET} current source. Since the saturation voltage is less than the DC shift applied to the I_{SENSE} signal, the OC comparator output is always high and in turn keeps the V_O low. Figure 7 demonstrates the interactions among the voltage of SS, I_{SET} and internal signal OC. Figure 8 further describes the specifications associated with the soft hiccup. The ratio among the charge time, delay time and discharge time is given at the bottom of Figure 8.

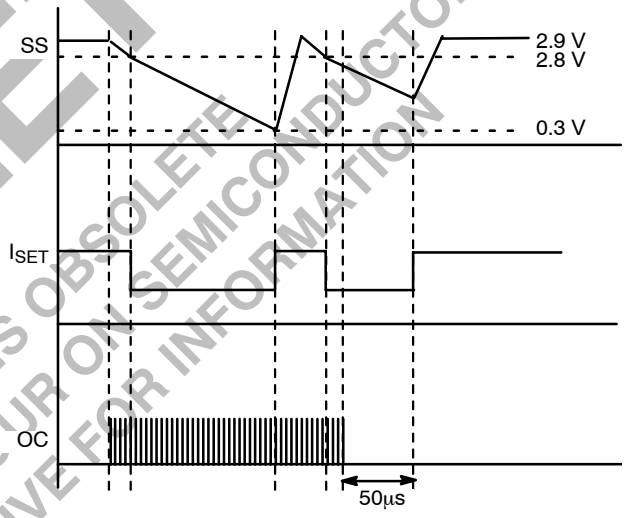


Figure 7. Illustrative Waveforms of the Soft Hiccup Operation

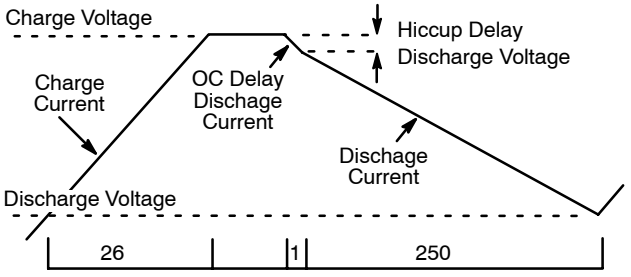


Figure 8. The SS Pin Voltage Under Ramp Up and Overcurrent Condition and Associated Specifications.

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The effect of the soft hiccup can be observed in Figure 9, which shows the output voltage as load increases. The output is maintained at the regulation value of 5.0 V until it goes into current limit. At the point of overcurrent inception (A), the current limit level changes to a lower level (B). The switchback to a lower current limit level can be seen as the bottom curve in Figure 9.

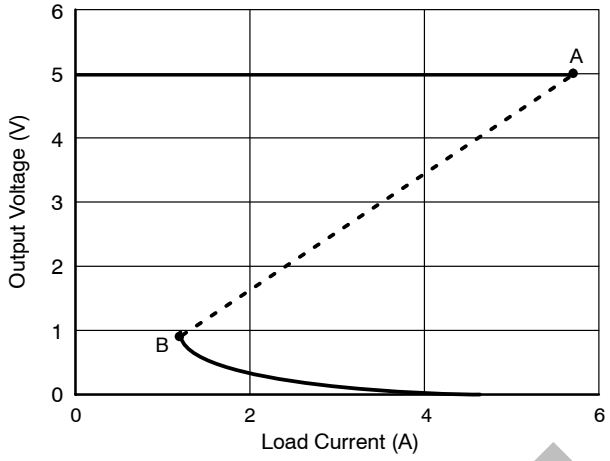


Figure 9. Overcurrent In a 5.0 V Output Converter Using Soft Hiccup

A typical overload scenario is shown in Figure 10. The top trace is the voltage on the Soft Start (SS) pin. The initial high discharge rate can be seen transitioning to a 40 ms discharge period. During this period the I_{SET} establishes a lower current limit level. The bottom trace shows the output current. The initial current spike is the output capacitors discharging. The next level around 4.0 A is the short circuit current level set by the I_{SET} current. The output then turns off allowing the current to reduce to a level that does not cause overcurrent pulses. This releases the SS pin to ramp back up. During ramp up, the output is still shorted as noted by the 8.0 A current level. When SS reaches the 2.9 V level, the short is again recognized and I_{SET} is turned back on shifting the short circuit current level.

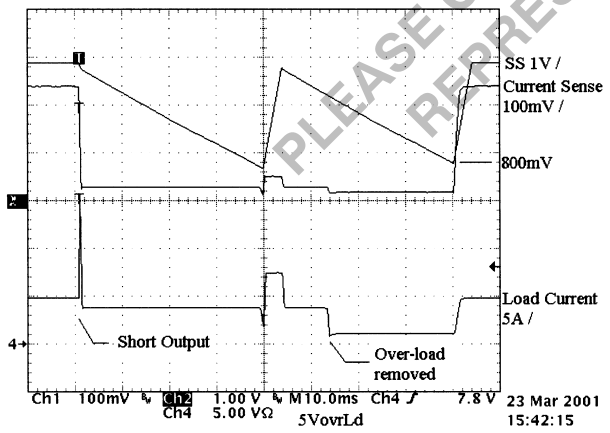


Figure 10. Over−Load Current and Soft Start Waveforms

The middle trace is a digitizing ‘scope trace of the current sense line. The scope interprets the voltages as an average voltage. This voltage is actually a narrow duty cycle peak voltage representing the peak current level in the switching transistor. The actual peak voltages can be seen in the Figure 11. The peaks are 0.85 V at full load, reducing to 0.6 V peak at the reduced short circuit level. The 1.1 V peak is the full short circuit current while SS ramps back up. The 0.32 V level is the normal load resistance, while I_{SET} is still on. The 1.0 V surge is created by ramp up into a normal 5.0 A load and followed by the 0.85 V at normal load.

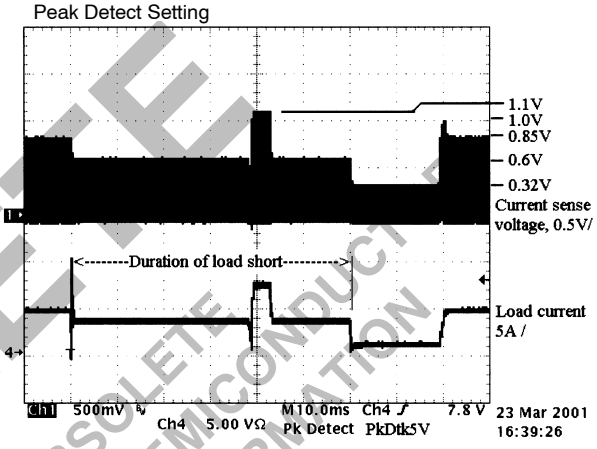


Figure 11. Over−Load Current and I_{SENSE} Voltage

Oscillator and Synchronization

The switching frequency is programmable through a capacitor connected to the C_T pin. When the C_T pin voltage reaches peak voltage (2.0 V), the internal discharge current discharges the C_T capacitor and V_O stays low. When the C_T voltage declines to valley voltage (0.9 V), the current source toggles to charge current and ramps up the C_T pin. This starts a new switching cycle. The duty cycle of the oscillator determines the maximum PWM duty cycle.

The switching frequency of the IC can be synchronized to an external frequency presented to the SYNCI pin. When pulses with amplitude over SYNCI input threshold are detected, the C_T pin immediately ramps down the external capacitor and the V_O pin is forced low. A new switching cycle begins when the C_T pin reaches valley voltage. During synchronization, the oscillator charge current is reduced by 80 μA, while discharge current is increased by 80 μA. This effectively slows down the internal oscillator to avoid any race condition with the sync frequency. As a result, the sync frequency can be either higher or lower than the internal oscillator frequency. CS51220 is able to synchronize up to 500 kHz and down to 25% below C_T frequency. The maximum duty cycle clamp is raised to 92% in synchronization mode. The original oscillator frequency is restored upon the removal of sync pulses.

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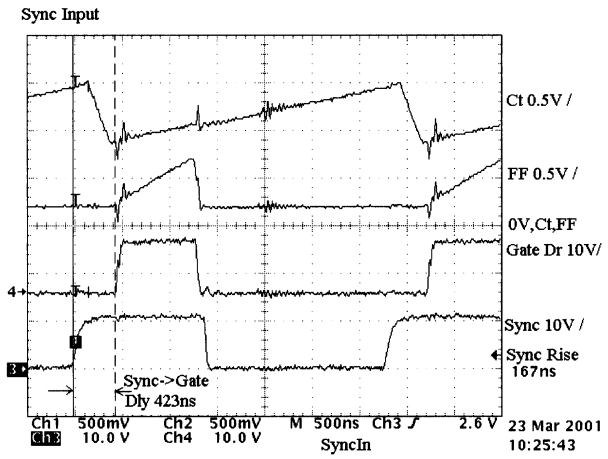


Figure 12. Synchronization Input Timing

Figure 12 shows the sync input from one CS51220 into another. The delay between receiving the sync input and the start of the next switching cycle is 423 ns. This delay must be taken into account when establishing the total delay between two regulators.

The SYNCO pin provides outgoing synchronization pulses whose delay can be programmed by setting the voltage on the V_{SD} pin. The feature allows two converters to run at interleaved phases. This implementation significantly reduces the input ripple, and thus the number of input capacitors. The phase delay is achieved by turning on SYNCO output only after the C_T pin voltage reaches the V_{SD} voltage. Therefore, the phase delay varies linearly with the V_{SD} voltage. The SYNCO output is reset during the falling edge of the C_T pin. For minimum phase delay (~ 240 ns), tie the V_{SD} pin to the ground. To entirely disable the SYNCO output, connect the V_{SD} pin to V_{REF}.

The waveform in Figure 13 shows the C_T ramp crossing the V_{SD} voltage set at 1.41 V.

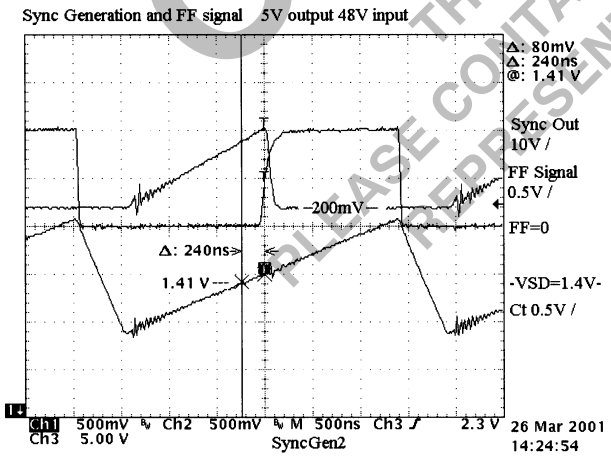


Figure 13. Synchronization Output Timing

The delay from the point of crossing to the output of the sync signal is 240 ns. The time for the sync out voltage is measured at the +2.0 V level, which is the level that triggers the next CS51220.

The desired effect on the input ripple is illustrated in Figure 14. This is the input current for two power converters operating from a 36 V line.

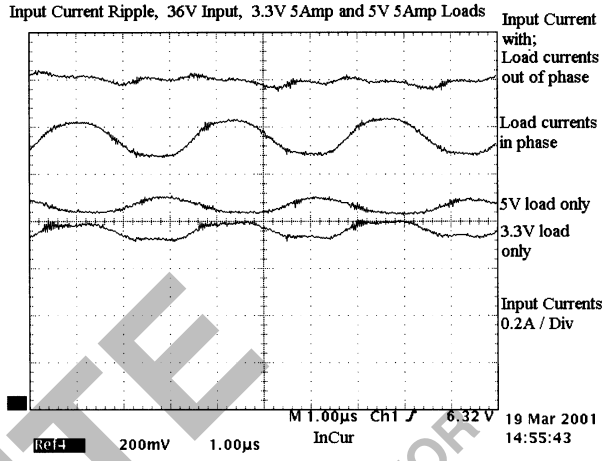


Figure 14. Input Current Ripple with Different Overlap Conditions

The top waveform in Figure 14 is the input current with the two supplies operating out of phase. The next down shows the same supplies but with both conduction times occurring simultaneously. The greatly increased ripple current can be observed. The last two waveforms are the two converters shown individually when operating out of phase.

DESIGN GUIDELINES

Program Volt−Second Clamp

Feed forward voltage mode control provides the volt−second clamp which clamps the product of the line voltage and switch on time. For the circuit shown in Figure 15, the charging current of the C_{FF} can be considered as a constant current equal to V_{IN}/R_{FF}, provided V_{IN} is much greater than the FF pin voltage. Then the volt−second clamp provided by CS51220 is given by

$$V_{IN}T_{ON(MAX)} = 1.0R_{FF}C_{FF}$$

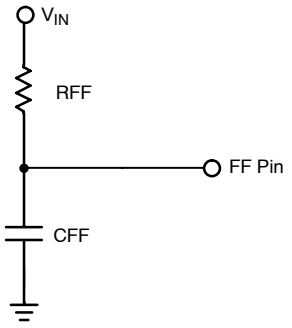


Figure 15. An RC Network Provides Both Volt−Second Clamp and Feed Forward Control

Select the time constant of the FF pin RC network to provide desirable volt−second clamp.

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Program Oscillator Frequency

CS51220 requires an external capacitor to program the oscillator frequency. The internally trimmed charge/discharge current determines the maximum duty cycle. The capacitor for a required switching frequency f_S can be calculated by:

$$CT = \frac{13400}{fS} - 95$$

where:

C_T = Timing capacitance is in pF

f_S = Switching frequency is in kHz

Figure 16 shows the relationship of C_T and f_S.

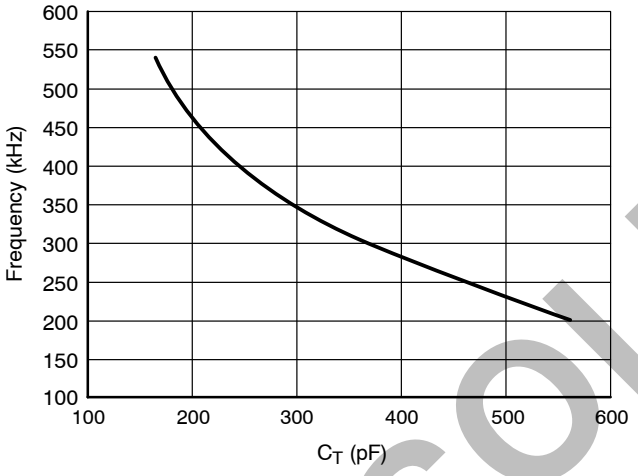


Figure 16. Operating Frequency

Synchronized Dual Converters with Soft Hiccup and Feed Forward

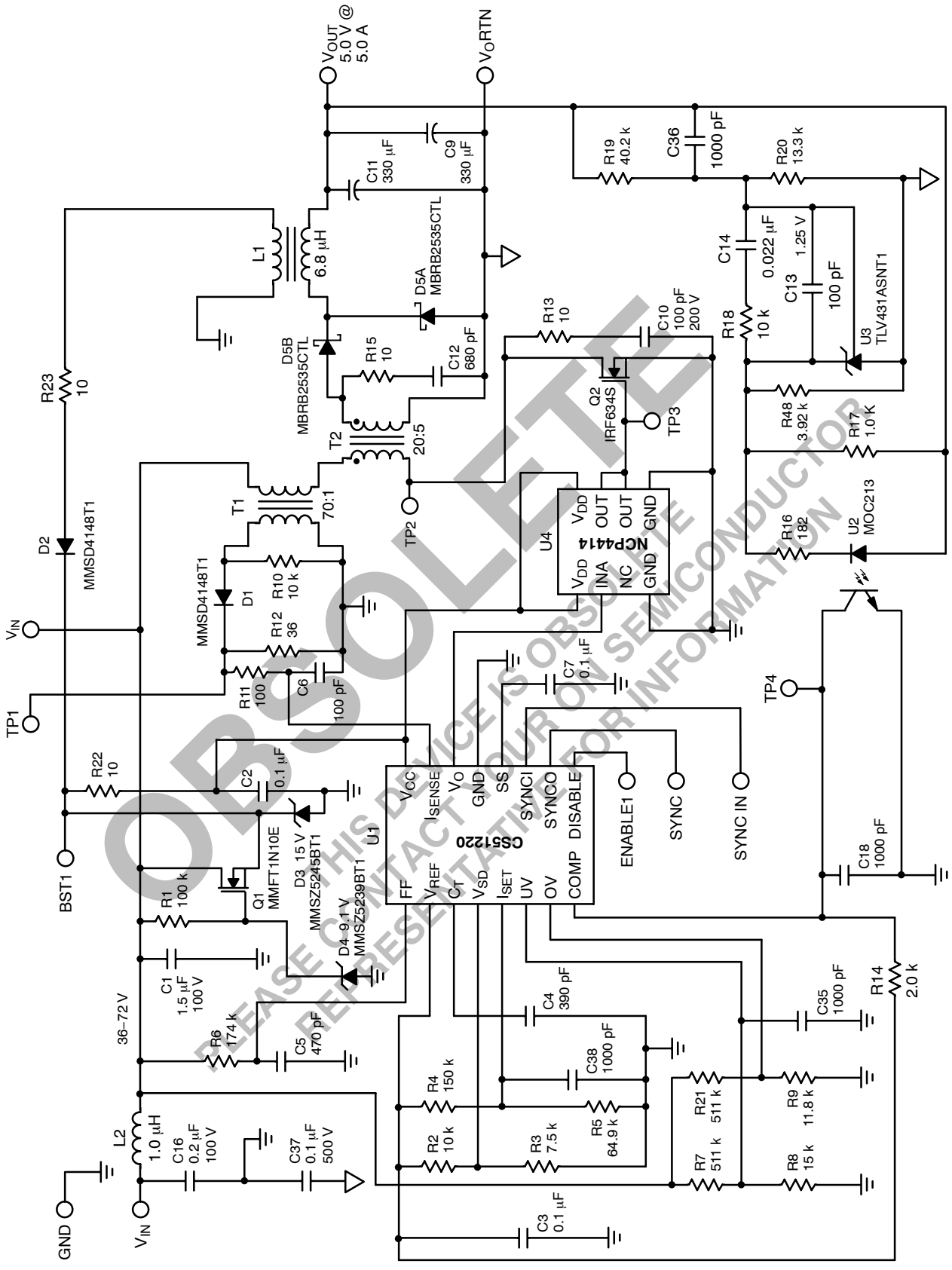
The circuits shown in Figures 17 and 18 illustrate typical applications for a dual output supply using independent but synchronized converters. These circuits demonstrate the use of the soft hiccup, feed forward, volt−second control and synchronization features of the CS51220.

In Figure 17, the feed forward circuit has a volt−second constant of 82 V/μs. This would limit the duty factor to 0.51 at 48 V input. With a turns ratio of 4:1 on the power transformer and 48 V input, a duty factor of 0.46 is required for 5.0 V output. This converter serves as the master synchronization generator. The voltage on the V_{SD} pin establishes the delay as it is compared to the ramp generated on the C_T pin.

Adjustable synchronization allows the conduction time for the two converters to be adjusted so that they are not on at the same time. This greatly reduces the ripple current from the 48 V source.

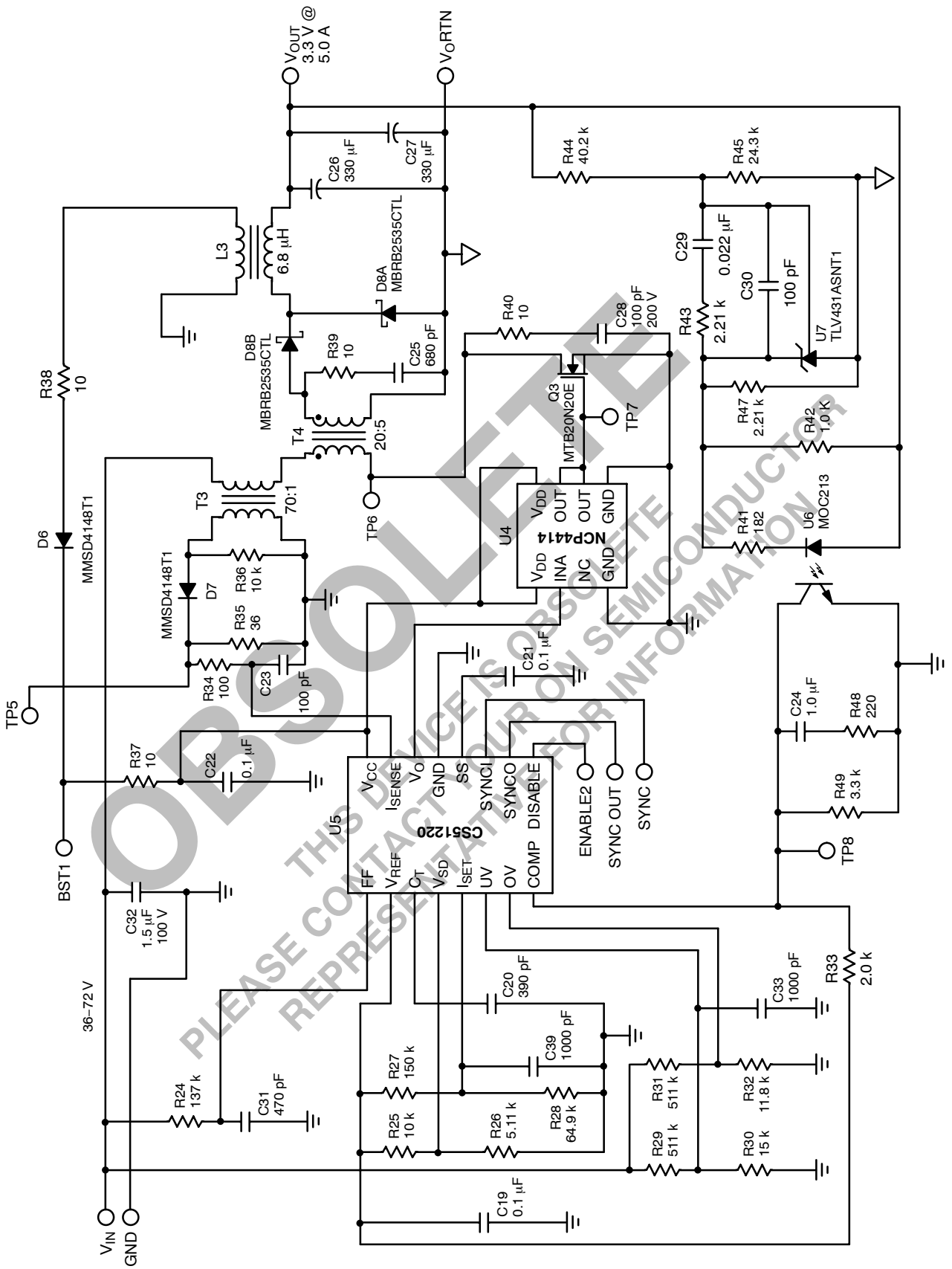
In Figure 18, the feed forward circuit has a volt−second constant of 63 V/μs. This would limit the duty factor to 0.39 at 48 V input. With a turns ratio of 4:1 on the power transformer and 48 V input, a duty factor of 0.33 is required for 3.3V output.

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Figure 17. Additional Application Diagram, 5.0 V Output Converter Used As Sync Master for the Dual Converter

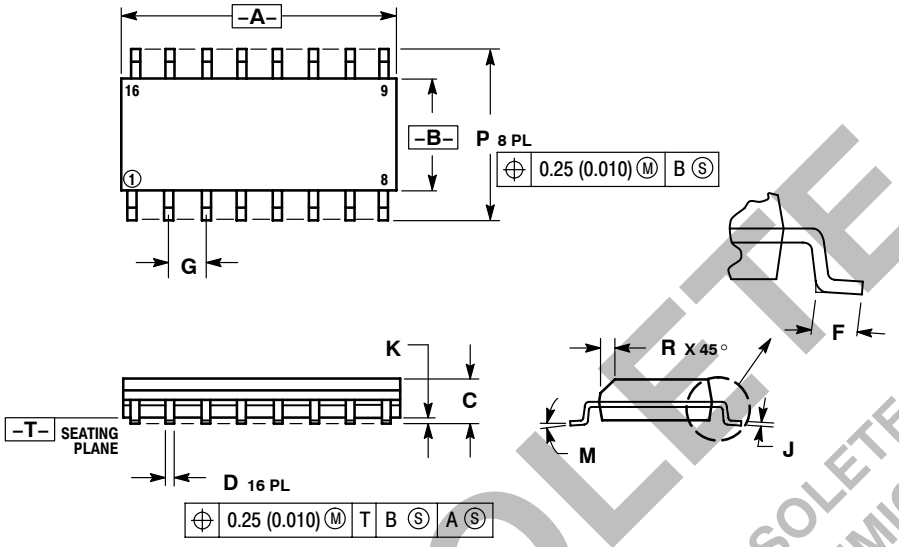


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Figure 18. Additional Application Diagram, 3.3 V Output Converter Synchronized to the 5.0 V Converter

PACKAGE DIMENSIONS

SO−16
D SUFFIX
CASE 751B−05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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