CS4525

# 30 W Digital TV Amplifier with Integrated ADC

## Digital Amplifier Features

- Fully Integrated Power MOSFETs
- No Heatsink Required
  - Programmable Power Foldback on Thermal Warning
  - High Efficiency (85%)
- > 100 dB Dynamic Range
- < 0.1% THD+N @ 1 W
- Configurable Outputs (10% THD+N)
  - 1 x 30 W into 4 Ω, Parallel Full-Bridge
  - 2 x 15 W into 8 Ω, Full-Bridge
  - 2 x 7 W into 4 Ω, Half-Bridge + 1 x 15 W into 8 Ω, Full-Bridge
- Built-In Protection with Error Reporting
  - Overcurrent/Undervoltage/Thermal Overload Shutdown
  - Thermal Warning Reporting
- PWM Popguard® for Half-Bridge Mode
- Click Free Start-Up
- Programmable Channel Delay for System Noise & Radiated Emissions Management

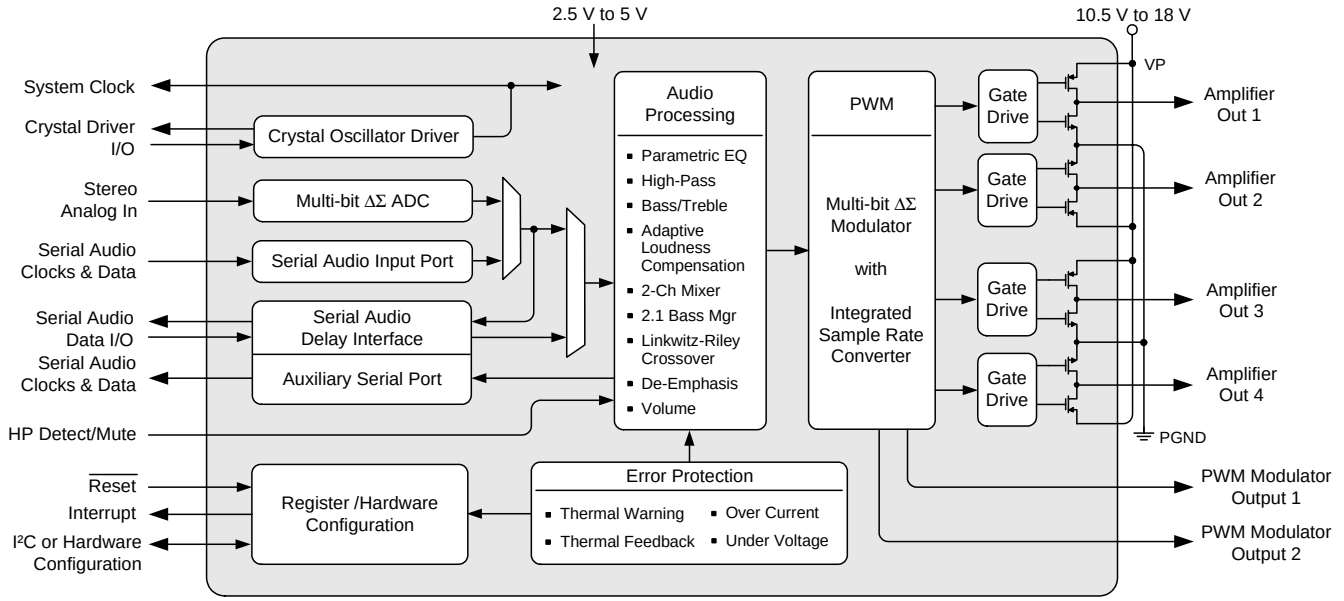
## ADC Features

- Stereo, 24-bit, 48 kHz Conversion
- Multi-bit Architecture
- 95 dB Dynamic Range (A-wtd)
- -88 dB THD+N
- 2 Vrms Input Supports SCART

## System Features

- Asynchronous 2-Channel Digital Serial Port
- 32 kHz to 96 kHz Input Sample Rates
- Operation with On-Chip Oscillator Driver or Applied SYS_CLK at 18.432, 24.576 or 27.000 MHz
- Integrated Sample Rate Converter (SRC)
  - Eliminates Clock-Jitter Effects
  - Input Sample Rate Independent Operation
  - Simplifies System Integration
- Spread Spectrum PWM Modulation
  - Reduces EMI Radiated Energy
- Low Quiescent Current

(**Features** continued on page 2)




*Advance Product Information*

This document contains information for a new product.
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## Software Mode System Features

- Digital Audio Processing
  - 3 Programmable Parametric EQ Filters for Channels 1 and 2
  - 2 Programmable Parametric EQ Filters for Channel 3
  - Selectable High-Pass Filter
  - Bass/Treble Tone Control
  - Adaptive Loudness Compensation
  - 2-Channel Mixer
  - 2.1 Bass Management
  - 24 dB/octave Linkwitz-Riley Crossover Filters
  - De-emphasis for 32 kHz, 44.1 kHz, 48 kHz
- Selectable Serial Audio Interface Formats
  - Left-Justified up to 24-bit
  - I²S up to 24-bit
  - Right-Justified 16-, 18-, 20-, 24-bits
- Digital Serial Connection to Additional CS4525 or DACs for Subwoofer
- Digital Interface to External Lip-Sync Delay
- PWM Switch Rate Shifting Eliminates AM Frequency Interference
- Digital Volume Control with Soft ramp
  - +24 to -103 dB in 0.5 dB steps
- Programmable Peak Detect and Limiter
- Flexible Power Output Configurations
- Thermal Foldback for Interruption-Free Power-Stage Protection
  - Supports Internal and External Power Stages
- Operation from On-Chip Oscillator Driver or Applied Systems Clock
- Supports I²C® Host Control Interface

## Hardware Mode System Features

- 2-Channel Stereo Full-Bridge Power Outputs
- Analog and Digital Inputs
- I²S and Left-Justified Serial Input Formats
- Thermal Foldback for Interruption-Free Protection of Internal Power Stage
- Operation from Applied Systems Clock
- External Mute Input

## Common Applications

- Integrated Digital TV's
- Flat Panel TV Monitors
- Computer/TV Monitors
- Mini/Micro Shelf Systems
- Digital Powered Speakers
- Portable Docking Stations
- Computer Desktop Audio

## General Description

The CS4525 is a stereo analog or digital input PWM high efficiency Class D amplifier audio system with an integrated stereo analog-to-digital (A/D) converter. The stereo power amplifiers can deliver up to 15 W per channel into 8 Ω speakers from a small space saving 48-pin QFN package. The PWM amplifier can achieve greater than 85% efficiency and the package is thermally enhanced for optimal heat dissipation which eliminates the need for a heatsink.

The power stage outputs can be configured as two full-bridge channels for 2 x 15 W operation, two half-bridge channels and one full-bridge channel for 2 x 7 W + 1 x 15 W operation, or one parallel full-bridge channel for 1 x 30 W operation. The CS4525 integrates on-chip over-current, under-voltage, over-temperature protection and error reporting as well as a thermal warning indicator and programmable foldback of the output power to allow cooling.

The main digital serial port on the CS4525 can support asynchronous operation with the integrated on-chip sample rate converter (SRC) which eases system integration. The SRC allows for a fixed PWM switching frequency regardless of incoming sample rate as well as optimal clocking for the A/D modulators.

An on-chip oscillator driver eliminates the need for an external crystal oscillator circuit, reducing overall design cost and conserving circuit board space. The CS4525 automatically uses the on-chip oscillator driver in the absence of an applied master clock.

The CS4525 is available in a 48-pin QFN package in Commercial grade (-10° to +70° C). The CRD4525 Customer Reference Design is also available.

Please refer to "Ordering Information" on page 90 for complete ordering information.

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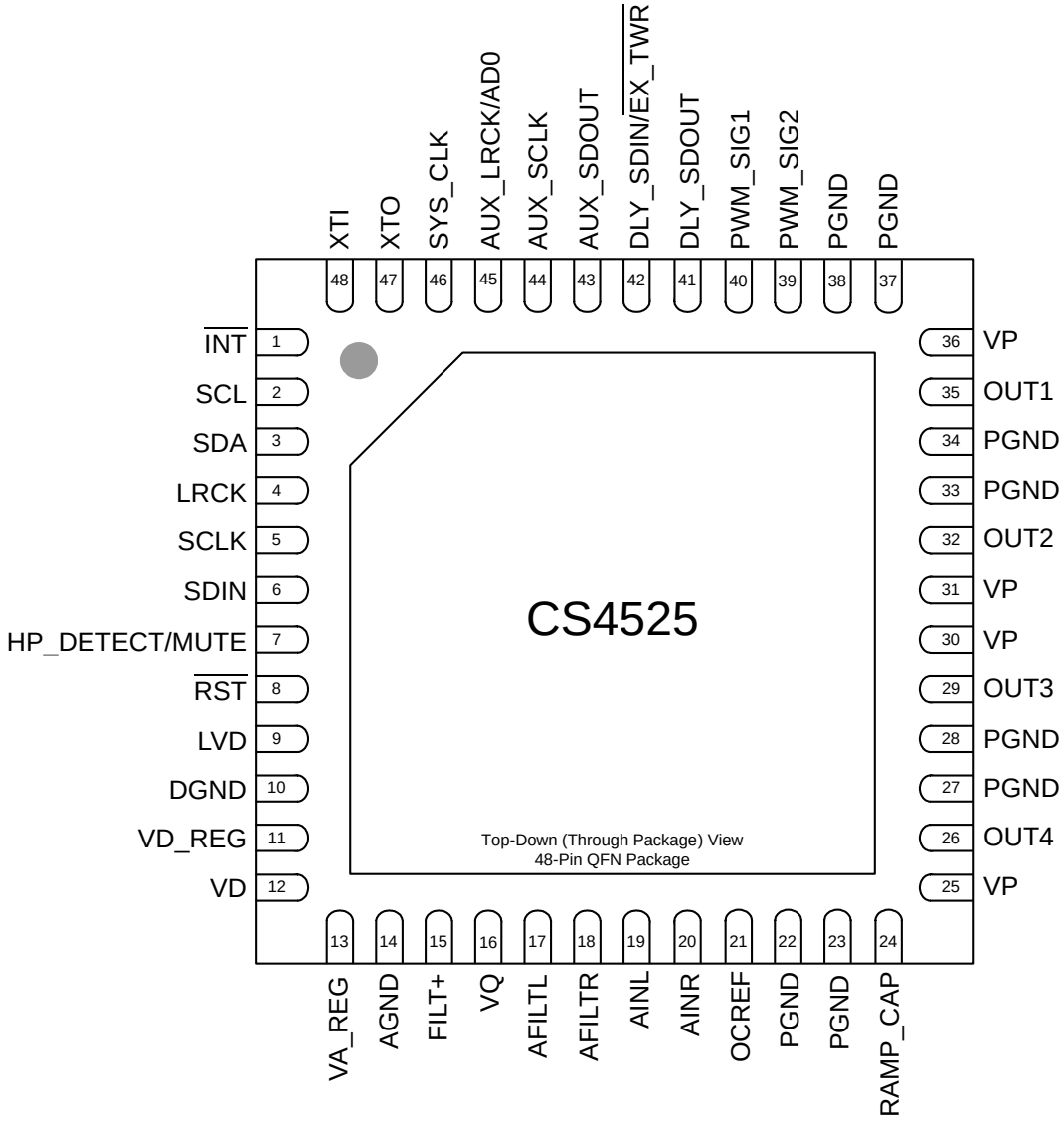
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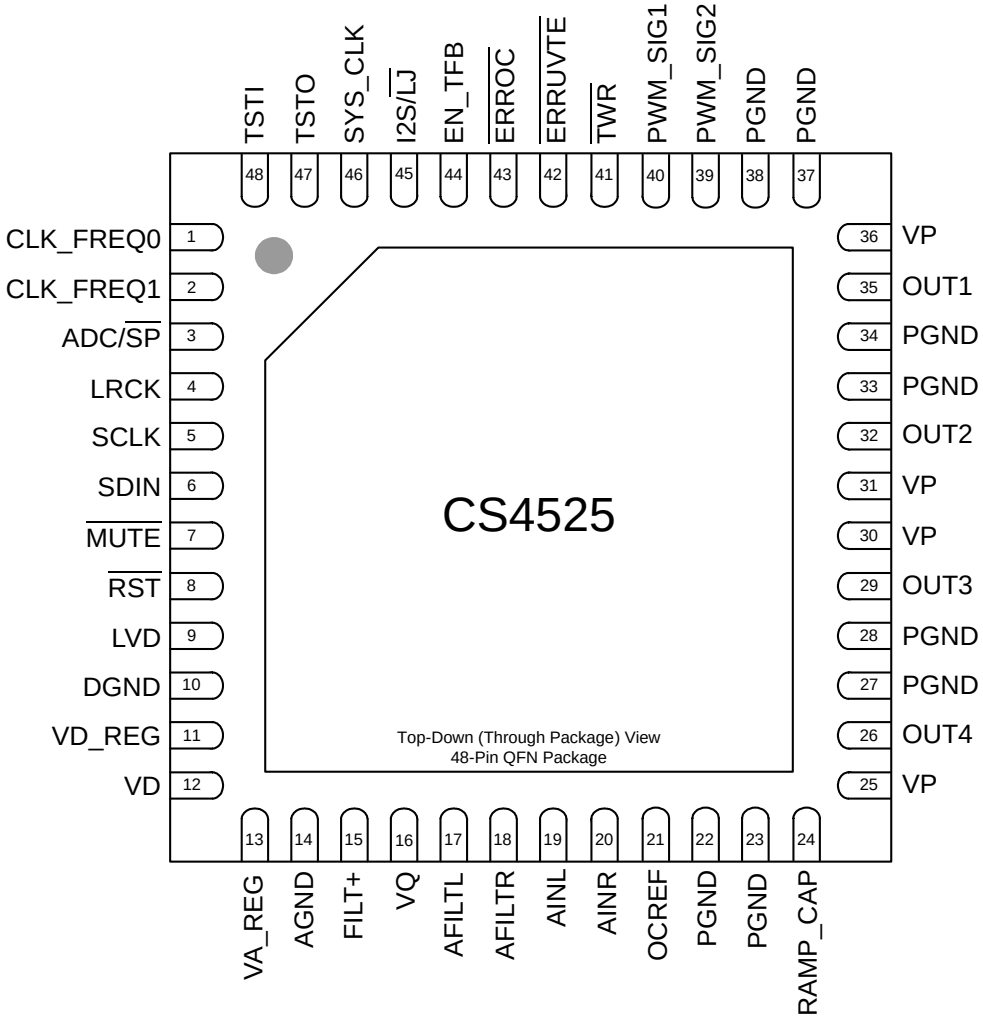
# 1. PIN DESCRIPTIONS - SOFTWARE MODE




| Pin Name | Pin # | Pin Description |
|---|---|---|
| $\overline{\text{INT}}$ | 1 | **Interrupt** *(Output)* - Indicates an interrupt condition has occurred. |
| SCL | 2 | **Serial Control Port Clock** (*Input*) - Serial clock for the I²C control port. |
| SDA | 3 | **Serial Control Data** (*Input/Output*) **-** Bi-directional data I/O for the I²C control port. |
| LRCK | 4 | **Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line. |
| SCLK | 5 | **Serial Clock** (*Input*) **-** Serial bit clock for the serial audio interface. |
| SDIN | 6 | **Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data. |
| HP_DETECT/ MUTE | 7 | **Headphone Detect / Mute** (*Input*) - Headphone detection or mute input signal. |
| $\overline{\text{RST}}$ | 8 | **Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when this pin is driven low. |

| | | |
|---|---|---|
| LVD | 9 | **VD Voltage Level Indicator** (*Input*) - Identifies the voltage level attached to VD. When applying 5.0 V to VD, LVD must be connected to VD. When applying 2.5 V or 3.3 V to VD, LVD must be DGND. |
| DGND | 10 | **Digital Ground** (*Input*) - Ground for the internal logic and digital I/O. |
| VD_REG | 11 | **Core Logic Power** (*Output*) - Internally generated low voltage power supply for digital logic. |
| VD | 12 | **Power** (*Input*) - Positive power supply for the internal regulators and digital I/O. |
| VA_REG | 13 | **Analog Power** *(Output)* **-** Internally generated positive power for the analog section and I/O. |
| AGND | 14 | **Analog Ground** (*Input*) - Ground reference for the internal analog section and I/O. |
| FILT+ | 15 | **Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal ADC sampling circuits. |
| VQ | 16 | **Common Mode Voltage** (*Output*) **-** Filter connection for internal common mode voltage. |
| AFILTL<br>AFILTR | 17<br>18 | **Antialias Filter Connection** (*Output*) - Antialias filter connection for ADC inputs. |
| AINL<br>AINR | 19<br>20 | **Analog Input** (*Input*) **-** The full-scale input level is specified in the ADC Analog Characteristics specification table. |
| OCREF | 21 | **Over Current Reference Setting** (*Input*) - Sets the reference for over current detection. |
| PGND | 22,23<br>27,28<br>33,34<br>37,38 | **Power Ground** (*Input*) - Ground for the individual output power half-bridge devices. |
| RAMP_CAP | 24 | **Output Ramp Capacitor** (*Input*) - Used for shaping the output ramp time for half-bridge configured outputs. |
| VP | 25,30,<br>31,36 | **High Voltage Power** (*Input*) - High voltage power supply for the individual half-bridge devices. |
| OUT4<br>OUT3<br>OUT2<br>OUT1 | 26<br>29<br>32<br>35 | **PWM Output** (*Output*) - Amplified PWM power outputs. |
| PWM_SIG2<br>PWM_SIG1 | 39<br>40 | **PWM Output** (*Output*) - PWM switching signals. |
| DLY_SDOUT | 41 | **Delay Serial Audio Data Out** (*Output*) - Output for two's complement serial audio data. Default pin configuration. |
| $\underline{\text{DLY_SDIN}}$/<br>$\underline{\text{EX_TWR}}$ | 42 | **Delay Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data. Default pin configuration.<br>**External Thermal Warning** (*Input*) - Input for an external thermal warning signal. Configurable via the I²C control port. |
| AUX_SDOUT | 43 | **Auxiliary Port Serial Audio Data Out** (*Output*) - Output for two's complement auxiliary port serial data. |
| AUX_SCLK | 44 | **Auxiliary Port Serial Clock** *(Output*) - Serial clock for the auxiliary port serial interface. |
| AUX_LRCK/<br>AD0 | 45 | **Auxiliary Port Left Right Clock** *(Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.<br>**AD0** *(Input*) - Sets the LSB of the I²C device address. Sensed on the release of $\overline{\text{RST}}$. |
| SYS_CLK | 46 | **System Clock** (*Input/Output*) -Clock source for the internal logic, processing, and modulators. |
| XTO | 47 | **Crystal Oscillator Output** *(Output)* - Crystal oscillator driver output. |
| XTI | 48 | **Crystal Oscillator Input** (*Input*) - Crystal oscillator driver input. |

## 2. PIN DESCRIPTIONS - HARDWARE MODE




| Pin Name | Pin # | Pin Description |
|---|---|---|
| CLK_FREQ0<br>CLK_FREQ1 | 1<br>2 | **Clock Frequency** *(Input)* - Determines the frequency of the clock expected to be driven into the SYS_CLK pin. |
| ADC/$\overline{SP}$ | 3 | **ADC/Serial Port** *(Input)* - Selects between the Analog to Digital Converter and the Serial Port for audio input. Selects the ADC when high or the serial port when low. |
| LRCK | 4 | **Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line. |
| SCLK | 5 | **Serial Clock** (*Input*) **-** Serial bit clock for the serial audio interface. |
| SDIN | 6 | **Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data. |
| $\overline{MUTE}$ | 7 | **Mute** (*Input*) - Mute input signal. |
| $\overline{RST}$ | 8 | **Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when this pin is driven low. |

| | | |
|---|---|---|
| LVD | 9 | **VD Voltage Level Indicator** (*Input*) - Identifies the voltage level attached to VD. When applying 5.0 V to VD, LVD must be connected to VD. When applying 2.5 V or 3.3 V to VD, LVD must be connected to DGND. |
| DGND | 10 | **Digital Ground** (*Input*) - Ground for the internal logic and I/O. |
| VD_REG | 11 | **Core Logic Power** (*Output*) - Internally generated low voltage power supply for digital logic. |
| VD | 12 | **Digital Power** (*Input*) - Positive power supply for the internal regulators and digital I/O. |
| VA_REG | 13 | **Analog Power** *(Output)* **-** Internally generated positive power for the analog section and I/O. |
| AGND | 14 | **Analog Ground** (*Input*) - Ground reference for the internal analog section and I/O. |
| FILT+ | 15 | **Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal ADC sampling circuits. |
| VQ | 16 | **Common Mode Voltage** (*Output*) **-** Filter connection for internal common mode voltage. |
| AFILTL<br>AFILTR | 17<br>18 | **Antialias Filter Connection** (*Output*) - Antialias filter connection for ADC inputs. |
| AINL<br>AINR | 19<br>20 | **Analog Input** (*Input*) **-** The full-scale input level is specified in the ADC Analog Characteristics specification table. |
| OCREF | 21 | **Over Current Reference Setting** (*Input*) - Sets the reference for over current detection. |
| PGND | 22,23<br>27,28<br>33,34<br>37,38 | **Power Ground** (*Input*) - Ground for the individual output power half-bridge devices. |
| RAMP_CAP | 24 | **Output Ramp Capacitor** (*Input*) - Used for shaping the output ramp time for half-bridge configured outputs. |
| VP | 25,30,<br>31,36 | **High Voltage Power** (*Input*) - High voltage power supply for the individual half-bridge devices. |
| OUT4<br>OUT3<br>OUT2<br>OUT1 | 26<br>29<br>32<br>35 | **PWM Output** (*Output*) - Amplified PWM power outputs. |
| PWM_SIG2<br>PWM_SIG1 | 39<br>40 | **PWM Output** (*Output*) - PWM switching signals. |
| $\overline{\text{TWR}}$ | 41 | **Thermal Warning Output** (*Output*) - Thermal warning output. |
| $\overline{\text{ERRUVTE}}$ | 42 | **Thermal and Undervoltage Error Output** (*Output*) - Error flag for thermal shutdown and undervoltage. |
| $\overline{\text{ERROC}}$ | 43 | **Overcurrent Error Output** *(Output)* - Overcurrent error flag. |
| EN_TFB | 44 | **Enable Thermal Feedback** *(Input)* - Enables the thermal foldback feature when high. |
| I2S/$\overline{\text{LJ}}$ | 45 | **I²S/Left Justified** *(Input)* - Selects between I²S and Left-Justified data format for the serial input and output ports. Selects I²S when high and LJ when low. |
| SYS_CLK | 46 | **System Clock** (*Input/Output*) -Clock source for the delta-sigma modulators. |
| TSTO | 47 | **Test Output** *(Output)* - This pin is an output used for the crystal oscillator driver available only in software mode. It must be left unconnected for normal hardware mode operation. |
| TSTI | 48 | **Test Input** (*Input*) - This pin is an input used for the crystal oscillator driver available only in software mode. It must be tied to digital ground for normal hardware mode operation. |

## 2.1 Digital I/O Pin Characteristics

The logic level for each input is set by its corresponding power supply and should not exceed the maximum ratings.

| Power Supply | Pin Number | Pin Name | I/O | Driver | Receiver |
|---|---|---|---|---|---|
| ***Software Mode*** | | | | | |
| VD | 1 | $\overline{\text{INT}}$ | Output | 2.5 V-5.0 V, Open Drain | |
| | 2 | SCL | Input | - | 2.5 V-5.0 V, with Hysteresis |
| | 3 | SDA | Input/Output | 2.5 V-5.0 V, Open Drain | 2.5 V-5.0 V, with Hysteresis |
| | 7 | HP_DETECT<br>MUTE | Input<br>Input | -<br>- | 2.5 V-5.0 V<br>2.5 V-5.0 V |
| | 41 | DLY_SDOUT | Output | 2.5 V-5.0 V, CMOS | - |
| | 42 | DLY_SDIN<br>$\overline{\text{EX_TWR}}$ | Input<br>Input | -<br>- | 2.5 V-5.0 V<br>2.5 V-5.0 V |
| | 43 | AUX_SDOUT | Output | 2.5 V-5.0 V, CMOS | - |
| | 44 | AUX_SCLK | Output | 2.5 V-5.0 V, CMOS | - |
| | 45 | AUX_LRCK | Output | 2.5 V-5.0 V, CMOS | - |
| ***Hardware Mode*** | | | | | |
| VD | 1 | SEL_OSC0 | Input | - | 2.5 V-5.0 V |
| | 2 | SEL_OSC1 | Input | - | 2.5 V-5.0 V |
| | 3 | ADC/$\overline{\text{SP}}$ | Input | - | 2.5 V-5.0 V |
| | 7 | $\overline{\text{MUTE}}$ | Input | - | 2.5 V-5.0 V |
| | 41 | $\overline{\text{TWR}}$ | Output | 2.5 V-5.0 V, Open Drain | - |
| | 42 | $\overline{\text{ERRUVTE}}$ | Output | 2.5 V-5.0 V, Open Drain | - |
| | 43 | $\overline{\text{ERROC}}$ | Output | 2.5 V-5.0 V, Open Drain | - |
| | 44 | EN_TFB | Input | - | 2.5 V-5.0 V |
| | 45 | I²S/$\overline{\text{LJ}}$ | Input | - | 2.5 V-5.0 V |
| ***All Modes*** | | | | | |
| VD | 4 | LRCK | Input | - | 2.5 V-5.0 V |
| | 5 | SCLK | Input | - | 2.5 V-5.0 V |
| | 6 | SDIN | Input | - | 2.5 V-5.0 V |
| | 8 | $\overline{\text{RST}}$ | Input | - | 2.5 V-5.0 V |
| | 9 | LVD | Input | - | 2.5 V-5.0 V |
| | 46 | SYS_CLK | Input/Output | 2.5 V-5.0 V, CMOS | 2.5 V-5.0 V |
| VD_REG | | PWM_SIG1 | Output | 2.5 V, CMOS | - |
| | | PWM_SIG2 | Output | 2.5 V, CMOS | - |
| VP | | OUT1-OUT4 | Output | 10.5 V-18.0 V Power MOSFET | - |

**Table 1. I/O Power Rails**

# 3. TYPICAL CONNECTION DIAGRAMS

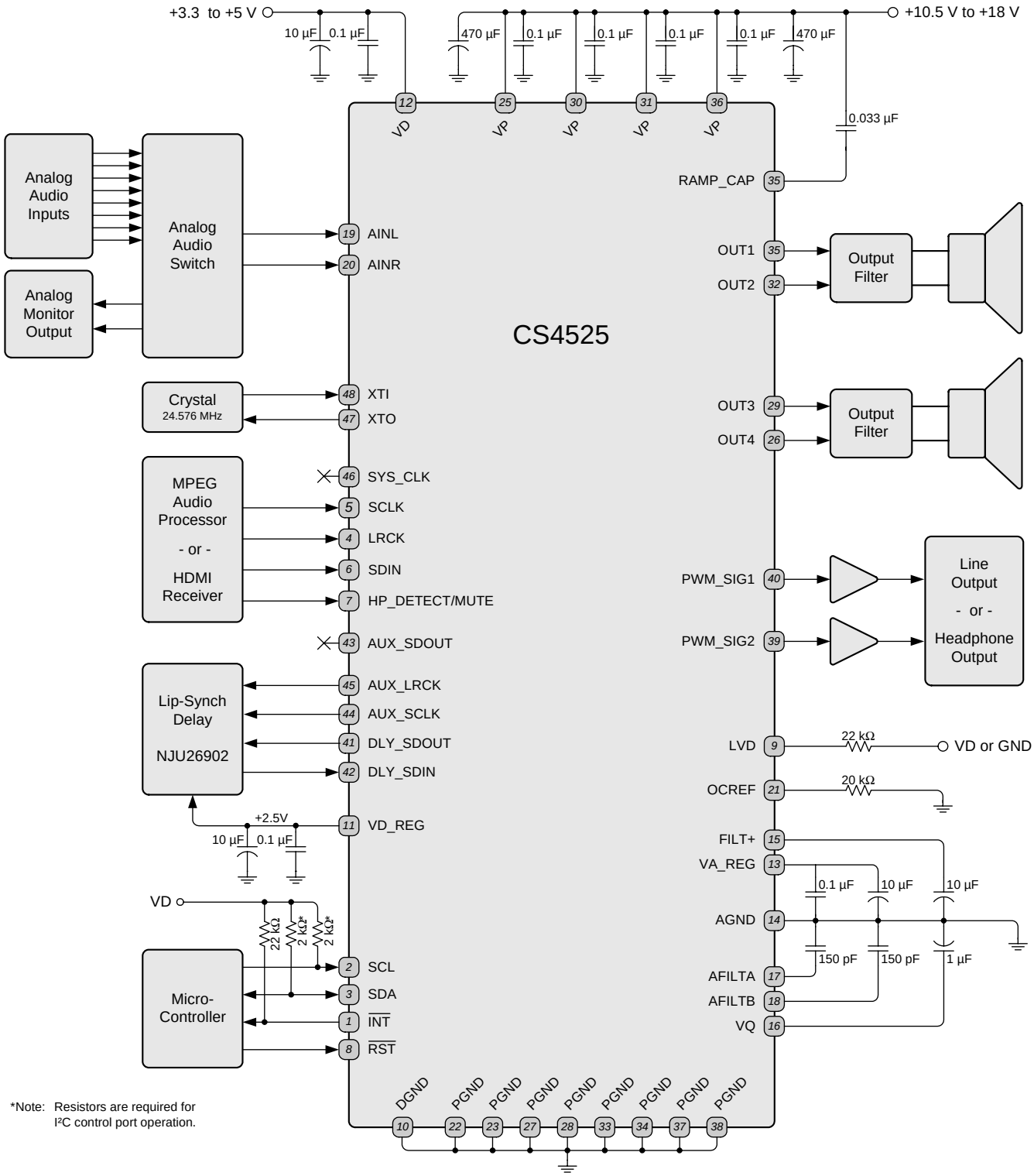



**Figure 1. Typical Connection Diagram - Software Mode**

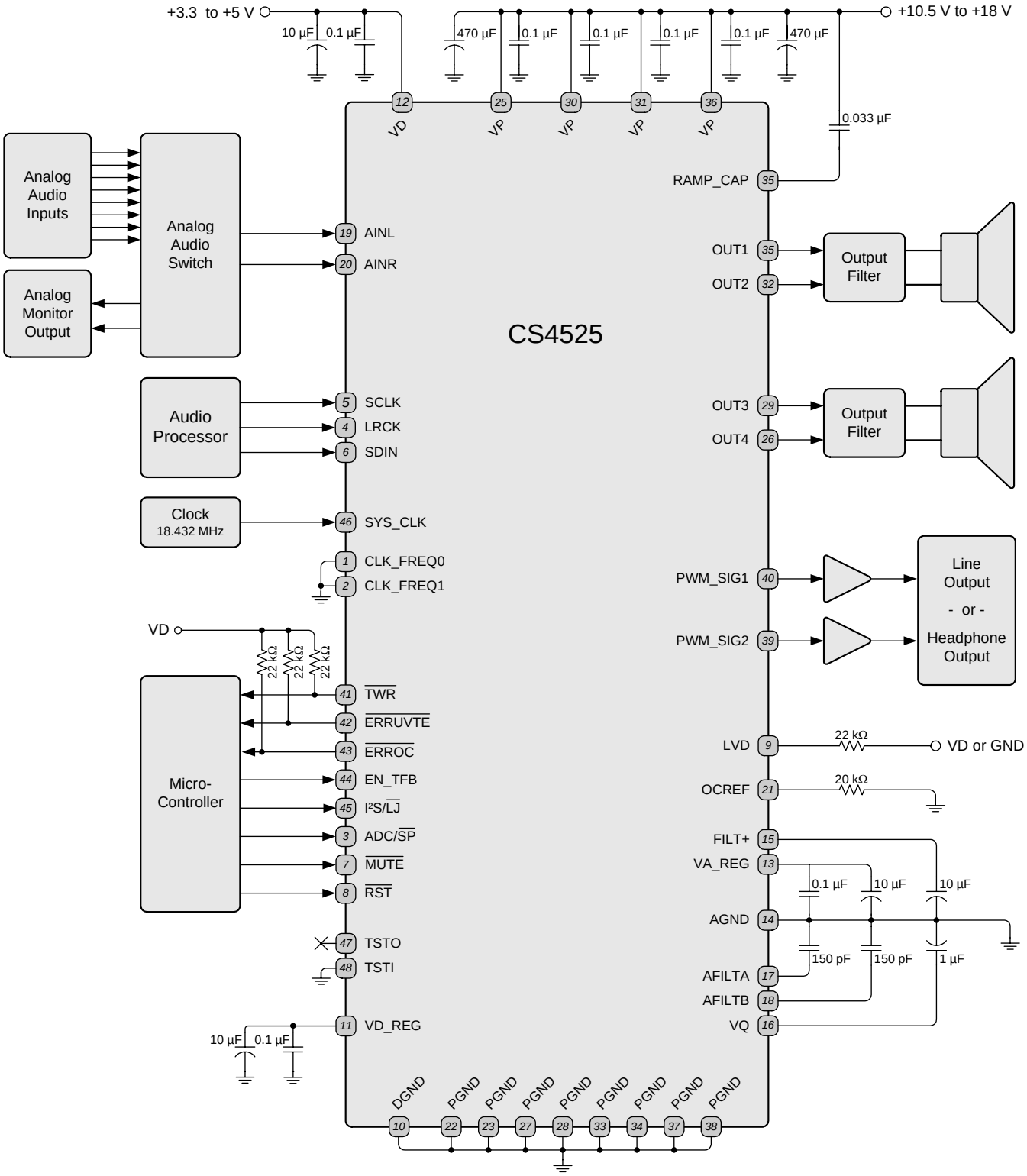



**Figure 2. Typical Connection Diagram - Hardware Mode**

# 4. TYPICAL SYSTEM CONFIGURATION DIAGRAMS

**2 x 7 W Stereo + 1 x 15 W Subwoofer**

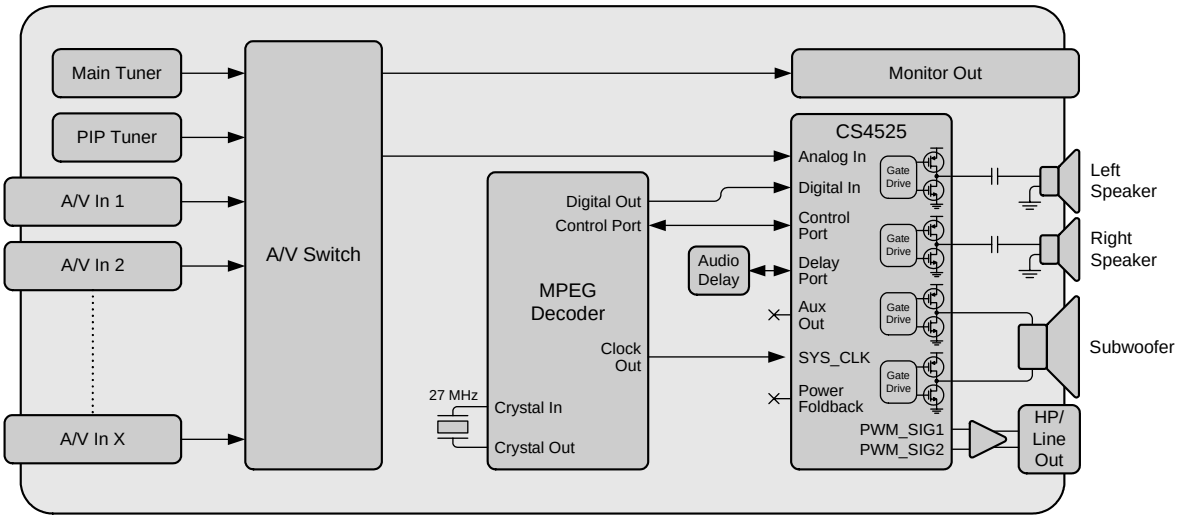



**Figure 3. Typical System Configuration 1**

**2 x 15 W Stereo + 1 x 30 W Subwoofer**

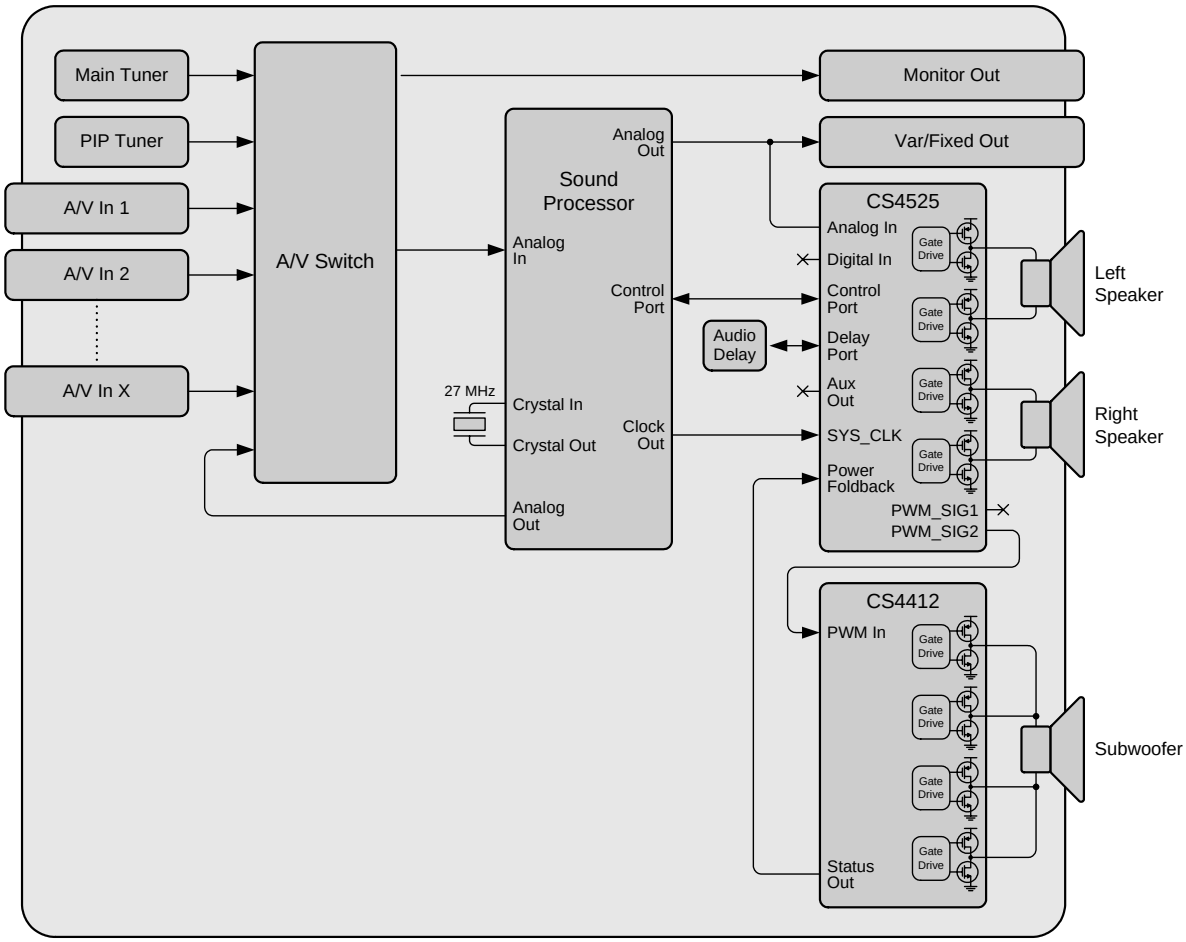



**Figure 4. Typical System Configuration 2**

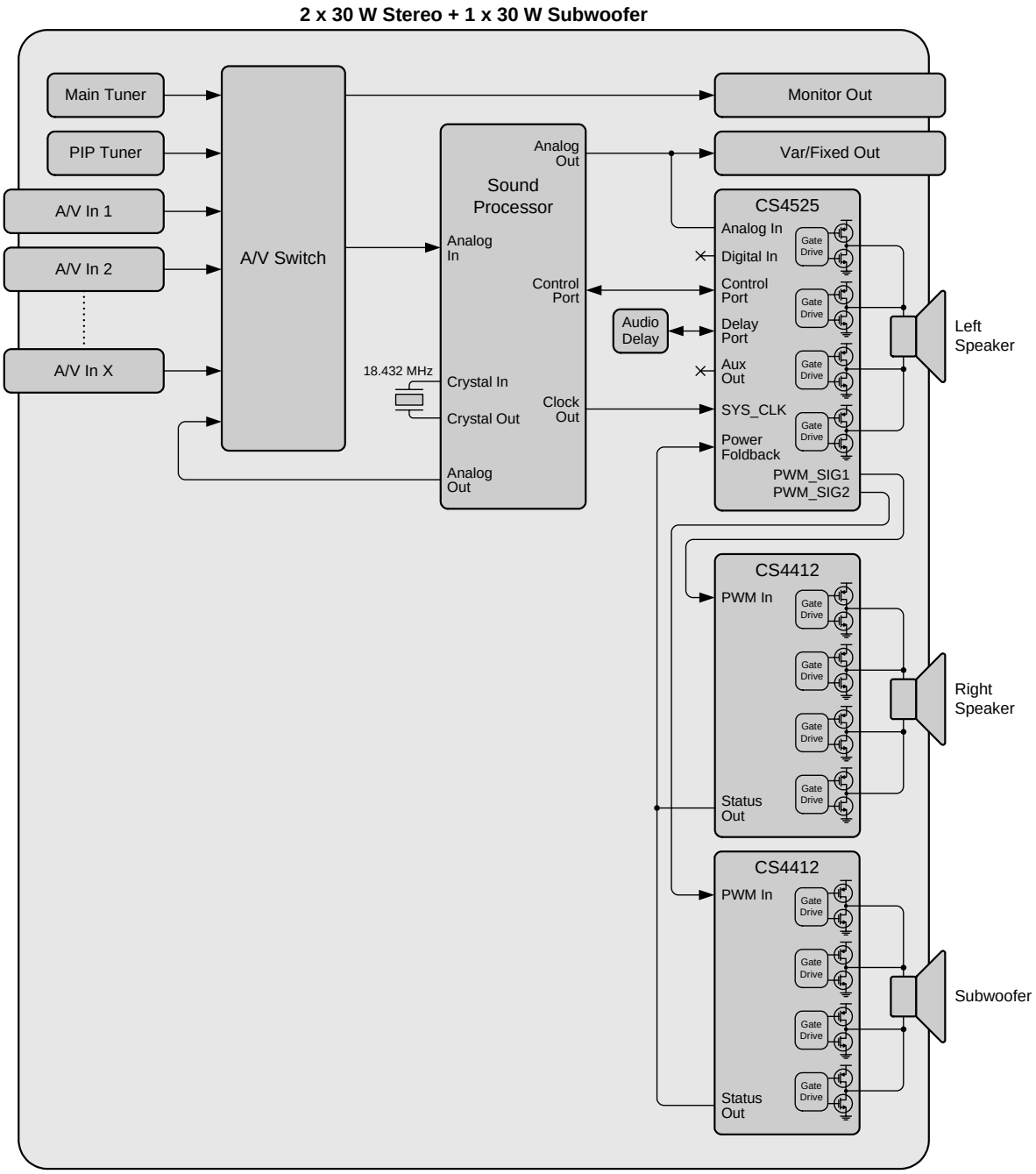



**Figure 5. Typical System Configuration 3**

**2 x 15 W Bi-Amp Stereo with Subwoofer Output**

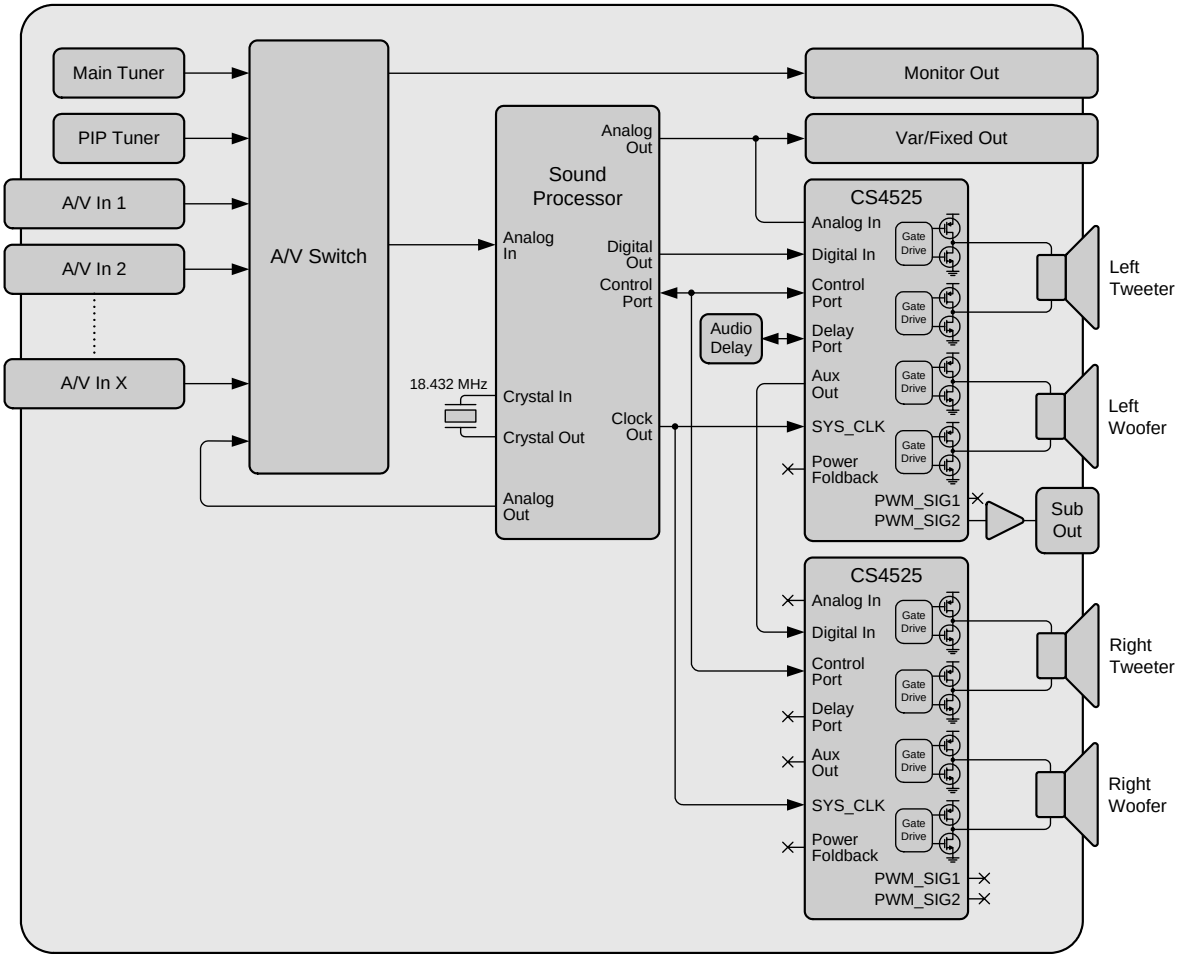



**Figure 6. Typical System Configuration 4**

# 5. CHARACTERISTIC AND SPECIFICATION TABLES

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and $T_A$ = 25° C.)

## SPECIFIED OPERATING CONDITIONS

(AGND = DGND=PGND=0 V, all voltages with respect to ground.)

| Parameters | Symbol | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| ***DC Power Supply*** | | | | | |
| Digital and Analog Core | VD | 2.375 | 2.5 | 2.625 | V |
| | VD | 3.135 | 3.3 | 3.465 | V |
| | VD | 4.75 | 5.0 | 5.25 | V |
| Amplifier Outputs | VP | 10.5 | - | 18.0 | V |
| ***Temperature*** | | | | | |
| Ambient Temperature Commercial | $T_A$ | -10 | - | +70 | °C |
| Junction Temperature | $T_J$ | | - | +150 | °C |

## ABSOLUTE MAXIMUM RATINGS

(AGND = DGND = PGND = 0 V; all voltages with respect to ground.)

| Parameters | Symbol | Min | Max | Units |
|---|---|---|---|---|
| DC Power Supply PWM Outputs | VP | -0.3 | 20.0 | V |
| Digital and Analog Core | VD | -0.3 | 6.0 | V |
| Input Current (Note 2) | $I_{in}$ | - | ±10 | mA |
| Analog Input Voltage (Note 3) | $V_{INA}$ | AGND-0.7 | VA_REG + 0.7 | V |
| Digital Input Voltage (Note 3) | $V_{IND}$ | -0.3 | VD + 0.4 | V |
| Ambient Operating Temperature - Power Applied Commercial | $T_A$ | -20 | +85 | °C |
| Storage Temperature | $T_{stg}$ | -65 | +150 | °C |

**Notes:**
1. Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.
2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
3. The maximum over/under voltage is limited by the input current.

## ANALOG INPUT CHARACTERISTICS

Test Conditions (unless otherwise specified): Input Signal: 1 kHz sine wave through the recommended passive input filter shown in Figure 27 on page 56; Sample Frequency = 48 kHz, 10 Hz to 20 kHz Measurement Bandwidth. Power outputs in power-down state (PDnOut1 = 1, PDnOut2 = 1, PDnOut3/4 = 1).

| Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ***Analog In to ADC*** | | | | | |
| Dynamic Range (Note 4) | A-weighted | 90 | 95 | - | dB |
| | unweighted | 87 | 92 | - | dB |
| Total Harmonic Distortion + Noise | -1 dB | - | -88 | -82 | dB |
| | -20 dB | - | -75 | - | dB |
| | -60 dB | - | -35 | - | dB |
| DC Accuracy | | | | | |
| Interchannel Gain Mismatch | | - | 0.1 | - | dB |
| Gain Drift | | - | ±100 | - | ppm/°C |
| **Input** | | | | | |
| Interchannel Isolation | | - | 90 | - | dB |
| Full-scale Input Voltage | | 1.96 | 2.18 | 2.40 | Vpp |
| Input Impedance | (Note 5) | 40 | - | - | kΩ |

**Notes:** 4. Referred to the typical full-scale voltage.

5. Measured between AINx and AGND.

## ADC DIGITAL FILTER CHARACTERISTICS

| Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Passband (Frequency Response) (Note 6) | to -0.1 dB corner | 0 | - | 0.4948 | Fs |
| Passband Ripple | | -0.09 | - | 0 | dB |
| Stopband | (Note 6) | 0.6677 | - | - | Fs |
| Stopband Attenuation | | 48.4 | - | - | dB |
| Total Group Delay | | - | 2.7/Fs | - | s |
| ***High-Pass Filter Characteristics*** | | | | | |
| Frequency Response | -3.0 dB | - | 3.7 | - | Hz |
| | -0.13 dB | - | 24.2 | - | Hz |
| Phase Deviation | 20 Hz | - | 10 | - | Deg |
| Passband Ripple | | - | - | 0.17 | dB |
| Filter Settling Time | | - | $10^5$/Fs | 0 | s |

**Notes:** 6. Filter response is clock dependent and scales with the ADC sampling frequency (Fs). With a 27.000 MHz or 24.576 MHz XTAL/SYS_CLK, Fs is equal to the applied clock divided by 512. With an 18.432 MHz XTAL/SYS_CLK, Fs is equal to the applied clock divided by 384.

## PWM POWER OUTPUT CHARACTERISTICS

AGND = DGND = PGND = 0 V; All voltages with respect to ground; VP = 18 V; $R_L$ = 8 Ω for full-bridge, $R_L$ = 4 Ω for half-bridge and parallel full-bridge; PWM Switch Rate = 384 kHz; 10 Hz to 20 kHz Measurement Bandwidth; Performance measurements taken with a full scale 997 Hz sine wave and AES17 filter; Unless otherwise specified.

| Parameters | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Power Output per Channel | | | | | | |
| Stereo Full-Bridge | $P_O$ | THD+N < 10% | - | 15 | - | W |
| | | THD+N < 1% | - | 12 | - | W |
| Half-Bridge | | THD+N < 10% | - | 7 | - | W |
| | | THD+N < 1% | - | 5.5 | - | W |
| Parallel Full-Bridge | | THD+N < 10% | - | 30 | - | W |
| | | THD+N < 1% | - | 23.5 | - | W |
| Total Harmonic Distortion + Noise | | | | | | |
| Stereo Full-Bridge | THD+N | $P_O$ = 1 W | - | 0.1 | - | % |
| | | $P_O$ = 0 dBFS = 11.3 W | - | 0.3 | - | % |
| Half-Bridge | | $P_O$ = 1 W | - | 0.1 | - | % |
| | | $P_O$ = 0 dBFS = 5.0 W | - | 0.3 | - | % |
| Parallel Full-Bridge | | $P_O$ = 1 W | - | 0.1 | - | % |
| | | $P_O$ = 0 dBFS = 22.6 W | - | 0.3 | - | % |
| Dynamic Range | | | | | | |
| Stereo Full-Bridge | DYR | $P_O$ = -60 dBFS, A-Weighted | - | 102 | - | dB |
| | | $P_O$ = -60 dBFS, Unweighted | - | 99 | - | dB |
| Half-Bridge | | $P_O$ = -60 dBFS, A-Weighted | - | 102 | - | dB |
| | | $P_O$ = -60 dBFS, Unweighted | - | 99 | - | dB |
| Parallel Full-Bridge | | $P_O$ = -60 dBFS, A-Weighted | - | 102 | - | dB |
| | | $P_O$ = -60 dBFS, Unweighted | - | 99 | - | dB |
| MOSFET On Resistance | $R_{DS(ON)}$ | $I_d$ = 0.5 A, $T_J$ = 50°C | - | 518 | 615 | mΩ |
| Efficiency | h | $P_O$ = 2 x 11.3 W, $R_L$ = 8 Ω | - | 85 | - | % |
| Minimum Output Pulse Width | $PW_{min}$ | No Load | - | 50 | - | ns |
| Rise Time of OUTx | $t_r$ | Resistive Load | - | 20 | - | ns |
| Fall Time of OUTx | $t_f$ | Resistive Load | - | 20 | - | ns |
| PWM Output Over-Current Error Trip Point | $I_{CE}$ | $T_A$ = 25°C, OCREF = 20 kΩ | 2.0 | - | - | A |
| Junction Thermal Warning Trip Point | $T_{TW}$ | | - | 120 | - | °C |
| Junction Thermal Error Trip Point | $T_{TE}$ | | - | 140 | - | °C |
| VP Under-Voltage Error Trip Point | $V_{UV}$ | $T_A$ = 25°C | 4 | - | - | V |
| Ramp-Up Time - Half-Bridge Configuration | $T_{RU}$ | Capacitor = 1000 µF | - | 0.8 | - | s |
| Ramp-Down Time- Half-Bridge Configuration | $T_{RD}$ | Capacitor = 1000 µF | - | 50 | - | s |

## SERIAL AUDIO INPUT PORT SWITCHING SPECIFICATIONS

Inputs: Logic 0 = DGND; Logic 1 = VD

| Parameters | Symbol | Min | Nominal | Max | Units |
|---|---|---|---|---|---|
| Supported Input Sample Rates | $F_{SI}$ | 28.5<br>39.5<br>39.5<br>86.4 | 32<br>44.1<br>48<br>96 | 35.2<br>52.8<br>52.8<br>105.6 | kHz<br>kHz<br>kHz<br>kHz |
| LRCK Duty Cycle | | 45 | - | 55 | % |
| SCLK Frequency Single-Speed Mode<br>Double-Speed Mode | $1/t_p$ | - | -<br>- | $128 \bullet F_{SI}$<br>$64 \bullet F_{SI}$ | Hz<br>Hz |
| SCLK Duty Cycle | | 45 | - | 55 | % |
| LRCK Setup Time Before SCLK Rising Edge | $t_{s(LK-SK)}$ | 40 | - | - | ns |
| SDIN Setup Time Before SCLK Rising Edge | $t_{s(SD-SK)}$ | 25 | - | - | ns |
| SDIN Hold Time After SCLK Rising Edge | $t_h$ | 10 | - | - | ns |
| $\overline{RST}$ pin Low Pulse Width (Note 7) | | 1 | - | - | ms |

**Notes:** 7. After powering up the CS4525, $\overline{RST}$ should be held low until the power supplies and clocks are stable.

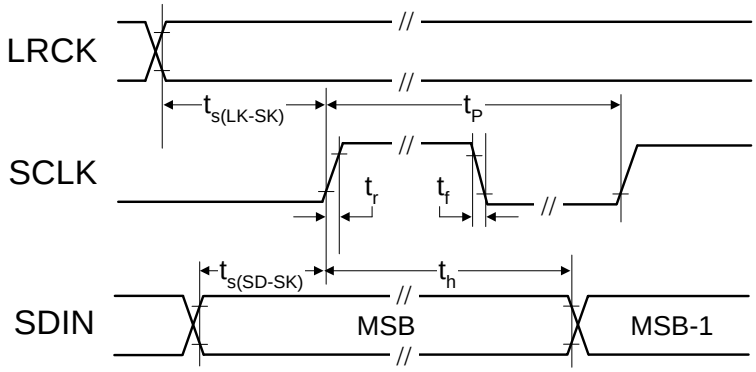



**Figure 7. Serial Audio Input Port Timing**

## AUX SERIAL AUDIO I/O PORT SWITCHING SPECIFICATIONS

Inputs: Logic 0 = DGND; Logic 1 = VD; AUX_SDOUT & DLY_SDOUT $C_L$ = 15 pF. (Note 8)

| Parameters | | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| ***Input Source: Analog Inputs (Internal ADC)*** | | | | | | |
| Output Sample Rate | ClkFreq[1:0] = '00'<br>ClkFreq[1:0] = '01'<br>ClkFreq[1:0] = '10' | $F_{SO}$ | -<br>-<br>- | $F_{CLK}/384$<br>$F_{CLK}/512$<br>$F_{CLK}/512$ | -<br>-<br>- | Hz<br>Hz<br>Hz |
| AUX_LRCK Duty Cycle | | | - | 50 | - | % |
| AUX_LRCK Period | | | - | $1/F_{SO}$ | - | s |
| AUX_SCLK Frequency | ClkFreq[1:0] = '00'<br>ClkFreq[1:0] = '01'<br>ClkFreq[1:0] = '10' | $F_{SCLKO}$ | -<br>-<br>- | $48 \bullet F_{SO}$<br>$64 \bullet F_{SO}$<br>$64 \bullet F_{SO}$ | -<br>-<br>- | Hz<br>Hz<br>Hz |
| AUX_SCLK Duty Cycle | | | - | 50 | - | % |
| AUX_SCLK Period | | | - | $1/F_{SCLKO}$ | - | s |
| ***Input Source: Serial Audio Input Port*** | | | | | | |
| Output Sample Rate | $F_{S-In}$ = 32kHz, 44.1 kHz, 48 kHz<br>$F_{S-In}$ = 96 kHz | $F_{SO}$ | -<br>- | $F_{SI}$<br>$F_{SI}/2$ | -<br>- | Hz<br>Hz |
| AUX_LRCK Duty Cycle | (Note 10) | | 45 | - | 55 | % |
| AUX_LRCK Period | (Note 9, 10) | | $T_{SI} - T_{CLK}$ | $T_{SI}$ | $T_{SI} + T_{CLK}$ | s |
| AUX_SCLK Frequency (Note 11) | $F_{S-In}$ = 32kHz, 44.1 kHz, 48 kHz<br>$F_{S-In}$ = 96 kHz | | -<br>- | $F_{SCLKI}$<br>$F_{SCLKI}/2$ | -<br>- | Hz<br>Hz |
| AUX_SCLK Duty Cycle | | | 30 | - | 70 | % |
| AUX_SCLK Period (Note 10, 11) | $F_{S-In}$ = 32kHz, 44.1 kHz, 48 kHz<br>$F_{S-In}$ = 96 kHz | | $T_{SCLKI} - T_{CLK}$<br>$2 \bullet T_{SCLKI} - T_{CLK}$ | $T_{SCLKI}$<br>$2 \bullet T_{SCLKI}$ | $T_{SCLKI} + T_{CLK}$<br>$2 \bullet T_{SCLKI} + T_{CLK}$ | s<br>s |
| ***Input Source: Analog Inputs or Serial Audio Input Port*** | | | | | | |
| AUX_LRCK Rising Edge to AUX_SCLK Falling Edge | | $t_{LTSF}$ | - | - | 20 | ns |
| AUX_SCLK Rising Edge to Data Output Valid | | $t_{SRDV}$ | - | - | $T_{CLK}$ + 20 | ns |
| DLY_SDIN Setup Time Before AUX_SCLK Rising Edge | | $t_{DIS}$ | 25 | - | - | ns |
| DLY_SDIN Hold Time After AUX_SCLK Rising Edge | | $t_{DIH}$ | 10 | - | - | ns |

**Notes:**

8. $F_{CLK}$ is the frequency of the applied crystal or the input SYS_CLK signal. $T_{CLK} = 1/F_{CLK}$.
9. $F_{SI}$ is the frequency of the input LRCK signal. $T_{SI} = 1/F_{SI}$
10. May vary during normal operation.
11. $F_{SCLKI}$ is the frequency of the input SCLK signal. $T_{SCLKI} = 1/F_{SCLKI}$.

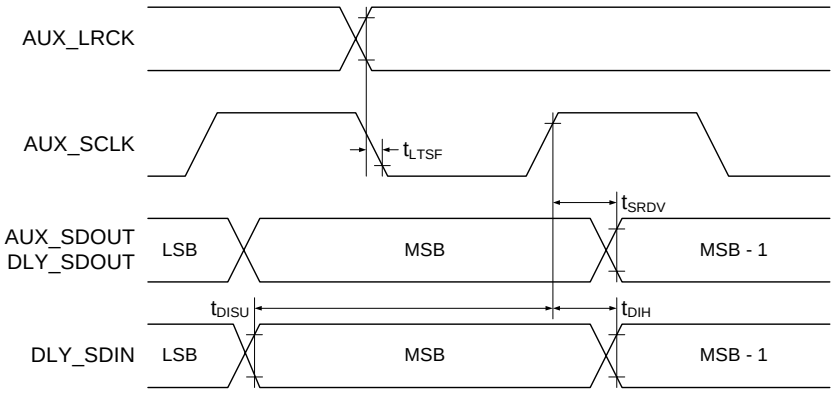



**Figure 8. AUX Serial Port Interface Master Mode Timing**

## XTI SWITCHING SPECIFICATIONS

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| External Crystal Operating Frequency (Note 12) | ClkFreq[1:0] = '00' | | 17.510 | 18.432 | 19.354 | MHz |
| | ClkFreq[1:0] = '01' | | 23.347 | 24.576 | 25.805 | MHz |
| | ClkFreq[1:0] = '10' | | 25.650 | 27.000 | 28.350 | MHz |
| XTI Duty Cycle | | | 45 | 50 | 55 | % |

**Notes:** 12. See "Clock Frequency (ClkFreq[1:0])" on page 64.

## SYS_CLK SWITCHING SPECIFICATIONS

Input: Logic 0 = DGND; Logic 1 = VD, SYS_CLK Output: $C_L$ = 20 pF.

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| External Clock Operating Frequency (Note 12) | ClkFreq[1:0] = '00' | | 17.510 | 18.432 | 19.354 | MHz |
| | ClkFreq[1:0] = '01' | | 23.347 | 24.576 | 25.805 | MHz |
| | ClkFreq[1:0] = '10' | | 25.650 | 27.000 | 28.350 | MHz |
| Rising Edge $\overline{RST}$ to start of SYS_CLK | | $t_{sclko}$ | | 1024*$t_{sclki}$ | | |
| SYS_CLK Period | | $t_{sclki}$ | 37.04 | --- | 54.25 | ns |
| SYS_CLK Duty Cycle | | | 45 | 50 | 55 | % |
| SYS_CLK high time | | $t_{clkih}$ | 16.67 | --- | 29.84 | ns |
| SYS_CLK low time | | $t_{clkil}$ | 16.67 | --- | 29.84 | ns |

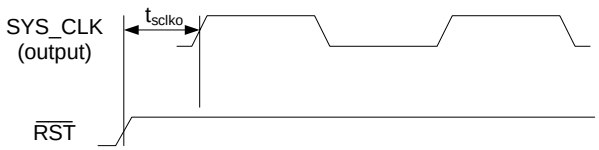



**Figure 9. SYS_CLK Timing from Reset**

## PWM_SIGX SWITCHING SPECIFICATIONS

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| PWM_SIGx Period | $t_{pwm}$ | 2.60 | - | 1.18 | µs |
| Rise Time of PWM_SIGx | $t_r$ | - | 2.1 | - | ns |
| Fall Time of PWM_SIGx | $t_f$ | - | 1.4 | - | ns |

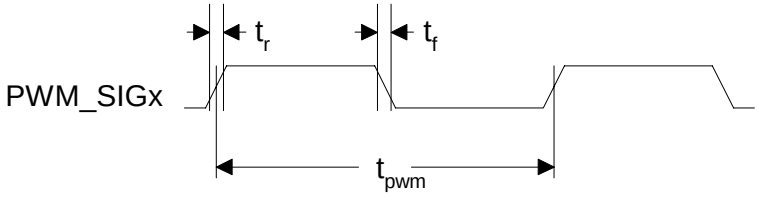



**Figure 10. PWM_SIGX Timing**

## I²C CONTROL PORT SWITCHING SPECIFICATIONS

Inputs: Logic 0 = DGND; Logic 1 = VD; SDA $C_L$ = 30 pF

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| SCL Clock Frequency | $f_{scl}$ | - | 100 | kHz |
| RST Rising Edge to Start | $t_{irs}$ | 500 | - | ns |
| Bus Free Time Between Transmissions | $t_{buf}$ | 4.7 | - | µs |
| Start Condition Hold Time (prior to first clock pulse) | $t_{hdst}$ | 4.0 | - | µs |
| Clock Low time | $t_{low}$ | 4.7 | - | µs |
| Clock High Time | $t_{high}$ | 4.0 | - | µs |
| Setup Time for Repeated Start Condition | $t_{sust}$ | 4.7 | - | µs |
| SDA Hold Time from SCL Falling (Note 13) | $t_{hdd}$ | 0 | - | µs |
| SDA Setup time to SCL Rising | $t_{sud}$ | 250 | - | ns |
| Rise Time of SCL and SDA | $t_{rc}$ | - | 1 | µs |
| Fall Time SCL and SDA | $t_{fc}$ | - | 300 | ns |
| Setup Time for Stop Condition | $t_{susp}$ | 4.7 | - | µs |
| Acknowledge Delay from SCL Falling | $t_{ack}$ | 300 | 1000 | ns |

**Notes:** 13. Data must be held for sufficient time to bridge the transition time, $t_{fc}$, of SCL.

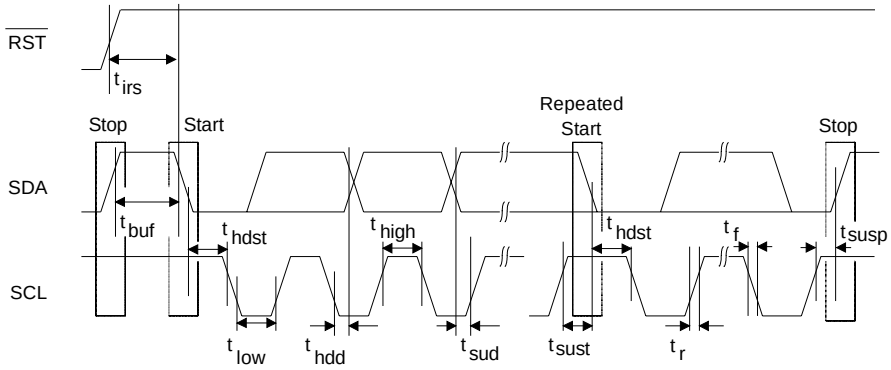



**Figure 11. Control Port Timing - I²C**

## DC ELECTRICAL CHARACTERISTICS

AGND = DGND = PGND = 0 V; All voltages with respect to ground; PWM switch rate = 384 kHz; Unless otherwise specified.

| Parameters | | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Normal Operation | (Note 14) | | | | |
| Power Supply Current | VD = 3.3 V | - | 20 | - | mA |
| Power Dissipation | VD = 3.3 V | - | 66 | - | mW |
| Power-Down Mode | (Note 15) | | | | |
| Power Supply Current | VD = 3.3 V | - | 4.3 | - | mA |
| ***VD_REG Characteristics*** | | | | | |
| Nominal Voltage | | 2.25 | 2.5 | 2.75 | V |
| DC current source | | - | - | 3 | mA |
| ***VA_REG Characteristics*** | | | | | |
| Nominal Voltage | | 2.25 | 2.5 | 2.75 | V |
| DC current source | | - | - | 1 | mA |
| ***VQ Characteristics*** | | | | | |
| Nominal Voltage | | - | 0.5•VA_REG | - | V |
| Output Impedance | | - | 23 | - | kΩ |
| DC current source/sink | (Note 16) | - | - | 10 | µA |
| Filt+ Nominal Voltage | | - | VA_REG | - | V |
| Power Supply Rejection Ratio (Note 17) | 1 kHz | - | 60 | - | dB |
| | 60 Hz | - | 40 | - | dB |

**Notes:**

14. Normal operation is defined as $\overline{RST}$ = HI.
15. Power-Down Mode is defined as $\overline{RST}$ = LOW with all input lines held static.
16. The DC current drain represents the allowed current from the VQ pin due to typical leakage through the electrolytic de-coupling capacitors.
17. Valid with the recommended capacitor values on FILT+ and VQ. Increasing the capacitance will increase the PSRR.

## DIGITAL INTERFACE SPECIFICATIONS

AGND = DGND = PGND = 0 V; All voltages with respect to ground; Unless otherwise specified.

| Parameters | | Symbol | Min | Max | Units |
|---|---|---|---|---|---|
| High-Level Input Voltage | | $V_{IH}$ | 0.7*VD_REG | VD | V |
| Low-Level Input Voltage | | $V_{IL}$ | - | 0.20*VD_REG | V |
| High-Level Output Voltage | $I_o$=2 mA | $V_{OH}$ | 0.90*VD | - | V |
| Low-Level Output Voltage | $I_o$=2 mA | $V_{OL}$ | - | 0.2 | V |
| Input Leakage Current | | $I_{in}$ | - | ±10 | uA |
| Input Capacitance | | | - | 8 | pF |

# 6. APPLICATIONS

## 6.1 Software Mode

Maximum device flexibility and features are available when the CS4525 is used in software mode. The available features are described in the following sections. All device configuration is achieved via the I²C control port as described in the I²C Control Port Description and Timing section on page 59.

### *6.1.1 System Clocking*

In software mode, the CS4525 can be clocked by a stable external clock source input on the SYS_CLK pin or by a clock internally generated through the use of its internal oscillator driver circuit in conjunction with an external crystal oscillator. The device automatically selects which of these clocks to use immediately after the release of $\overline{\text{RST}}$.

The internal clock is used to synchronize the input serial audio signals with the internal clock domain and to clock the internal digital processing, sample-rate converter, and PWM modulators. It is also used to determine the sample rate of the serial audio input signals in order to automatically configure the various internal filter coefficients.

To ensure proper operation, the CS4525 must be informed of the nominal frequency of the supplied SYS_CLK signal or the attached crystal via the ClkFreq[1:0] bits in the Clock Config register. These bits must be set to the appropriate value before the PDnAll bit is cleared to initiate a power-up sequence. See the SYS_CLK Switching Specifications and XTI Switching Specifications tables on page 23 for complete input frequency range specifications.

| Referenced Control | Register Location |
|---|---|
| ClkFreq[1:0] | "Clock Frequency (ClkFreq[1:0])" on page 64 |
| PDnAll | "Power Down (PDnAll)" on page 81 |

#### *6.1.1.1 SYS_CLK Input Clock Mode*

If an input clock is detected on the SYS_CLK pin and oscillations are not detected on the XTI pin following the release of $\overline{\text{RST}}$, the device will automatically use the SYS_CLK input as its clock source. The applied SYS_CLK clock signal must oscillate within the frequency ranges specified in the SYS_CLK switching specifications table on page 23. In this mode, XTI should be connected to ground and XTO should be left unconnected.

Figure 12 below demonstrates a typical clocking configuration using the SYS_CLK input.

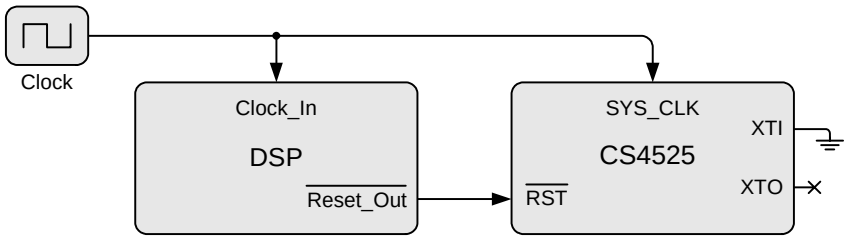



**Figure 12. Typical SYS_CLK Input Clocking Configuration**

#### 6.1.1.2 Crystal Oscillator Mode

To use an external crystal in conjunction with the internal crystal driver, a 20 pF fundamental mode parallel resonant crystal must be connected between the XTI and XTO pins. This crystal must oscillate within the frequency ranges specified in the XTI switching specifications table on page 23. Nothing other than the crystal and its load capacitors should be connected to XTI and XTO.

If an external crystal is connected to the XTI/XTO pins following the release of $\overline{RST}$, the device will automatically use the crystal as its clock source regardless of the presence of an input clock signal on the SYS_CLK pin.

In this mode, the CS4525 will automatically drive the generated internal clock out of the SYS_CLK pin. This can be disabled with the EnSysClk bit which will cause the SYS_CLK pin to become high-impedance. Also, the DivSysClk bit allows the frequency of the generated internal clock to be divided by 2 prior to being driven out of the SYS_CLK.

It should be noted that the internal oscillator driver is disabled when the CS4525 is in reset (RST is low). Any external devices connected to the SYS_CLK output will not receive a clock signal until the CS4525 is taken out of reset.

Figure 13 below demonstrates a typical clocking configuration using the crystal oscillator.

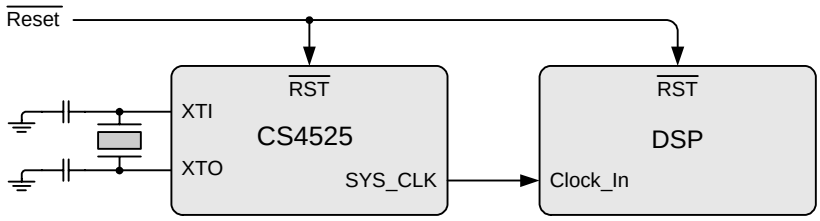



**Figure 13. Typical Crystal Oscillator Clocking Configuration**

| Referenced Control | Register Location |
|---|---|
| EnSysClk | "SYS_CLK Output Enable (EnSysClk)" on page 64 |
| DivSysClk | "SYS_CLK Output Divider (DivSysClk)" on page 64 |

### 6.1.2 Power-Up and Power-Down

The CS4525 will remain in a completely powered-down state with the control port inaccessible until the RST pin is brought high. Once RST is high, the control port will be accessible, but all other internal blocks will remain powered-down until they are powered-up via the control port or until hardware mode is entered.

When an external crystal is present on the XTI/XTO pins, software mode will be automatically entered 10 ms after the release of RST. If SYS_CLK is used as an input, software mode is entered by writing to the control port within 10 ms after the release of RST. If the control port is not written within this time, the device will begin to operate in hardware mode.

#### 6.1.2.1 Recommended Power-Up Sequence

1. Hold RST low until the power supplies and the input SYS_CLK (if used) are stable.
2. Bring RST high.
   *The device will remain in a low-power state and the control port will be accessible. The device will automatically enter software mode after 10 ms if an external crystal is present on the XTI/XTO pins, at which time the output SYS_CLK signal will become active.*
3. If SYS_CLK is used as an input, initiate a control port write to set the PDnAll bit in register 5Fh within 10 ms following the release of RST.
   *This operation causes the device to enter software mode and places it in power-down mode.*
4. If the LVD pin is tied low and VD is connected to 2.5 V, clear the SelectVD bit in the Power Ctrl register to indicate the 2.5 V VD supply level.
5. The desired register settings can be loaded while keeping the PDnAll bit set.
6. Clear the PDnAll bit to initiate the power-up sequence.

#### 6.1.2.2 Recommended Power-Down Sequence

1. Set the PDnAll bit to power-down the device while eliminating audible pops.
2. Bring RST low to bring the device's power consumption to an absolute minimum.
3. Remove power.

| Referenced Control | Register Location |
|---|---|
| PDnAll | "Power Down (PDnAll)" on page 81 |
| LVD | "Select VD Level (SelectVD)" on page 81 |

### 6.1.3 Input Source Selection

The CS4525 can accept analog or digital audio input signals. Digital audio input signals are supplied through the serial audio input port as outlined in "Serial Audio Interfaces" on page 57. Analog audio input signals are supplied through the internal ADC as outlined in "Analog Inputs" on page 56. The input source is selected by the ADC/SP bit in the Input Config register.

In software mode, the serial audio input port supports I²S, Left-Justified and Right-Justified data formats. The serial audio input port digital interface format is configured by the DIF[2:0] bits in the Input Config register.

The CS4525 internal ADC includes a dedicated high-pass filter to remove any DC content from the ADC output signal prior to the internal ADC/serial audio input port input multiplexor. This high-pass filter can be bypassed by clearing the EnAnHPF bit.

| Referenced Control | Register Location |
|---|---|
| ADC/SP | "Input Source Selection (ADC/SP)" on page 66 |
| DIF[2:0] | "Input Serial Port Digital Interface Format (DIF [2:0])" on page 66 |
| EnAnHPF | "ADC High-Pass Filter Enable (EnAnHPF)" on page 66 |

### 6.1.4 Digital Sound Processing

The CS4525 implements flexible digital sound processing operations including bass management cross-over, 2-way speaker crossovers, high- and low-pass shelving filters, programmable parametric EQ filters, adaptive loudness compensation, channel mixers, and volume controls.

The digital signal flow is shown in Figure 14 below. The signal processing blocks are described in detail in the following sections.

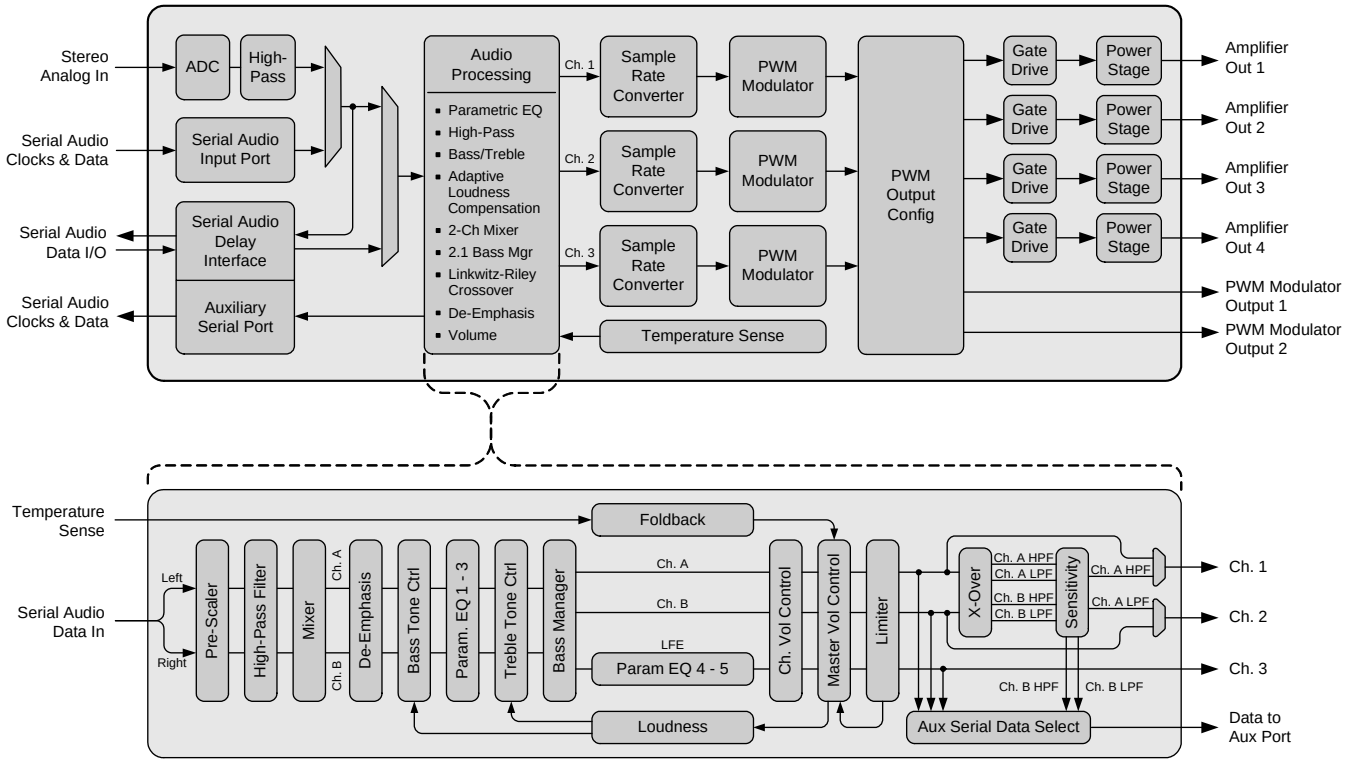



**Figure 14. Digital Signal Flow**

#### 6.1.4.1 Pre-Scaler

Applying any gain to a full-scale signal in the digital domain will cause the signal to clip. To prevent this, a pre-scaler block is included prior to the internal digital signal processing blocks. This allows the input signal to be attenuated before processing to ensure that any signal boosting, such as gain in a shelving filter, will not cause a channel to clip.

The pre-scaler block allows up to -14.0 dB of attenuation in 2.0 dB increments and is controlled with the PreScale[2:0] bits.

| Referenced Control | Register Location |
|---|---|
| PreScale[2:0]..... | "Pre-Scale Attenuation (PreScale[2:0])" on page 70 |

#### 6.1.4.2 Digital Signal Processing High-Pass Filter

The CS4525 includes a high-pass filter at the beginning of the digital signal processing chain to remove any DC content from the input signal prior to the remaining internal digital signal processing blocks. The high-pass filter operates by continuously subtracting a measure of the DC offset from the input signal and may be used regardless of the input data source.

The digital signal processing high-pass filter can be disabled by clearing the EnDigHPF bit.

| Referenced Control | Register Location |
|---|---|
| EnDigHPF | "Digital Signal Processing High-Pass Filter (EnDigHPF)" on page 71 |

#### 6.1.4.3 Channel Mixer

The CS4525 implements independent channel mixers to provide for both mono mixes and channel swaps for the left and right channels. The channel mixers are controlled by the LChMix[1:0] and RChMix[1:0] bits in the Mixer Config register.

To allow stereo headphone operation when a mono mix is configured, when the HP_DETECT/MUTE pin is configured for headphone detection (the HP/Mute bit is set), the operation of the left channel mixer is affected by the active state of the headphone detection input signal. In this configuration, when the left channel mixer is configured for a mono mix (LChMix[1:0] = 01 or 10) and the headphone detection input signal becomes active, the left channel mixer will be automatically reconfigured to output the left channel, thereby disabling the mono mix. When the headphone detection input signal becomes inactive, the mixer will be automatically reconfigured to operate as dictated by the LChMix[1:0] bits.

It should be noted that the right channel mixer output is unaffected by the headphone detection input signal and will always operate as dictated by the RChMix[1:0] bits.

| Referenced Control | Register Location |
|---|---|
| LChMix[1:0[ | "Left Channel Mixer (LChMix[1:0])" on page 71 |
| RChMix[1:0] | "Right Channel Mixer (RChMix[1:0])" on page 70 |
| HP/Mute | "HP_Detect/Mute Pin Mode (HP/Mute)" on page 65 |

### 6.1.4.4 De-Emphasis

The CS4525 includes an on-chip digital de-emphasis filter optimized for a sample rate of 44.1 kHz to accommodate audio recordings that utilize 50/15 µs pre-emphasis equalization as a means of noise reduction. The filter response is shown in Figure 15. The de-emphasis filter is enabled and disabled by the DeEmph bit in the Tone Config register.

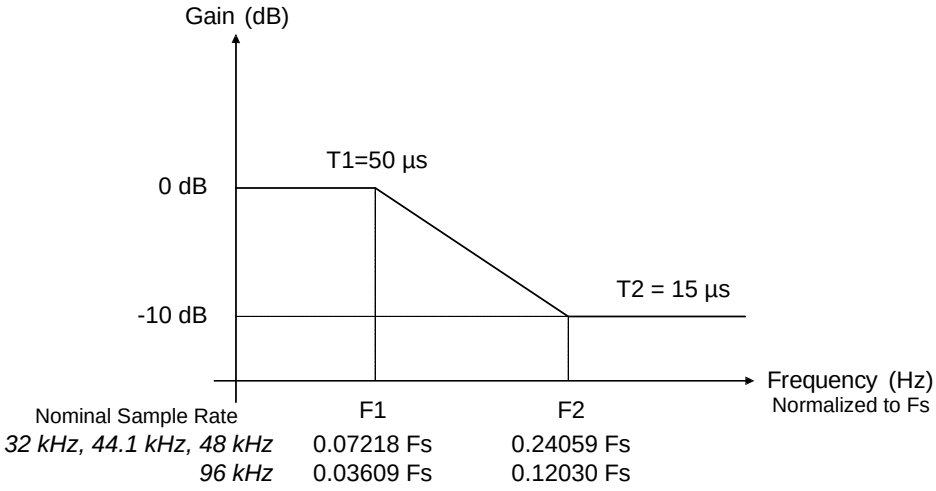



**Figure 15. De-Emphasis Filter**

| Referenced Control | Register Location |
|---|---|
| DeEmph | "De-Emphasis Control (DeEmph)" on page 71 |

### 6.1.4.5 Tone Control

The CS4525 implements configurable bass and treble shelving filters to easily accommodate system tone control requirements. Each shelving filter has 4 selectable corner frequencies, and provides a cut/boost range from -10.5 dB to +12.0 dB in 1.5 dB increments. The tone control is enabled by the EnToneCtrl bit in the Tone Config register.

Each tone control is implemented with one of two preset internal filter sets. One set is optimized for a 32 kHz sample rate, and the other is optimized for 44.1 kHz, 48 kHz, and 96 kHz sample rates. The CS4525 automatically detects the input sample rate and chooses the appropriate filter set to apply. The available corner frequencies are shown in tables 2 and 3 below and are configured with the BassFc[1:0] and TrebFc[1:0] bits in the Tone Config register.

Note that the corner frequency of each filter set scales linearly with the input sample rate.

When the internal ADC is used as the serial audio data source, the input sample rate is nominally 48 kHz and the corresponding shelving frequency corners are available.

| Input Sample Rate | Bass Fc 0 | Bass Fc 1 | Bass Fc 2 | Bass Fc 3 |
|---|---|---|---|---|
| 32 kHz | 50 Hz | 100 Hz | 200 Hz | 250 Hz |
| 44.1 kHz | 48 Hz | 96 Hz | 192 Hz | 240 Hz |
| 48 kHz, 96 kHz | 52 Hz | 104 Hz | 208 Hz | 260 Hz |

**Table 2. Bass Shelving Filter Corner Frequencies**

| Input Sample Rate | Treble Fc 0 | Treble Fc 1 | Treble Fc 2 | Treble Fc 3 |
|---|---|---|---|---|
| 32 kHz | 5.0 kHz | 7.0 kHz | 10.0 kHz | 15.0 kHz |
| 44.1 kHz | 4.8 kHz | 6.7 kHz | 9.6 kHz | 14.4 kHz |
| 48 kHz, 96 kHz | 5.2 kHz | 7.3 kHz | 10.4 kHz | 15.6 kHz |

**Table 3. Treble Shelving Filter Corner Frequencies**

The cut/boost level of the bass and treble shelving filters are set by the Bass[3:0] and Treble[3:0] bits in the Tone Control register.

| Referenced Control | Register Location |
|---|---|
| EnToneCtrl | “Tone Control Enable (EnToneCtrl)” on page 72 |
| TrebFc[1:0] | “Treble Corner Frequency (TrebFc[1:0])” on page 72 |
| BassFc[1:0] | “Bass Corner Frequency (BassFc[1:0])” on page 72 |
| Treble[3:0] | “Treble Gain Level (Treb[3:0])” on page 72 |
| Bass[3:0] | “Bass Gain Level (Bass[3:0])” on page 73 |

### 6.1.4.6 Parametric EQ

The CS4525 implements 5 fully programmable parametric EQ filters. Three of the filters are 2-channel filters dedicated to the channel A/B pair, and the remaining two are single-channel filters dedicated to the LFE channel generated by the bass manager.

The filters are implemented in the bi-quad form shown below.

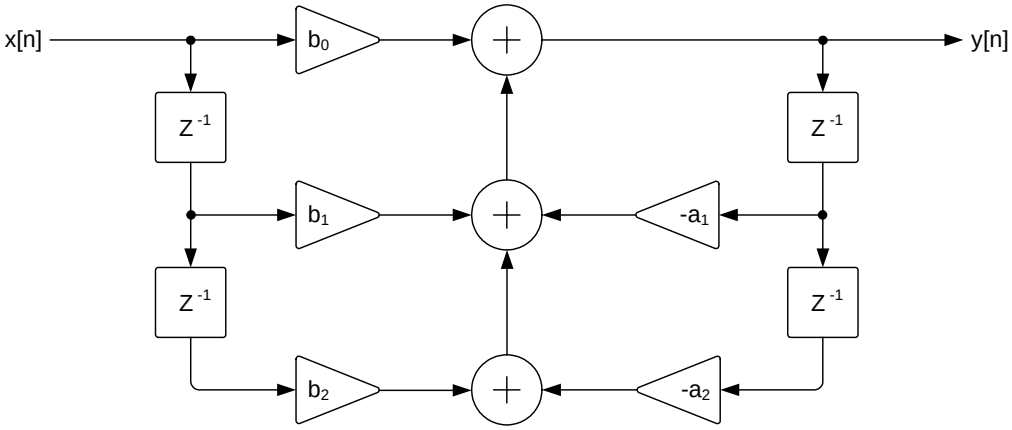



**Figure 16. Bi-Quad Filter Architecture**

This architecture is represented by the equation shown below where y[n] represents the output sample value and x[n] represents the input sample value.

$$y[n] = b_0x[n] + b_1x[n-1] + b_2x[n-2] - a_1x[n-1] - a_2x[n-2]$$

**Equation 1. Bi-Quad Filter Equation**

The coefficients are represented in binary form by 24-bit signed values stored in 3.21 two's complement format. The 3 MSB's represent the sign bit and the whole-number portion of the decimal coefficient, and the 21 LSB's represent the fractional portion of the decimal coefficient. The coefficient values must be in the range of -3.99996 decimal (80 00 00 hex) to 3.99996 decimal (7F FF FF hex).

The binary coefficient values are stored in registers 0Ah - 54h. Each 24-bit coefficient is split into 3 bytes, each of which is mapped to an individually accessible register location. See the "Register Quick Reference" section beginning on page 61 for the specific register locations for each coefficient.

By default, all $b_0$ coefficients are set to 1 decimal, and all other coefficients are set to 0 decimal. This implements a pass-through function.

Parametric equalizers 1, 2, and 3 can be independently enabled and disabled for channel A and B with the EnChAPEq and EnChBPEq bits located in the EQ Config register. The EnLFEPEq bit in the same register enables and disables parametric equalizers 4 and 5 for the LFE channel.

| Referenced Control | Register Location |
|---|---|
| EnChAPEq | "Enable Channel A Parametric EQ (EnChAPEq)" on page 74 |
| EnChBPEq | "Enable Channel B Parametric EQ (EnChBPEq)" on page 74 |
| EnLFEPEq | "Enable LFE Parametric EQ (EnLFEPEq)" on page 74 |

#### 6.1.4.7 Adaptive Loudness Compensation

The CS4525 includes adaptive loudness compensation to enhance the audibility of program material at low volume levels. The adaptive loudness compensation feature operates by varying the bass and treble boost of the tone control shelving filters as the volume level changes.

The level of boost added to the shelving filters is determined by the average of the effective volume settings of channels A and B after the master volume control. As this average volume setting decreases from 0 dB, the boost of the bass and treble shelving filters is gradually increased until it reaches the maximum boost level of 12.0 dB. As the volume is increased, the boost applied due to the adaptive loudness compensation feature will be gradually removed until it reaches the level specified by the Treble[3:0] and Bass[3:0] bits in the Tone Control register.

The adaptive loudness compensation feature is enabled by setting the Loudness bit in the Tone Config register. When the loudness feature is enabled, it immediately evaluates the effective average volume and applies bass and treble boost accordingly. When disabled, any treble or bass boost applied due to the loudness feature will be removed.

Because the adaptive loudness compensation filter operates by adjusting the boost level of the tone control shelving filters, it is necessary that they be enabled with the EnToneCtrl bit in the Tone Config register in order for the loudness feature to be operational. If the tone control filters are disabled, the adaptive loudness compensation feature will not be functional.

| Referenced Control | Register Location |
|---|---|
| Loudness | “Adaptive Loudness Compensation Control (Loudness)” on page 71 |
| EnToneCtrl | “Tone Control Enable (EnToneCtrl)” on page 72 |
| TrebFc[1:0] | “Treble Corner Frequency (TrebFc[1:0])” on page 72 |
| BassFc[1:0] | “Bass Corner Frequency (BassFc[1:0])” on page 72 |
| Treble[3:0] | “Treble Gain Level (Treb[3:0])” on page 72 |
| Bass[3:0] | “Bass Gain Level (Bass[3:0])” on page 73 |

### 6.1.4.8 Bass Management

The CS4525 implements a dedicated stereo 24 dB/octave Linkwitz-Riley crossover with adjustable cross-over frequency to achieve bass management for 2.1 configurations. The filter's stereo high-pass outputs are used to drive the full-range speakers, and its stereo low-pass outputs are each attenuated by 6 dB and summed to drive the LFE channel.

The bass management crossover is implemented with one of two preset internal filter sets. One set is optimized for a 32 kHz sample rate, and the other is optimized for 44.1 kHz, 48 kHz, and 96 kHz sample rates. The CS4525 automatically detects the input sample rate and chooses the appropriate filter set to apply. The available bass management cross-over frequencies are shown in Table 4 below and are configured with the BassMgr[2:0] bits in the EQ Config register.

Note that the corner frequency of each filter set scales linearly with the input sample rate.

When the internal ADC is used as the serial audio data source, the input sample rate is nominally 48 kHz and the corresponding shelving frequency corners are available.

| | Input Sample Rate | | |
|---|---|---|---|
| | **32 kHz** | **44.1 kHz** | **48 kHz, 96 kHz** |
| **Bass Manager Freq 1** | 80 Hz | 77 Hz | 83 Hz |
| **Bass Manager Freq 2** | 120 Hz | 115 Hz | 125 Hz |
| **Bass Manager Freq 3** | 160 Hz | 153 Hz | 167 Hz |
| **Bass Manager Freq 4** | 200 Hz | 192 Hz | 209 Hz |
| **Bass Manager Freq 5** | 240 Hz | 230 Hz | 250 Hz |
| **Bass Manager Freq 6** | 280 Hz | 268 Hz | 292 Hz |
| **Bass Manager Freq 7** | 320 Hz | 307 Hz | 334 Hz |

**Table 4. Bass Management Cross-Over Frequencies**

The BassMgr[2:0] bits also allow the bass manager to be disabled. When disabled, the bass management crossover is bypassed and no signal is presented on the LFE channel.

To allow full-range headphone operation, when the HP_DETECT/MUTE pin is configured for headphone detection (the HP/Mute bit is set), the operation of the bass manager is affected by the active state of the headphone detection input signal. In this configuration, when the bass manager is enabled, (BassMgr[2:0] bits not equal to '000') and the headphone detection input signal becomes active, the bass manager will be automatically disabled. When the headphone detection input signal becomes inactive, the bass manager will be automatically reconfigured to operate as dictated by the BassMgr[2:0] bits.

| Referenced Control | Register Location |
|---|---|
| BassMgr[2:0] | "Bass Cross-Over Frequency (BassMgr[2:0])" on page 73 |
| HP/Mute | "HP_Detect/Mute Pin Mode (HP/Mute)" on page 65 |

#### 6.1.4.9 Volume and Muting Control

The CS4525's volume control architecture provides the ability to control the level of each output channel on both an individual and master basis.

Individual control allows the volume and mute state of a single channel to be changed independently from the other channels within the device. The CS4525 provides 3 individual volume and muting controls, each permanently assigned to one channel within the device.

Each channel has a corresponding Ch X Vol register used to gain or attenuate the channel from +24 dB to -103 dB in 0.5 dB steps. Each output can be independently muted via the MuteChX bits in the Mute Control register.

Master control allows the volume of all channels to be changed simultaneously by offsetting each channel's individual volume setting by +24 dB to -103 dB in 0.5 dB steps. Master volume control is accomplished via the Master Vol register.

The PWM outputs can be configured to output silence as a modulated signal or an exact 50% duty cycle signal during a mute condition. This selection is achieved via the Mute50/50 bit in the Volume Cfg register.

The AutoMute bit in the same register dictates whether the device will automatically mute after the reception of 8192 consecutive samples of static 0 or -1. When the AutoMute function is enabled, a single sample of non-static data will cause the automatic mute to be released.

The CS4525 implements soft-ramp and zero-crossing detection capabilities to provide noise-free level transitions. When the zero-crossing function is enabled, all volume and muting changes are made on an output signal zero-crossing. The zero-crossing detection function is implemented independently for each channel. When the soft-ramp function is enabled, the volume is ramped from its initial to its final level at a rate of ½ dB every 4 samples for 32, 44.1, and 48 kHz sample rates, and ½ dB every 8 samples for a 96 kHz sampling rate.

All volume and muting changes are implemented as dictated by the soft-ramp and zero-cross settings configured by the SZCMode[1:0] bits in the Volume Cfg register.

| Referenced Control | Register Location |
|---|---|
| Ch X Vol | "Channel 1, 2, & 3 Volume Control (Address 58h, 59h, & 5Ah)" on page 78 |
| Master Vol | "Master Volume Control (Address 57h)" on page 77 |
| Mute50/50 | "Enable 50% Duty Cycle for Mute Condition (Mute50/50)" on page 75 |
| AutoMute | "Auto-Mute (AutoMute)" on page 75 |
| SZCMode | "Soft Ramp and Zero Cross Control (SZCMode[1:0])" on page 75 |

### *6.1.4.10 Peak Signal Limiter*

When enabled, the limiter monitors the digital output following the volume control block, detects when peak levels exceed a selectable maximum threshold level and lowers the volume at a programmable attack rate until the signal peaks fall below the maximum threshold. When the signal level falls below a selectable minimum threshold, the volume returns to its original level (as determined by the individual and master volume control registers) at a programmable release rate. Attack and release rates are affected by the soft ramp/zero cross settings and sample rate, Fs.

*Recommended settings*: Best limiting performance may be realized with the fastest attack and slowest release setting with soft ramp enabled in the control registers. Use the “minimum” bits to set a threshold slightly below the maximum threshold to cushion the sound as the limiter attacks and releases.

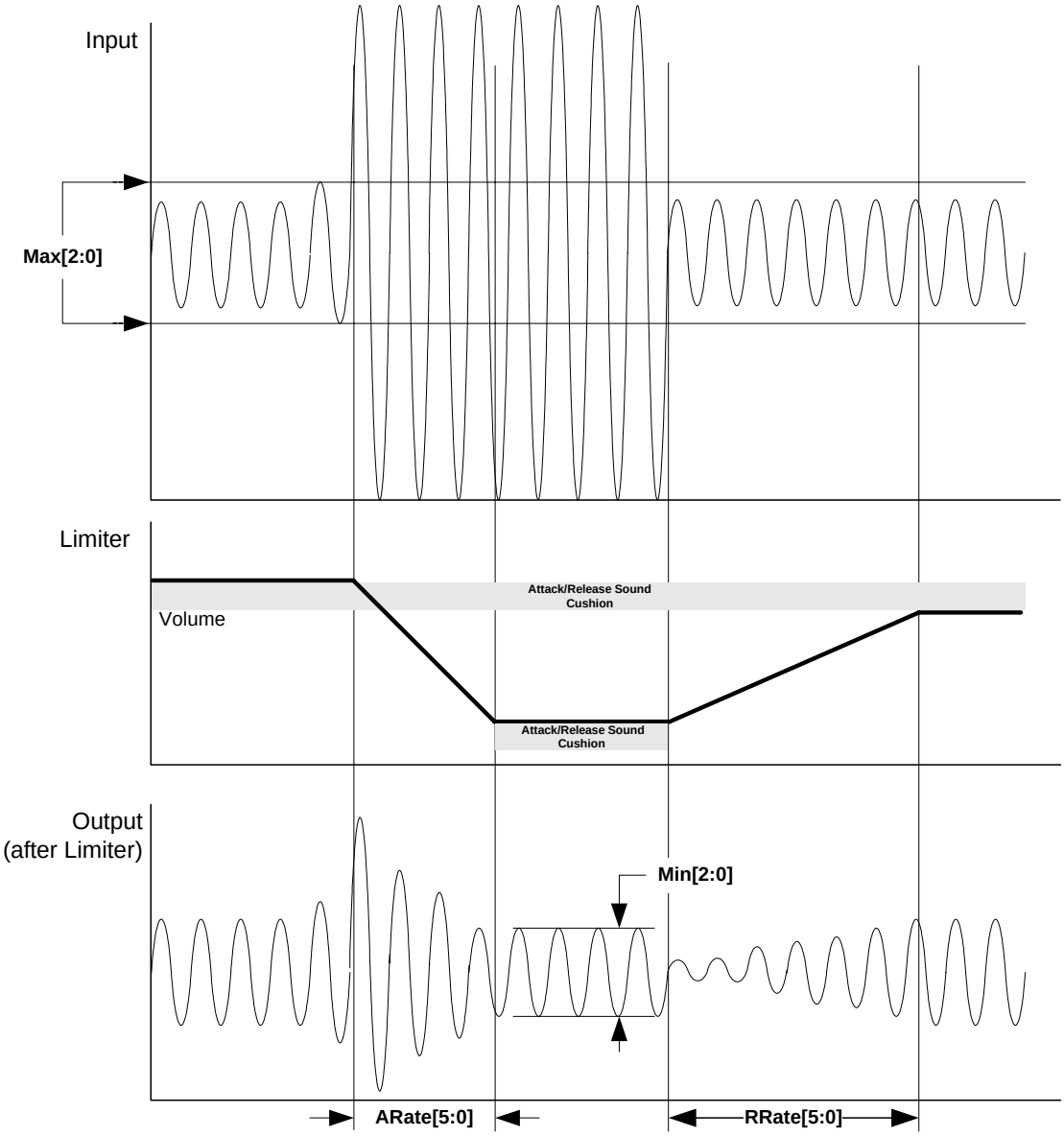



**Figure 17. Peak Signal Detection & Limiting**

By default, the limiter affects all channels when the maximum threshold is exceeded on any single channel. This default functionality is designed to keep all output channels at the same volume level while the limiter is in use. This behavior can be disabled by clearing the LimitAll bit in the Limiter Cfg 1 register.

When the LimitAll feature is activated, attenuation will be applied to all channels when a single channel exceeds the maximum threshold and released when the level of all channels is below the minimum threshold. When the LimitAll feature is de-activated, limiter attenuation will be applied and released on a per-channel basis and will only affect the channel on which the limiter event occurred.

The limiter can be enabled by setting the EnLimiter bit in the Limiter Cfg register.

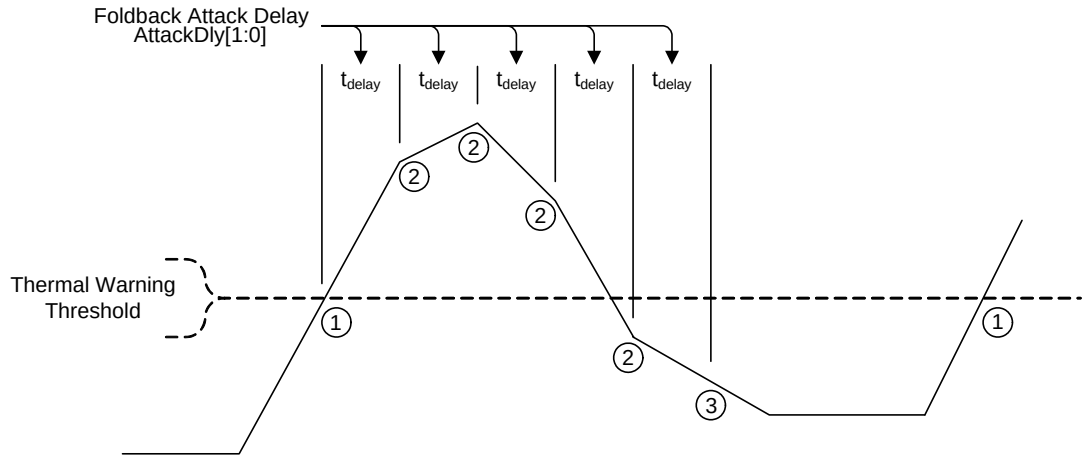
| Referenced Control | Register Location |
|---|---|
| EnLimiter | “Peak Detect and Limiter Enable (EnLimiter)” on page 80 |
| LimitAll | “Peak Signal Limit All Channels (LimitAll)” on page 79 |
| Max[2:0] | “Maximum Threshold (Max[2:0])” on page 79 |
| Min[2:0] | “Minimum Threshold (Min[2:0])” on page 79 |
| ARate[5:0] | “Limiter Attack Rate (ARate[5:0])” on page 80 |
| RRate[5:0] | “Limiter Release Rate (RRate[5:0])” on page 80 |

#### 6.1.4.11 Thermal Foldback

The CS4525 implements comprehensive thermal foldback features to guard against damaging thermal overload conditions.

The thermal foldback algorithm begins limiting the volume of the digital audio input to the amplifier stage as the junction temperatures rise above the maximum safe operating range specified by the thermal warning trip point listed in the PWM Power Output Characteristics table on page 20. This effectively limits the output power capability of the device, thereby allowing the temperature to reduce to acceptable levels without fully interrupting operation. As the device cools, the applied attenuation is gradually released until a new thermal equilibrium is reached or all applied attenuation has been released thereby allowing the device to again achieve its full output power capability.

Attenuation applied due to thermal foldback reduces the audio output level in a linear manner. Figure 18 below demonstrates the foldback process.




1. When the junction temperature crosses the thermal warning threshold, the foldback attack delay timer is started.

2. When the foldback attack delay timer reaches $t_{delay}$ seconds, the junction temperature is checked. If the junction temperature is above the thermal warning threshold, the output volume level is lowered by 0.5 dB and the foldback attack timer is restarted.

   The junction temperature is checked after each foldback attack timer timeout, and if necessary, the output volume level is lowered accordingly.

   If the junction temperature is found to be below the thermal warning threshold, the foldback attack timer is restarted once again, but the output volume level is not altered. The foldback algorithm then proceeds to step 3.

3. The junction temperature is checked once again after the next foldback attack timer timeout. If it has remained below the thermal warning threshold since the last check, the device will begin to release any attenuation applied as a result of the foldback event. Setting the LockAdj bit will prevent the device from removing the applied attenuation when the thermal overload condition has cleared.

   If the junction temperature crosses the thermal warning threshold again, the foldback algorithm will once again enter step 1.

**Figure 18. Foldback Process**

The AttackDly[1:0] bits in the Foldback Cfg register allow the foldback attack delay timeout period to be adjusted from approximately 0.5 seconds to approximately 2.0 seconds. The maximum attenuation applied by the thermal foldback algorithm can be restricted to -30 dB by setting the EnFloor bit in the same register.

The foldback adjustment lock feature causes the attenuation applied by the foldback algorithm to be maintained after the foldback condition has subsided. The applied attenuation will continue to be applied until the master volume or all active channel volume controls are lowered below the foldback attenuation level, or until a subsequent foldback condition occurs causing the applied attenuation to be lowered further. If the foldback algorithm applies attenuation while this feature is enabled, when the feature is subsequently disabled, the applied attenuation will be gradually released as long as the temperature remains within the safe operating range. This foldback lock adjustment feature is enabled by the LockAdj bit in the Foldback Cfg register.

Thermal warnings will only affect the foldback algorithm and cause attenuation to be applied when enabled by the EnTherm bit in the Foldback Cfg register.

The CS4525 can be configured to accept an external thermal warning indicator input. When in this configuration, an active input signal indicates that a thermal warning threshold has been exceeded. If thermal foldback is enabled, the foldback algorithm will respond as described above making no distinction between an internal or external thermal warning condition. See “External Warning Input Port” on page 43 for more information.

| Referenced Control | Register Location |
|---|---|
| EnTherm | “Enable Thermal Foldback (EnTherm)” on page 69 |
| AttackDly[1:0] | “Foldback Attack Delay (AttackDly[1:0])” on page 69 |
| EnFloor | “Enable Foldback Floor (EnFloor)” on page 70 |
| LockAdj | “Lock Foldback Adjust (LockAdj)” on page 69 |

#### *6.1.4.12 2-Way Crossover & Sensitivity Control*

The CS4525 implements a dedicated stereo 24 dB/octave Linkwitz-Riley crossover filter with adjustable cross-over frequency and sensitivity control to facilitate 2-way speaker configurations. The filter's high-pass output can be used to drive the tweeter, and its low-pass output is used can be drive the mid-range/woofer. The sensitivity control is included to adjust the level of the high-pass and low-pass outputs to compensate for differences in the tweeter and mid-range/woofer sensitivity.

The two-way crossover is implemented with one of two preset internal filter sets. One set is optimized for a 32 kHz sample rate, and the other is optimized for 44.1 kHz, 48 kHz, and 96 kHz sample rates. The CS4525 automatically detects the input sample rate and chooses the appropriate filter set to apply. The available cross-over frequencies are shown in Table 5 below and are configured with the 2WayFreq[2:0] bits in the Volume Cfg register.

Note that the corner frequency of each filter set scales linearly with the input sample rate.

When the internal ADC is used as the serial audio data source, the input sample rate is nominally 48 kHz and the corresponding shelving frequency corners are available.

| | Input Sample Rate | | |
|---|---|---|---|
| | **32 kHz** | **44.1 kHz** | **48 kHz, 96 kHz** |
| **X-Over Freq 0** | 2.0 kHz | 1.92 kHz | 2.09 kHz |
| **X-Over Freq 1** | 2.2 kHz | 2.11 kHz | 2.30 kHz |
| **X-Over Freq 2** | 2.4 kHz | 2.30 kHz | 2.50 kHz |
| **X-Over Freq 3** | 2.6 kHz | 2.49 kHz | 2.71 kHz |
| **X-Over Freq 4** | 2.8 kHz | 2.68 kHz | 2.92 kHz |
| **X-Over Freq 5** | 3.0 kHz | 2.88 kHz | 3.13 kHz |
| **X-Over Freq 6** | 3.2 kHz | 3.07 kHz | 3.34 kHz |
| **X-Over Freq 7** | 3.4 kHz | 3.26 kHz | 3.55 kHz |

**Table 5. 2-Way Cross-Over Frequencies**

The sensitivity level of the high- and low-pass outputs of the crossovers can be independently adjusted from 0 dB to -7.5 dB in 0.5 dB increments. The maximum attenuation level of -7.5 dB will compensate for an approximate 4 dB difference in sound pressure level (SPL) between the tweeter and the mid-range/woofer drivers. The sensitivity is adjusted using the HighPass[3:0] and LowPass[3:0] bits in the Sensitivity register. Note that these bits affect the sensitivity of both channel 1 and channel 2 low- and high-pass outputs.

The 2-way crossover can be enabled by setting the En2Way bit in the Volume Cfg register.

| Referenced Control | Register Location |
|---|---|
| En2Way | "Enable 2-Way Crossover (En2Way)" on page 76 |
| 2WayFreq[2:0] | "2-Way Cross-Over Frequency (2WayFreq[2:0])" on page 76 |
| HighPass[3:0] | "Channel 1 and Channel 2 High-Pass Sensitivity Adjust (HighPass[3:0])" on page 77 |
| LowPass[3:0] | "Channel 1 and Channel 2 Low-Pass Sensitivity Adjust (LowPass[3:0])" on page 76 |

### 6.1.5 Auxiliary Serial Output

The CS4525 includes a stereo auxiliary serial output which allows an external device to leverage on its internal signal processing and routing capabilities. The auxiliary serial output can receive its data from any of the sources shown in the Digital Signal Flow diagram on page 29.

The supported output data routing configurations are shown in Table 6 below. By default, the serial port is configured to output channels 1 and 2 on the auxiliary output data channels 1 and 2 respectively.

| LChDSel[1:0] | Aux Left Channel Data |
|---|---|
| 00 | Channel A |
| 01 | Channel B |
| 10 | LFE Channel |
| 11 | Channel B X-Over HPF |

| RChDSel[1:0] | Aux Right Channel Data |
|---|---|
| 00 | Channel A |
| 01 | Channel B |
| 10 | LFE Channel |
| 11 | Channel B X-Over LPF |

**Table 6. Auxiliary Serial Port Data Output**

The data output on each channel is set by the LChDSel[1:0] and RChDSel[1:0] bits in the Aux Port Configuration register. The auxiliary port can be enabled using the EnAuxPort bit in the same register. When enabled, the port operates as a master and clocks out data in the format dictated by the AuxI²S/LJ bits. When disabled, the AUX_LRCK, AUX_SCLK, and AUX_SDOUT pins continuously drive a logic '0'.

| Referenced Control | Register Location |
|---|---|
| EnAuxPort | "Enable Aux Serial Port (EnAuxPort)" on page 67 |
| LChDSel[1:0] | "Aux Serial Port Left Channel Data Select (LChDSel[1:0])" on page 68 |
| RChDSel[1:0] | "Aux Serial Port Right Channel Data Select (RChDSel[1:0])" on page 67 |
| AuxI²S/LJ | "Aux/Delay Serial Port Digital Interface Format (AuxI²S/LJ)" on page 67 |

### 6.1.6 Serial Audio Delay & Warning Input Port

The CS4525 includes a configurable delay and warning port to allow easy system integration of external lip-sync delay devices or warning inputs from external amplifiers. The port can be configured as a serial audio delay interface, an external warning input port, or disabled by the DlyPortCfg[1:0] bits in the Aux Config register. When disabled, the DLY_SDOUT and DLY_SDIN/EX_TWR pins become high-impedance.

| Referenced Control | Register Location |
|---|---|
| DlyPortCfg | "Delay & Warning Port Configuration (DlyPortCfg[1:0])" on page 67 |

#### 6.1.6.1 Serial Audio Delay Interface

Video processing and reproduction circuitry in digital video display devices can often introduce noticeably more delay than is introduced by the device's audio processing and reproduction circuitry. This can result in a phenomenon known as lip-synch delay - a delay present between the video and audio content being reproduced.

To help overcome this problem, the CS4525 delay and warning port can be configured as serial audio delay interface. This interface consists of a serial audio input/output port to facilitate the use of an external serial audio delay device. The port routes the serial data from the selected input source (the ADC or the serial input port) out to an external serial audio delay device, and then back in to the CS4525 internal digital sound processing blocks. The delay serial audio interface signals include DLY_SDOUT and DLY_SDIN/EX_TWR and are clocked from AUX_LRCK and AUX_SCLK. The serial data is output on the DLY_SDOUT pin and input on the DLY_SDIN/EX_TWR in the format specified by the AuxI²S/LJ bits in

the Aux Config register. Because the delay interface uses the auxiliary port clock signals, the auxiliary serial port must be enabled using the EnAuxPort bit in the Aux Port Configuration register to allow the delay interface to operate properly.

| Referenced Control | Register Location |
|---|---|
| AuxI²S/LJ | "Aux/Delay Serial Port Digital Interface Format (AuxI²S/LJ)" on page 67 |
| EnAuxPort | "Enable Aux Serial Port (EnAuxPort)" on page 67 |

#### 6.1.6.2 External Warning Input Port

When implementing external PWM power stage devices with thermal warning indicator outputs, it can be useful to provide these warning signals as in input to the internal thermal foldback algorithm. This allows the CS4525 to automatically respond to the external devices' thermal warning conditions without completely disrupting the system's operation.

When configured as an external warning input port, the DLY_SDIN/$\overline{\text{EX_TWR}}$ is an active-low thermal warning input to the foldback algorithm and the DLY_SDOUT pin becomes high-impedance.

In order for the foldback algorithm to act on the external thermal warning input signal, the thermal foldback algorithm must be enabled by the EnTherm bit in the Foldback Cfg register. See "Thermal Foldback" on page 39 for more information.

| Referenced Control | Register Location |
|---|---|
| EnTherm | "Enable Thermal Foldback (EnTherm)" on page 69 |

### 6.1.7 PWM Output Configuration

The CS4525 supports flexible PWM output configurations to enable a wide variety of system implementations. The 3 internal modulators can be used to generate multiple power output configurations and a number of independently selected logic-level PWM output channel combinations. PWM PopGuard is available for pop-free power up in half-bridge configurations, and PWM signal delays may be inserted to manage system switching noise.

#### 6.1.7.1 PWM Power Output Configurations

Three PWM power output configurations are supported as shown in Table 7 below. The configurations support stereo full-bridge, stereo half-bridge with full-bridge LFE, and mono parallel full-bridge output.

| OutputCfg[1:0] | Power Configuration | Output Signal | Output Pin(s) |
|---|---|---|---|
| 00 | 2 Ch. Full-Bridge | Channel 1 +<br>Channel 1 -<br>Channel 2 +<br>Channel 2 - | OUT1<br>OUT2<br>OUT3<br>OUT4 |
| 01 | 2 Ch. Half-Bridge<br>+<br>1 Ch. Full-Bridge | Channel 1 +<br>Channel 2 +<br>Channel 3 +<br>Channel 3 - | OUT1<br>OUT2<br>OUT3<br>OUT4 |
| 10 | 1 Ch. Parallel Full-Bridge | Channel 1 +<br>Channel 1 - | OUT1, OUT2<br>OUT3, OUT4 |

**Table 7. PWM Power Output Configurations**

The configurations are selected by the OutputCfg[1:0] bits in the Output Cfg register and must only be changed when the device is in power-down mode (the PDnAll bit is set). Any attempt to write the OutputCfg[1:0] bits while the device is powered-up will be ignored.

It should be noted that signal on channels 1, 2, and 3 is dependent upon the digital sound processing blocks being used. For instance, if the 2-way crossover is enabled, channel 1 and 2 contain the 2-way crossover channel A high- and low-pass outputs respectively. For more information, see the Digital Sound Processing section and Figure 14 on page 29.

| Referenced Control | Register Location |
|---|---|
| OutputCfg[1:0] | "Output Configuration (OutputCfg[1:0])" on page 68 |
| PDnAll | "Power Down (PDnAll)" on page 81 |

### 6.1.7.2 PWM_SIG Logic-Level Output Configurations

Four channel mapping output configurations are supported for the PWM_SIG output pins as shown in Table 8 below. The configurations support stereo, channel 1 with LFE, and channel 2 with LFE. When disabled, the PWM_SIG pins continuously drive a logic '0'. The configurations are selected by the PWMDSel[1:0] bits in the Output Cfg register

| PWMDSel[1:0] | PWM_SIG1 | PWM_SIG2 |
|---|---|---|
| 00 | Output disabled. | Output disabled. |
| 01 | Channel 1 | Channel 2 |
| 10 | Channel 1 | Channel 3 |
| 11 | Channel 2 | Channel 3 |

**Table 8. PWM Logic-Level Output Configurations**

To allow stereo headphone operation when the PWM logic-level outputs are mapped in a non-stereo output configuration, if the HP_DETECT/MUTE pin is configured for headphone detection (the HP/Mute bit is set), the PWM logic-level output mapping is affected by the active state of the headphone detection input signal. In this configuration, the PWM_SIG1 and PWM_SIG2 output pins will output audio from channel 1 and channel 2 respectively regardless of the setting of the PWMDSel[1:0] bits when the headphone detection input is active. When the headphone detection input signal becomes inactive, the PWM logic-level outputs will be automatically reconfigured to the channel mapping dictated by the PWMDSel[1:0] bits. See the Headphone Detection & Hardware Mute Input section on page 47 for more information.

It should be noted that signal on channels 1, 2, and 3 is dependent upon the digital sound processing blocks being used. For instance, if the 2-way crossover is enabled, channel 1 and 2 contain the 2-way crossover channel A high- and low-pass outputs respectively. For more information, see the Digital Sound Processing section and Figure 14 on page 29.

| Referenced Control | Register Location |
|---|---|
| PWMDSel[1:0] | "PWM Signals Output Data Select (PWMDSel[1:0])" on page 68 |
| HP/Mute | "HP_Detect/Mute Pin Mode (HP/Mute)" on page 65 |
| PDnAll | "Power Down (PDnAll)" on page 81 |

#### 6.1.7.3 PWM PopGuard Transient Control

The CS4525 uses PopGuard technology to minimize the effects of power-up and power-down output transients commonly produced by half-bridge, single supply amplifiers implemented with external DC-blocking capacitors connected in series with the audio outputs.

PWM PopGuard operates by linearly ramping the PWM power outputs up to and down from their bias point of VP/2 when a channel is powered up and down respectively using the PDnOutX or PDnAll bits. This gradual voltage ramp minimizes output transients while the DC blocking capacitor is charged and discharged.

The PWM PopGuard output ramp time can be varied from approximately 0.70 seconds to approximately 0.85 seconds and can be completely disabled via the RmpSpeed[1:0] bits in the Foldback Cfg register. All output channels are affected by the RmpSpeed[1:0] bits, and PWM PopGuard is disabled by default.

| Referenced Control | Register Location |
|---|---|
| RmpSpeed[1:0] | “Ramp Speed (RmpSpd[1:0])” on page 70 |
| PDnAll | “Power Down (PDnAll)” on page 81 |
| PDnOutX | “Power Down PWM Power Output X (PDnOutX)” on page 81 |

#### 6.1.7.4 PWM Channel Delay

The CS4525 includes a PWM output signal delay mechanism. This mechanism allows the PWM switching edges to be offset between channels as a method of managing switching noise and reducing radiated emissions.

The OutputDly[3:0] bits in the Output Cfg register are used to adjust the channel delay amount from 0 to 15 SYS_CLK or crystal input clock cycles, whichever is used as the input clock source. The absolute delay time is calculated by multiplying the setting of the OutputDly[3:0] bits by the period of the input clock source. By default, no delay is inserted.

When the power outputs are configured for 2-channel full-bridge operation, the OUT3/OUT4 signal pair is delayed from the OUT1/OUT2 signal pair by the delay amount as shown in Figure 19 below.

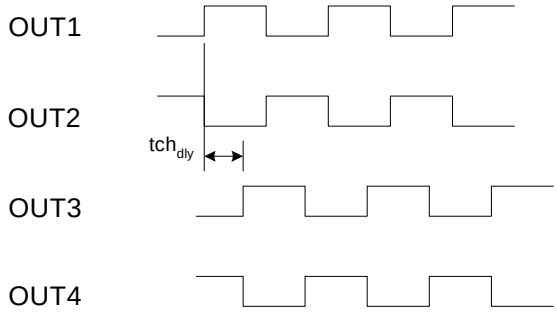



**Figure 19. 2-Channel Full-Bridge PWM Output Delay**

When the power outputs are configured for 3-channel (2-channel half-bridge and 1-channel full-bridge) operation, OUT2 is delayed from OUT1 by the delay amount, and the OUT3/OUT4 pair is delayed from OUT2 by the delay amount as shown in Figure 20 below.

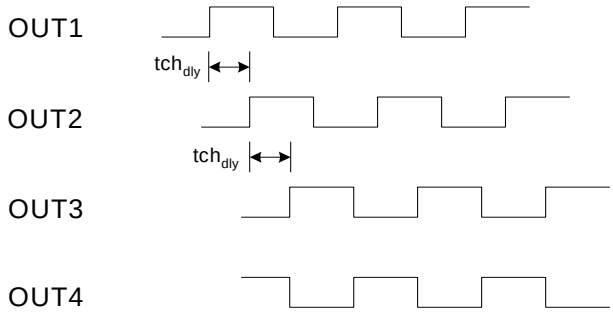



**Figure 20. 3-Channel PWM Output Delay**

The OutputDly[3:0] bits can only be changed when all modulators and associated logic are in the power-down state by setting the PDnAll bit. Attempts to write these bits while the PDnAll bit is cleared will be ignored.

| Referenced Control | Register Location |
|---|---|
| OutputDly[3:0] | "Channel Delay Settings (OutputDly[3:0])" on page 68 |

#### 6.1.7.5 PWM AM Frequency Shift

When using a PWM amplifier in a system containing an AM tuner, it is possible that the PWM switch rate conflicts with the desired tuning frequency of the AM tuner. To overcome this effect, the CS4525 includes PWM switch rate shift feature.

The feature adjusts the PWM switching frequency and quantization levels to remove interference when the desired tuning frequency of an AM tuner is positioned near the PWM switching rate. This feature is enabled by setting the FreqShift bit in the Clock Config register. When this feature is enabled, the output switch rate is lowered and the quantization levels are increased as shown in Table 9 below.

| Supplied XTAL or SYS_CLK Frequency | PWM Switch Rate | Quantization Levels |
|---|---|---|
| 18.432 MHz | 329.143 kHz | 56 |
| 24.576 MHz | 341.300 kHz | 72 |
| 27.000 MHz | 375 kHz | 72 |

**Table 9. PWM Output Switching Rates and Quantization Levels**

The nominal PWM switching frequencies and quantization levels are discussed in "PWM Modulators and Sample Rate Converters" on page 53.

| Referenced Control | Register Location |
|---|---|
| FreqShift | "AM Frequency Shifting (FreqShift)" on page 65 |

### 6.1.8 Headphone Detection & Hardware Mute Input

The CS4525 includes a configurable HP_DETECT/MUTE input pin which can be used as a hardware mute input or a headphone detection input. The function of this pin is set by the HP/Mute bit in the Clock Config register.

When configured as a mute input pin, all PWM modulators and the AUX_SDOUT signal will be placed in a mute state when the pin is active.

When configured as a headphone detect input pin and the HP_DETECT/MUTE input is active, the PWM_SIG1 and PWM_SIG2 output pins will output audio from channel 1 and channel 2 respectively regardless of the setting of the PWMDSel[1:0] bits; see "PWM_SIG Logic-Level Output Configurations" on page 44 for more information. The OUT1 - OUT4 PWM driver outputs will mute by outputting a non-modulated 50% duty cycle signal. If the Ch1Mix[1:0] bits are configured for a mono mix on channel 1, the mix will be disabled and channel 1 will be output on PWM_SIG1 while the headphone detect input signal is active; see "Channel Mixer" on page 30 for more information. If the bass manager is enabled, it will be automatically disabled while the headphone detect input signal is active; see "Bass Management" on page 35 for more information.

When configured as a headphone detect input pin and the input is inactive, the OUT1 - OUT4 driver outputs will output audio according to the channel mixer and bass manager registers settings, and the PWM_SIG output pins will mute by outputting a non-modulated 50% duty cycle.

In both configurations, the active logic input level is determined by the HP/MutePol bit.

| Referenced Control | Register Location |
|---|---|
| HP/$\overline{\text{Mute}}$ | "HP_Detect/Mute Pin Mode (HP/Mute)" on page 65 |
| HP/MutePol | "HP_Detect/Mute Pin Active Logic Level (HP/MutePol)" on page 65 |
| PWMDSel[1:0] | "PWM Signals Output Data Select (PWMDSel[1:0])" on page 68 |

### 6.1.9 Interrupt Reporting

The CS4525 has comprehensive interrupt reporting capabilities. Many conditions including SRC lock, ADC overflow, digital data path overflow, and amplifier errors can cause an interrupt.

The $\overline{\text{INT}}$ output pin is intended to drive an interrupt input pin on a host microcontroller. The $\overline{\text{INT}}$ pin is an open-drain active-low output and requires an external pull-up for proper operation.

If an interrupt source is un-masked, its occurrence will cause the interrupt output pin to become active. To enhance flexibility, each interrupt source may be masked such that its occurrence does not cause the interrupt output pin to become active. This masking function is accomplished by clearing an interrupt's respective mask bit located in the 4 LSB's of the Interrupt register.

When a specific interrupt condition occurs, it's respective bit located in the 4 MSB's of the Interrupt register will be set to indicate that a change has occurred for the associated interrupt type. When the interrupt register is read, the contents of the 4 MSB's will be cleared. The Int Status register may then be read to determine the current state of the interrupt source.

For specific information regarding interrupt types and reporting, see the Interrupt, Int Status and Amp Error register descriptions.

| Referenced Control | Register Location |
|---|---|
| Interrupt Register | "Interrupt Register (Address 60h)" on page 82 |
| Int Status Register | "Interrupt Status Register (Address 61h) - Read Only" on page 84 |
| Amp Error Register | "Amplifier Error Status (Address 62h) - Read Only" on page 85 |

### 6.1.10 Automatic Power Stage Shut-Down

To prevent permanent damage, the CS4525 will automatically shut down its internal PWM power output stages when a thermal error, PWM power output over-current error, or VP under-voltage condition occurs. In the shut-down state, all digital functions of the device will operate as normal, however the PWM power output pins become high-impedance.

The levels of the over-current error, thermal error, and VP under-voltage trip points are listed in the PWM Power Output Characteristics table on page 20. Automatic shut-down will occur whenever any of these preset thresholds are crossed.

Once in the shut-down state, the PDnAll bit in the Power Ctrl register must be set and then cleared to resume normal device operation.

| Referenced Control | Register Location |
|---|---|
| PDnAll | "Power Down (PDnAll)" on page 81 |

## 6.2 Hardware Mode

A limited feature set is available when the CS4525 powers up in hardware mode. The available features are described in the following sections. All device configuration is achieved via hardware control input pins.

### *6.2.1 System Clocking*

In hardware mode, the CS4525 must be clocked by a stable external clock source input on the SYS_CLK pin. This input clock is used to synchronize the input serial audio signals with the internal clock domain and to clock the internal digital processing, sample-rate converter, and PWM modulators. It is also used to determine the sample rate of the serial audio input signals in order to automatically configure the various internal filter coefficients.

To ensure proper operation, the CS4525 must be informed of the nominal frequency of the supplied SYS_CLK signal via the ClkFreq[1:0] hardware control pins. These pins must be set to the appropriate level before the $\overline{\text{RST}}$ signal is released to initiate a power-up sequence. The nominal clock frequencies indicated by the states of the ClkFreq[1:0] pins are shown in Table 10 below. See the SYS_CLK Switching Specifications table on page 23 for complete input frequency range specifications.

| ClkFreq1 | ClkFreq0 | Nominal SYS_CLK Frequency |
|---|---|---|
| Low | Low | 18.432 MHz |
| Low | High | 24.576 MHz |
| High | Low | 27.000 MHz |
| High | High | Reserved |

**Table 10. SYS_CLOCK Frequency Selection**

Figure 12 below demonstrates a typical clocking configuration using the SYS_CLK input.

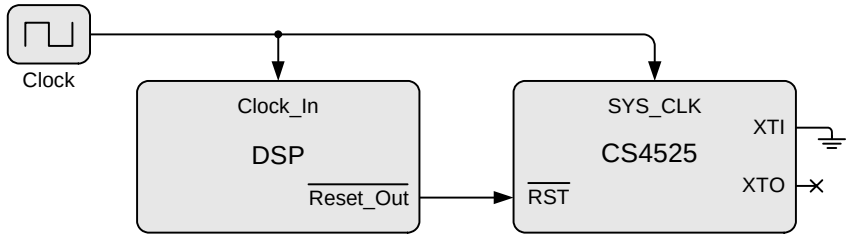



**Figure 21. Typical SYS_CLK Input Clocking Configuration**

### *6.2.2 Power-Up and Power-Down*

The CS4525 will remain in a completely powered-down state until the $\overline{\text{RST}}$ pin is brought high.

#### *6.2.2.1 Recommended Power-Up Sequence*

1. Hold $\overline{\text{RST}}$ low until the power supplies and the input SYS_CLK signal are stable.
2. Bring $\overline{\text{RST}}$ high.
   *Hardware mode will be entered after approximately 10 ms.*

#### *6.2.2.2 Recommended Power-Down Sequence*

1. Bring $\overline{\text{MUTE}}$ low to mute the device's outputs and minimize audible pops.
2. Bring $\overline{\text{RST}}$ low to halt the operation of the device.
   *The device's power consumption will be brought to an absolute minimum.*
3. Remove power.

### 6.2.3 Input Source Selection

The CS4525 can accept analog or digital audio input signals. Digital audio input signals are supplied through the serial audio input port as outlined in "Serial Audio Interfaces" on page 57. Analog audio input signals are supplied through the internal ADC as outlined in "Analog Inputs" on page 56. The input source is selected by the ADC/$\overline{SP}$ pin as shown in Table 11 below and can be changed at any time without causing any audible pops or clicks.

| ADC/$\overline{SP}$ | Selected Input Source |
|---|---|
| Low | Digital Audio Inputs (Serial Port) |
| High | Analog Audio Inputs (ADC) |

**Table 11. Input Source Selection**

In hardware mode, the serial audio input port supports both I²S and left-justified formats. The serial audio interface format is selected by the I2S/$\overline{LJ}$ pin as shown in Table 12 below.

| I2S/$\overline{LJ}$ | Selected Serial Audio Interface Format |
|---|---|
| Low | Left-Justified |
| High | I²S |

**Table 12. Serial Audio Interface Format Selection**

### 6.2.4 PWM Channel Delay

In hardware mode, the CS4525 offsets the PWM switching edges between channels as a method of managing switching noise and reducing radiated emissions.

The OUT3/OUT4 signal pair is delayed from the OUT1/OUT2 signal pair by 4 SYS_CLK cycles as shown in Figure 22 below. The absolute delay time is calculated by multiplying the period SYS_CLK by 4.

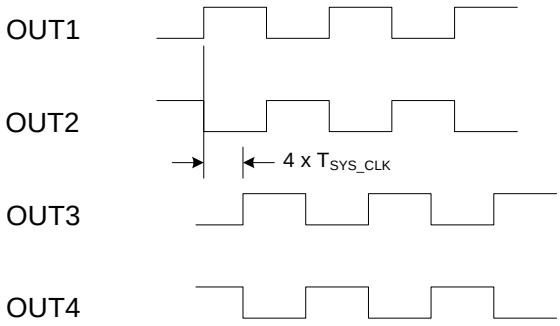



**Figure 22. Hardware Mode PWM Output Delay**

### 6.2.5 Digital Signal Flow

In hardware mode, the CS4525 operates as a 2-channel full-bridge PWM amplifier with analog or digital inputs. To protect against over-temperature conditions, thermal foldback is included for the internal power stages.

The digital signal flow is shown in Figure 14 below.

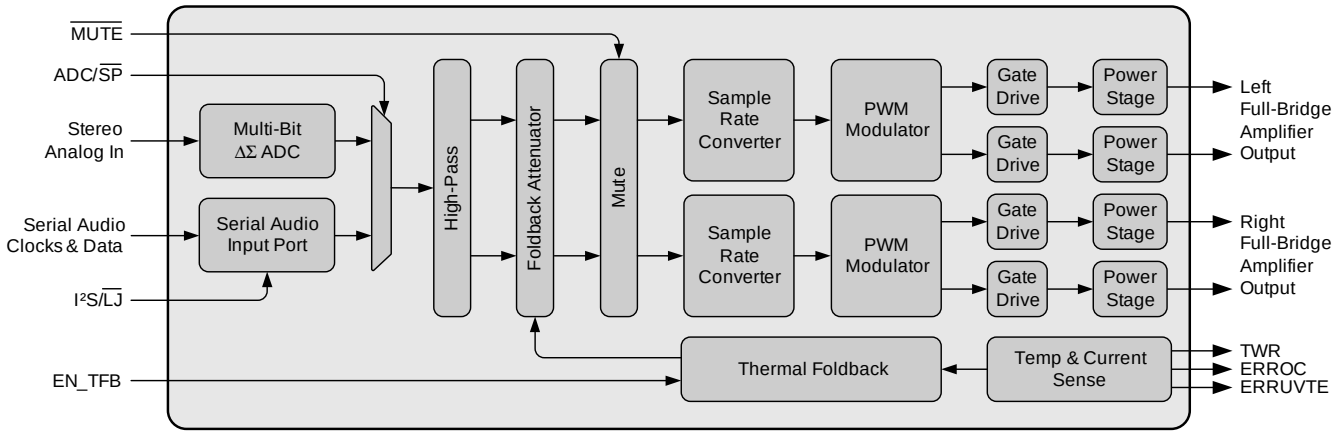



**Figure 23. Hardware Mode Digital Signal Flow**

#### 6.2.5.1 High-Pass Filter

The CS4525 includes a high-pass filter at the beginning of the digital signal processing chain to remove any DC content from the input signal prior to the remaining internal digital signal processing blocks. The high-pass filter operates by continuously subtracting a measure of the DC offset from the input signal; it is always enabled.

#### 6.2.5.2 Mute Control

The CS4525 includes a dedicated $\overline{\text{MUTE}}$ input pin. When low, the PWM outputs will output silence as an exact non-modulated 50% duty cycle signal. When high, the selected input source will be presented at the amplifier outputs.

It should be noted that the auto-mute, soft-ramp, and zero-crossing detection features available in software mode are disabled in hardware mode.

#### 6.2.5.3 Warning and Error Reporting

The CS4525 is capable of reporting various error and warning conditions on its $\overline{\text{TWR}}$, $\overline{\text{ERROC}}$, and $\overline{\text{ERRUVTE}}$ pins.

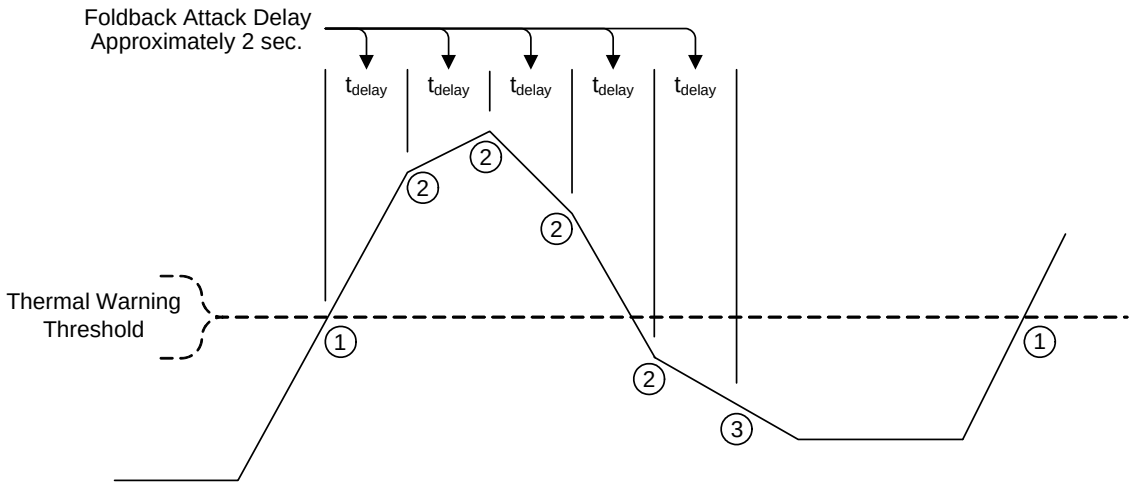
- The $\overline{\text{TWR}}$ pin indicates the presence of a thermal warning condition. When active concurrently with the $\overline{\text{ERRUVTE}}$ pin, indicates a thermal error condition.
- The $\overline{\text{ERROC}}$ pin indicates the presence of an over-current condition on one or both of the output channels.
- The $\overline{\text{ERRUVTE}}$ pin indicates the presence of a VP undervoltage or thermal error condition.

The trip point for each warning and error condition is defined in the PWM Power Output Characteristics table on page 20. Each pin implements an active-low open-drain driver and requires an external pull-up for proper operation.

### 6.2.6 Thermal Foldback

In hardware mode, the CS4525 implements a thermal foldback feature to guard against damaging thermal overload conditions. The thermal foldback feature begins limiting the volume of the digital audio input to the amplifier stage as the junction temperatures rise above the maximum safe operating range specified by the thermal warning trip point listed in the PWM Power Output Characteristics table on page 20. This effectively limits the output power capability of the device, thereby allowing the temperature to reduce to acceptable levels without fully interrupting operation. As the device cools, the applied attenuation is gradually released until a new thermal equilibrium is reached or all applied attenuation has been released thereby allowing the device to again achieve its full output power capability.

Attenuation applied due to thermal foldback reduces the audio output level in a linear manner. Figure 18 below demonstrates the foldback process.




(1) When the junction temperature crosses the thermal warning threshold, the foldback attack delay timer is started.

(2) When the foldback attack delay timer reaches $t_{delay}$ seconds, the junction temperature is checked. If it is above the thermal warning threshold, the output volume level is lowered by 0.5 dB and the foldback attack timer is restarted.

The junction temperature is checked after each foldback attack timer timeout, and if necessary, the output volume level is lowered accordingly.

If the junction temperature is found to be below the thermal warning threshold, the foldback attack timer is restarted once again, but the output volume level is not altered. The foldback algorithm then proceeds to step 3.

(3) The junction temperature is checked once again after the next foldback attack timer timeout. If is has remained below the thermal warning threshold since the last check, the device will begin to release any attenuation applied as a result of the foldback event.

If the junction temperature crosses the thermal warning threshold again, the foldback algorithm will once again enter step 1.

**Figure 24. Foldback Process**

Thermal warning conditions will only affect the foldback algorithm and cause attenuation to be applied if enabled by the EN_TFB pin as shown in Table 13 below.

| EN_TFB | Selected Thermal Foldback Enable State |
|---|---|
| Low | Thermal foldback disabled. |
| High | Thermal foldback enabled. |

**Table 13. Thermal Foldback Enable Selection**

### 6.2.7 Automatic Power Stage Shut-Down

To protect itself from permanent damage, the CS4525 will automatically shut down its internal PWM power output stages when a thermal error, PWM power output over-current error, or VP under-voltage condition occurs. In the shut-down state, all digital functions of the device will operate as normal, however the PWM power output pins become high-impedance.

The levels of the over-current error, thermal error, and VP under-voltage trip points are listed in the PWM Power Output Characteristics table on page 20. Automatic shut-down will occur whenever any of these preset thresholds are crossed.

Once in the shut-down state, the $\overline{\text{RST}}$ signal must be toggled low and then high to resume normal device operation.

## 6.3 PWM Modulators and Sample Rate Converters

The CS4525 includes 3 pairs of PWM modulators and sample rate converters, each clocked from the external crystal or system clock applied at power-up. All 3 modulator and sample rate converter pairs are available in software mode (see Figure 14 on page 29), and 2 pairs are used in hardware mode (see Figure 23 on page 51).

One of the characteristics of a PWM modulator is that the frequency content of the out-of-band noise generated is dependent on the PWM switching frequency. As the power stage external LC and snubber filter component values are used to attenuate this out-of band energy, their component values are also based on this switching frequency.

To easily accommodate input sample rates ranging from 32 kHz to 96 kHz without requiring the adjustment of output filter component values, the CS4525 utilizes a sample rate converter (SRC) to keep the PWM switching frequency fixed regardless of the input sample rate. The SRC operates by upsampling the variable input sample rate to a fixed output switching rate, typically 384 kHz for most audio applications. Table 14 below shows the PWM output switching rate and quantization levels as a function of the supplied external crystal or system clock.

Additionally, as the output of the SRC is clocked from a very stable crystal or oscillator, the SRC also allows the PWM modulator output to be independent of the input serial audio clock jitter. This results in very low jitter PWM output and higher dynamic range.

| Supplied XTAL or SYS_CLK Frequency | PWM Switch Rate | Quantization Levels |
|---|---|---|
| 18.432 MHz | 384 kHz | 48 |
| 24.576 MHz | 384 kHz | 64 |
| 27.000 MHz | 421.875 kHz | 64 |

**Table 14. PWM Output Switching Rates and Quantization Levels**

## 6.4 Output Filters

The filter placed after the PWM outputs can greatly affect the output performance. The filter not only reduces radiated EMI (snubber filter), but also filters high frequency content from the switching output before going to the speaker (low-pass LC filter).

### *6.4.1 Half-Bridge Output Filter*

Figure 25 shows the output filter for a half-bridge configuration. The transient-voltage suppression circuit (snubber circuit) is comprised of a resistor (20 Ω, ¼ W) and capacitors (220 pF) and should be placed as close as possible to the corresponding PWM output pin to greatly reduce radiated EMI.

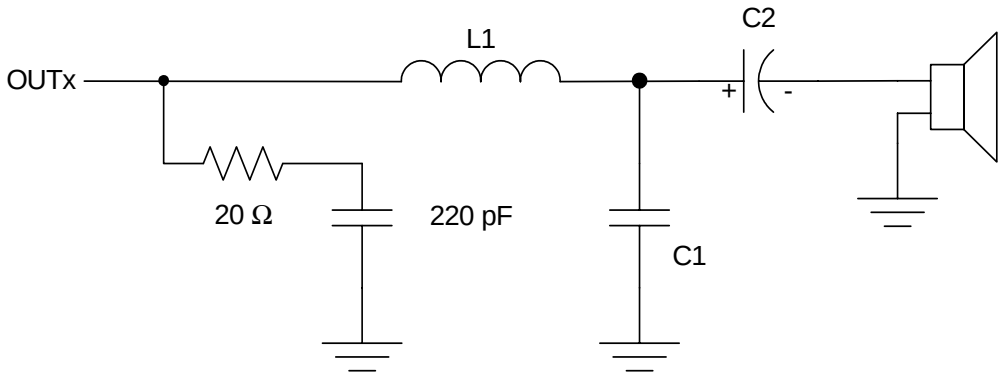



**Figure 25. Output Filter - Half-Bridge**

The inductor, L1, and capacitor, C1, comprise the low-pass filter. Along with the nominal load impedance of the speaker, these values set the cutoff frequency of the filter. Table 15 shows the component values for L1 and C1 based on nominal speaker (load) impedance for a corner frequency (-3 dB point) of approximately 35 kHz.

| Load | L1 | C1 |
|---|---|---|
| 4 Ω | 22 µH | 1.0 µF |
| 6 Ω | 33 µH | 0.68 µF |
| 8 Ω | 47 µH | 0.47 µF |

**Table 15. Low-Pass Filter Components - Half-Bridge**

C2 is the DC-blocking capacitor. Table 16 shows the component values for C2 based on corner frequency (-3 dB point) and a nominal speaker (load) impedances of 4 Ω, 6 Ω, and 8 Ω. This capacitor should also be chosen to have a ripple current rating above the amount of current that will passed through it.

| Load | Corner Frequency | C2 |
|---|---|---|
| 4 Ω | 40 Hz | 1000 µF |
| | 58 Hz | 680 µF |
| | 120 Hz | 330 µF |
| 6 Ω | 39 Hz | 680 µF |
| | 68 Hz | 390 µF |
| | 120 Hz | 220 µF |
| 8 Ω | 42 Hz | 470 µF |
| | 60 Hz | 330 µF |
| | 110 Hz | 180 µF |

**Table 16. DC-Blocking Capacitors Values - Half-Bridge**

### 6.4.2 Full-Bridge Output Filter (Stereo or Parallel)

Figure 26 shows the output filter for a full-bridge configuration. The transient-voltage suppression circuit (snubber circuit) is comprised of a resistor (20 Ω) and capacitor (330 pF) and should be placed as close as possible to the corresponding PWM output pins to greatly reduce radiated EMI. The inductors, L1, and capacitor, C1, comprise the low-pass filter. Along with the nominal load impedance of the speaker, these values set the cutoff frequency of the filter. Table 17 shows the component values based on nominal speaker (load) impedance for a corner frequency (-3 dB point) of approximately 35 kHz.

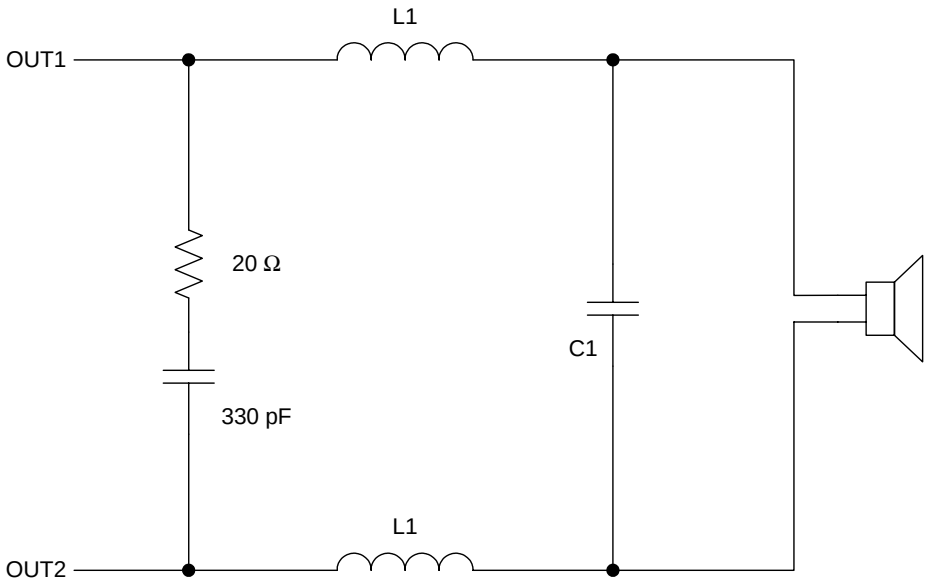



**Figure 26. Output Filter - Full-Bridge**

| Load | L1 | C1 |
|---|---|---|
| 4 Ω | 10 µH | 1.0 µF |
| 6 Ω | 15 µH | 0.47 µF |
| 8 Ω | 22 µH | 0.47 µF |

**Table 17. Low-Pass Filter Components - Full-Bridge**

## 6.5 Analog Inputs

Very few components are required to interface between the audio source and the CS4525's analog inputs, AINL and AINR. A single order passive low-pass filter is recommended to prevent high-frequency content from aliasing into the audio band due to the analog-to-digital conversion process. Also, a DC-blocking capacitor is required as the CS4525's analog inputs are internally biased to VQ.

The recommended analog input circuit is shown in Figure 27 below will accommodate full-scale input voltages as defined in the Analog Input Characteristics table on page 19. This circuit provides the necessary high-frequency filtering with a first-order passive low-pass filter that has less than 0.05 dB of attenuation at 24 kHz. It also includes a DC blocking capacitor to accommodate the analog input pins' bias level.

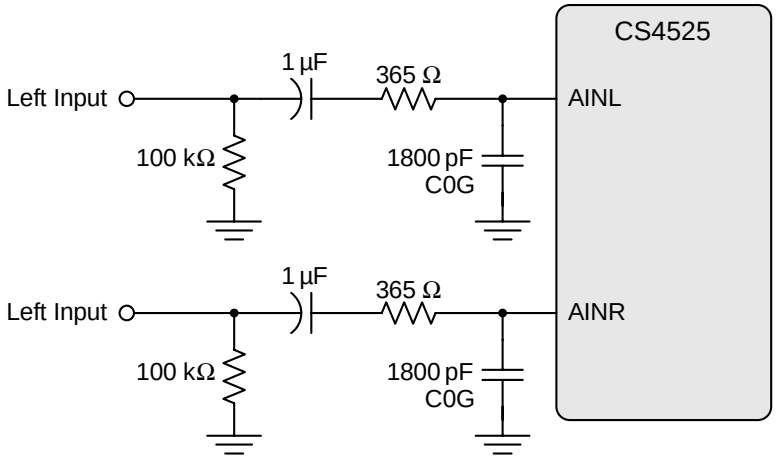



**Figure 27. Recommended Unity Gain Input Filter**

To interface 2 $V_{RMS}$ input signals with the CS4525's analog inputs, an external resistor divider is required. Figure 28 shows the recommended input circuit for 2 $V_{RMS}$ inputs. It includes a -10.5 dB passive attenuator to condition the input signal for the CS4525's full-scale input voltage, a first-order passive low-pass filter that has less than 0.05 dB of attenuation at 24 kHz, and a DC blocking capacitor to accommodate for the analog input pins' bias level. The passive attenuator network should be placed as close as possible to the CS4525's analog input pins to reduce the potential for noise and signal coupling into the analog input traces.

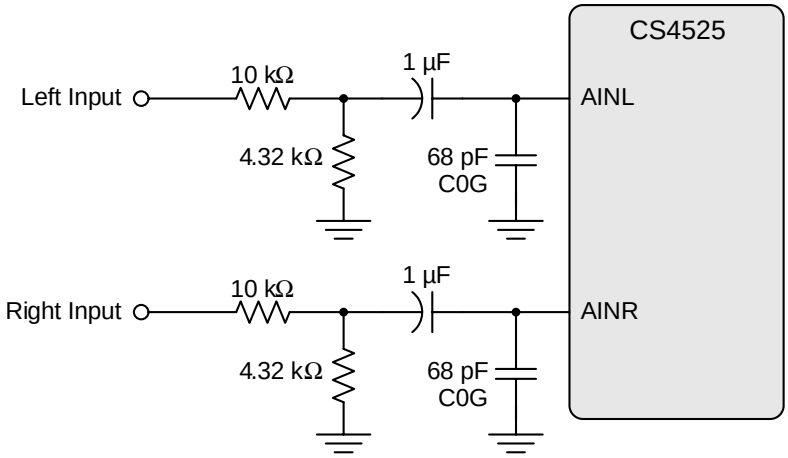



**Figure 28. Recommended 2 $V_{RMS}$ Input Filter**

It should be noted that the external DC blocking capacitor forms a high-pass filter with the CS4525's input impedance. Both filters shown above have less than 0.2 dB attenuation at 20 Hz due to this effect. Increasing the value of this capacitor will lower this high-pass corner frequency, and decreasing it's value will increase the corner frequency.

## 6.6 Serial Audio Interfaces

The CS4525 interfaces to external digital audio devices via the serial audio input port and the auxiliary/delay serial ports.

The serial audio input port provides support for I²S, Left-Justified and Right-Justified data formats and operates in slave mode only, with LRCK and SCLK as inputs. The input LRCK signal must be equal to the sample rate, Fs and must be synchronous to the serial bit clock, SCLK, which is used to sample the data bits.

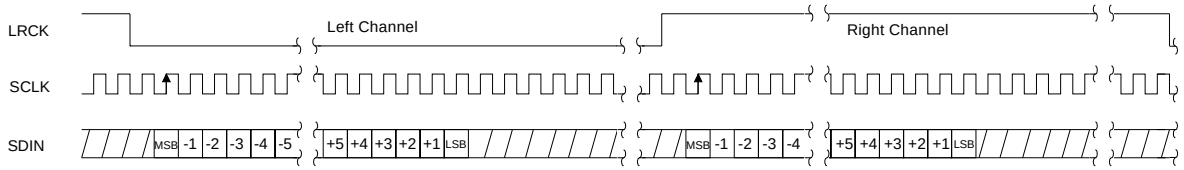
The auxiliary/delay serial port (available in software mode only) supports I²S and Left-Justified data formats and operates in master mode, with AUX_LRCK and AUX_SCLK as outputs.

Each of the supported formats is described in detail in sections 6.6.1 - 6.6.3 below.

For additional information, application note AN282 presents a tutorial of the 2-channel serial audio interface. AN282 can be downloaded from the Cirrus Logic web site at http://www.cirrus.com.

### *6.6.1 I²S Data Format*

In I²S format, data is received most significant bit first one SCLK delay after the transition of LRCK and is valid on the rising edge of SCLK. The left channel data is presented when LRCK is low; the right channel data is presented when LRCK is high.

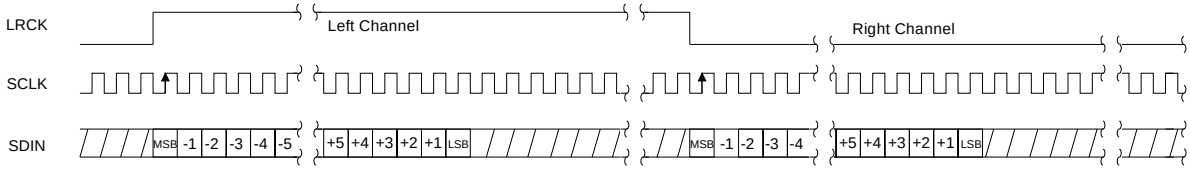



| I²S Mode, Data Valid on Rising Edge of SCLK | |
|---|---|
| Bits/Sample | SCLK Rates |
| 16 | 32, 48, 64, 128 Fs |
| 18 to 24 | 48, 64, 128 Fs |

**Figure 29. I²S Serial Audio Formats**

### *6.6.2 Left-Justified Data Format*

In Left-Justified format, data is received most significant bit first on the first SCLK after a LRCK transition and is valid on the rising edge of SCLK. The left channel data is presented when LRCK is high and the right channel data is presented when LRCK is low.

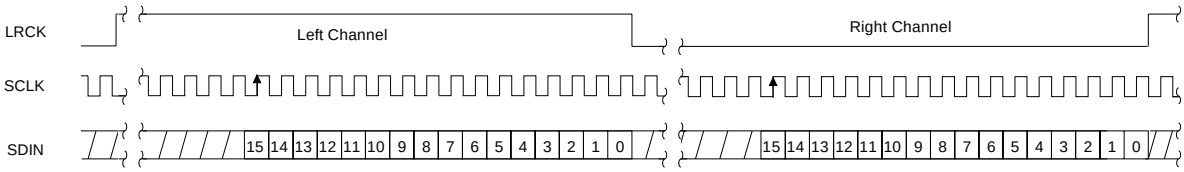



| Left-Justified Mode, Data Valid on Rising Edge of SCLK | |
|---|---|
| Bits/Sample | SCLK Rate(s) |
| 16 | 32, 48, 64, 128 Fs |
| 18 to 24 | 48, 64, 128 Fs |

**Figure 30. Left-Justified Serial Audio Formats**

### 6.6.3 Right-Justified Data Format

In Right-Justified format, data is received most significant bit first and with the least significant bit presented on the last SCLK before the LRCK transition and is valid on the rising edge of SCLK. For the Right-Justified format, the left channel data is presented when LRCK is high and the right channel data is presented when LRCK is low. Either 16 bits per sample or 24 bits per sample are supported.




| Right-Justified Mode, Data Valid on Rising Edge of SCLK | |
|---|---|
| Bits/Sample | Supported SCLK Rate(s) |
| 16 | 32, 48, 64, 128 Fs |
| 24 | 48, 64, 128 Fs |

**Figure 31. Right-Justified Serial Audio Formats**

## 6.7 I²C Control Port Description and Timing

The control port is used to access the registers allowing the CS4525 to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to the audio sample serial port. However, to avoid potential interference problems, the control port pins should remain static if no operation is required. The control port operates in I²C Mode, with the CS4525 acting as a slave device.

SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL. A 47 kΩ pull-up or pull-down on the AUX_LRCK/AD0 pin will set AD0, the least significant bit of the chip address. A pull-up to VD will set AD0 to '1' and a pull-down to DGND will set AD0 to '0'. The state of AUX_LRCK/AD0 is sensed, and AD0 is set upon the release of $\overline{\text{RESET}}$.

The signal timings for a read and write cycle are shown in Figure 32 and Figure 25. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS4525 after a Start condition consists of a 7 bit chip address field and a R/$\overline{\text{W}}$ bit (high for a read, low for a write). The upper 6 bits of the 7-bit address field are fixed at 100101. To communicate with a CS4525, the chip address field, which is the first byte sent to the CS4525, should match 100101 followed by the setting of AD0. The eighth bit of the address is the R/$\overline{\text{W}}$ bit. If the operation is a write, the next byte is the memory address pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS4525 after each input byte is read, and is input to the CS4525 from the microcontroller after each transmitted byte.

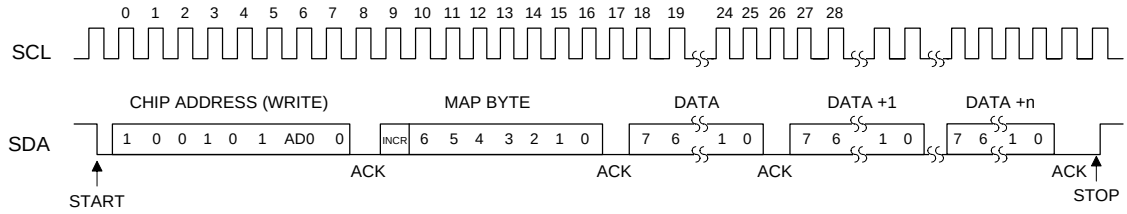



**Figure 32. Control Port Timing, I²C Write**

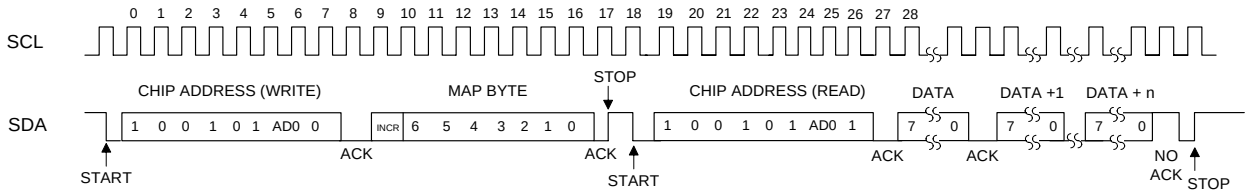



**Figure 33. Control Port Timing, I²C Read**

Since the read operation can not set the MAP, an aborted write operation is used as a preamble. As shown in Figure 25, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

Send start condition.
Send 100101x0 (chip address & write operation).
Receive acknowledge bit.
Send MAP byte, auto increment off.
Receive acknowledge bit.
Send stop condition, aborting write.
Send start condition.
Send 100101x1(chip address & read operation).

Receive acknowledge bit.

Receive byte, contents of selected register.

Send acknowledge bit.

Send stop condition.

Setting the auto increment bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

# 7. PCB LAYOUT CONSIDERATIONS

## 7.1 Power Supply, Grounding

As with any high-resolution converter, the CS4525 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized.

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. Decoupling capacitors should be as close to the pins of the CS4525 as possible. The lowest value ceramic capacitor should be closest to the pin and should be mounted on the same side of the board as the CS4525 to minimize inductance effects. All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+ and VQ decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from FILT+ and AGND. The CRD4525 reference design demonstrates the optimum layout and power supply arrangements.

### *7.1.1 Integrated VD Regulator*

The CS4525 includes two internal linear regulators, one from the VD supply voltage to provide a fixed 2.5 - V supply to its internal digital blocks, and another from the VD supply voltage to provide a fixed 2.5 - V supply to its internal analog blocks. The LVD pin must be set to indicate the voltage present on the VD pin as shown in Table 18 below.

| LVD | Indicated VD Supply Level |
|---|---|
| Low | 2.5 V or 3.3 V Nominal |
| High | 5 V Nominal |

**Table 18. Input Source Selection**

The output of the digital regulator is presented on the VD_REG pin and may be used to provide an external device with up to 3 mA of current at its nominal output voltage of 2.5 - V. The output of the analog regulator is presented on the VA_REG pin and must only be connected to the bypass capacitors as shown in the typical connection diagrams.

If a nominal supply voltage of 2.5 V is used as the VD supply (see the Specified Operating Conditions table on page 18), the VD, VD_REG, and VA_REG pins must all be connected to the VD supply source. In this configuration, the internal regulators are bypassed and the external supply source is used to directly drive the internal digital and analog sections.

## 7.2 QFN Thermal Pad

The CS4525 is available in a compact QFN package. The underside of the QFN package reveals a large metal pad that serves as a thermal relief to provide for maximum heat dissipation. This pad must mate with an equally dimensioned copper pad on the PCB and must be electrically connected to ground. A series of thermal vias should be used to connect this copper pad to one or more larger ground planes on other PCB layers. The CRD4525 reference design demonstrates the optimum thermal pad and via configuration.

# 8. REGISTER QUICK REFERENCE

This table shows the register names and their associated default values.

| Adr | Name | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| 01h | Clock Config page 64 | EnSysClk 1 | DivSysClk 0 | ClkFreq1 0 | ClkFreq0 1 | HP/MutePol 0 | HP/$\overline{\text{Mute}}$ 0 | PhaseShift 0 | FreqShift 0 |
| 02h | Input Config page 66 | ADC/$\overline{\text{SP}}$ 0 | EnAnHPF 1 | Reserved 0 | SPRate1 x | SPRate0 x | DIF2 0 | DIF1 0 | DIF0 0 |
| 03h | Aux Config page 67 | EnAuxPort 0 | DlyPortCfg1 0 | DlyPortCfg0 0 | AuxI²S/$\overline{\text{LJ}}$ 0 | RChDSel1 0 | RChDSel0 1 | LChDSel1 0 | LChDSel0 0 |
| 04h | Output Cfg page 68 | OutputCfg1 0 | OutputCfg0 0 | PWMDSel1 0 | PWMDSel0 0 | OutputDly3 0 | OutputDly2 0 | OutputDly1 0 | OutputDly0 0 |
| 05h | Foldback Cfg page 69 | Reserved 0 | EnTherm 0 | LockAdj 0 | AttackDly1 0 | AttackDly0 1 | EnFloor 0 | RmpSpd1 1 | RmpSpd0 1 |
| 06h | Mixer Config page 70 | PreScale2 0 | PreScale1 0 | PreScale0 0 | Reserved 0 | RChMix1 0 | RChMix0 0 | LChMix1 0 | LChMix0 0 |
| 07h | Tone Config page 71 | DeEmph 0 | Loudness 0 | EnDigHPF 0 | TrebFc1 0 | TrebFc0 0 | BassFc1 0 | BassFc0 1 | EnToneCtrl 0 |
| 08h | Tone Control page 72 | Treble3 1 | Treble2 0 | Treble1 0 | Treble0 0 | Bass3 1 | Bass2 0 | Bass1 0 | Bass0 0 |
| 09h | EQ Config page 73 | Freeze 0 | Reserved 0 | BassMgr2 0 | BassMgr1 0 | BassMgr0 0 | EnLFEPEq 0 | EnChBPEq 0 | EnChAPEq 0 |
| 0Ah | Channel 1&2 BiQuad 1 A1 Coeff | MSB | ..... | | | | | | MSB-7 |
| 0Bh | | MSB-8 | ..... | | | | | | LSB+8 |
| 0Ch | | LSB+7 | ..... | | | | | | LSB |
| 0Dh | Channel 1&2 BiQuad 1 A2 Coeff | MSB | ..... | | | | | | MSB-7 |
| 0Eh | | MSB-8 | ..... | | | | | | LSB+8 |
| 0Fh | | LSB+7 | ..... | | | | | | LSB |
| 10h | Channel 1&2 BiQuad 1 B0 Coeff | MSB | ..... | | | | | | MSB-7 |
| 11h | | MSB-8 | ..... | | | | | | LSB+8 |
| 12h | | LSB+7 | ..... | | | | | | LSB |
| 13h | Channel 1&2 BiQuad 1 B1 Coeff | MSB | ..... | | | | | | MSB-7 |
| 14h | | MSB-8 | ..... | | | | | | LSB+8 |
| 15h | | LSB+7 | ..... | | | | | | LSB |
| 16h | Channel 1&2 BiQuad 1 B2 Coeff | MSB | ..... | | | | | | MSB-7 |
| 17h | | MSB-8 | ..... | | | | | | LSB+8 |
| 18h | | LSB+7 | ..... | | | | | | LSB |
| 19h | Channel 1&2 BiQuad 2 A1 Coeff | MSB | ..... | | | | | | MSB-7 |
| 1Ah | | MSB-8 | ..... | | | | | | LSB+8 |
| 1Bh | | LSB+7 | ..... | | | | | | LSB |
| 1Ch | Channel 1&2 BiQuad 2 A2 Coeff | MSB | ..... | | | | | | MSB-7 |
| 1Dh | | MSB-8 | ..... | | | | | | LSB+8 |
| 1Eh | | LSB+7 | ..... | | | | | | LSB |
| 1Fh | Channel 1&2 BiQuad 2 B0 Coeff | MSB | ..... | | | | | | MSB-7 |
| 20h | | MSB-8 | ..... | | | | | | LSB+8 |
| 21h | | LSB+7 | ..... | | | | | | LSB |
| 22h | Channel 1&2 BiQuad 2 B1 Coeff | MSB | ..... | | | | | | MSB-7 |
| 23h | | MSB-8 | ..... | | | | | | LSB+8 |
| 24h | | LSB+7 | ..... | | | | | | LSB |

| Adr | Name | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| 25h | Channel 1&2 BiQuad 2 B2 Coeff | MSB | ..... | | | | | | MSB-7 |
| 26h | | MSB-8 | ..... | | | | | | LSB+8 |
| 27h | | LSB+7 | ..... | | | | | | LSB |
| 28h | Channel 1&2 BiQuad 3 A1 Coeff | MSB | ..... | | | | | | MSB-7 |
| 29h | | MSB-8 | ..... | | | | | | LSB+8 |
| 2Ah | | LSB+7 | ..... | | | | | | LSB |
| 2Bh | Channel 1&2 BiQuad 3 A2 Coeff | MSB | ..... | | | | | | MSB-7 |
| 2Ch | | MSB-8 | ..... | | | | | | LSB+8 |
| 2Dh | | LSB+7 | ..... | | | | | | LSB |
| 2Eh | Channel 1&2 BiQuad 3 B0 Coeff | MSB | ..... | | | | | | MSB-7 |
| 2Fh | | MSB-8 | ..... | | | | | | LSB+8 |
| 30h | | LSB+7 | ..... | | | | | | LSB |
| 31h | Channel 1&2 BiQuad 3 B1 Coeff | MSB | ..... | | | | | | MSB-7 |
| 32h | | MSB-8 | ..... | | | | | | LSB+8 |
| 33h | | LSB+7 | ..... | | | | | | LSB |
| 34h | Channel 1&2 BiQuad 3 B2 Coeff | MSB | ..... | | | | | | MSB-7 |
| 35h | | MSB-8 | ..... | | | | | | LSB+8 |
| 36h | | LSB+7 | ..... | | | | | | LSB |
| 37h | Channel 3 BiQuad 1 A1 Coeff | MSB | ..... | | | | | | MSB-7 |
| 38h | | MSB-8 | ..... | | | | | | LSB+8 |
| 39h | | LSB+7 | ..... | | | | | | LSB |
| 3Ah | Channel 3 BiQuad 1 A2 Coeff | MSB | ..... | | | | | | MSB-7 |
| 3Bh | | MSB-8 | ..... | | | | | | LSB+8 |
| 3Ch | | LSB+7 | ..... | | | | | | LSB |
| 3Dh | Channel 3 BiQuad 1 B0 Coeff | MSB | ..... | | | | | | MSB-7 |
| 3Eh | | MSB-8 | ..... | | | | | | LSB+8 |
| 3Fh | | LSB+7 | ..... | | | | | | LSB |
| 40h | Channel 3 BiQuad 1 B1 Coeff | MSB | ..... | | | | | | MSB-7 |
| 41h | | MSB-8 | ..... | | | | | | LSB+8 |
| 42h | | LSB+7 | ..... | | | | | | LSB |
| 43h | Channel 3 BiQuad 1 B2 Coeff | MSB | ..... | | | | | | MSB-7 |
| 44h | | MSB-8 | ..... | | | | | | LSB+8 |
| 45h | | LSB+7 | ..... | | | | | | LSB |
| 46h | Channel 3 BiQuad 2 A1 Coeff | MSB | ..... | | | | | | MSB-7 |
| 47h | | MSB-8 | ..... | | | | | | LSB+8 |
| 48h | | LSB+7 | ..... | | | | | | LSB |
| 49h | Channel 3 BiQuad 2 A2 Coeff | MSB | ..... | | | | | | MSB-7 |
| 4Ah | | MSB-8 | ..... | | | | | | LSB+8 |
| 4Bh | | LSB+7 | ..... | | | | | | LSB |
| 4Ch | Channel 3 BiQuad 2 B0 Coeff | MSB | ..... | | | | | | MSB-7 |
| 4Dh | | MSB-8 | ..... | | | | | | LSB+8 |
| 4Eh | | LSB+7 | ..... | | | | | | LSB |
| 4Fh | Channel 3 BiQuad 2 B1 Coeff | MSB | ..... | | | | | | MSB-7 |
| 50h | | MSB-8 | ..... | | | | | | LSB+8 |
| 51h | | LSB+7 | ..... | | | | | | LSB |
| 52h | Channel 3 BiQuad 2 B2 Coeff | MSB | ..... | | | | | | MSB-7 |
| 53h | | MSB-8 | ..... | | | | | | LSB+8 |
| 54h | | LSB+7 | ..... | | | | | | LSB |

| Adr | Name | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| 55h | Volume Cfg | SZCMode1 | SZCMode0 | Mute50/50 | AutoMute | En2Way | 2WayFreq2 | 2WayFreq1 | 2WayFreq0 |
| | page 75 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 56h | Sensitivity | LowPass3 | LowPass2 | LowPass1 | LowPass0 | HighPass3 | HighPass2 | HighPass1 | HighPass0 |
| | page 76 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 57h | Master Vol | MVol7 | MVol6 | MVol5 | MVol4 | MVol3 | MVol2 | MVol1 | MVol0 |
| | page 77 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 58h | Ch 1 Vol | Ch1Vol7 | Ch1Vol6 | Ch1Vol5 | Ch1Vol4 | Ch1Vol3 | Ch1Vol2 | Ch1Vol1 | Ch1Vol0 |
| | page 78 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 59h | Ch 2 Vol | Ch2Vol7 | Ch2Vol6 | Ch2Vol5 | Ch2Vol4 | Ch2Vol3 | Ch2Vol2 | Ch2Vol1 | Ch2Vol0 |
| | page 78 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 5Ah | Ch 3 Vol | Ch3Vol7 | Ch3Vol6 | Ch3Vol5 | Ch3Vol4 | Ch3Vol3 | Ch3Vol2 | Ch3Vol1 | Ch3Vol0 |
| | page 78 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 5Bh | Mute Control | InvADC | InvCh3 | InvCh2 | InvCh1 | MuteADC | MuteCh3 | MuteCh2 | MuteCh1 |
| | page 78 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 5Ch | Limiter Cfg 1 | Max2 | Max1 | Max0 | Min2 | Min1 | Min0 | LimitAll | EnLimiter |
| | page 79 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 5Dh | Limiter Cfg 2 | Reserved | Reserved | RRate5 | RRate4 | RRate3 | RRate2 | RRate1 | RRate0 |
| | page 80 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 5Eh | Limiter Cfg 3 | Reserved | Reserved | ARate5 | ARate4 | ARate3 | ARate2 | ARate1 | ARate0 |
| | page 80 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 5Fh | Power Ctrl | Reserved | Reserved | SelectVD | PDnADC | PDnOut3/4 | PDnOut2 | PDnOut1 | PDnAll |
| | page 81 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 60h | Interrupt | SRCLock | ADCOvfl | ChOvfl | AmpErr | SRCLockM | ADCOvflM | ChOvflM | AmpErrM |
| | page 82 | x | x | x | x | 0 | 0 | 0 | 0 |
| 61h | Int Status | SRCLockSt | ADCOvflSt | Ch3OvflSt | Ch2OvflSt | Ch1OvflSt | RampDone | Reserved | Reserved |
| | page 84 | x | x | x | x | x | x | 0 | 0 |
| 62h | Amp Error | OverCurr4 | OverCurr3 | OverCurr2 | OverCurr1 | ExtAmpSt | UnderV | ThermErr | ThermWarn |
| | page 85 | x | x | x | x | x | x | x | x |
| 63h | Device ID | DeviceID4 | DeviceID3 | DeviceID2 | DeviceID1 | DeviceID0 | RevID2 | RevID1 | RevID0 |
| | page 87 | 1 | 1 | 0 | 0 | 0 | x | x | x |

# 9. REGISTER DESCRIPTIONS

All registers are read/write unless otherwise stated. All “Reserved” bits must maintain their default state.

## 9.1 Clock Configuration (Address 01h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EnSysClk | DivSysClk | ClkFreq1 | ClkFreq0 | HP/MutePol | HP/$\overline{\text{Mute}}$ | PhaseShift | FreqShift |

### 9.1.1 SYS_CLK Output Enable (EnSysClk)

*Default = 1*

*Function:*
This bit controls the output driver for the SYS_CLK signal. When cleared, the output driver is disabled and the SYS_CLK pin is high-impedance. When set, the output driver is enabled.

If the SYS_CLK output is unused, this bit should be set to ‘0’b to disable the driver.

| EnSysClk Setting | Output Driver State |
|---|---|
| 0 | Output driver disabled. |
| 1 | Output driver enabled. |

### 9.1.2 SYS_CLK Output Divider (DivSysClk)

*Default = 0*

*Function:*
This bit determines the divider for the XTAL clock signal for generating the SYS_CLK signal.

This divider is only available if the clock source is an external crystal attached to XTI/XTO and the SYS_CLK output is enabled.

| DivSysClk Setting | SYS_CLK Output Frequency |
|---|---|
| 0 | $F_{SYS_CLK} = F_{XTAL}$ |
| 1 | $F_{SYS_CLK} = F_{XTAL}/2$ |

### 9.1.3 Clock Frequency (ClkFreq[1:0])

*Default = 01*

*Function:*
These bits must be set to identify the nominal clock frequency of the crystal attached to the XTI/XTO pins or that of the input SYS_CLK signal. See the XTI Switching Specifications table on page 23 and the SYS_CLK Switching Specifications table on page 23 for complete input frequency range specifications.

| ClkFreq[1:0] Setting | Specified Nominal Input Clock Frequency |
|---|---|
| 00 | 18.432 MHz |
| 01 | 24.576 MHz |
| 10 | 27.000 MHz |
| 11 | Reserved |

### 9.1.4 HP_Detect/Mute Pin Active Logic Level (HP/MutePol)

*Default = 0*

*Function:*
This bit determines the active logic level for the HP_DETECT/MUTE input signal.

| HP/MutePol Setting | Headphone Detect/Mute Input Polarity |
|---|---|
| 0 | Active low. |
| 1 | Active high. |

### 9.1.5 HP_Detect/Mute Pin Mode (HP/$\overline{\text{Mute}}$)

*Default = 0*

*Function:*
Configures the function of HP_DETECT/MUTE input pin. See "Headphone Detection & Hardware Mute Input" on page 47 for more information.

| HP/Mute Setting | HP_DETECT/MUTE Pin Function |
|---|---|
| 0 | Mute input signal. |
| 1 | Headphone detect input signal. |

### 9.1.6 Modulator Phase Shifting (PhaseShift)

*Default = 0*

*Function:*
When enabled, forces the output of the PWM modulator to output differential signals which are the inverse of each other and have been phase shifted by 180 degrees. This causes, for instance, the differential signal pair to be exactly in phase with one another during a mute condition, thereby reducing the amount of switching current through the load.

| PhaseShift Setting | Modulator Phase Shift State |
|---|---|
| 0 | 180º phase shift disabled. |
| 1 | 180º phase shift enabled. |

### 9.1.7 AM Frequency Shifting (FreqShift)

*Default = 0*

*Function:*
Controls the state of the PWM AM frequency shift feature. See "PWM AM Frequency Shift" on page 47 for more information.

| FreqShift Setting | AM Frequency Shift State |
|---|---|
| 0 | Frequency shift disabled. |
| 1 | Frequency shift enabled. |

## 9.2 Input Configuration (Address 02h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADC/$\overline{SP}$ | EnAnHPF | Reserved | SPRate1 | SPRate0 | DIF2 | DIF1 | DIF0 |

### 9.2.1 Input Source Selection (ADC/$\overline{SP}$)

*Default = 0*

*Function:*
This bit selects the audio input source.

| ADC/SP Setting | Audio Input Source |
|---|---|
| 0 | Digital input from the serial audio input port. |
| 1 | Analog input from the internal ADC. |

### 9.2.2 ADC High-Pass Filter Enable (EnAnHPF)

*Default = 1*

*Function:*
Controls the operation of the ADC high-pass filter.

| EnAnHPF Setting | ADC High-Pass Filter State |
|---|---|
| 0 | ADC high-pass filter disabled. |
| 1 | ADC high-pass filter enabled. |

### 9.2.3 Serial Port Sample Rate (SPRate[1:0]) - Read Only

*Default = XX*

*Function:*
Identifies the sample rate of the incoming LRCK signal on the serial audio input port.

| SPRate[1:0] Setting | Identified Input Sample Rate |
|---|---|
| 00 | 32 kHz |
| 01 | 44.1 kHz |
| 10 | 48 kHz |
| 11 | 96 kHz |

### 9.2.4 Input Serial Port Digital Interface Format (DIF [2:0])

*Default = 000*

*Function:*
Selects the serial audio interface format used for the data in on SDIN. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in the section “Serial Audio Interfaces” on page 57.

| DIF[2:0] Setting | Input Serial Port Serial Audio Interface Format |
|---|---|
| 000 | Left-Justified, up to 24-bit data. |
| 001 | I²S, up to 24-bit data. |
| 010 | Right-Justified, 24-bit data. |
| 011 | Right-Justified, 20-bit data. |
| 100 | Right-Justified, 18-bit data. |
| 101 | Right-Justified, 16-bit data. |
| 110 | Reserved. |
| 111 | Reserved. |

## 9.3 AUX Port Configuration (Address 03h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EnAuxPort | DlyPortCfg1 | DlyPortCfg0 | AuxI²S/$\overline{LJ}$ | RChDSel1 | RChDSel0 | LChDSel1 | LChDSel0 |

### 9.3.1 Enable Aux Serial Port (EnAuxPort)

*Default = 0*

*Function:*
Controls the operation of the auxiliary serial port.

| EnAuxPort Setting | Auxiliary Port State |
|---|---|
| 0 | Auxiliary port disabled. |
| 1 | Auxiliary port enabled. |

### 9.3.2 Delay & Warning Port Configuration (DlyPortCfg[1:0])

*Default = 00*

*Function:*
Controls the operation of the delay and warning port. See "Serial Audio Delay & Warning Input Port" on page 42 for more information.

| DlyPortCfg[1:0] Setting | Delay Port Configuration |
|---|---|
| 00 | Port disabled. |
| 01 | Port configured as serial audio delay interface. |
| 10 | Port configured as an external thermal warning indicator for the foldback algorithm. |
| 11 | Port disabled. |

### 9.3.3 Aux/Delay Serial Port Digital Interface Format (AuxI²S/$\overline{LJ}$)

*Default = 0*

*Function:*
Selects the serial audio interface format for the data on AUX_SDOUT, DLY_SDIN, DLY_SDOUT. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in the "Serial Audio Interfaces" on page 57.

| AuxI²S/LJ Setting | Auxiliary/Delay Port Serial Audio Interface Format |
|---|---|
| 0 | Left-Justified, up to 24-bit. |
| 1 | I²S, up to 24-bit. |

### 9.3.4 Aux Serial Port Right Channel Data Select (RChDSel[1:0])

*Default = 01*

*Function:*
Selects the data to be sent over the right channel of the auxiliary port serial data output signal.

| RChDSel[1:0] Setting | Aux Serial Port Right Channel Output Data Source |
|---|---|
| 00 | Channel A. |
| 01 | Channel B. |
| 10 | LFE Channel. |
| 11 | Channel B crossover low-pass output. |

### 9.3.5 Aux Serial Port Left Channel Data Select (LChDSel[1:0])

*Default = 00*

*Function:*
Selects the data to be sent over the left channel of the auxiliary port serial data output signal.

| LChDSel[1:0] Setting | Aux Serial Port Left Channel Output Data Source |
|---|---|
| 00 | Channel A. |
| 01 | Channel B. |
| 10 | LFE Channel. |
| 11 | Channel B crossover high-pass output. |

## 9.4 Output Configuration Register (Address 04h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OutputCfg1 | OutputCfg0 | PWMDSel1 | PWMDSel0 | OutputDly3 | OutputDly2 | OutputDly1 | OutputDly0 |

### 9.4.1 Output Configuration (OutputCfg[1:0])

*Default = 00*

*Function:*
Identifies the power output configuration. This parameter can only be changed when all modulators and associated logic are in the power-down state (the PDnAll bit is set). Attempts to write this register while the PDnAll is cleared will be ignored. See "PWM Power Output Configurations" on page 43 for more information.

| OutputCfg[1:0] Setting | Power Output Configuration |
|---|---|
| 00 | Channel 1 & 2 Full-Bridge. |
| 01 | Channel 1 & 2 Half-Bridge + Channel 3 Full-Bridge. |
| 10 | Channel 1 Parallel Full-Bridge. |
| 11 | Reserved. |

### 9.4.2 PWM Signals Output Data Select (PWMDSel[1:0])

*Default = 00*

*Function:*
Selects the PWM data output on the PWM_SIG1 and PWM_SIG2 output signals.See "PWM_SIG Logic-Level Output Configurations" on page 44 for more information.

| PWMDSel Setting | PWM Signal Output Mapping |
|---|---|
| 00 | PWM_SIG1 output disabled.<br>PWM_SIG2 output disabled. |
| 01 | Channel 1 output on PWM_SIG1.<br>Channel 2 output on PWM_SIG2. |
| 10 | Channel 1 output on PWM_SIG1.<br>Channel 3 output on PWM_SIG2. |
| 11 | Channel 2 output on PWM_SIG1.<br>Channel 3 output on PWM_SIG2. |

### 9.4.3 Channel Delay Settings (OutputDly[3:0])

*Default = 0000*

*Function:*
The channel delay bits allow delay adjustment of each of the power output audio channels. The value of this register determines the amount of delay inserted in the output path. The delay time is calculated by multiplying the register value by the period of the SYS_CLK or crystal input clock source. These bits can

only be changed while all modulators and associated logic are in the power-down state (the PDnAll bit is set). Attempts to write these bits while the PDnAll bit is cleared will be ignored. See "PWM Channel Delay" on page 50 for more information.

| OutputDly[3:0] Setting | Output Delay in Input Clock Source Cycles |
|---|---|
| 0000 | 0 - No Delay |
| 0001 | 1 |
| 0010 | 2 |
| ..... | ..... |
| 1000 | 8 |
| ..... | ..... |
| 1111 | 15 - Max Delay |

## 9.5 Foldback and Ramp Configuration (Address 05h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | EnTherm | LockAdj | AttackDly1 | AttackDly0 | EnFloor | RmpSpeed1 | RmpSpeed0 |

### *9.5.1 Enable Thermal Foldback (EnTherm)*

*Default = 0*

*Function:*
Enables the thermal foldback feature. See "Thermal Foldback" on page 39 for more information.

| EnTherm Setting | Thermal Foldback State |
|---|---|
| 0 | Disabled. |
| 1 | Enabled. |

### *9.5.2 Lock Foldback Adjust (LockAdj)*

*Default = 0*

*Function:*
Controls the operation of the foldback lock adjustment feature. See "Thermal Foldback" on page 39 for more information.

| LockAdj Setting | Foldback Adjustment Lock State |
|---|---|
| 0 | Attenuation lock disabled. |
| 1 | Attenuation lock enabled. |

### *9.5.3 Foldback Attack Delay (AttackDly[1:0])*

*Default = 01*

*Function:*
Controls the foldback attack delay. See "Thermal Foldback" on page 39 for more information.

| AttackDly[1:0] Setting | Foldback Attack Time |
|---|---|
| 00 | Approximately 0.5 seconds. |
| 01 | Approximately 1.0 seconds. |
| 10 | Approximately 1.5 seconds. |
| 11 | Approximately 2.0 seconds. |

### 9.5.4 Enable Foldback Floor (EnFloor)

*Default = 0*

*Function:*
Controls the foldback attenuation floor feature. See "Thermal Foldback" on page 39 for more information.

| EnFloor Setting | Attenuation Floor |
|---|---|
| 0 | No foldback attenuation floor imposed. |
| 1 | Maximum foldback attenuation limited to -30 dB. |

### 9.5.5 Ramp Speed (RmpSpd[1:0])

*Default = 11*

*Function:*
Controls the PWM output ramp speed. See "PWM PopGuard Transient Control" on page 45 for more information.

| RmpSpd[1:0] Setting | Ramp Speed |
|---|---|
| 00 | Approximately 0.70 seconds. |
| 01 | Approximately 0.75 seconds. |
| 10 | Approximately 0.85 seconds. |
| 11 | Immediate. PWM PopGuard Disabled. |

## 9.6 Mixer / Pre-Scale Configuration (Address 06h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PreScale2 | PreScale1 | PreScale0 | Reserved | RChMix1 | RChMix0 | LChMix1 | LChMix0 |

### 9.6.1 Pre-Scale Attenuation (PreScale[2:0])

*Default = 000*

*Function:*
Controls the pre-scale attenuation level. See "Pre-Scaler" on page 29 for more information.

| PreScale[2:0] Setting | Pre-Scale Attenuation Setting |
|---|---|
| 000 | No pre-scale attenuation applied. |
| 001 | -2.0 dB |
| 010 | -4.0 dB |
| ... | ... |
| 100 | -8.0 dB |
| ... | ... |
| 111 | -14.0 dB |

### 9.6.2 Right Channel Mixer (RChMix[1:0])

*Default = 00*

*Function:*
Controls the right channel mixer output. See "Channel Mixer" on page 30 for more information.

| RChMix[1:0] Setting | Right Channel Mixer Output on Channel B |
|---|---|
| 00 | Right Channel |
| 01 | (Left Channel + Right Channel) / 2 |
| 10 | (Left Channel + Right Channel) / 2 |
| 11 | Left Channel |

### 9.6.3 Left Channel Mixer (LChMix[1:0])

*Default = 00*

*Function:*
Controls the left channel mixer output. See "Channel Mixer" on page 30 for more information.

| LChMix[1:0] Setting | Left Channel Mixer Output on Channel A |
|---|---|
| 00 | Left Channel |
| 01 | (Left Channel + Right Channel) / 2 |
| 10 | (Left Channel + Right Channel) / 2 |
| 11 | Right Channel |

## 9.7 Tone Configuration (Address 07h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DeEmph | Loudness | EnDigHPF | TrebFc1 | TrebFc0 | BassFc1 | BassFc0 | EnToneCtrl |

### 9.7.1 De-Emphasis Control (DeEmph)

*Default = 0*

*Function:*
Controls the operation of the internal de-emphasis filter. See "De-Emphasis" on page 31 for more information.

| DeEmph Setting | De-Emphasis State |
|---|---|
| 0 | No de-emphasis applied. |
| 1 | 44.1 kHz 50/15 µs de-emphasis filter applied. |

### 9.7.2 Adaptive Loudness Compensation Control (Loudness)

*Default = 0*

*Function:*
Controls the operation of the adaptive loudness compensation feature. See "Adaptive Loudness Compensation" on page 34 for more information.

| Loudness Setting | Adaptive Loudness Compensation State |
|---|---|
| 0 | Disabled. |
| 1 | Enabled. |

### 9.7.3 Digital Signal Processing High-Pass Filter (EnDigHPF)

*Default = 0*

*Function:*
Controls the operation of the digital signal processing high-pass filter. See "Digital Signal Processing High-Pass Filter" on page 30 for more information.

| EnDigHPF Setting | Digital Signal Processing High-Pass Filter State |
|---|---|
| 0 | Digital signal processing high-pass filter disabled. |
| 1 | Digital signal processing high-pass filter enabled. |

### 9.7.4 Treble Corner Frequency (TrebFc[1:0])

*Default = 00*

*Function:*
Sets the corner frequency for the treble shelving filter as shown below.

| TrebFc[1:0] Setting | Treble Corner Frequency |
|---|---|
| 00 | Selects Treble Fc 0 - Approximately 5 kHz |
| 01 | Selects Treble Fc 1 - Approximately 7 kHz |
| 10 | Selects Treble Fc 2 - Approximately 10 kHz |
| 11 | Selects Treble Fc 3 - Approximately 15 kHz |

### 9.7.5 Bass Corner Frequency (BassFc[1:0])

*Default = 01*

*Function:*
Sets the corner frequency for the bass shelving filter as shown below.

| BassFc[1:0] Setting | Bass Corner Frequency |
|---|---|
| 00 | Selects Bass Fc 0 - Approximately 50 Hz |
| 01 | Selects Bass Fc 1 - Approximately 100 Hz |
| 10 | Selects Bass Fc 2 - Approximately 200 Hz |
| 11 | Selects Bass Fc 3 - Approximately 250 Hz |

### 9.7.6 Tone Control Enable (EnToneCtrl)

*Default = 0*

*Function:*
When set, enables the bass and treble shelving filters. When cleared, disables the bass and treble shelving filters.

| EnToneCtrl Setting | Tone Control Filter State |
|---|---|
| 0 | Bass and treble shelving filters disabled. |
| 1 | Bass and treble shelving filters enabled. |

## 9.8 Tone Control (Address 08h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Treble3 | Treble2 | Treble1 | Treble0 | Bass3 | Bass2 | Bass1 | Bass0 |

### 9.8.1 Treble Gain Level (Treb[3:0])

*Default = 1000*

*Function:*
Sets the gain/attenuation level of the treble shelving filter.The level can be adjusted in 1.5 dB increments from +12.0 to -10.5 dB.

| Treb[3:0] Setting | Treble Shelving Filter Gain/Attenuation |
|---|---|
| 0000 | +12 dB |
| 0001 | +10.5 dB |
| ... | ... |
| 1000 | 0 dB |
| ... | ... |
| 1110 | -9.0 dB |
| 1111 | -10.5 dB |

### 9.8.2 Bass Gain Level (Bass[3:0])

*Default = 1000*

*Function:*
Sets the gain/attenuation level of the bass shelving filter. The level can be adjusted in 1.5 dB increments from +12.0 to -10.5 dB.

| Bass[3:0] Setting | Bass Shelving Filter Gain/Attenuation |
|---|---|
| 0000 | +12 dB |
| 0001 | +10.5 dB |
| ... | |
| 1000 | 0 dB |
| ... | |
| 1110 | -9.0 dB |
| 1111 | -10.5 dB |

## 9.9 2.1 Bass Manager/Parametric EQ Control (Address 09h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Freeze | Reserved | BassMgr2 | BassMgr1 | BassMgr0 | EnLFEPEq | EnChBPEq | EnChAPEq |

### 9.9.1 Freeze Controls (Freeze)

*Default = 0*

*Function:*
This function will freeze the previous output of, and allow modifications to be made to the master volume control (address 57h), channel X volume control (address 58h - 5Ah), and bi-quad coefficients for channel 1, channel 2 and channel 3 (address 0Ah - 54h) registers without the changes taking effect until the Freeze bit is disabled. To make multiple changes in these control port registers take effect simultaneously, enable the Freeze bit, make all register changes, then disable the Freeze bit.

| Freeze Setting | Register Freeze State |
|---|---|
| 0 | Register freeze disabled. |
| 1 | Register freeze enabled. |

### 9.9.2 Bass Cross-Over Frequency (BassMgr[2:0])

*Default = 000*

*Function:*
Controls the operation and cross-over frequency of the bass manager. See “Bass Management” on page 35 for more information.

| BassMgr[2:0] Setting | Bass Manager Crossover Setting |
|---|---|
| 000 | Bass manager disabled. |
| 001 | Selects Bass Manager Frequency 1 - Approximately 80 Hz |
| 010 | Selects Bass Manager Frequency 2 - Approximately 120 Hz |
| 011 | Selects Bass Manager Frequency 3 - Approximately 160 Hz |
| 100 | Selects Bass Manager Frequency 4 - Approximately 200 Hz |
| 101 | Selects Bass Manager Frequency 5 - Approximately 240 Hz |
| 110 | Selects Bass Manager Frequency 6 - Approximately 280 Hz |
| 111 | Selects Bass Manager Frequency 7 - Approximately 320 Hz |

### 9.9.3 Enable LFE Parametric EQ (EnLFEPEq)

*Default = 0*

*Function:*
Enables the parametric EQ 4 and 5 bi-quad filters for the LFE channel.

| EnLFEPEq Setting | LFE Parametric EQ State |
|---|---|
| 0 | Disabled. |
| 1 | Enabled. |

### 9.9.4 Enable Channel B Parametric EQ (EnChBPEq)

*Default = 0*

*Function:*
Enables the parametric EQ 1, 2, and 3 bi-quad filters for channel B.

| EnChBPEq Setting | Channel B Parametric EQ State |
|---|---|
| 0 | Disabled. |
| 1 | Enabled. |

### 9.9.5 Enable Channel A Parametric EQ (EnChAPEq)

*Default = 0*

*Function:*
Enables the parametric EQ 1, 2, and 3 bi-quad filters for channel A.

| EnChAPEq Setting | Channel A Parametric EQ State |
|---|---|
| 0 | Disabled. |
| 1 | Enabled. |

## 9.10 Volume and 2-Way Cross-Over Configuration (Address 55h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SZCMode1 | SZCMode0 | Mute50/50 | AutoMute | En2Way | 2WayFreq2 | 2WayFreq1 | 2WayFreq0 |

### 9.10.1 Soft Ramp and Zero Cross Control (SZCMode[1:0])

*Default = 10*

*Function:*
Sets the soft ramp and zero crossing detection modes by which volume and muting changes will be implemented.

| SZCMode[1:0] Setting | Soft Ramp & Zero Crossing Mode |
|---|---|
| 00 | Immediate Change<br>When immediate change is selected, all level changes will take effect immediately in one step. |
| 01 | Zero Cross<br>Zero cross dictates that signal level changes, both muting and attenuation, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period (approximately 18.7 ms for a PWM switch rate of 384/768 kHz and 17.0 ms for a PWM switch rate of 421.875/843.75 kHz) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. |
| 10 | Soft Ramp<br>Soft ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in ½ dB steps, from the current level to the new level at a rate of ½ dB per 4 sample periods for 32, 44.1, and 48 kHz, and ½ dB per 8 sample periods for 96 kHz. |
| 11 | Soft Ramp on Zero Cross<br>Soft ramp on zero cross dictates that signal level changes, both muting and attenuation, will occur in ½ dB steps and be implemented on a signal zero crossing. The ½ dB level change will occur after a timeout period (approximately 18.7 ms for a PWM switch rate of 384/768 kHz and 17.0 ms for a PWM switch rate of 421.875/843.75 kHz) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. |

### 9.10.2 Enable 50% Duty Cycle for Mute Condition (Mute50/50)

*Default = 0*

*Function:*
Enables the outputs of the amplifiers to switch at an exact 50%-duty-cycle signal (not modulated) for all mute conditions. This bit does not cause a mute condition to occur. The Mute50/50 bit only defines operation during a normal mute condition.

| Mute50/50 Setting | 50% Duty Cycle Mute State |
|---|---|
| 0 | 50% duty cycle for mute conditions disabled. |
| 1 | 50% duty cycle for mute conditions enabled. |

### 9.10.3 Auto-Mute (AutoMute)

*Default = 1*

*Function:*
When enabled, the outputs of the CS4525 will mute following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting is done independently for each channel. See "Volume and Muting Control" on page 36 for more information.

| AutoMute Setting | AutoMute State |
|---|---|
| 0 | Auto-mute on static 0's or -1's disabled. |
| 1 | Auto-mute on static 0's or -1's enabled. |

### 9.10.4 Enable 2-Way Crossover (En2Way)

*Default = 0*

*Function:*
Enables the 2-way crossover filters for channel 1 and channel 2.

| En2Way Setting | 2-Way Crossover State |
|---|---|
| 0 | 2-way crossover disabled. |
| 1 | 2-way crossover enabled. |

### 9.10.5 2-Way Cross-Over Frequency (2WayFreq[2:0])

*Default = 000*

*Function:*
Selects the cross-over frequency for the 2-Way Linkwitz-Riley filters.

| 2WayFreq Setting | 2-Way Crossover Frequency |
|---|---|
| 000 | Selects X-Over Freq 0 - Approximately 2.0 kHz |
| 001 | Selects X-Over Freq 1 - Approximately 2.2 kHz |
| 010 | Selects X-Over Freq 2 - Approximately 2.4 kHz |
| 011 | Selects X-Over Freq 3 - Approximately 2.6 kHz |
| 100 | Selects X-Over Freq 4 - Approximately 2.8 kHz |
| 101 | Selects X-Over Freq 5 - Approximately 3.0 kHz |
| 110 | Selects X-Over Freq 6 - Approximately 3.2 kHz |
| 111 | Selects X-Over Freq 7 - Approximately 3.4 kHz |

## 9.11 Channel 1-2: 2-Way Sensitivity Control (Address 56h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LowPass3 | LowPass2 | LowPass1 | LowPass0 | HighPass3 | HighPass2 | HighPass1 | HighPass0 |

### 9.11.1 Channel 1 and Channel 2 Low-Pass Sensitivity Adjust (LowPass[3:0])

*Default = 0000*

*Function:*
Controls the 2-way cross-over low-pass sensitivity adjustment. See “2-Way Crossover & Sensitivity Control” on page 41 for more information.

| LowPass[3:0] Setting | Sensitivity Compensation Level |
|---|---|
| 0000 | 0.0 dB |
| 0001 | -0.5 dB |
| 0010 | -1.0 dB |
| ... | ... |
| 1000 | -4.0 dB |
| ... | ... |
| 1110 | -7.0 dB |
| 1111 | -7.5 dB |

### 9.11.2 Channel 1 and Channel 2 High-Pass Sensitivity Adjust (HighPass[3:0])

*Default = 0000*

*Function:*
Controls the 2-way cross-over high-pass sensitivity adjustment. See "2-Way Crossover & Sensitivity Control" on page 41 for more information.

| HighPass[3:0] Setting | Sensitivity Compensation Level |
|---|---|
| 0000 | 0.0 dB |
| 0001 | -0.5 dB |
| 0010 | -1.0 dB |
| ... | ... |
| 1000 | -4.0 dB |
| ... | ... |
| 1110 | -7.0 dB |
| 1111 | -7.5 dB |

## 9.12 Master Volume Control (Address 57h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MVol7 | MVol6 | MVol5 | MVol4 | MVol3 | MVol2 | MVol1 | MVol0 |

### 9.12.1 Master Volume Control (MVol[7:0])

*Default = 30h*

*Function:*
Sets the gain/attenuation level of the master volume control. See "Volume and Muting Control" on page 36 for more information.

| MVol[7:0] Setting | Master Volume Setting |
|---|---|
| 0000 0000 | +24 dB |
| ... | ... |
| 0011 0000 | 0.0 dB |
| 0011 0001 | -0.5 dB |
| 0011 0010 | -1.0 dB |
| ... | ... |
| 1111 1110 | -103.0 dB |
| 1111 1111 | Master Mute |

## 9.13 Channel 1, 2, & 3 Volume Control (Address 58h, 59h, & 5Ah)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ChXVol7 | ChXVol6 | ChXVol5 | ChXVol4 | ChXVol3 | ChXVol2 | ChXVol1 | ChXVol0 |

### 9.13.1 Channel X Volume Control (ChXVol[7:0])

*Default = 30h*

*Function:*
Sets the gain/attenuation levels of the channel 1, 2, and 3 individual volume controls. See "Volume and Muting Control" on page 36 for more information.

| ChXVol[7:0] Setting | Channel X Volume Setting |
|---|---|
| 0000 0000 | +24 dB |
| ..... | ..... |
| 0011 0000 | 0.0 dB |
| 0011 0001 | -0.5 dB |
| 0011 0010 | -1.0 dB |
| ..... | ..... |
| 1111 1110 | -103.0 dB |
| 1111 1111 | Channel Mute |

## 9.14 Mute/Invert Control (Address 5Bh)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| InvADC | InvCh3 | InvCh2 | InvCh1 | MuteADC | MuteCh3 | MuteCh2 | MuteCh1 |

### 9.14.1 ADC Invert Signal Polarity (InvADC)

*Default = 0*

*Function:*
When set, the signal polarity of the ADC will be inverted.

| InvADC Setting | ADC Signal Inversion State |
|---|---|
| 0 | ADC signal polarity not inverted. |
| 1 | ADC signal polarity inverted. |

### 9.14.2 Invert Signal Polarity (InvChX)

*Default = 0*

*Function:*
When set, the signal polarity of the respective channels will be inverted.

| InvChX Setting | Channel X Signal Inversion State |
|---|---|
| 0 | Channel X signal polarity not inverted. |
| 1 | Channel X signal polarity inverted. |

### 9.14.3 ADC Channel Mute (MuteADC)

*Default = 0*

*Function:*
The output of the ADC will mute when enabled.

| MuteADC Setting | ADC Mute State |
|---|---|
| 0 | ADC un-muted. |
| 1 | ADC muted. |

### 9.14.4 Independent Channel Mute (MuteChX)

*Default = 0*

*Function:*
The PWM outputs of the CS4525 will mute when enabled. The muting function is affected, similar to attenuation changes, by the soft and zero cross bits (SZCMode[1:0]). See "Volume and Muting Control" on page 36 for more information.

| MuteChX Setting | Channel X Mute State |
|---|---|
| 0 | Channel X un-muted. |
| 1 | Channel X muted. |

## 9.15 Limiter Configuration 1 (Address 5Ch)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Max2 | Max1 | Max0 | Min2 | Min1 | Min0 | LimitAll | EnLimiter |

### 9.15.1 Maximum Threshold (Max[2:0])

*Default = 000*

*Function:*
Sets the maximum level, below full scale, at which to limit and attenuate the output signal at the limiter attack rate.

| Max[2:0] Setting | Maximum Threshold Setting |
|---|---|
| 000 | 0.0 dB |
| 001 | -3.0 dB |
| 010 | -6.0 dB |
| 011 | -9.0 dB |
| 100 | -12.0 dB |
| 101 | -18.0 dB |
| 110 | -24.0 dB |
| 111 | -30.0 dB |

### 9.15.2 Minimum Threshold (Min[2:0])

*Default = 000*

*Function:*
Sets a minimum level below full scale at which the limiter will begin to release its applied attenuation.

| Min[2:0] Setting | Minimum Threshold Setting |
|---|---|
| 000 | 0.0 dB |
| 001 | -3.0 dB |
| 010 | -6.0 dB |
| 011 | -9.0 dB |
| 100 | -12.0 dB |
| 101 | -18.0 dB |
| 110 | -24.0 dB |
| 111 | -30.0 dB |

### 9.15.3 Peak Signal Limit All Channels (LimitAll)

*Default = 1*

*Function:*
When cleared, the peak signal limiter will limit the maximum signal amplitude to prevent clipping on the specific channel indicating clipping. The other channels will not be affected. When set, the peak signal

limiter will limit the maximum signal amplitude to prevent clipping on all channels in response to any single channel indicating clipping. See "Peak Signal Limiter" on page 37 for more information.

| LimitAll Setting | Limit All Channels Configuration |
|---|---|
| 0 | Only individual channels affected by any limiter event. |
| 1 | All channels affected by any limiter event. |

### 9.15.4 Peak Detect and Limiter Enable (EnLimiter)

*Default = 0*

*Function:*
Limits the maximum signal amplitude to prevent clipping when this function is enabled. Peak signal limiting is performed by digital attenuation.

| EnLimiter Setting | Peak Signal Limiter State |
|---|---|
| 0 | Peak signal limiter disabled. |
| 1 | Peak signal limiter enabled. |

## 9.16 Limiter Configuration 2 (Address 5Dh)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | RRate5 | RRate4 | RRate3 | RRate2 | RRate1 | RRate0 |

### 9.16.1 Limiter Release Rate (RRate[5:0])

*Default = 000000*

*Function:*
Sets the rate at which the limiter releases the digital attenuation from levels below the minimum setting in the limiter threshold register.

The limiter release rate is a function of the sampling frequency, Fs, and the soft and zero cross setting.

| RRate[5:0] Setting | Limiter Release Rate |
|---|---|
| 00000 | Fastest release. |
| ..... | ..... |
| 11111 | Slowest release. |

## 9.17 Limiter Configuration 3 (Address 5Eh)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | ARate5 | ARate4 | ARate3 | ARate2 | ARate1 | ARate0 |

### 9.17.1 Limiter Attack Rate (ARate[5:0])

*Default = 000000*

*Function:*
Sets the rate at which the limiter attenuates the analog output from levels above the maximum setting in the limiter threshold register. The limiter attack rate is a function of the sampling frequency, Fs, and the soft and zero cross setting.

| ARate[5:0] Setting | Limiter Attack Rate |
|---|---|
| 00000 | Fastest attack. |
| ..... | ..... |
| 11111 | Slowest attack. |

## 9.18 Power Control (Address 5Fh)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | SelectVD | PDnADC | PDnOut3/4 | PDnOut2 | PDnOut1 | PDnAll |

### *9.18.1 Select VD Level (SelectVD)*

*Default = 1*

*Function:*
This bit selects between a VD of 2.5 V or 3.3 V when the LVD pin is connected to DGND. This bit is ignored when the LVD pin is connected to VD.

| SelectVD Setting | Selected VD Level |
|---|---|
| 0 | VD = 2.5 V. |
| 1 | VD = 3.3 V. |

### *9.18.2 Power Down ADC (PDnADC)*

*Default = 1*

*Function:*
The ADC will enter a power down state when this bit is enabled.

| PDnADC Setting | ADC Power-Down State |
|---|---|
| 0 | Normal ADC operation. |
| 1 | ADC power-down enabled. |

### *9.18.3 Power Down PWM Power Output X (PDnOutX)*

*Default = 1*

*Function:*
When set, the specific PWM power output will enter a power-down state. Only the output power stage is powered down. The PWM modulator is not affected, nor is the setup or delay register values. When set to normal operation, the specific output will power up according to the state of the RmpSpd[1:0] bits and the channel output configuration selected. When transitioning from normal operation to power down, the specific output will power down according to the state of the RmpSpd[1:0] bits and the channel output configuration selected.

| PDnChX Setting | Power Output X Power-Down State |
|---|---|
| 0 | Normal power output X operation. |
| 1 | Power output X power-down enabled. |

### *9.18.4 Power Down (PDnAll)*

*Default = 1*

*Function:*
The entire device will enter a low-power state when this function is enabled, and the contents of the control registers are retained in this mode. The power-down bit defaults to ‘enabled’ on power-up and must be disabled before normal operation can occur.

| PDnAll Setting | Device Power-Down State |
|---|---|
| 0 | Normal device operation. |
| 1 | Device power-down enabled. |

## 9.19 Interrupt Register (Address 60h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SRCLock | ADCOvfl | ChOvfl | AmpErr | SRCStateM | ADCOvflM | ChOvflM | AmpErrM |

Bits [7:4] in this register are read only. A ‘1’b in these bit positions indicates that the associated condition has occurred at least once since the register was last read. A ‘0’b indicates that the associated condition has not occurred since the last reading of the register. Reading the register resets bits to [7:4] ‘0’b. These bits are considered “edge-trigger” events. The operation of these 4 bits is not affected by the interrupt mask bits and the condition of each bit can be polled instead of generating an interrupt as required.

### *9.19.1 SRC Lock State Transition Interrupt Bit (SRCLock)*

*Default = 0*

*Function:*
This bit is read only. When set, indicates that the SRC has transitioned from an unlock to lock state or from a lock state to an unlock state since the last read of this register. Conditions which cause the SRC to transition states, such as loss of LRCK, SCLK, an LRCK ratio change, or the SRC achieving lock, will cause this bit to be set. This interrupt bit is an edge-triggered event and will be cleared following a read of this register.

If this bit is set, indicating a SRC state change condition, and the SRCLockM bit is set, the INT pin will go active. To determine the current lock state of the SRC, read the SRCLockSt bit in the interrupt status register.

| SRCLock Setting | SRC Lock State Change Status |
|---|---|
| 0 | SRC lock state unchanged since last read of this register. |
| 1 | SRC lock state changed since last read of this register. |

### *9.19.2 ADC Overflow Interrupt Bit (ADCOvfl)*

*Default = 0*

*Function:*
This bit is read only. When set, indicates that an over-range condition occurred anywhere in the CS4525 ADC signal path and has been clipped to positive or negative full scale as appropriate since the last read of this register. This interrupt bit is an edge-triggered event and will be cleared following a read of this register.

If this bit is set, indicating an ADC over-range condition, and the ADCOvflM bit is set, the INT pin will go active. To determine the current overflow state of the ADC, read the ADCOvflSt bit in the interrupt status register.

| ADCOvfl Setting | ADC Overflow Event Status |
|---|---|
| 0 | ADC overflow condition has not occurred since last read of this register. |
| 1 | ADC overflow condition has occurred since last read of this register. |

### *9.19.3 Channel Overflow Interrupt Bit (ChOvfl)*

*Default = 0*

*Function:*
This bit is read only. When set, indicates that the magnitude of an output sample on channel 1, 2, or 3 has exceeded full scale and has been clipped to positive or negative full scale as appropriate since the last read of this register. This interrupt bit is an edge-triggered event and will be cleared following a read of this register.

If this bit is set, indicating a channel over-range condition, and the ChOvflM bit is set, the INT pin will go active. To determine the current overflow state of each channel, read the ChXOvflSt bits in the interrupt status register.

| ChOvfl Setting | Channel Overflow Event Status |
|---|---|
| 0 | A channel overflow condition has not occurred since last read of this register. |
| 1 | A channel overflow condition has occurred since last read of this register. |

### 9.19.4 Amplifier Error Interrupt Bit (AmpErr)

*Default = 0*

*Function:*
This bit is read only. When set, indicates that an error was detected in the power amplifier section since the last read of this register. This interrupt bit is an edge-triggered event and will be cleared following a read of this register. This bit is the logical OR of all the bits in the amplifier error status register. Read the amplifier error status register to determine which condition occurred.

If this bit is set, indicating an amplifier stage error condition, and the AmpErrM bit is set to a '1'b, the INT pin will go active. To determine the actual current state of the amplifier error condition, read the amplifier error status register.

| AmpErr Setting | Amplifier Error Event Status |
|---|---|
| 0 | An amplifier error condition has not occurred since last read of this register. |
| 1 | An amplifier error condition has occurred since last read of this register. |

### 9.19.5 Mask Bit for SRC State (SRCLockM)

*Default = 0*

*Function:*
This bit serves as a mask for the SRC status interrupt source. If this bit is set, the SRCLock interrupt is unmasked, meaning that if the SRCLock bit is set, the INT pin will go active. If the SRCLockM bit is cleared, the SRCLock condition is masked, meaning that its occurrence will not affect the INT pin. However, the SRCLock and SRCLockSt bits will continue to reflect the lock status of the SRC.

| SRCLockM Setting | SRCLock INT Pin Mask State |
|---|---|
| 0 | SRCLock condition masked. |
| 1 | SRCLock condition un-masked. |

### 9.19.6 Mask Bit for ADC Overflow (ADCOvflM)

*Default = 0*

*Function:*
This bit serves as a mask for the ADC overflow interrupt source. If this bit is set, the ADCOvfl interrupt is unmasked, meaning that if the ADCOvfl bit is set, the INT pin will go active. If the ADCOvflM bit is cleared, the ADCOvfl condition is masked, meaning that its occurrence will not affect the INT pin. However, the ADCOvfl and ADCOvflSt bits will continue to reflect the overflow state of the ADC.

| ADCOvflM Setting | ADCOvfl INT Pin Mask State |
|---|---|
| 0 | ADCOvfl condition masked. |
| 1 | ADCOvfl condition un-masked. |

### 9.19.7 Mask Bit for Channel X Overflow (ChOvflM)

*Default = 0*

*Function:*
This bit serves as a mask for the channel overflow interrupt source. If this bit is set, the ChOvfl interrupt is unmasked, meaning that if the ChOvfl bit is set, the INT pin will go active. If the ChOvflM bit is cleared, the ChOvfl condition is masked, meaning that its occurrence will not affect the INT pin. However, the ChOvfl and ChXOvflSt bits will continue to reflect the overflow state of the individual channels.

| ChOvflM Setting | ChOvfl INT Pin Mask State |
|---|---|
| 0 | ChOvfl condition masked. |
| 1 | ChOvfl condition un-masked. |

### 9.19.8 Mask Bit for Amplifier Error (AmpErrM)

*Default = 0*

*Function:*
This bit serves as a mask for the amplifier error interrupt sources. If this bit is set, the AmpErr interrupt is unmasked, meaning that if the AmpErr bit is set, the INT pin will go active. If the AmpErrM bit is cleared, the AmpErr condition is masked, meaning that its occurrence will not affect the INT pin. However, the AmpErr and the amplifier error bits in the amplifier error status register will continue to reflect the status of the amplifier error conditions.

| AmpErrM Setting | AmpErr INT Pin Mask State |
|---|---|
| 0 | AmpErr condition masked. |
| 1 | AmpErr condition un-masked. |

## 9.20 Interrupt Status Register (Address 61h) - Read Only

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SRCLockSt | ADCOvflSt | Ch3OvflSt | Ch2OvflSt | Ch1OvflSt | RampDone | Reserved | Reserved |

All bits in this register are considered “level-trigger” events, meaning as long as a condition continues, the corresponding bit will remain set. These status bits are not affected by the interrupt mask bit and the condition of each bit can be polled. These bits will not be cleared following a read to this register, nor can they be written to cause an interrupt condition.

### 9.20.1 SRC State Transition (SRCLockSt)

*Default = 0*

*Function:*
This bit is read only and reflects the current lock state of the SRC. When set, indicates the SRC is currently locked. When cleared, indicates the SRC is currently unlocked.

| SRCLockSt Setting | SRC Lock State |
|---|---|
| 0 | SRC is currently unlocked. |
| 1 | SRC is currently locked. |

### 9.20.2 ADC Overflow (ADCOvfl)

*Default = 0*

*Function:*
This bit is read only and will identify the presence of an overflow condition within the ADC. When set, indicates that an over-range condition is currently occurring in the CS4525 ADC signal path and has been clipped to positive or negative full scale.

| ADCOvfl Setting | ADC Overflow State |
|---|---|
| 0 | An ADC overflow condition is not currently present. |
| 1 | An ADC overflow condition is currently present. |

### 9.20.3 Channel X Overflow (ChXOvfl)

*Default = 0*

*Function:*
These bits are read only and will identify the presence of an overflow condition anywhere in the associated channel's signal path. When set, indicates that an over-range condition is currently occurring in the channel's signal path and has been clipped to positive or negative full scale.

| ChXOvfl Setting | Channel X Overflow State |
|---|---|
| 0 | An overflow condition is not currently present on channel X. |
| 1 | An overflow condition is currently present on channel X. |

### 9.20.4 Ramp-Up Cycle Complete (RampDone)

*Default = 0*

*Function:*
When set, indicates that all active channels have completed the configured ramp-up interval.

| RampDone Setting | Ramp Completion State |
|---|---|
| 0 | Ramp-up interval not completed on all channels. |
| 1 | Ramp-up interval completed on all channels. |

## 9.21 Amplifier Error Status (Address 62h) - Read Only

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OverCurr4 | OverCurr3 | OverCurr2 | OverCurr1 | ExtAmpErr | UnderV | ThermErr | ThermWarn |

All bits in this register are considered "level-trigger" events, meaning as long as a condition continues, the corresponding bit will remain set. These status bits are not affected by the interrupt mask bit and the condition of each bit can be polled. These bits will not be cleared following a read to this register, nor can they be written to cause an interrupt condition.

### 9.21.1 Over-Current Detected On Channel X (OverCurrX)

*Default = 0*

*Function:*
When set, indicates an over current condition is currently present on the corresponding amplifier output.

| OverCurrX Setting | Amplifier Over-Current Status |
|---|---|
| 0 | An over current condition is not currently present on amplifier output X. |
| 1 | An over current condition is currently present on amplifier output X. |

### 9.21.2 External Amplifier State (ExtAmpSt)

*Default = 0*

*Function:*
When set, indicates a thermal warning condition is currently being reported by an external amplifier. For proper operation, the delay serial port must be configured to support an external thermal warning input signal. This status bit reflects the active state of the external thermal warning input signal.

| ExtAmpSt Setting | External Amplifier Status |
|---|---|
| 0 | A thermal warning condition is not currently being reported by an external amplifier. |
| 1 | A thermal warning condition is currently being reported by an external amplifier. |

### 9.21.3 Under Voltage Detected (UnderV)

*Default = 0*

*Function:*
When set, indicates an undervoltage condition is currently present on the VP voltage rail.

| UnderV Setting | VP Under Voltage Status |
|---|---|
| 0 | An under-voltage condition is not currently present on the VP supply. |
| 1 | An under-voltage condition is currently present on the VP supply. |

### 9.21.4 Thermal Error Detected (ThermErr)

*Default = 0*

*Function:*
When set, indicates a thermal error condition (specified by the thermal error trip point listed in the PWM Power Output Characteristics table on page 20) is currently present.

| ThermErr Setting | Thermal Error Status |
|---|---|
| 0 | A thermal error condition is not currently present. |
| 1 | A thermal error condition is currently present. |

### 9.21.5 Thermal Warning Detected (ThermWarn)

*Default = 0*

*Function:*
When set, indicates a thermal warning condition (specified by the thermal warning trip point listed in the PWM Power Output Characteristics table on page 20) is currently present.

| ThermWarn Setting | Thermal Warning Status |
|---|---|
| 0 | A thermal warning condition is not currently present. |
| 1 | A thermal warning condition is currently present. |

## 9.22 Chip I.D. and Revision Register (Address 63h) - Read Only

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DeviceID4 | DeviceID3 | DeviceID2 | DeviceID1 | DeviceID0 | RevID2 | RevID1 | RevID0 |

### *9.22.1 Device Identification (DeviceID[4:0])*

*Default =11000*

*Function:*
Identification code for the CS4525.

| DeviceID[4:0] Setting | Device ID Notes |
|---|---|
| 11000 | Permanent device identification code. |

### *9.22.2 Device Revision (RevID[2:0])*

*Default = 000*

*Function:*
CS4525 revision level.

| RevID[2:0] Setting | Device Revision ID |
|---|---|
| 000 | Revision A0. |

# 10.PARAMETER DEFINITIONS

**Dynamic Range (DYR)**

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth, typically 20 Hz to 20 kHz. Dynamic Range is a signal-to-noise ratio measurement over the specified band width made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

**Total Harmonic Distortion + Noise (THD+N)**

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

**Frequency Response**

FR is the deviation in signal level verses frequency. The 0 dB reference point is 1 kHz. The amplitude corner, Ac, lists the maximum deviation in amplitude above and below the 1 kHz reference point. The listed minimum and maximum frequencies are guaranteed to be within the Ac from minimum frequency to maximum frequency inclusive.

**Interchannel Isolation**

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

**Interchannel Gain Mismatch**

The gain difference between left and right channels. Units in decibels.

**Gain Drift**

The change in gain value with temperature. Units in ppm/°C.

**Fs**

Sampling Frequency.

**Resolution**

The number of bits in a serial audio data word.

**SRC**

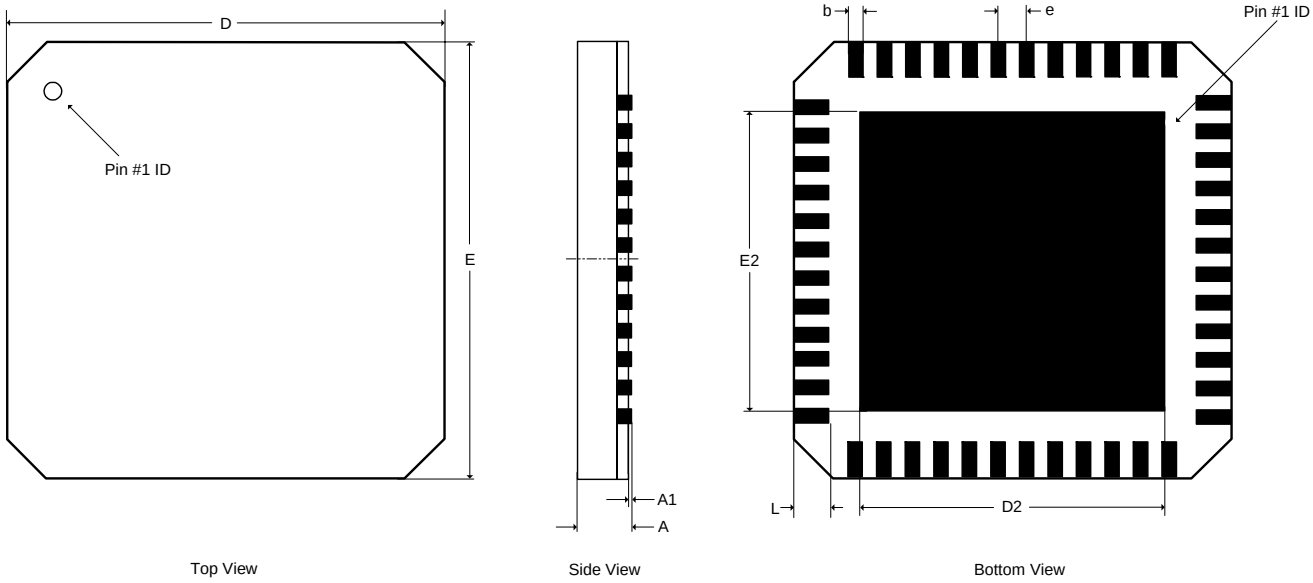
Sample Rate Converter. Converts data derived at one sample rate to a differing sample rate.

# 11.REFERENCES

1. Cirrus Logic, "*AN18: Layout and Design Rules for Data Converters and Other Mixed Signal Devices*," Version 6.0, February 1998.
2. Cirrus Logic, "*AN22: Overview of Digital Audio Interface Data Structures*, *Version 2.0*", February 1998.; A useful tutorial on digital audio specifications.
3. Philips Semiconductor, "*The I²C-Bus Specification: Version 2*," Dec. 1998. http://www.semiconductors.philips.com

# 12.PACKAGE DIMENSIONS

## 48L QFN (9 × 9 MM BODY) PACKAGE DRAWING




| | INCHES | | | MILLIMETERS | | | NOTE |
|---|---|---|---|---|---|---|---|
| DIM | MIN | NOM | MAX | MIN | NOM | MAX | |
| A | -- | -- | 0.0354 | -- | -- | 0.90 | 1 |
| A1 | 0.0000 | -- | 0.0020 | 0.00 | -- | 0.05 | 1 |
| b | 0.0118 | 0.0138 | 0.0157 | 0.30 | 0.35 | 0.40 | 1,2 |
| D | | 0.3543 BSC | | | 9.00 BSC | | 1 |
| D2 | 0.2618 | 0.2677 | 0.2736 | 6.65 | 6.80 | 6.95 | 1 |
| E | | 0.3543 BSC | | | 9.00 BSC | | 1 |
| E2 | 0.2618 | 0.2677 | 0.2736 | 6.65 | 6.80 | 6.95 | 1 |
| e | | 0.0256 BSC | | | 0.65 BSC | | 1 |
| L | 0.0177 | 0.0217 | 0.0276 | 0.45 | 0.55 | 0.70 | 1 |

***JEDEC #: MO-220***

*Controlling Dimension is Millimeters.*

**Table 19:**

**Notes:** 1. Dimensioning and tolerance per ASME Y4.5M - 1994.

2. Dimensioning lead width applies to the plated terminal and is measured between 0.20 mm and 0.25 mm from the terminal tip.

# 13.THERMAL CHARACTERISTICS

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Junction to Case Thermal Impedance | $\theta_{JC}$ | - | 1 | - | °C/Watt |

## 13.1 Thermal Flag

This device is designed to have the metal flag on the bottom of the device soldered directly to a metal plane on the PCB. To enhance the thermal dissipation capabilities of the system, this metal plane should be coupled with vias to a large metal plane on the backside (and inner ground layer, if applicable) of the PCB.

In either case, it is beneficial to use copper fill in any unused regions inside the PCB layout, especially those immediately surrounding the CS4525. In addition to improving in electrical performance, this practice also aids in heat dissipation.

The heat dissipation capability required of the metal plane for a given output power can be calculated as follows:

$\theta_{CA} = [(T_{J(MAX)} - T_A) / P_D] - \theta_{JC}$

where,
$\theta_{CA}$ = Thermal resistance of the metal plane in °C/Watt
$T_{J(MAX)}$ = Maximum rated operating junction temperature in °C, equal to 150 °C
$T_A$ = Ambient temperature in °C
$P_D$ = RMS power dissipation of the device, equal to $0.15*P_{RMS}$ (assuming 85% efficiency)
$\theta_{JC}$ = Junction-to-case thermal resistance of the device in °C/Watt

# 14.ORDERING INFORMATION

| Product | Description | Package | Pb-Free | Grade | Temp Range | Container | Order# |
|---|---|---|---|---|---|---|---|
| CS4525 | Digital TV Amp with Integrated ADC | 48-QFN | Yes | Commercial | -10° to +70°C | Rail | CS4525-CNZ |
| | | | | | | Tape and Reel | CS4525-CNZR |
| CRD4525 | 2 x 15 W Reference Design Board | - | - | - | - | - | CRD4525 |
| CRD4412 | 1 x 30 W Reference Design Daughter Card | - | - | - | - | - | CRD4412 |

# 15.REVISION HISTORY

| Release | Changes |
|---|---|
| A1 | Initial Release |

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find one nearest you, go to www.cirrus.com.

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