CS4382A

114 dB, 192 kHz 8-Channel D/A Converter

Features

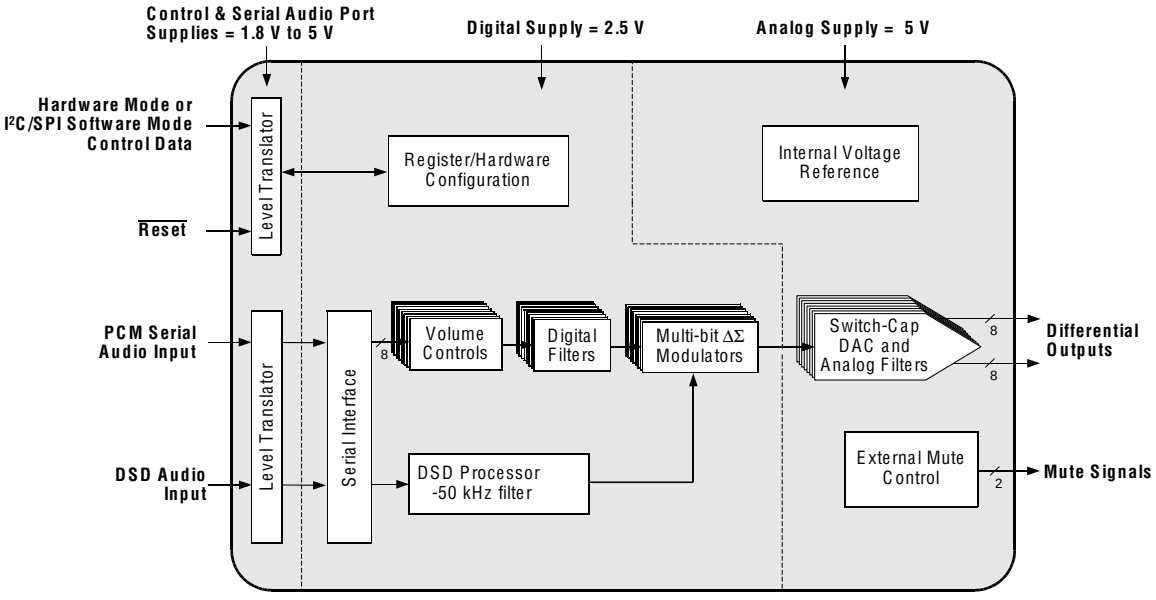
- Advanced Multi-bit Delta Sigma Architecture
- 24-bit Conversion
- Up to 192 kHz Sample Rates
- 114 dB Dynamic Range
- -100 dB THD+N
- Direct Stream Digital® (DSD™) Mode
- On-chip 50 kHz Filter
- Matched PCM and DSD Analog Output Levels
- Selectable Digital Filters
- Volume Control with 1 dB Step Size and Soft Ramp
- Low Clock-jitter Sensitivity
- +5 V Analog Supply, +2.5 V Digital Supply
- Separate 1.8 to 5 V Logic Supplies for the Control & Serial Ports

Description

The CS4382A is a complete 8-channel digital-to-analog system. This D/A system includes digital de-emphasis, 1 dB step size volume control, ATAPI channel mixing, selectable fast and slow digital interpolation filters followed by an oversampled, multi-bit delta-sigma modulator which includes mismatch shaping technology that eliminates distortion due to capacitor mismatch. Following this stage is a multi-element switched capacitor stage and low-pass filter with differential analog outputs.

The CS4382A also has a proprietary DSD processor which allows for 50 kHz on-chip filtering without an intermediate decimation stage. The CS4382A is available in a 48-pin LQFP package in both Commercial (-40°C to +85°C) and Automotive grades (-40°C to +105°C). The CDB4382A Customer Demonstration board is also available for device evaluation and implementation suggestions. Please see "Ordering Information" on page 48 for complete details.

The CS4382A accepts PCM data at sample rates from 4 kHz to 216 kHz, DSD audio data, and delivers excellent sound quality. These features are ideal for multi-channel audio systems including SACD players, A/V receivers, digital TV's, mixing consoles, effects processors, sound cards, and automotive audio systems.



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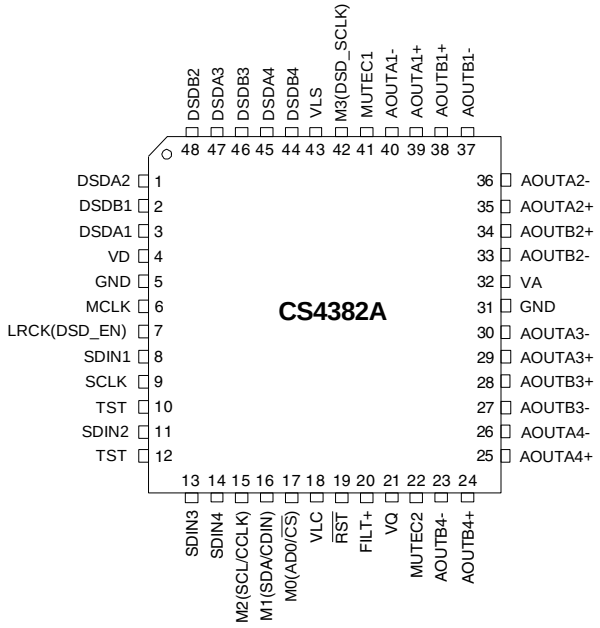
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1. PIN DESCRIPTION



Pin Name	#	Pin Description
VD	4	**Digital Power** (*Input*) **-** Positive power supply for the digital section.
GND	5 31	**Ground** (*Input*) - Ground reference. Should be connected to analog ground.
MCLK	6	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
LRCK	7	**Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line. The frequency of the left/right clock must be at the audio sample rate, Fs.
SDIN1 SDIN2 SDIN3 SDIN4	8 11 13 14	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
SCLK	9	**Serial Clock** (*Input*) - Serial clock for the serial audio interface.
VLC	18	**Control Port Power** (*Input*) **-** Determines the required signal level for the Control Port. Refer to the Recommended Operating Conditions for appropriate voltages.
$\overline{\text{RST}}$	19	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when low.
FILT+	20	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits. Requires the capacitive decoupling to analog ground, as shown in the Typical Connection Diagram.
VQ	21	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage. VQ must be capacitively coupled to analog ground, as shown in the Typical Connection Diagram. The nominal voltage level is specified in the Analog Characteristics and Specifications section. VQ presents an appreciable source impedance and any current drawn from this pin will alter device performance. However, VQ can be used to bias the analog circuitry assuming there is no AC signal component and the DC current is less than the maximum specified in the Analog Characteristics and Specifications section.
MUTEC1 MUTEC234	41 22	**Mute Control** (*Output*) - The Mute Control pins go high during power-up initialization, reset, muting, power-down or if the master clock to left/right clock frequency ratio is incorrect. These pins are intended to be used as a control for external mute circuits to prevent the clicks and pops that can occur in any single supply system. The use of external mute circuits are not mandatory but may be desired for designs requiring the absolute minimum in extraneous clicks and pops.

Pin Name	#	Pin Description
AOUTA1 +,- AOUTB1 +,- AOUTA2 +,- AOUTB2 +,- AOUTA3 +,- AOUTB3 +,- AOUTA4 +,- AOUTB4 +,-	39, 40 38, 37 35, 36 34, 33 29, 30 28, 27 25, 26 24, 23	**Differential Analog Output** (*Output*) - The full-scale differential analog output level is specified in the Analog Characteristics specification table.
VA	32	**Analog Power** (*Input*) **-** Positive power supply for the analog section.
VLS	43	**Serial Audio Interface Power** (*Input*) **-** Determines the required signal level for the serial audio interface. Refer to the Recommended Operating Conditions for appropriate voltages.
TST	10 12	**Test -** These pins need to be tied to analog ground.
Software Mode Definitions		
SCL/CCLK	15	**Serial Control Port Clock** (*Input*) - Serial clock for the serial Control Port. Requires an external pull-up resistor to the logic interface voltage in I²C® Mode as shown in the Typical Connection Diagram.
SDA/CDIN	16	**Serial Control Data** (*Input/Output*) - SDA is a data I/O line in I²C Mode and requires an external pull-up resistor to the logic interface voltage, as shown in the Typical Connection Diagram. CDIN is the input data line for the Control Port interface in SPI™ Mode.
AD0/$\overline{CS}$	17	**Address Bit 0 (I²C) / Control Port Chip Select (SPI)** (*Input*) - AD0 is a chip address pin in I²C Mode; $\overline{CS}$ is the chip select signal for SPI format.
Stand-Alone Definitions		
M0 M1 M2 M3	17 16 15 42	**Mode Selection** (*Input*) - Determines the operational mode of the device.
DSD Definitions		
DSD_SCLK	42	**DSD Serial Clock** (*Input*) - Serial clock for the Direct Stream Digital audio interface.
DSD_EN	7	**DSD-Enable** *(Input)* - When held at logic '1' the device will enter DSD Mode (Stand-Alone mode only).
DSDA1 DSDB1 DSDA2 DSDB2 DSDA3 DSDB3 DSDA4 DSDB4	3 2 1 48 47 46 45 44	**Direct Stream Digital Input** (*Input*) - Input for Direct Stream Digital serial audio data.

2. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

(GND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Typ	Max	Units
DC Power Supply	Analog Power	VA	4.75	5.0	5.25	V
	Digital Internal Power	VD	2.37	2.5	2.63	V
	Serial Data Port Interface Power	VLS	1.71	5.0	5.25	V
	Control Port Interface Power	VLC	1.71	5.0	5.25	V
Ambient Operating Temperature (power applied)						
	Commercial Grade (-CQZ)	T_A	-40	-	+85	°C
	Automotive Grade (-DQZ)		-40	-	+105	°C

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supply	Analog Power	VA	-0.3	6.0	V
	Digital Internal Power	VD	-0.3	3.2	V
	Serial Data Port Interface Power	VLS	-0.3	6.0	V
	Control Port Interface Power	VLC	-0.3	6.0	V
Input Current	Any Pin Except Supplies	I_{in}	-	±10	mA
Digital Input Voltage	Serial Data Port Interface	V_{IND-S}	-0.3	VLS+ 0.4	V
	Control Port Interface	V_{IND-C}	-0.3	VLC+ 0.4	V
Ambient Operating Temperature (power applied)		T_{op}	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

DAC ANALOG CHARACTERISTICS - COMMERCIAL (-CQZ)

Test Conditions (unless otherwise specified): VA = VLS = VLC = 5 V; VD = 2.5 V; T_A = 25°C; Full-Scale 997 Hz input sine wave (Note 1); Tested under max ac-load resistance; Valid with FILT+ and VQ capacitors as shown in "Typical Connection Diagram" on page 19; Measurement Bandwidth 10 Hz to 20 kHz.

Parameters			Symbol	Min	Typ	Max	Unit
FS = 48 kHz, 96 kHz, 192 kHz and DSD							
Dynamic Range	24-bit	A-weighted		108	114	-	dB
		Unweighted		105	111	-	dB
	16-bit	A-weighted		-	97	-	dB
	(Note 2)	Unweighted		-	94	-	dB
Total Harmonic Distortion + Noise		24-bit					
		0 dB		-	-100	-94	dB
		-20 dB		-	-91	-	dB
		-60 dB	THD+N	-	-51	-45	dB
	(Note 2) 16-bit	0 dB		-	-94	-	dB
		-20 dB		-	-74	-	dB
		-60 dB		-	-34	-	dB
Idle Channel Noise / Signal-to-noise Ratio				-	114	-	dB
Interchannel Isolation		(1 kHz)		-	110	-	dB
DC Accuracy							
Interchannel Gain Mismatch				-	0.1	-	dB
Gain Drift				-	100	-	ppm/°C
Analog Output							
Full-scale Differential Output Voltage			V_{FS}	128%•V_A	132%•V_A	136%•V_A	Vpp
Output Impedance		(Note 3)	Z_{OUT}	-	130	-	Ω
Max DC Current Draw From an AOUT Pin			I_{OUTmax}	-	1.0	-	mA
Min AC-load Resistance			R_L	-	3	-	kΩ
Max Load Capacitance			C_L	-	100	-	pF
Quiescent Voltage			V_Q	-	50%•V_A	-	VDC
Max Current draw from V_Q			I_{QMAX}	-	10	-	µA

Notes:

1. One-half LSB of triangular PDF dither is added to data.
2. Performance limited by 16-bit quantization noise.
3. V_{FS} is tested under load R_L and includes attenuation due to Z_{OUT}

DAC ANALOG CHARACTERISTICS - AUTOMOTIVE (-DQZ)

Test Conditions (unless otherwise specified): VA = 4.75 to 5.25 V; VLS = 1.71 to 5.25 V; VLC = 1.71 to 5.25 V; VD = 2.37 to 2.63 V; T_A = -40°C to 85°C; Full-Scale 997 Hz input sine wave (Note 1); Tested under max ac-load resistance; Valid with FILT+ and VQ capacitors as shown in "Typical Connection Diagram" on page 19; Measurement Bandwidth 10 Hz to 20 kHz.

Parameters			Symbol	Min	Typ	Max	Unit
FS = 48 kHz, 96 kHz, 192 kHz and DSD							
Dynamic Range	24-bit	A-weighted		105	114	-	dB
		Unweighted		102	111	-	dB
	16-bit	A-weighted		-	97	-	dB
	(Note 2)	Unweighted		-	94	-	dB
Total Harmonic Distortion + Noise		24-bit					
		0 dB		-	-100	-91	dB
		-20 dB		-	-91	-	dB
		-60 dB	THD+N	-	-51	-42	dB
	(Note 2) 16-bit	0 dB		-	-94	-	dB
		-20 dB		-	-74	-	dB
		-60 dB		-	-34	-	dB
Idle Channel Noise / Signal-to-noise Ratio				-	114	-	dB
Interchannel Isolation		(1 kHz)		-	110	-	dB
DC Accuracy							
Interchannel Gain Mismatch				-	0.1	-	dB
Gain Drift				-	100	-	ppm/°C
Analog Output							
Full-scale Differential Output Voltage			V_{FS}	128%•V_A	132%•V_A	136%•V_A	Vpp
Output Impedance		(Note 3)	Z_{OUT}	-	130	-	Ω
Max DC Current Draw From an AOUT Pin			I_{OUTmax}	-	1.0	-	mA
Min AC-load Resistance			R_L	-	3	-	kΩ
Max Load Capacitance			C_L	-	100	-	pF
Quiescent Voltage			V_Q	-	50%•V_A	-	VDC
Max Current draw from V_Q			I_{QMAX}	-	10	-	µA

POWER AND THERMAL CHARACTERISTICS

Parameters		Symbol	Min	Typ	Max	Units
Power Supplies						
Power Supply Current	Normal Operation, VA= 5 V	I_A	-	84	91	mA
(Note 4)	VD= 2.5 V	I_D	-	20	25	mA
	(Note 5) Interface Current, VLC=5 V	I_{LC}	-	2	-	µA
	VLS=5 V	I_{LS}	-	75	-	µA
	(Note 6) Power-down State (all supplies)	I_{pd}	-	200	-	µA
Power Dissipation (Note 4)	VA = 5 V, VD = 2.5 V					
	Normal Operation		-	470	520	mW
	(Note 6) Power-down		-	1	-	mW
Package Thermal Resistance	Multi-layer	θ_{JA}	-	48	-	°C/Watt
	Two-layer	θ_{JA}	-	65	-	°C/Watt
		θ_{JC}	-	15	-	°C/Watt
Power Supply Rejection Ratio (Note 7)	(1 kHz)	PSRR	-	60	-	dB
	(60 Hz)		-	40	-	dB

Notes:

4. Current consumption increases with increasing FS within a given speed mode and is signal-dependent. Max values are based on highest FS and highest MCLK.
5. I_{LC} measured with no external loading on the SDA pin.
6. Power-down Mode is defined as $\overline{RST}$ pin = Low with all clock and data lines held static.
7. Valid with the recommended capacitor values on FILT+ and VQ as shown in Figures 5 and 6.

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs.
See Note 12.

Parameter		Fast Roll-Off Min	Fast Roll-Off Typ	Fast Roll-Off Max	Unit
Combined Digital and On-chip Analog Filter Response - Single-Speed Mode - 48 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.454	Fs
	to -3 dB corner	0	-	.499	Fs
Frequency Response	10 Hz to 20 kHz	-0.01	-	+0.01	dB
Stop Band		0.547	-	-	Fs
Stop-band Attenuation	(Note 10)	102	-	-	dB
Group Delay		-	10.4/Fs	-	s
De-emphasis Error (Note 11)	Fs = 32 kHz	-	-	±0.23	dB
(Relative to 1 kHz)	Fs = 44.1 kHz	-	-	±0.14	dB
	Fs = 48 kHz	-	-	±0.09	dB
Combined Digital and On-chip Analog Filter Response - Double-Speed Mode - 96 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.430	Fs
	to -3 dB corner	0	-	.499	Fs
Frequency Response	10 Hz to 20 kHz	-0.01	-	+0.01	dB
Stop Band		.583	-	-	Fs
Stop-band Attenuation	(Note 10)	80	-	-	dB
Group Delay		-	6.15/Fs	-	s
Combined Digital and On-chip Analog Filter Response - Quad-Speed Mode - 192 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.105	Fs
	to -3 dB corner	0	-	.490	Fs
Frequency Response	10 Hz to 20 kHz	-0.01	-	+0.01	dB
Stop Band		.635	-	-	Fs
Stop-band Attenuation	(Note 10)	90	-	-	dB
Group Delay		-	7.1/Fs	-	s

Notes:

8. Slow roll-off interpolation filter is only available in Software Mode.
9. Response is clock-dependent and will scale with Fs.
10. For Single-Speed Mode, the Measurement Bandwidth is from stopband to 3 Fs.
    For Double-Speed Mode, the Measurement Bandwidth is from stopband to 3 Fs.
    For Quad-Speed Mode, the Measurement Bandwidth is from stopband to 1.34 Fs.
11. De-emphasis is available only in Single-Speed Mode; only 44.1 kHz De-emphasis is available in Hardware Mode.
12. Amplitude vs. Frequency plots of this data are available in Section 7. “Filter Plots” on page 42.

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

(CONTINUED)

Parameter		Slow Roll-Off (Note 8) Min	Typ	Max	Unit
Single-Speed Mode - 48 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	0.417	Fs
	to -3 dB corner	0	-	0.499	Fs
Frequency Response	10 Hz to 20 kHz	-0.01	-	+0.01	dB
Stop Band		.583	-	-	Fs
Stop-band Attenuation	(Note 10)	64	-	-	dB
Group Delay		-	7.8/Fs	-	s
De-emphasis Error (Note 11)	Fs = 32 kHz	-	-	±0.36	dB
(Relative to 1 kHz)	Fs = 44.1 kHz	-	-	±0.21	dB
	Fs = 48 kHz	-	-	±0.14	dB
Double-Speed Mode - 96 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.296	Fs
	to -3 dB corner	0	-	.499	Fs
Frequency Response	10 Hz to 20 kHz	-0.01	-	+0.01	dB
Stop Band		.792	-	-	Fs
Stop-band Attenuation	(Note 10)	70	-	-	dB
Group Delay		-	5.4/Fs	-	s
Quad-Speed Mode - 192 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.104	Fs
	to -3 dB corner	0	-	.481	Fs
Frequency Response	10 Hz to 20 kHz	-0.01	-	+0.01	dB
Stop Band		.868	-	-	Fs
Stop-band Attenuation	(Note 10)	75	-	-	dB
Group Delay		-	6.6/Fs	-	s

DSD COMBINED DIGITAL & ON-CHIP ANALOG FILTER RESPONSE

Parameter		Min	Typ	Max	Unit
DSD Processor mode					
Passband (Note 9)	to -3 dB corner	0	-	50	kHz
Frequency Response	10 Hz to 20 kHz	-0.05	-	+0.05	dB
Roll-off		27	-	-	dB/Oct

DIGITAL CHARACTERISTICS

Parameters		Symbol	Min	Typ	Max	Units
Input Leakage Current	(Note 13)	I_{in}	-	-	±10	µA
Input Capacitance			-	8	-	pF
High-level Input Voltage	Serial I/O Control I/O	V_{IH} V_{IH}	70% 70%	- -	- -	V_{LS} V_{LC}
Low-level Input Voltage	Serial I/O Control I/O	V_{IL} V_{IL}	- -	- -	30% 30%	V_{LS} V_{LC}
Low-level Output Voltage (I_{OL} = -1.2 mA)	Control I/O = 3.3 V, 5 V Control I/O = 1.8 V, 2.5 V	V_{OL} V_{OL}	- -	- -	20% 25%	V_{LC} V_{LC}
Maximum MUTEC Drive Current		I_{max}	-	3	-	mA
MUTEC High-level Output Voltage		V_{OH}	-	VA	-	V
MUTEC Low-level Output Voltage		V_{OL}	-	0	-	V

13. Any pin except supplies. Transient currents of up to ±100 mA on the input pins will not cause SCR latch-up.

SWITCHING CHARACTERISTICS - PCM

(Inputs: Logic 0 = GND, Logic 1 = VLS, C_L = 30 pF)

Parameters		Symbol	Min	Max	Units
$\overline{\text{RST}}$ pin Low Pulse Width	(Note 14)		1	-	ms
MCLK Frequency			1.024	55.2	MHz
MCLK Duty Cycle	(Note 15)		45	55	%
Input Sample Rate - LRCK	Single-speed Mode Double-speed Mode Quad-speed Mode	F_s F_s F_s	4 50 100	54 108 216	kHz kHz kHz
LRCK Duty Cycle			45	55	%
SCLK Duty Cycle			45	55	%
SCLK High Time		t_{sckh}	8	-	ns
SCLK Low Time		t_{sckl}	8	-	ns
LRCK Edge to SCLK rising edge		t_{lcks}	5	-	ns
SDIN Setup Time before SCLK rising edge		t_{ds}	3	-	ns
SDIN Hold Time after SCLK rising edge		t_{dh}	5	-	ns

Notes:

14. After powering up, $\overline{\text{RST}}$ should be held low until after the power supplies and clocks are settled.
15. See Table 1 on page 21 for suggested MCLK frequencies.

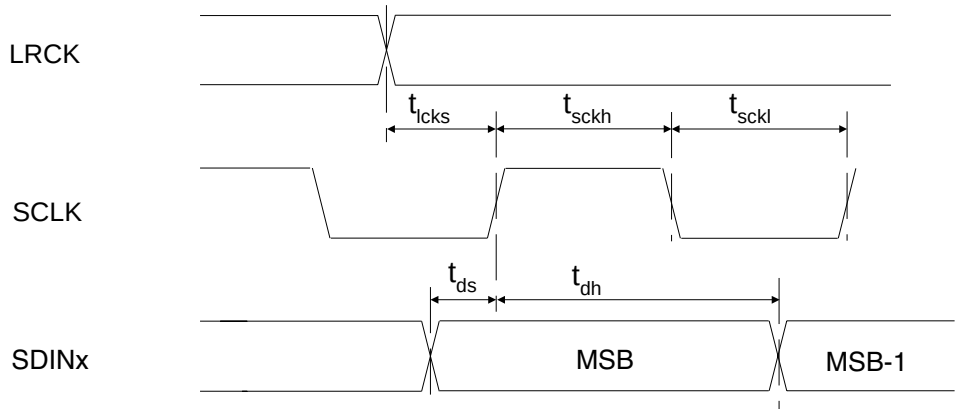


Figure 1. Serial Audio Interface Timing

SWITCHING CHARACTERISTICS - DSD

(Logic 0 = AGND = DGND; Logic 1 = VLS; C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
MCLK Duty Cycle		40	-	60	%
DSD_SCLK Pulse Width Low	t_{sclkl}	160	-	-	ns
DSD_SCLK Pulse Width High	t_{sclkh}	160	-	-	ns
DSD_SCLK Frequency (64x Oversampled) (128x Oversampled)		1.024 2.048	- -	3.2 6.4	MHz MHz
DSD_A / _B valid to DSD_SCLK rising setup time	t_{sdlrs}	20	-	-	ns
DSD_SCLK rising to DSD_A or DSD_B hold time	t_{sdh}	20	-	-	ns

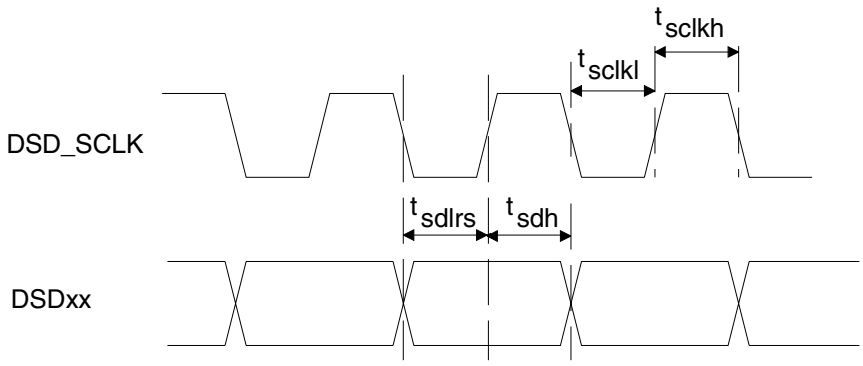


Figure 2. Direct Stream Digital - Serial Audio Input Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - I²C FORMAT

(Inputs: Logic 0 = GND, Logic 1 = VLC, C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{\text{RST}}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 16)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}, t_{rc}	-	1	µs
Fall Time SCL and SDA	t_{fc}, t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns

Notes:

16. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

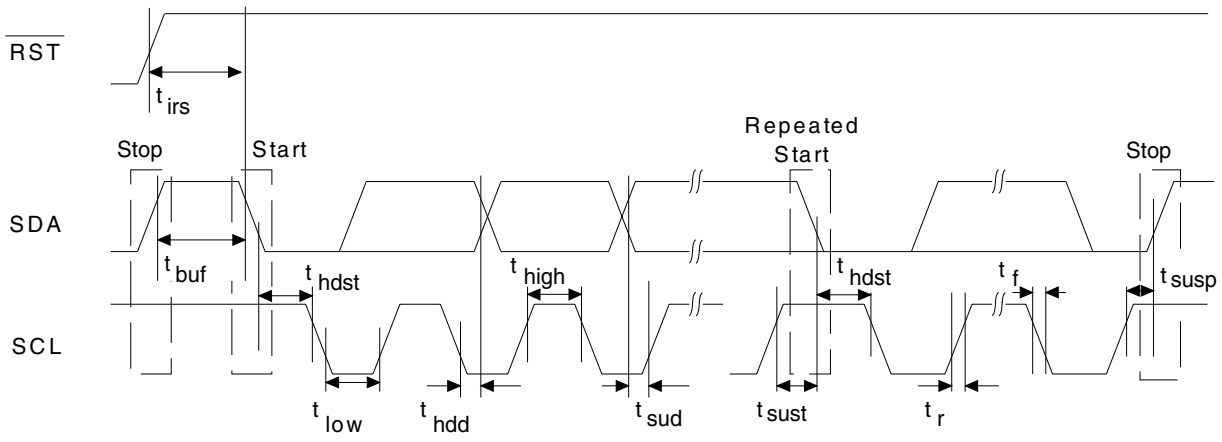


Figure 3. Control Port Timing - I²C Format

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI FORMAT

(Inputs: Logic 0 = GND, Logic 1 = VLC, C_L = 30 pF)

Parameter		Symbol	Min	Max	Unit
CCLK Clock Frequency		f_{sclk}	-	6	MHz
$\overline{RST}$ Rising Edge to CS Falling		t_{srs}	500	-	ns
CCLK Edge to $\overline{CS}$ Falling	(Note 17)	t_{spi}	500	-	ns
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 18)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 19)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 19)	t_{f2}	-	100	ns

Notes:

17. t_{spi} only needed before first falling edge of $\overline{CS}$ after $\overline{RST}$ rising edge. t_{spi} = 0 at all other times.
18. Data must be held for sufficient time to bridge the transition time of CCLK.
19. For F_{SCK} < 1 MHz.

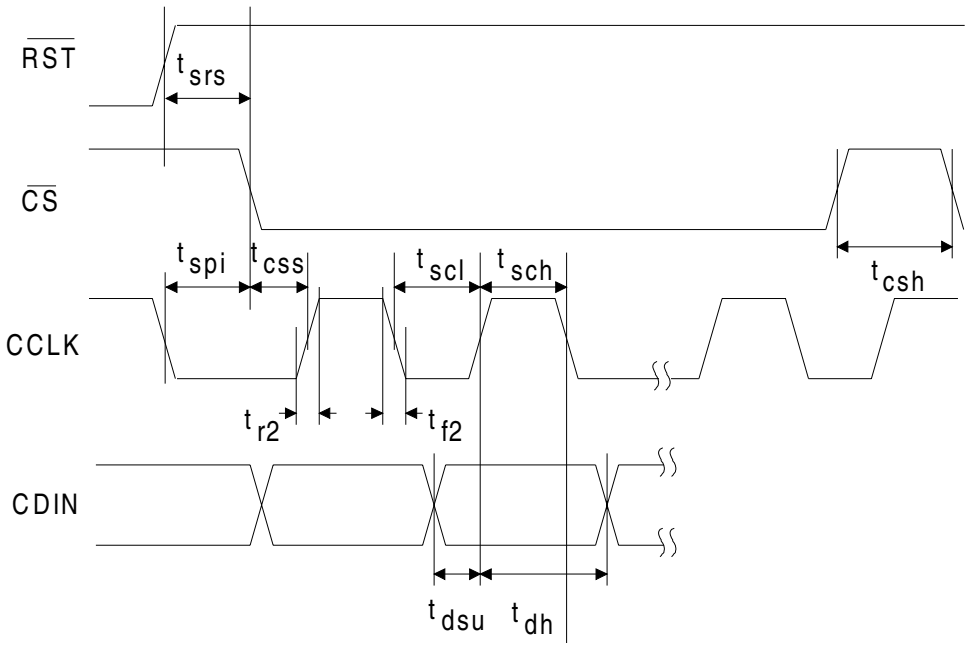


Figure 4. Control Port Timing - SPI Format

3. TYPICAL CONNECTION DIAGRAM

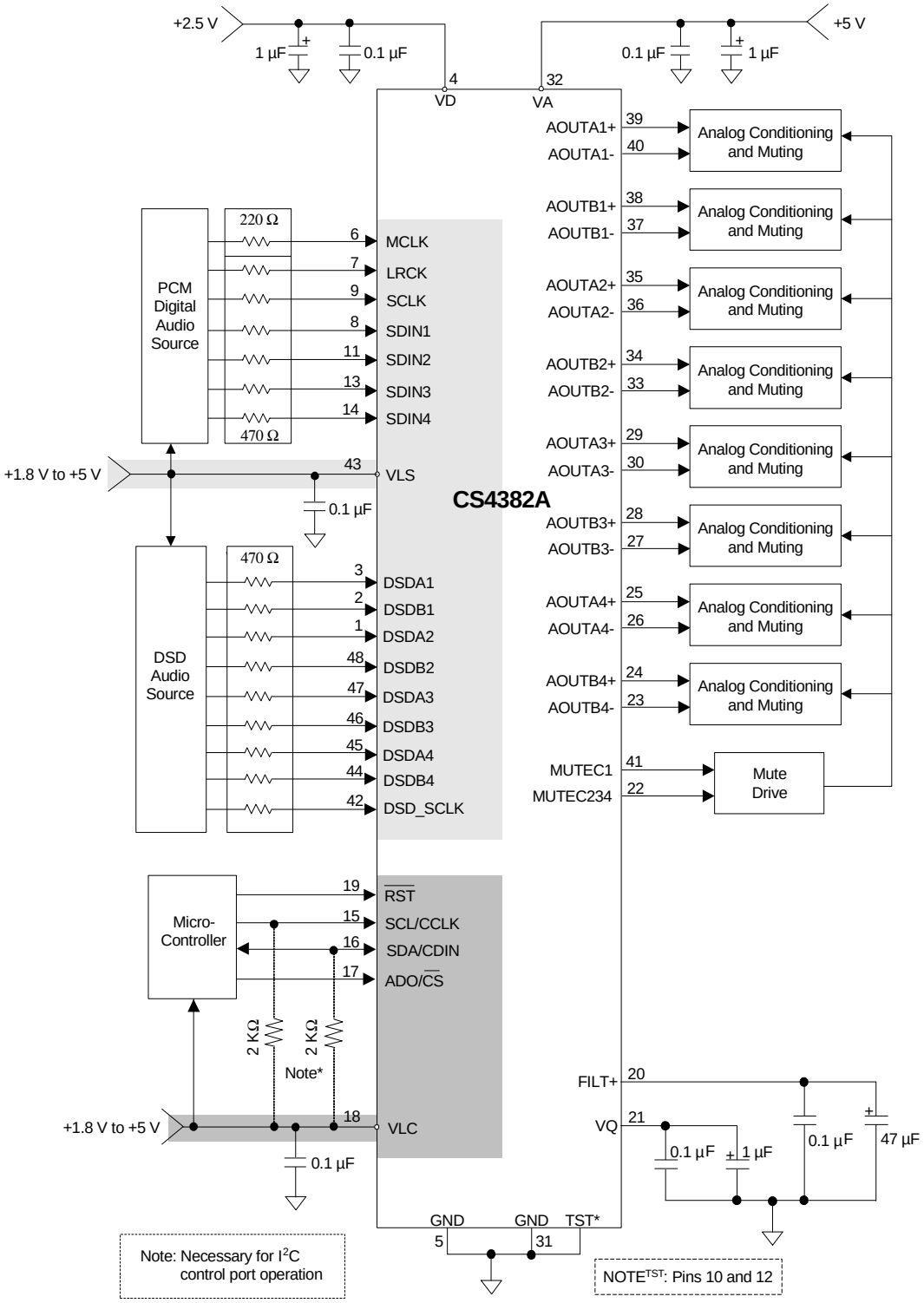


Figure 5. Typical Connection Diagram, Software Mode

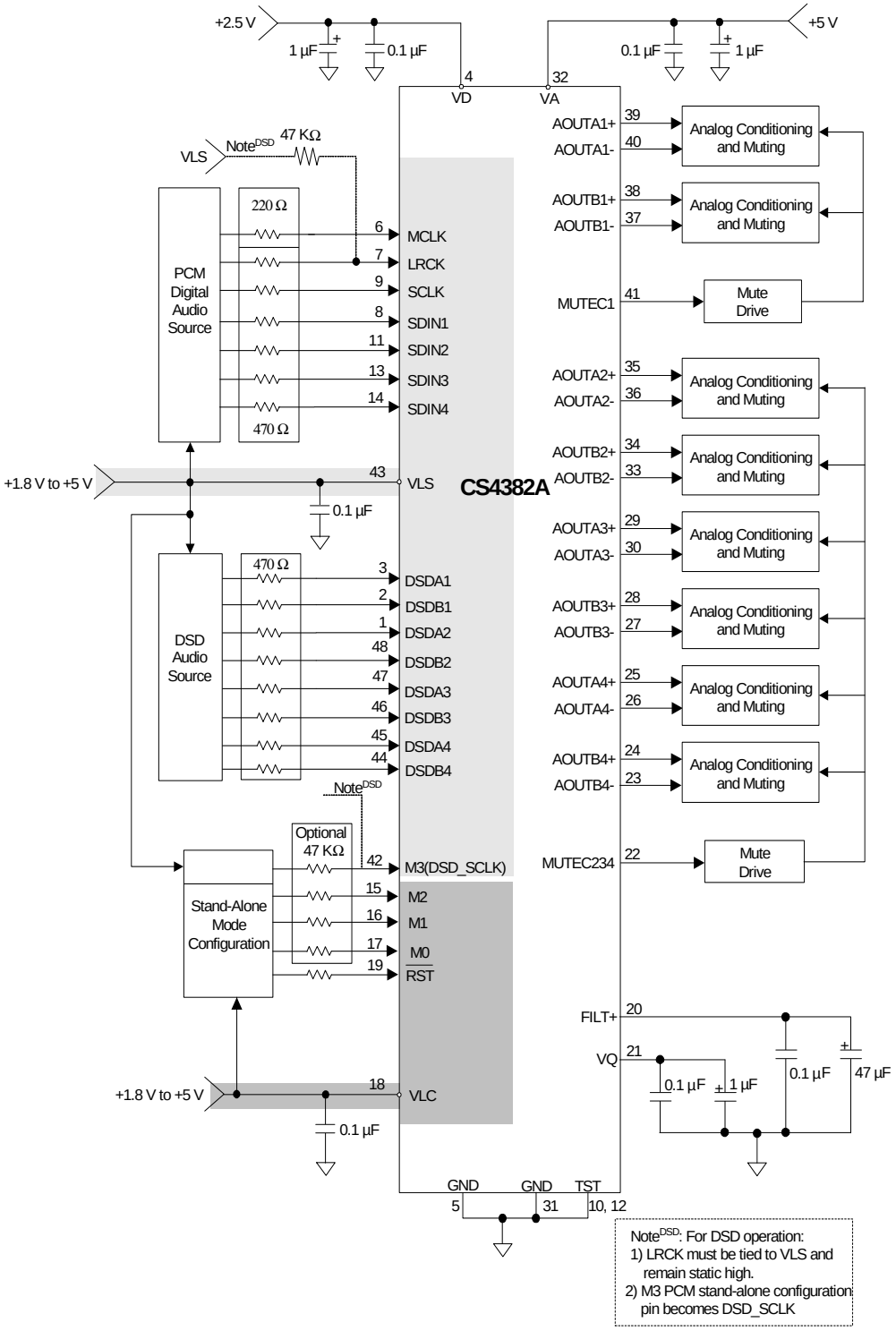


Figure 6. Typical Connection Diagram, Hardware Mode

4. APPLICATIONS

The CS4382A serially accepts two's-complement formatted PCM data at standard audio sample rates including 48, 44.1, and 32 kHz in SSM, 96, 88.2, and 64 kHz in DSM, and 192, 176.4, and 128 kHz in QSM. Audio data is input via the serial data input pins (SDINx). The Left/Right Clock (LRCK) determines which channel is currently being input on SDINx, and the Serial Clock (SCLK) clocks audio data into the input data buffer.

The CS4382A can be configured in Hardware Mode by the M0, M1, M2, M3, and DSD_EN pins and in Software Mode through I²C or SPI.

4.1 Master Clock

MCLK/LRCK must be an integer ratio as shown in Table 1. The LRCK frequency is equal to Fs, the frequency at which words for each channel are input to the device. The MCLK-to-LRCK frequency ratio is detected automatically during the initialization sequence by counting the number of MCLK transitions during a single LRCK period. Internal dividers are then set to generate the proper internal clocks. Table 1 illustrates several standard audio sample rates and the required MCLK and LRCK frequencies. Please note there is no required phase relationship, but MCLK, LRCK, and SCLK must be synchronous.

Speed Mode (sample-rate range)	Sample Rate (kHz)	MCLK (MHz)				Software Mode Only
MCLK Ratio		**256x**	**384x**	**512x**	**768x**	**1024x***
Single-Speed (4 to 50 kHz)	32	8.1920	12.2880	16.3840	24.5760	32.7680
	44.1	11.2896	16.9344	22.5792	33.8688	45.1584
	48	12.2880	18.4320	24.5760	36.8640	49.1520
MCLK Ratio		**128x**	**192x**	**256x**	**384x**	**512x***
Double-Speed (50 to 100 kHz)	64	8.1920	12.2880	16.3840	24.5760	32.7680
	88.2	11.2896	16.9344	22.5792	33.8688	45.1584
	96	12.2880	18.4320	24.5760	36.8640	49.1520
MCLK Ratio		**64x**	**96x**	**128x**	**192x**	**256x***
Quad-Speed (100 to 200 kHz)	176.4	11.2896	16.9344	22.5792	33.8688	45.1584
	192	12.2880	18.4320	24.5760	36.8640	49.1520
Note: These modes are only available in Software Mode by setting the MCLKDIV bit = 1.						

Table 1. Common Clock Frequencies

4.2 Mode Select

In Hardware Mode, operation is determined by the Mode Select pins. The states of these pins are continually scanned for any changes; however, the mode should only be changed while the device is in reset ($\overline{\text{RST}}$ pin low) to ensure proper switching from one mode to another. These pins require connection to supply or ground as outlined in Figure 6. VLC supplies M0, M1, and M2. VLS supplies M3 and DSD_EN. Tables 2 - 4 show the decode of these pins.

In Software Mode, the operational mode and data format are set in the FM and DIF registers. See "Digital Interface Format (DIF)" on page 34 and "Functional Mode (FM)" on page 40.

M1 (DIF1)	M0 (DIF0)	DESCRIPTION	FORMAT	FIGURE
0	0	Left-justified, up to 24-bit data	0	Figure 7
0	1	I²S, up to 24-bit data	1	Figure 8
1	0	Right-justified, 16-bit Data	2	Figure 9
1	1	Right-justified, 24-bit Data	3	Figure 10

Table 2. Digital Interface Format, Stand-Alone Mode Options

M3	M2 (DEM)	DESCRIPTION
0	0	Single-speed without De-emphasis (4 to 50 kHz sample rates)
0	1	Single-speed with 44.1 kHz De-Emphasis; see Figure 13
1	0	Double-speed (50 to 100 kHz sample rates)
1	1	Quad-speed (100 to 200 kHz sample rates)

Table 3. Mode Selection, Stand-Alone Mode Options

DSD_EN (LRCK)	M2	M1	M0	DESCRIPTION
1	0	0	0	64x oversampled DSD data with a 4x MCLK to DSD data rate
1	0	0	1	64x oversampled DSD data with a 6x MCLK to DSD data rate
1	0	1	0	64x oversampled DSD data with a 8x MCLK to DSD data rate
1	0	1	1	64x oversampled DSD data with a 12x MCLK to DSD data rate
1	1	0	0	128x oversampled DSD data with a 2x MCLK to DSD data rate
1	1	0	1	128x oversampled DSD data with a 3x MCLK to DSD data rate
1	1	1	0	128x oversampled DSD data with a 4x MCLK to DSD data rate
1	1	1	1	128x oversampled DSD data with a 6x MCLK to DSD data rate

Table 4. Direct Stream Digital (DSD), Stand-Alone Mode Options

4.3 Digital Interface Formats

The serial port operates as a slave and supports the I²S, Left-justified, and Right-justified digital interface formats with varying bit depths from 16 to 24 as shown in Figures 7-12. Data is clocked into the DAC on the rising edge.

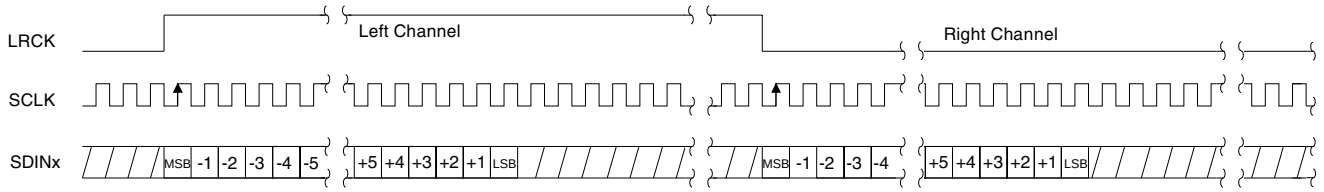


Figure 7. Format 0 - Left-Justified up to 24-bit Data

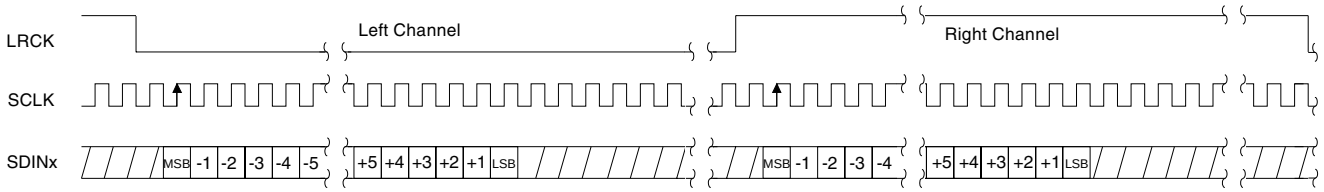


Figure 8. Format 1 - I²S up to 24-bit Data

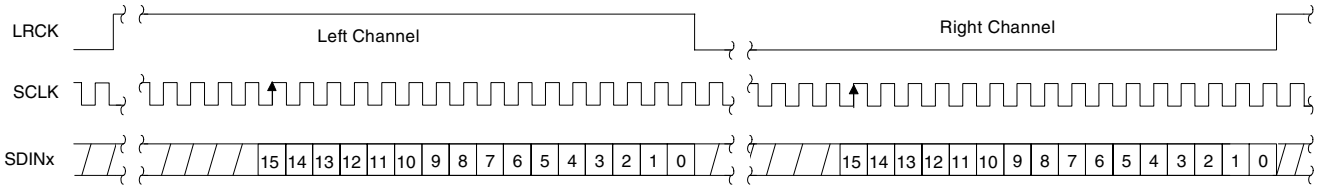


Figure 9. Format 2 - Right-Justified 16-bit Data

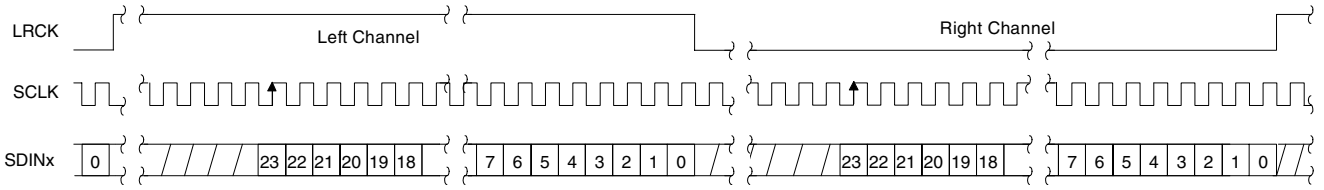


Figure 10. Format 3 - Right-Justified 24-bit Data

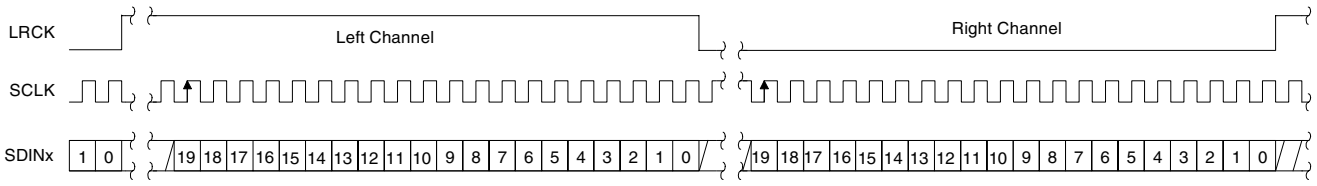


Figure 11. Format 4 - Right-Justified 20-bit Data

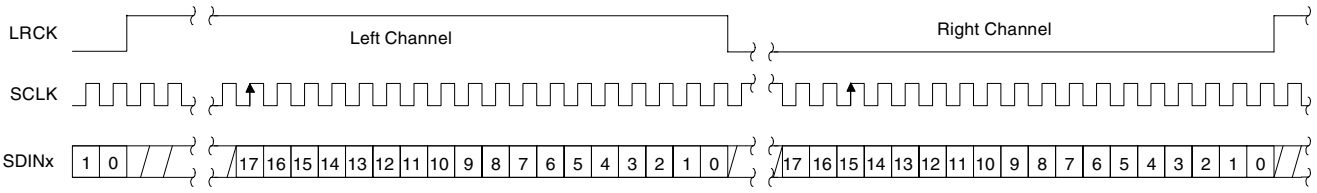


Figure 12. Format 5 - Right-Justified 18-bit Data

4.4 Oversampling Modes

The CS4382A operates in one of three oversampling modes based on the input sample rate. Mode selection is determined by the DSD_EN, M3, and M2 pins in Hardware Mode or the FM bits in Software Mode. Single-speed mode supports input sample rates up to 50 kHz and uses a 128x oversampling ratio. Double-speed Mode supports input sample rates up to 100 kHz and uses an oversampling ratio of 64x. Quad-speed Mode supports input sample rates up to 200 kHz and uses an oversampling ratio of 32x.

4.5 Interpolation Filter

To accommodate the increasingly complex requirements of digital audio systems, the CS4382A incorporates selectable interpolation filters for each mode of operation. A “fast” and a “slow” roll-off filter is available in each of Single, Double, and Quad-Speed modes. These filters have been designed to accommodate a variety of musical tastes and styles. The FILT_SEL bit is used to select which filter is used (see the “Filter Plots” on page 42 for more details).

When in Hardware Mode, only the “fast” roll-off filter is available.

Filter specifications can be found in Section 2, and filter response plots can be found in Figures 19 to 42.

4.6 De-emphasis

The CS4382A includes on-chip digital de-emphasis filters. The de-emphasis feature is included to accommodate older audio recordings that utilize pre-emphasis equalization as a means of noise reduction. Figure 13 shows the de-emphasis curve. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate (Fs) if the input sample rate does not match the coefficient which has been selected.

In Software Mode, the required de-emphasis filter coefficients for 32 kHz, 44.1 kHz, or 48 kHz are selected via the de-emphasis control bits.

In Hardware Mode, only the 44.1 kHz coefficient is available (enabled through the M2 pin). If the input sample rate is not 44.1 kHz and de-emphasis has been selected, the corner frequencies of the de-emphasis filter will be scaled by a factor of the actual Fs over 44,100.

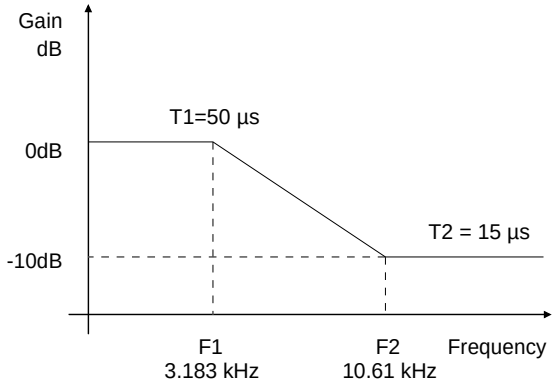


Figure 13. De-Emphasis Curve

4.7 ATAPI Specification

The CS4382A implements the channel mixing functions of the ATAPI CD-ROM specification. The ATAPI functions are applied per A-B pair. Refer to Table 8 on page 41 and Figure 14 for additional information.

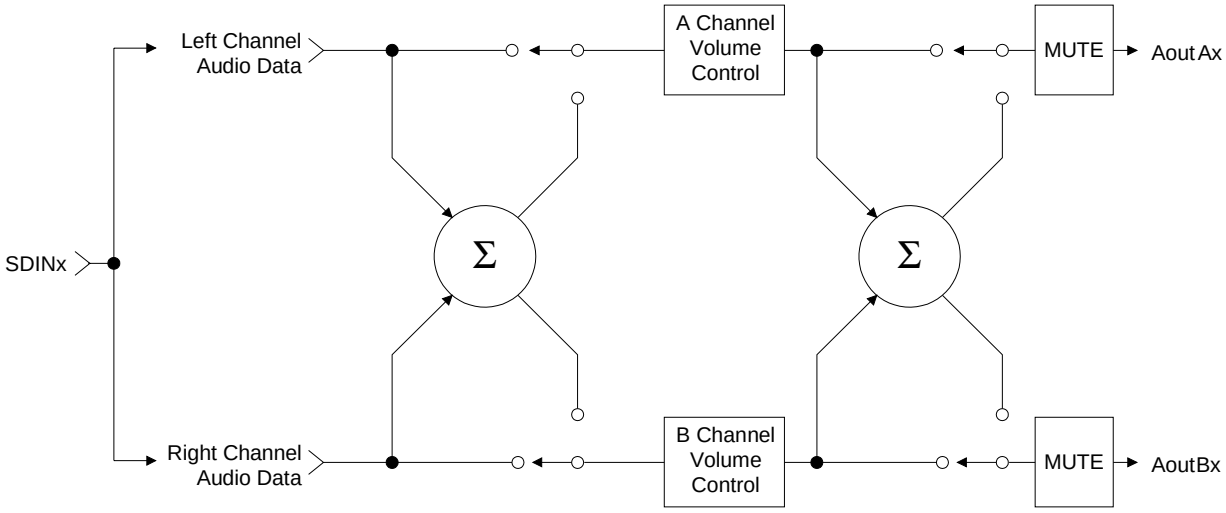


Figure 14. ATAPI Block Diagram (x = channel pair 1, 2, 3, or 4)

4.8 Direct Stream Digital (DSD) Mode

In Stand-alone Mode, DSD operation is selected by holding DSD_EN(LRCK) high and applying the DSD data and clocks to the appropriate pins. The M[2:0] pins set the expected DSD rate and MCLK ratio.

In Control Port Mode, the FM bits set the device into DSD Mode (DSD_EN pin is not required to be held high). The DIF register then controls the expected DSD rate and MCLK ratio.

During DSD operation, the PCM related pins should either be tied low or remain active with clocks (except LRCK in Stand-alone Mode). When the DSD related pins are not being used, they should either be tied static low or remain active with clocks (except M3 in Stand-alone Mode).

4.9 Grounding and Power Supply Arrangements

As with any high-resolution converter, the CS4382A requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. The Typical Connection Diagram shows the recommended power arrangements, with VA, VD, VLC, and VLS connected to clean supplies. If the ground planes are split between digital ground and analog ground, the GND pins of the CS4382A should be connected to the analog ground plane.

All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the DAC.

4.9.1 Capacitor Placement

Decoupling capacitors should be placed as close to the DAC as possible, with the low-value ceramic capacitor being the closest. To further minimize impedance, these capacitors should be located on the same layer as the DAC. If desired, all supply pins with similar voltage ratings may be connected to the same supply, but a decoupling capacitor should still be placed on each supply pin.

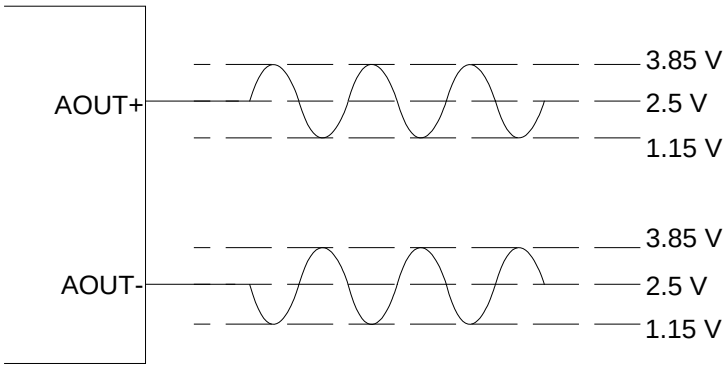
Notes: All decoupling capacitors should be referenced to analog ground.

The CDB4382A evaluation board demonstrates the optimum layout and power supply arrangements.

4.10 Analog Output and Filtering

The application note “Design Notes for a 2-pole Filter with Differential Input” discusses the second-order Butterworth filter and differential-to-single-ended converter which was implemented on the CS4382A evaluation board, CDB4382A, as seen in Figure 16. The CS4382A does not include phase or amplitude compensation for an external filter. Therefore, the DAC system phase and amplitude response will be dependent on the external analog circuitry. The off-chip filter has been designed to attenuate the typical full-scale output level to below 2 Vrms.

Figure 15 shows how the full-scale differential analog output level specification is derived.



Full-Scale Output Level= (AOUT+) - (AOUT-)= 6.7 Vpp

Figure 15. Full-Scale Output

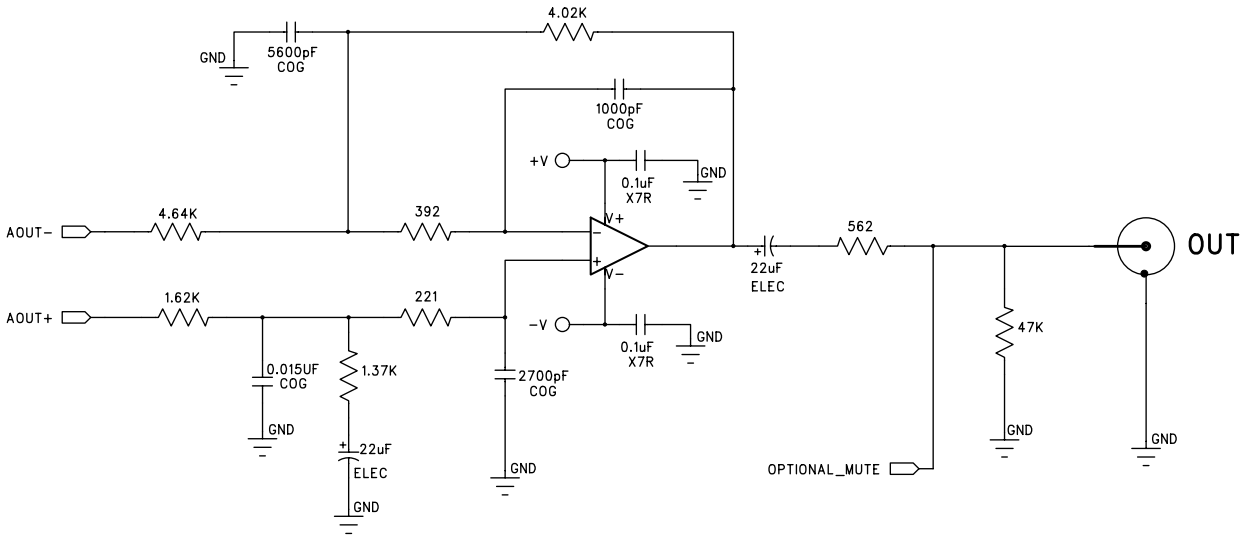


Figure 16. Recommended Output Filter

4.11 Mute Control

The Mute Control pins go active during power-up initialization, reset, muting, or if the MCLK-to-LRCK ratio is incorrect. These pins are intended to be used as control for external mute circuits to prevent the clicks and pops that can occur in any single-ended, single-supply system.

Use of the Mute Control function is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle channel noise/signal-to-noise ratios which are only limited by the external mute circuit. Please see the CDB4382A data sheet for a suggested mute circuit.

4.12 Recommended Power-Up Sequence

4.12.1 Hardware Mode

1. Hold $\overline{\text{RST}}$ low until the power supplies and configuration pins are stable, and the master and left/right clocks are locked to the appropriate frequencies, as discussed in Section 4.1. In this state, the registers are reset to the default settings, FILT+ will remain low, and VQ will be connected to VA/2. If $\overline{\text{RST}}$ can not be held low long enough the SDINx pins should remain static low until all other clocks are stable, and if possible the $\overline{\text{RST}}$ should be toggled low again once the system is stable.
2. Bring $\overline{\text{RST}}$ high. The device will remain in a low power state with FILT+ low and will initiate the Hardware power-up sequence after approximately 512 LRCK cycles in Single-Speed Mode (1024 LRCK cycles in Double-Speed Mode, and 2048 LRCK cycles in Quad-Speed Mode).

4.12.2 Software Mode

1. Hold $\overline{\text{RST}}$ low until the power supply is stable, and the master and left/right clocks are locked to the appropriate frequencies, as discussed in Section 4.1. In this state, the registers are reset to the default settings; FILT+ will remain low, and VQ will be connected to VA/2.
2. Bring $\overline{\text{RST}}$ high. The device will remain in a low-power state with FILT+ low for 512 LRCK cycles in Single-speed Mode (1024 LRCK cycles in Double-speed Mode, and 2048 LRCK cycles in Quad-speed Mode).
3. In order to reduce the chances of clicks and pops, perform a write to the CP_EN bit prior to the completion of approximately 512 LRCK cycles in Single-speed Mode (1024 LRCK cycles in Double-speed Mode, and 2048 LRCK cycles in Quad-speed Mode). The desired register settings can be loaded while keeping the PDN bit set to 1. Set the RMP_UP and RMP_DN bits to 1; then set the format and mode control bits to the desired settings.

   If more than the stated number of LRCK cycles passes before CPEN bit is written, the chip will enter Hardware Mode and begin to operate with the M0-M3 as the mode settings. CPEN bit may be written at anytime, even after the Hardware sequence has begun. It is advised that if the CPEN bit cannot be set in time, the SDINx pins should remain static low (this way, no audio data can be converted incorrectly by the Hardware Mode settings).
4. Set the PDN bit to 0. This will initiate the power-up sequence, which lasts approximately 50 µs.

4.13 Recommended Procedure for Switching Operational Modes

For systems where the absolute minimum in clicks and pops is required, it is recommended that the MUTE bits are set prior to changing significant DAC functions (such as changing sample rates or clock sources). The mute bits may then be released after clocks have settled and the proper modes have been set.

It is required to have the device held in reset if the minimum high/low time specs of MCLK cannot be met during clock source changes.

4.14 Control Port Interface

The Control Port is used to load all the internal register settings in order to operate in Software Mode (see the “Filter Plots” on page 42). The operation of the Control Port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the Control Port pins should remain static if no operation is required.

The Control Port operates in one of two modes: I²C or SPI.

4.14.1 MAP Auto Increment

The device has MAP (memory address pointer) auto-increment capability enabled by the INCR bit (also the MSB) of the MAP. If INCR is set to 0, MAP will stay constant for successive I²C writes or reads and SPI writes. If INCR is set to 1, MAP will auto increment after each byte is written, allowing block reads or writes of successive registers.

4.14.2 I²C Mode

In the I²C Mode, data is clocked into and out of the bi-directional serial control data line, SDA, by the serial Control Port clock, SCL (see Figure 17 for the clock to data relationship). There is no CS pin. Pin AD0 enables the user to alter the chip address (001100[AD0][R/W]) and should be tied to VLC or GND, as required, before powering up the device. If the device ever detects a high-to-low transition on the AD0/CS pin after power-up, SPI Mode will be selected.

4.14.2.1 I²C Write

To write to the device, follow the procedure below while adhering to the Control Port Switching Specifications in Section 2.

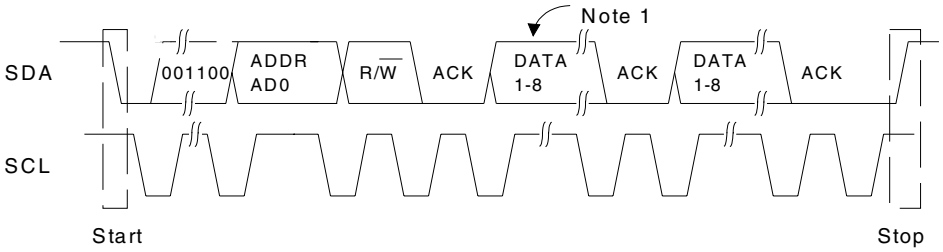
1. Initiate a START condition to the I²C bus followed by the address byte. The upper 6 bits must be 001100. The seventh bit must match the setting of the AD0 pin, and the eighth must be 0. The eighth bit of the address byte is the R/W bit.
2. Wait for an acknowledge (ACK) from the part; then write to the memory address pointer, MAP. This byte points to the register to be written.
3. Wait for an acknowledge (ACK) from the part; then write the desired data to the register pointed to by the MAP.
4. If the INCR bit (see Section 4.14.1) is set to 1, repeat the previous step until all the desired registers are written, then initiate a STOP condition to the bus.
5. If the INCR bit is set to 0 and further I²C writes to other registers are desired, it is necessary to initiate a repeated START condition and follow the procedure detailed from step 1. If no further writes to other registers are desired, initiate a STOP condition to the bus.

4.14.2.2 I²C Read

To read from the device, follow the procedure below while adhering to the Control Port Switching Specifications.

1. Initiate a START condition to the I²C bus followed by the address byte. The upper 6 bits must be 001100. The seventh bit must match the setting of the AD0 pin, and the eighth must be 1. The eighth bit of the address byte is the R/W bit.
2. After transmitting an acknowledge (ACK), the device will then transmit the contents of the register pointed to by the MAP. The MAP register will contain the address of the last register written to the MAP, or the default address (see Section 4.14.1) if an I²C read is the first operation performed on the device.
3. Once the device has transmitted the contents of the register pointed to by the MAP, issue an ACK.
4. If the INCR bit is set to 1, the device will continue to transmit the contents of successive registers. Continue providing a clock and issue an ACK after each byte until all the desired registers are read; then initiate a STOP condition to the bus.
5. If the INCR bit is set to 0 and further I²C reads from other registers are desired, it is necessary to initiate a repeated START condition and follow the procedure detailed from steps 1 and 2 from the I²C Write

instructions followed by step 1 of the I²C Read section. If no further reads from other registers are desired, initiate a STOP condition to the bus.



Note: If operation is a write, this byte contains the Memory Address Pointer, MAP.

Figure 17. Control Port Timing, I²C Mode

4.14.3 SPI Mode

In SPI Mode, data is clocked into the serial control data line, CDIN, by the serial Control Port clock, CCLK (see Figure 18 for the clock-to-data relationship). There is no AD0 pin. Pin $\overline{CS}$ is the chip select signal and is used to control SPI writes to the Control Port. When the device detects a high-to-low transition on the AD0/$\overline{CS}$ pin after power-up, SPI Mode will be selected. All signals are inputs and data is clocked in on the rising edge of CCLK.

4.14.3.1 SPI Write

To write to the device, follow the procedure below while adhering to the Control Port Switching Specifications in Section 2.

1. Bring $\overline{CS}$ low.
2. The address byte on the CDIN pin must then be 00110000.
3. Write to the memory address pointer, MAP. This byte points to the register to be written.
4. Write the desired data to the register pointed to by the MAP.
5. If the INCR bit (see Section 4.14.1) is set to 1, repeat the previous step until all the desired registers are written, then bring $\overline{CS}$ high.
6. If the INCR bit is set to 0 and further SPI writes to other registers are desired, it is necessary to bring $\overline{CS}$ high, and follow the procedure detailed from step 1. If no further writes to other registers are desired, bring $\overline{CS}$ high.

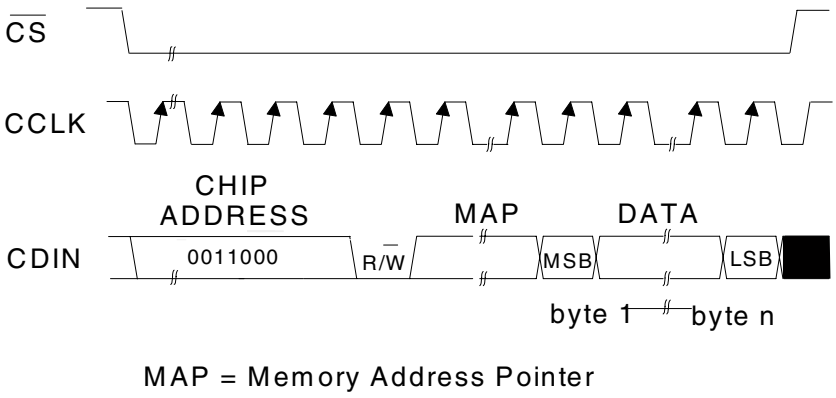


Figure 18. Control Port Timing, SPI Mode

4.15 Memory Address Pointer (MAP)

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	MAP4	MAP3	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	0

4.16 INCR (Auto Map Increment Enable)

Default = '0'
0 - Disabled
1 - Enabled

4.16.1 MAP4-0 (Memory Address Pointer)

Default = '00000'

5. REGISTER QUICK REFERENCE

Addr	Function	7	6	5	4	3	2	1	0
01h	Mode Control 1	CPEN	FREEZE	MCLKDIV	DAC4_DIS	DAC3_DIS	DAC2_DIS	DAC1_DIS	PDN
	default	0	0	0	0	0	0	0	1
02h	Mode Control 2	Reserved	DIF2	DIF1	DIF0	Reserved	Reserved	Reserved	Reserved
	default	0	0	0	0	0	0	0	0
03h	Mode Control 3	SZC1	SZC0	SNGLVOL	RMP_UP	MUTEC+/-	AMUTE	Reserved	MUTEC
	default	1	0	0	0	0	1	0	0
04h	Filter Control	Reserved	Reserved	Reserved	FILT_SEL	Reserved	DEM1	DEM0	RMP_DN
	default	0	0	0	0	0	0	0	0
05h	Invert Control	INV_B4	INV_B3	INV_B3	INV_A3	INV_B2	INV_A2	INV_B1	INV_A1
	default	0	0	0	0	0	0	0	0
06h	Mixing Control Pair 1 (AOUTx1)	P1_A=B	P1ATAPI4	P1ATAPI3	P1ATAPI2	P1ATAPI1	P1ATAPI0	FM1	FM0
	default	0	0	1	0	0	1	0	0
07h	Vol. Control A1	A1_MUTE	A1_VOL6	A1_VOL5	A1_VOL4	A1_VOL3	A1_VOL2	A1_VOL1	A1_VOL0
	default	0	0	0	0	0	0	0	0
08h	Vol. Control B1	B1_MUTE	B1_VOL6	B1_VOL5	B1_VOL4	B1_VOL3	B1_VOL2	B1_VOL1	B1_VOL0
	default	0	0	0	0	0	0	0	0
09h	Mixing Control Pair 2 (AOUTx2)	P2_A=B	P2ATAPI4	P2ATAPI3	P2ATAPI2	P2ATAPI1	P2ATAPI0	Reserved	Reserved
	default	0	0	1	0	0	1	0	0
0Ah	Vol. Control A2	A2_MUTE	A2_VOL6	A2_VOL5	A2_VOL4	A2_VOL3	A2_VOL2	A2_VOL1	A2_VOL0
	default	0	0	0	0	0	0	0	0
0Bh	Vol. Control B2	B2_MUTE	B2_VOL6	B2_VOL5	B2_VOL4	B2_VOL3	B2_VOL2	B2_VOL1	B2_VOL0
	default	0	0	0	0	0	0	0	0
0Ch	Mixing Control Pair 3 (AOUTx3)	P3_A=B	P3ATAPI4	P3ATAPI3	P3ATAPI2	P3ATAPI1	P3ATAPI0	Reserved	Reserved
	default	0	0	1	0	0	1	0	0
0Dh	Vol. Control A3	A3_MUTE	A3_VOL6	A3_VOL5	A3_VOL4	A3_VOL3	A3_VOL2	A3_VOL1	A3_VOL0
	default	0	0	0	0	0	0	0	0
0Eh	Vol. Control B3	B3_MUTE	B3_VOL6	B3_VOL5	B3_VOL4	B3_VOL3	B3_VOL2	B3_VOL1	B3_VOL0
	default	0	0	0	0	0	0	0	0
0Fh	Mixing Control Pair 4 (AOUTx4)	P4_A=B	P4ATAPI4	P4ATAPI4	P4ATAPI2	P4ATAPI1	P4ATAPI0	Reserved	Reserved
	default	0	0	1	0	0	1	0	0
10h	Vol. Control A4	A4_MUTE	A4_VOL6	A4_VOL5	A4_VOL4	A4_VOL3	A4_VOL2	A4_VOL1	A4_VOL0
	default	0	0	0	0	0	0	0	0
11h	Vol. Control B4	B4_MUTE	B4_VOL6	B4_VOL5	B4_VOL4	B4_VOL3	B4_VOL2	B4_VOL1	B4_VOL0
	default	0	0	0	0	0	0	0	0
12h	Chip Revision	PART4	PART3	PART2	PART1	PART0	REV2	REV1	REV0
	default	0	1	1	1	0	x	x	x

6. REGISTER DESCRIPTION

Note: All registers are read/write in I²C Mode and write only in SPI, unless otherwise noted.

6.1 Mode Control 1 (Address 01h)

7	6	5	4	3	2	1	0
CPEN	FREEZE	MCLKDIV	DAC4_DIS	DAC3_DIS	DAC2_DIS	DAC1_DIS	PDN
0	0	0	0	0	0	0	1

6.1.1 Control Port Enable (CPEN)

Default = 0
0 - Disabled
1 - Enabled

Function:

This bit defaults to 0, allowing the device to power-up in Stand-Alone Mode. The Control Port Mode can be accessed by setting this bit to 1. This will allow the operation of the device to be controlled by the registers and the pin definitions will conform to Control Port Mode. To accomplish a clean power-up, the user should write this bit within 10 ms following the release of Reset.

6.1.2 Freeze Controls (FREEZE)

Default = 0
0 - Disabled
1 - Enabled

Function:

This function allows modifications to be made to the registers without the changes taking effect until the FREEZE is disabled. To make multiple changes in the Control Port registers take effect simultaneously, enable the FREEZE Bit, make all register changes, then Disable the FREEZE bit.

6.1.3 Master Clock Divide Enable (MCLKDIV)

Default = 0
0 - Disabled
1 - Enabled

Function:

The MCLKDIV bit enables a circuit which divides the externally applied MCLK signal by 2 prior to all other internal circuitry.

6.1.4 DAC Pair Disable (DACx_DIS)

Default = 0
0 - DAC Pair x Enabled
1 - DAC Pair x Disabled

Function:

When the bit is set, the respective DAC channel pair (AOUTAx and AOUTBx) will remain in a reset state. It is advised that changes to these bits be made while the power-down (PDN) bit is enabled to eliminate the possibility of audible artifacts.

6.1.5 Power Down (PDN)

Default = 1
0 - Disabled
1 - Enabled

Function:

The entire device will enter a low-power state when this function is enabled, and the contents of the control registers are retained in this mode. The power-down bit defaults to 'enabled' on power-up and must be disabled before normal operation in Control Port Mode can occur.

6.2 Mode Control 2 (Address 02h)

7	6	5	4	3	2	1	0
Reserved	DIF2	DIF1	DIF0	Reserved	Reserved	Reserved	Reserved
0	0	0	0	0	0	0	0

6.2.1 Digital Interface Format (DIF)

Default = 000 - Format 0 (Left-Justified, up to 24-bit data)

Function:

These bits select the interface format for the serial audio input. The Functional Mode bits determine whether PCM or DSD Mode is selected.

PCM Mode: The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in Figures 7-12.

Note: While in PCM Mode, the DIF bits should only be changed when the power-down (PDN) bit is set to ensure proper switching from one mode to another.

DIF2	DIF1	DIF0	DESCRIPTION	Format	FIGURE
0	0	0	Left-Justified, up to 24-bit data	0	7
0	0	1	I²S, up to 24-bit data	1	8
0	1	0	Right-Justified, 16-bit data	2	9
0	1	1	Right-Justified, 24-bit data	3	10
1	0	0	Right-Justified, 20-bit data	4	11
1	0	1	Right-Justified, 18-bit data	5	12
1	1	0	Reserved	-	
1	1	1	Reserved	-	

Table 5. Digital Interface Formats - PCM Mode

DSD Mode: The relationship between the oversampling ratio of the DSD audio data and the required master clock-to-DSD-data-rate is defined by the Digital Interface Format pins.

DIF2	DIF1	DIFO	DESCRIPTION
0	0	0	64x oversampled DSD data with a 4x MCLK to DSD data rate
0	0	1	64x oversampled DSD data with a 6x MCLK to DSD data rate
0	1	0	64x oversampled DSD data with a 8x MCLK to DSD data rate
0	1	1	64x oversampled DSD data with a 12x MCLK to DSD data rate
1	0	0	128x oversampled DSD data with a 2x MCLK to DSD data rate
1	0	1	128x oversampled DSD data with a 3x MCLK to DSD data rate
1	1	0	128x oversampled DSD data with a 4x MCLK to DSD data rate
1	1	1	128x oversampled DSD data with a 6x MCLK to DSD data rate

Table 6. Digital Interface Formats - DSD Mode

6.3 Mode Control 3 (Address 03h)

7	6	5	4	3	2	1	0
SZC1	SZC0	SNGLVOL	RMP_UP	MUTEC+/-	AMUTE	Reserved	MUTEC
1	0	0	0	0	1	0	0

6.3.1 Soft Ramp and Zero Cross Control (SZC)

Default = 10
00 - Immediate Change
01 - Zero Cross
10 - Soft Ramp
11 - Soft Ramp on Zero Crossings

Function:

Immediate Change

When Immediate Change is selected, all level changes will take effect immediately in one step.

Zero Cross

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods.

Soft Ramp on Zero Crossing

Soft Ramp and Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

6.3.2 Single Volume Control (SNGLVOL)

Default = 0
0 - Disabled
1 - Enabled

Function:

The individual channel volume levels are independently controlled by their respective Volume Control Bytes when this function is disabled. The volume on all channels is determined by the A1 Channel Volume Control Byte, and the other Volume Control Bytes are ignored when this function is enabled.

6.3.3 Soft Volume Ramp-Up After Error (RMP_UP)

Default = 0
0 - Disabled
1 - Enabled

Function:

An un-mute will be performed after a LRCK/MCLK ratio change or error, and after changing the Functional Mode. When this feature is enabled, this un-mute is affected, similar to attenuation changes, by the Soft and Zero Cross bits in the Mode Control 3 register. When disabled, an immediate un-mute is performed in these instances.

Notes: For best results, it is recommended that this feature be used in conjunction with the RMP_DN bit.

6.3.4 Mutec Polarity (MUTEC+/-)

Default = 0
0 - Active High
1 - Active Low

Function:

The active polarity of the MUTEC pin(s) is determined by this register. When set to 0 (default), the MUTEC pins are high when active. When set to 1 the MUTEC pin(s) are low when active.

Note: When the onboard mute circuitry is designed for active low, the MUTEC outputs will be high (un-muted) for the period of time during reset and before this bit is enabled to 1.

6.3.5 Auto-Mute (AMUTE)

Default = 1
0 - Disabled
1 - Enabled

Function:

The Digital-to-Analog converter output will mute following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting is done independently for each channel. The quiescent voltage on the output will be retained, and the Mute Control pin will go active during the mute period. The muting function is affected, similar to volume control changes, by the Soft and Zero Cross bits in the Mode Control 3 register.

6.3.6 Mutec Pin Control (MUTEC)

Default = 0
0 - Two Mute control signals
1 - Single mute control signal on MUTEC1

Function:

Selects how the internal mute signals are routed to the MUTEC1 and MUTEC234 pins. When set to '0', a logical AND of DAC pair 1 mute control signals are output on MUTEC1 and a logical AND of the mute control signals of DAC pairs 2, 3, and 4 are output on MUTEC234. When set to '1', a logical AND of all DAC pair mute control signals is output on the MUTEC1 pin, MUTEC234 will remain static. For more information on the use of the mute control function see the MUTEC1 and MUTEC234 pins in Section 5.

6.4 Filter Control (Address 04h)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	FILT_SEL	Reserved	DEM1	DEM0	RMP_DN
0	0	0	0	0	0	0	0

6.4.1 Interpolation Filter Select (FILT_SEL)

Default = 0
0 - Fast roll-off
1 - Slow roll-off

Function:

This function allows the user to select whether the interpolation filter has a fast or slow roll off. For filter characteristics, please see Section 2.

6.4.2 De-Emphasis Control (DEM)

Default = 00
00 - Disabled
01 - 44.1 kHz
10 - 48 kHz
11 - 32 kHz

Function:

Selects the appropriate digital filter to maintain the standard 15 µs/50 µs digital de-emphasis filter response at 32, 44.1 or 48 kHz sample rates. (see Figure 13)

De-emphasis is only available in Single-Speed Mode.

6.4.3 Soft Ramp-Down Before Filter Mode Change (RMP_DN)

Default = 0
0 - Disabled
1 - Enabled

Function:

If either the FILT_SEL or DEM bits are changed, the DAC will stop conversion for a period of time to change filter values. This bit selects how the data is effected prior to and after the change of the filter values. When this bit is enabled, the DAC will ramp down the volume prior to a filter-mode change and ramp

from mute to the original volume value after a filter-mode change according to the settings of the Soft and Zero Cross bits in the Mode Control 3 register. When disabled, an immediate mute and unmute is performed.

Loss of clocks or a change in the FM bits will always cause an immediate mute; unmute in these conditions is affected by the RMP_UP bit.

Note: For best results, it is recommended that this feature be used in conjunction with the RMP_UP bit.

6.5 Invert Control (Address 05h)

7	6	5	4	3	2	1	0
INV_B4	INV_A4	INV_B3	INV_A3	INV_B2	INV_A2	INV_B1	INV_A1
0	0	0	0	0	0	0	0

6.5.1 Invert Signal Polarity (Inv_Xx)

Default = 0
0 - Disabled
1 - Enabled

Function:

When enabled, these bits will invert the signal polarity of their respective channels.

6.6 Mixing Control Pair 1 (Channels A1 & B1)(Address 06h)
Mixing Control Pair 2 (Channels A2 & B2)(Address 09h)
Mixing Control Pair 3 (Channels A3 & B3)(Address 0Ch)
Mixing Control Pair 4 (Channels A4 & B4)(Address 0Fh)

7	6	5	4	3	2	1	0
Px_A=B	PxATAPI4	PxATAPI3	PxATAPI2	PxATAPI1	PxATAPI0	PxFM1	PxFM0
0	0	1	0	0	1	0	0

6.6.1 Channel A Volume = Channel B Volume (A=B)

Default = 0
0 - Disabled
1 - Enabled

Function:

The AOUTAx and AOUTBx volume levels are independently controlled by the A and the B Channel Volume Control Bytes when this function is disabled. The volume on both AOUTAx and AOUTBx are determined by the A Channel Attenuation and Volume Control Bytes (per A-B pair), and the B Channel Bytes are ignored when this function is enabled.

6.6.2 ATAPI Channel Mixing and Muting (ATAPI)

Default = 01001 - AOUTAx=aL, AOUTBx=bR (Stereo)

Function:

The CS4382A implements the channel mixing functions of the ATAPI CD-ROM specification. The ATAPI functions are applied per A-B pair. Refer to Table 7 and Figure 14 for additional information.

ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0	AOUTAx	AOUTBx
0	0	0	0	0	MUTE	MUTE
0	0	0	0	1	MUTE	bR
0	0	0	1	0	MUTE	bL
0	0	0	1	1	MUTE	b[(L+R)/2]
0	0	1	0	0	aR	MUTE
0	0	1	0	1	aR	bR
0	0	1	1	0	aR	bL
0	0	1	1	1	aR	b[(L+R)/2]
0	1	0	0	0	aL	MUTE
0	1	0	0	1	aL	bR
0	1	0	1	0	aL	bL
0	1	0	1	1	aL	b[(L+R)/2]
0	1	1	0	0	a[(L+R)/2]	MUTE
0	1	1	0	1	a[(L+R)/2]	bR
0	1	1	1	0	a[(L+R)/2]	bL
0	1	1	1	1	a[(L+R)/2]	b[(L+R)/2]
1	0	0	0	0	MUTE	MUTE
1	0	0	0	1	MUTE	bR
1	0	0	1	0	MUTE	bL
1	0	0	1	1	MUTE	[(aL+bR)/2]
1	0	1	0	0	aR	MUTE
1	0	1	0	1	aR	bR
1	0	1	1	0	aR	bL
1	0	1	1	1	aR	[(bL+aR)/2]
1	1	0	0	0	aL	MUTE
1	1	0	0	1	aL	bR
1	1	0	1	0	aL	bL
1	1	0	1	1	aL	[(aL+bR)/2]
1	1	1	0	0	[(aL+bR)/2]	MUTE
1	1	1	0	1	[(aL+bR)/2]	bR
1	1	1	1	0	[(bL+aR)/2]	bL
1	1	1	1	1	[(aL+bR)/2]	[(aL+bR)/2]

Table 7. ATAPI Decode

6.6.3 Functional Mode (FM)

Default = 00
00 - Single-Speed Mode (4 to 50 kHz sample rates)
01 - Double-Speed Mode (50 to 100 kHz sample rates)
10 - Quad-Speed Mode (100 to 200 kHz sample rates)
11 - Direct Stream Digital Mode

Function:

Selects the required range of input sample rates or DSD Mode. All DAC pairs are required to be set to the same functional mode setting before a speed-mode change is accepted. When DSD Mode is selected for any channel pair, all pairs switch to DSD Mode.

6.7 Volume Control (Addresses 07h, 08h, 0Ah, 0Bh, 0Dh, 0Eh)

7	6	5	4	3	2	1	0
xx_MUTE	xx_VOL6	xx_VOL5	xx_VOL4	xx_VOL3	xx_VOL2	xx_VOL1	xx_VOL0
0	0	0	0	0	0	0	0

Note: These eight registers provide individual volume and mute control for each of the eight channels. The values for “xx” in the bit fields above are as follows:
Register address 07h - xx = A1
Register address 08h - xx = B1
Register address 0Ah - xx = A2
Register address 0Bh - xx = B2
Register address 0Dh - xx = A3
Register address 0Eh - xx = B3
Register address 10h - xx = A4
Register address 11h - xx = B4

6.7.1 Mute (MUTE)

Default = 0
0 - Disabled
1 - Enabled

Function:

The Digital-to-Analog converter output will mute when enabled. The quiescent voltage on the output will be retained. The muting function is affected, similarly to attenuation changes, by the Soft and Zero Cross bits. The MUTE pins will go active during the mute period according to the MUTEC bit.

6.7.2 Volume Control (XX_VOL)

Default = 0 (No attenuation)

Function:

The Digital Volume Control registers allow independent control of the signal levels in 1 dB increments from 0 to -127 dB. Volume settings are decoded as shown in Table 8. The volume changes are implemented as dictated by the Soft and Zero Cross bits. All volume settings less than -127 dB are equivalent to enabling the MUTE bit.

Binary Code	Decimal Value	Volume Setting
0 0 0 0 0 0 0	0	0 dB
0 0 1 0 1 0 0	20	-20 dB
0 1 0 1 0 0 0	40	-40 dB
0 1 1 1 1 0 0	60	-60 dB
1 0 1 1 0 1 0	90	-90 dB

Table 8. Example Digital Volume Settings

6.8 Chip Revision (Address 12h)

7	6	5	4	3	2	1	0
PART4	PART3	PART2	PART1	PART0	REV2	REV1	REV0
0	1	1	1	0	-	-	-

6.8.1 Part Number ID (PART) [Read Only]

01110 - CS4382A

6.8.2 Revision ID (REV) [Read Only]

000 - Revision A
001 - Revision B

Function:

This read-only register can be used to identify the model and revision number of the device.

7. FILTER PLOTS

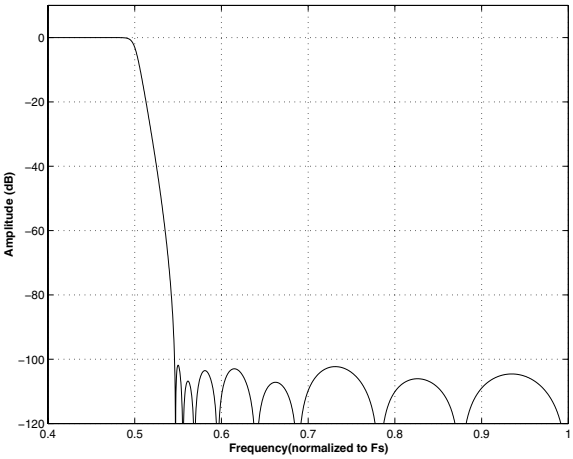


Figure 19. Single-Speed (fast) Stopband Rejection

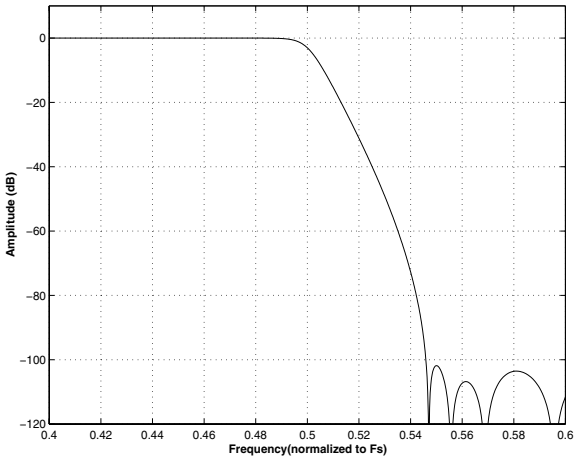


Figure 20. Single-Speed (fast) Transition Band

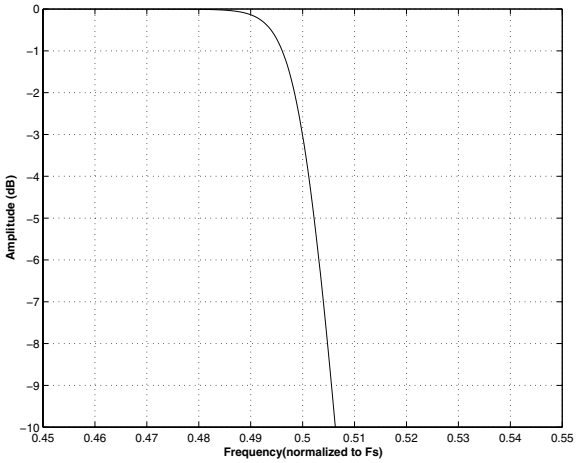


Figure 21. Single-Speed (fast) Transition Band (detail)

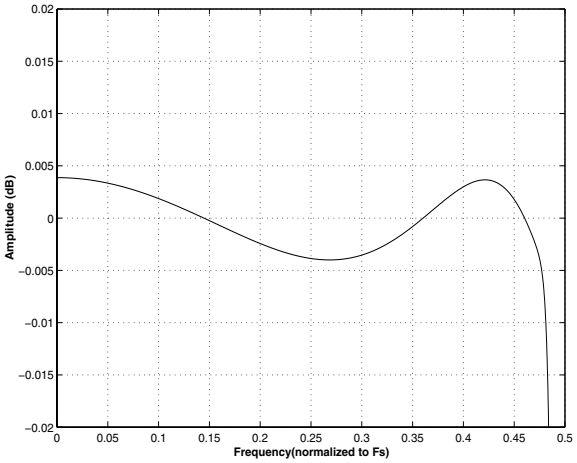


Figure 22. Single-Speed (fast) Passband Ripple

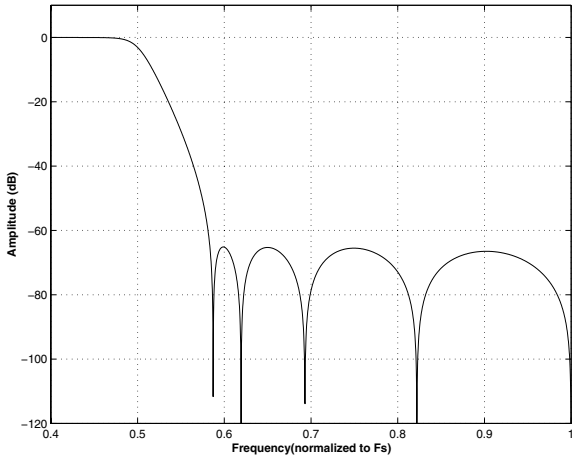


Figure 23. Single-Speed (slow) Stopband Rejection

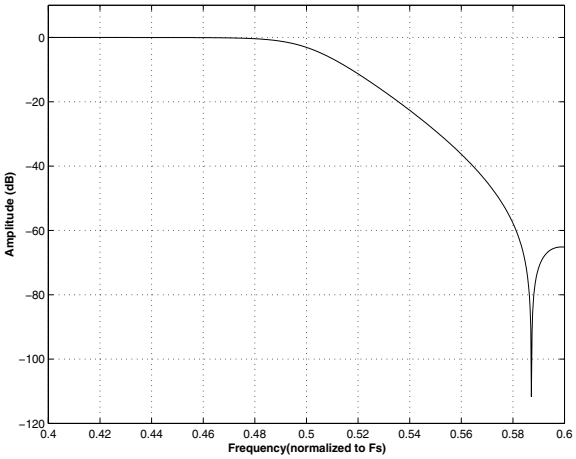


Figure 24. Single-Speed (slow) Transition Band

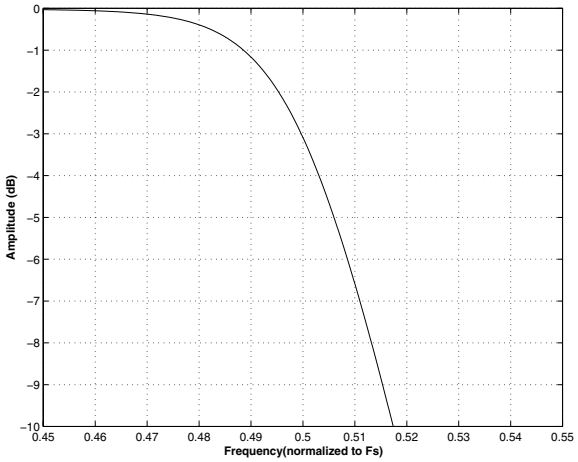


Figure 25. Single-Speed (slow) Transition Band (detail)

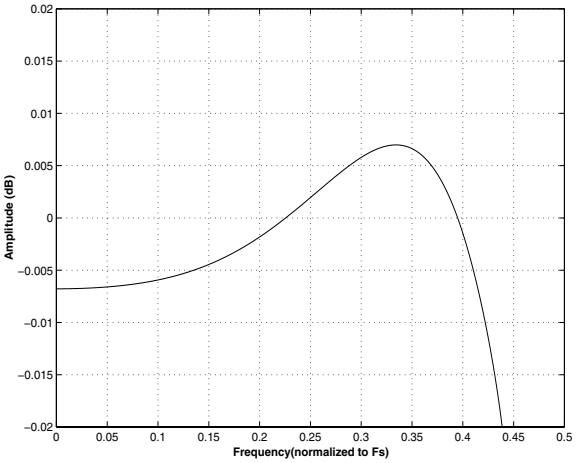


Figure 26. Single-Speed (slow) Passband Ripple

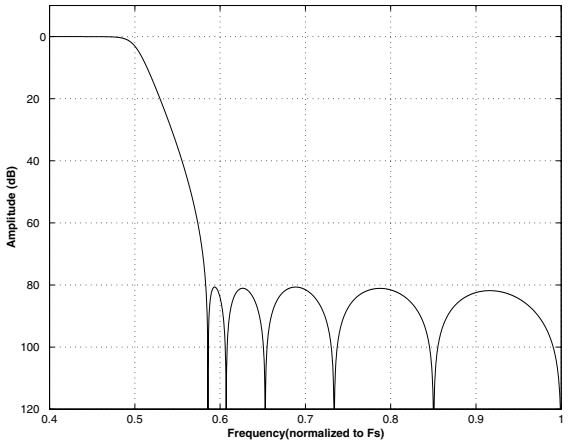


Figure 27. Double-Speed (fast) Stopband Rejection

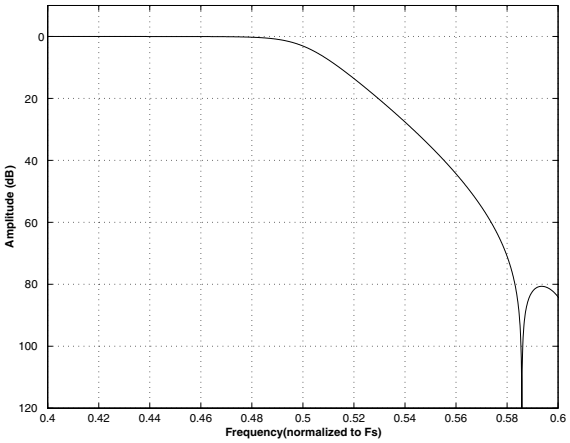


Figure 28. Double-Speed (fast) Transition Band

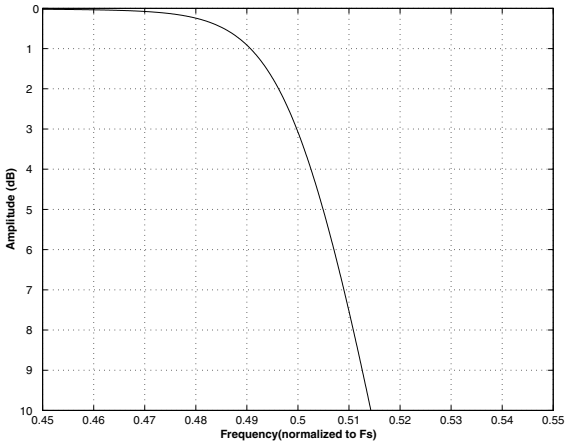


Figure 29. Double-Speed (fast) Transition Band (detail)

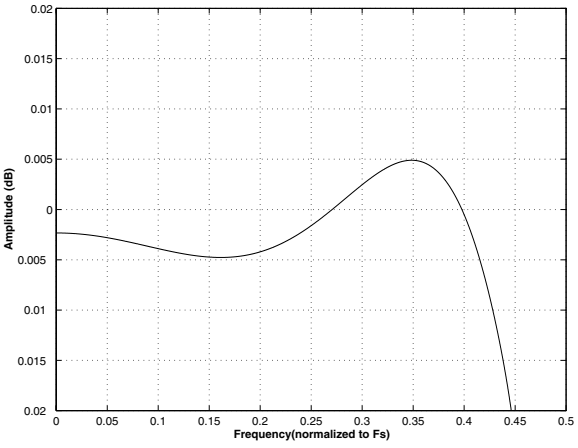


Figure 30. Double-Speed (fast) Passband Ripple

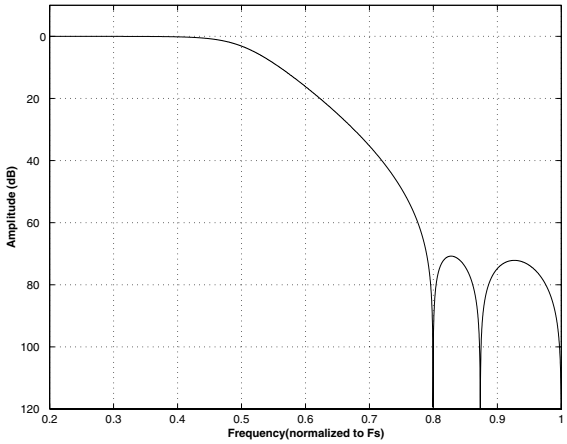


Figure 31. Double-Speed (slow) Stopband Rejection

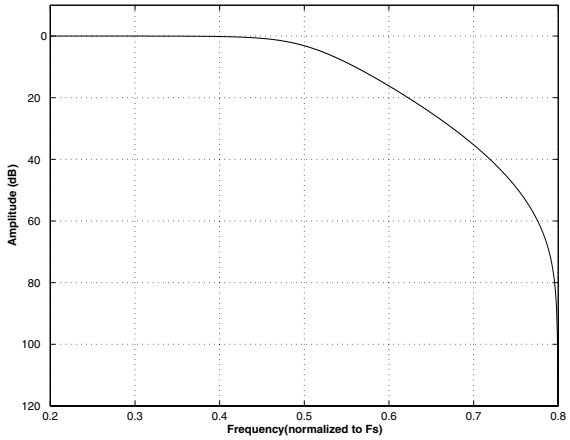


Figure 32. Double-Speed (slow) Transition Band

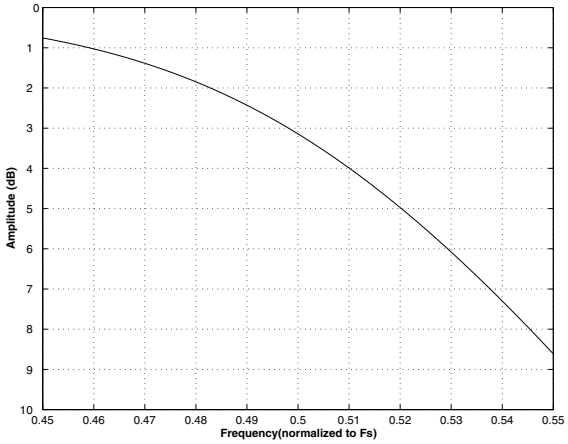


Figure 33. Double-Speed (slow) Transition Band (detail)

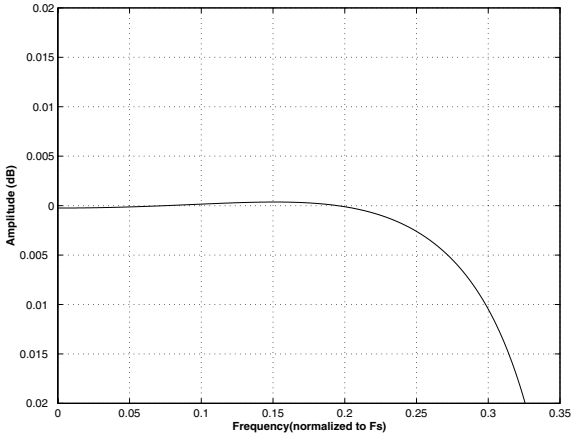


Figure 34. Double-Speed (slow) Passband Ripple

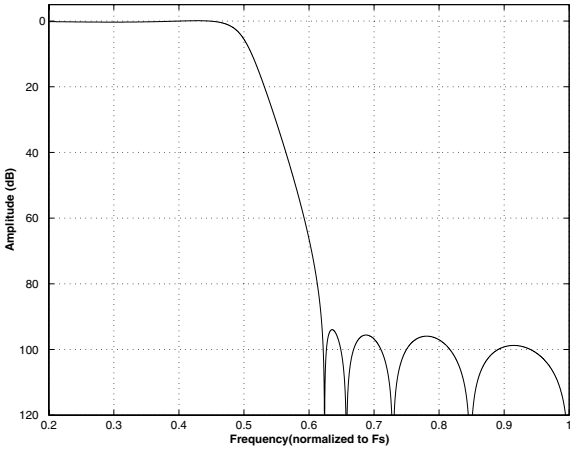


Figure 35. Quad-Speed (fast) Stopband Rejection

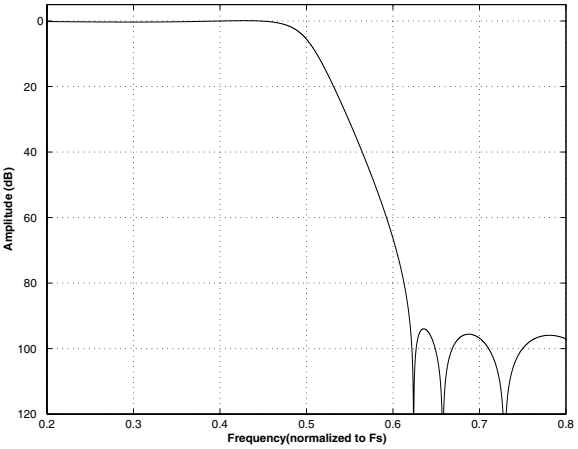


Figure 36. Quad-Speed (fast) Transition Band

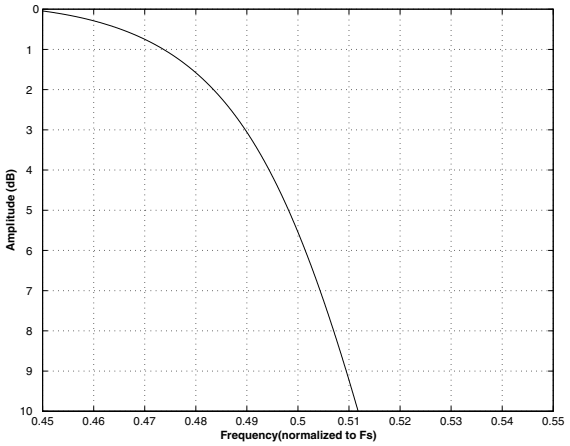


Figure 37. Quad-Speed (fast) Transition Band (detail)

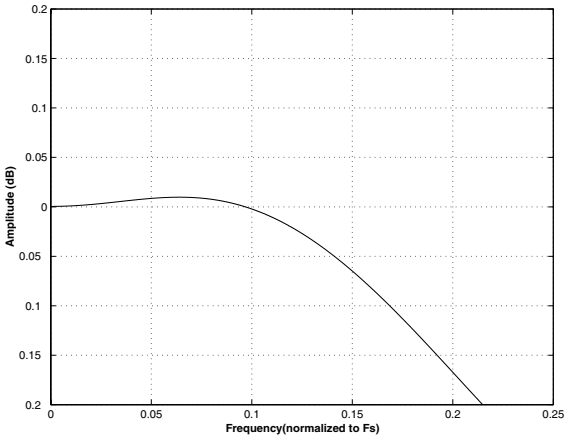


Figure 38. Quad-Speed (fast) Passband Ripple

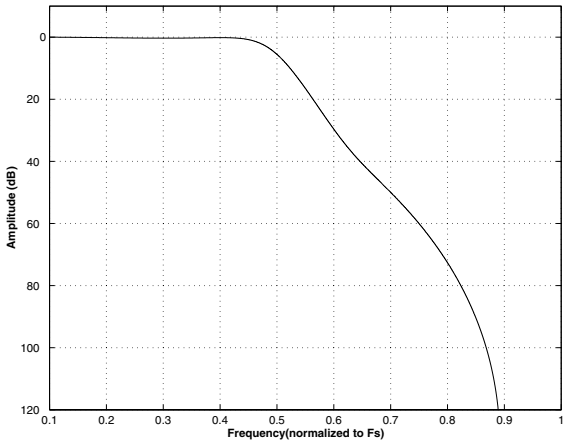


Figure 39. Quad-Speed (slow) Stopband Rejection

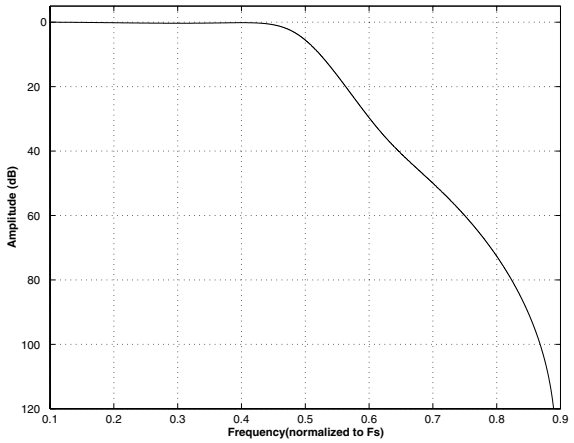


Figure 40. Quad-Speed (slow) Transition Band

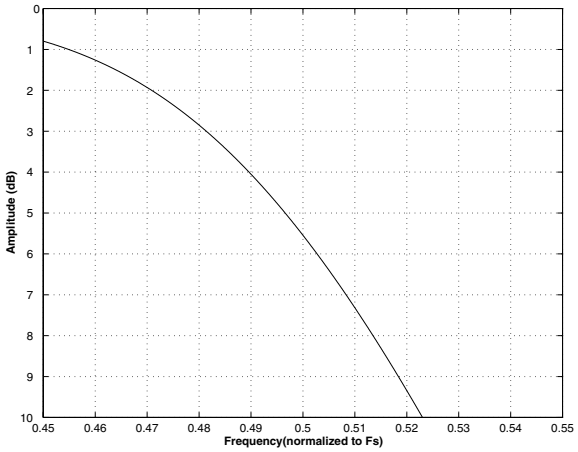


Figure 41. Quad-Speed (slow) Transition Band (detail)

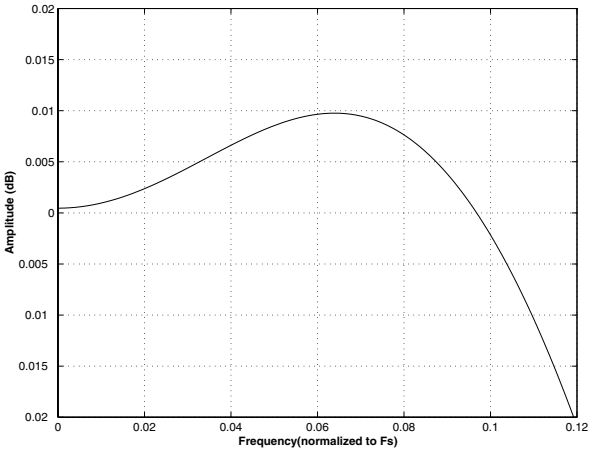


Figure 42. Quad-Speed (slow) Passband Ripple

8. PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Dynamic Range

The ratio of the full-scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

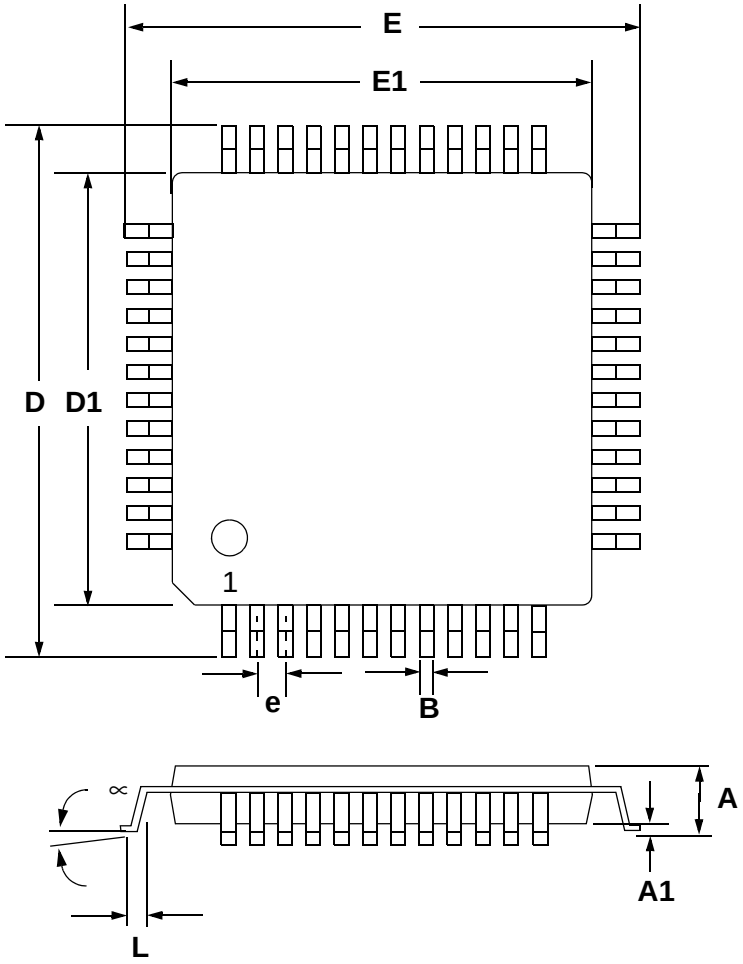
The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

9. PACKAGE DIMENSIONS

48L LQFP PACKAGE DRAWING



	INCHES			MILLIMETERS		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	---	0.055	0.063	---	1.40	1.60
A1	0.002	0.004	0.006	0.05	0.10	0.15
B	0.007	0.009	0.011	0.17	0.22	0.27
D	0.343	0.354	0.366	8.70	9.0 BSC	9.30
D1	0.272	0.28	0.280	6.90	7.0 BSC	7.10
E	0.343	0.354	0.366	8.70	9.0 BSC	9.30
E1	0.272	0.28	0.280	6.90	7.0 BSC	7.10
e*	0.016	0.020	0.024	0.40	0.50 BSC	0.60
L	0.018	0.24	0.030	0.45	0.60	0.75
µ	0.000°	4°	7.000°	0.00°	4°	7.00°

* Nominal pin pitch is 0.50 mm
Controlling dimension is mm.
JEDEC Designation: MS022

10.ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS4382A	114 dB, 192 kHz 8-channel D/A Converter	48-pin LQFP	YES	Commercial	-40°C to +85°C	Tray	CS4382A-CQZ
						Tape & Reel	CS4382A-CQZR
				Automotive	-40°C to +105°C	Tray	CS4382A-DQZ
						Tape & Reel	CS4382A-DQZR
CDB4382A	CS4382A Evaluation Board		-	-	-	-	CDB4382A

11.REFERENCES

1. *How to Achieve Optimum Performance from Delta-Sigma A/D & D/A Converters*, by Steven Harris. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.
2. CDB4382A data sheet, available at http://www.cirrus.com.
3. *Design Notes for a 2-Pole Filter with Differential Input*, by Steven Green. Cirrus Logic Application Note AN48.
4. *The I²C Bus Specification: Version 2.0*, Philips Semiconductors, December 1998 http://www.semiconductors.philips.com.

12.REVISION HISTORY

Release	Changes
PP1	Updated output impedance spec in "DAC Analog Characteristics - Automotive (-DQZ)" on page 10. Improved interchannel isolation spec in "DAC Analog Characteristics - Automotive (-DQZ)" on page 10.
PP2	Corrected package type.
F1	Corrected register description in "DAC Pair Disable (DACx_DIS)" on page 33. Added note to "Digital Interface Format (DIF)" on page 34. Added PCM mode format changeable in reset only to "Mode Select" on page 21. Updated ambient operating temperature range for Commercial and Automotive grade. Updated "DAC Analog Characteristics - Commercial (-CQZ)" on page 9. Updated "DAC Analog Characteristics - Automotive (-DQZ)" on page 10. Updated "Power and Thermal Characteristics" on page 11. Updated "Digital Characteristics" on page 14. Updated Legal Information under "IMPORTANT NOTICE" on page 50

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.

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