CIRRUS LOGIC®
Leading the Digital Entertainment Revolution™

CS4361

20-pin, 24-bit, 192 kHz, 6-channel D/A Converter

Features

- Multi-bit Delta-sigma Modulator
- 24-bit Conversion
- Automatically detects sample rates up to 192 kHz.
- 105 dB Dynamic Range
- -95 dB THD+N
- Low Clock Jitter Sensitivity
- +3.3 V or +5 V Core Power
- +1.8 V to +5 V Interface Power
- Filtered Line Level Outputs
- On-chip Digital De-emphasis
- Popguard™ Technology
- Mute Output Control
- Small 20-pin TSSOP Package

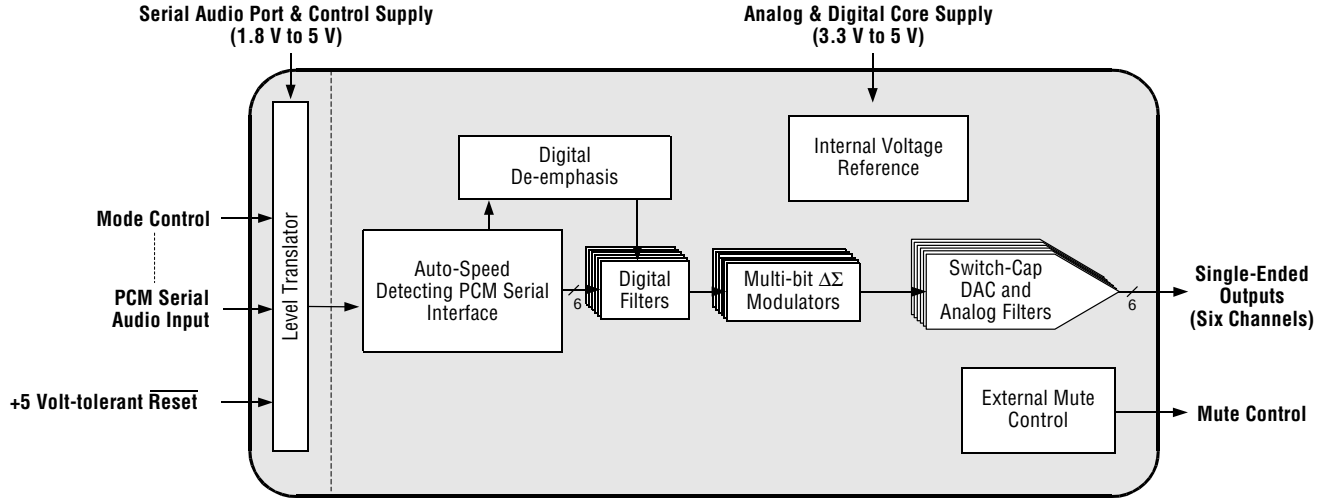
Description

The CS4361 is a complete 6-channel digital-to-analog output system including interpolation, multi-bit D/A conversion, and output analog filtering in a small 20-pin package. The CS4361 supports all major audio data interface formats.

The CS4361 is based on a fourth order, multi-bit, delta-sigma modulator with a linear analog low-pass filter. This device also includes auto-speed mode detection using both sample rate and master clock ratio as a method of auto-selecting sampling rates between 2 kHz and 216 kHz.

The CS4361 contains on-chip digital de-emphasis, operates from a single +3.3 V or +5 V power supply with separate built-in level shifter for the digital interface, and requires minimal support circuitry. These features are ideal for DVD players & recorders, digital televisions, home theater and set top box products, and automotive audio systems.

ORDERING INFORMATION
See page 20



Advance Product Information

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Table 1. Revision History

Release	Date	Changes
A1	January 2005	Initial Release
A2	January 2005	Correction to PDF file size.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to www.cirrus.com

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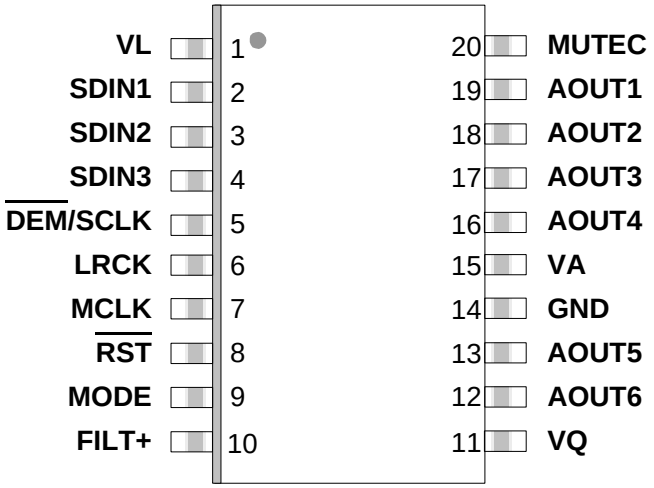
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1. PIN DESCRIPTIONS



Pin Name	#	Pin Description
SDIN1 **SDIN2** **SDIN3**	2 3 4	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
$\overline{\text{DEM}}$/SCLK	5	**De-emphasis/External Serial Clock Input** (*Input*) - used for de-emphasis filter control or external serial clock input.
LRCK	6	**Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	7	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
VQ	11	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
FILT+	10	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
AOUT1 **AOUT2** **AOUT3** **AOUT4** **AOUT5** **AOUT6**	19 18 17 16 13 12	**Analog Output** (*Output*) - The full scale analog output level is specified in the Analog Characteristics specification table.
GND	14	**Ground** (*Input*) - ground reference.
VA	15	**Analog Power** (*Input*) **-** Positive power for the analog and core digital sections.
VL	1	**Interface Power** (*Input*) **-** Positive power for the digital interface level shifters.
$\overline{\text{RST}}$	8	**$\overline{\text{Reset}}$** (*Input*) **-** Applies reset to the internal circuitry when low.
MUTEC	20	**Mute Control** (*Output*) **-** Control signal for optional external muting circuitry.
MODE	9	**Mode Control** (*Input*) **-** Selects operational modes (see table 3).

2.CHARACTERISTICS AND SPECIFICATIONS

All Min/Max characteristics and specifications are guaranteed over the specified operating conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltage and T_A = 25°C.

SPECIFIED OPERATING CONDITIONS

AGND = 0 V; all voltages with respect to ground.

Parameters		Symbol	Min	Nom	Max	Units
DC Power Supply		VA VA VL	4.75 3.0 1.7	5.0 3.3 3.3	5.25 3.6 5.25	V V
Specified Temperature Range	-CZZ -DZZ	T_A	-10 -40	- -	+70 +85	°C °C

ABSOLUTE MAXIMUM RATINGS

AGND = 0 V; all voltages with respect to ground.

Parameters	Symbol	Min	Max	Units
DC Power Supply	VA VL	-0.3 -0.3	6.0 VA	V V
Input Current, Any Pin Except Supplies	I_{in}	-	±10	mA
Digital Input Voltage (pin 8, $\overline{RST}$)	V_{IND}	-0.3	VA+0.4	V
Digital Input Voltage (all other digital pins)	V_{IND}	-0.3	VL+0.4	V
Ambient Operating Temperature (power applied)	T_{op}	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

DAC ANALOG CHARACTERISTICS

Full-scale output sine wave, 997 Hz (Note 1), Fs = 48/96/192 kHz; Test load R_L = 3 kΩ, C_L = 10 pF (see Figure 1). Measurement bandwidth is 10 Hz to 20 kHz, unless otherwise specified.

Parameter			5 V Nom			3.3 V Nom			Unit
			Min	Typ	Max	Min	Typ	Max	
Dynamic Performance for CS4361-CZZ (-10 to 70°C)									
Dynamic Range	18 to 24-Bit	A-weighted	99	105	-	97	103	-	dB
		unweighted	96	102	-	94	100	-	dB
	16-Bit	A-weighted	90	96	-	90	96	-	dB
		unweighted	87	93	-	87	93	-	dB
Total Harmonic Distortion + Noise									
	18 to 24-Bit	0 dB	-	-95	-89	-	-95	-89	dB
		-20 dB	-	-82	-76	-	-80	-74	dB
		-60 dB	-	-42	-36	-	-40	-34	dB
	16-Bit	0 dB	-	-93	-87	-	-93	-87	dB
		-20 dB	-	-73	-67	-	-73	-67	dB
		-60 dB	-	-33	-27	-	-33	-27	dB
Dynamic Performance for CS4361-DZZ (-40 to 85°C)									
Dynamic Range	18 to 24-Bit	A-weighted	95	105	-	93	103	-	dB
		unweighted	92	102	-	90	100	-	dB
	16-Bit	A-weighted	86	96	-	86	96	-	dB
		unweighted	83	93	-	83	93	-	dB
Total Harmonic Distortion + Noise									
	18 to 24-Bit	0 dB	-	-95	-85	-	-95	-85	dB
		-20 dB	-	-82	-72	-	-80	-70	dB
		-60 dB	-	-42	-32	-	-40	-30	dB
	16-Bit	0 dB	-	-93	-83	-	-93	-83	dB
		-20 dB	-	-73	-63	-	-73	-63	dB
		-60 dB	-	-33	-23	-	-33	-23	dB

Note: 1. One-half LSB of triangular PDF dither added to data.

DAC ANALOG CHARACTERISTICS - ALL MODES

Parameter	Symbol	Min	Typ	Max	Unit
Interchannel Isolation (1 kHz)		-	100	-	dB
DC Accuracy					
Interchannel Gain Mismatch		-	0.1	0.25	dB
Gain Drift		-	100	-	ppm/°C
Analog Output					
Full Scale Output Voltage		0.60•VA	0.65•VA	0.70•VA	Vpp
Quiescent Voltage	V_Q	-	0.5•VA	-	VDC
Max DC Current draw from an AOUT pin	I_{OUTmax}	-	10	-	µA
Max Current draw from VQ	I_{Qmax}	-	100	-	µA
Min AC-Load Resistance (see Figure 2 on page 8)	R_L	-	3	-	kΩ
Max Load Capacitance (see Figure 2)	C_L	-	100	-	pF
Output Impedance	Z_{OUT}	-	100	-	Ω

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs. (See note 5)

Parameter		Symbol	Min	Typ	Max	Unit
Combined Digital and On-chip Analog Filter Response			***Single Speed Mode***			
Passband (Note 2)	to -0.05 dB corner to -3 dB corner		0 0	- -	.4780 .4996	Fs Fs
Frequency Response 10 Hz to 20 kHz			-.01	-	+.08	dB
StopBand			.5465	-	-	Fs
StopBand Attenuation	(Note 3)		50	-	-	dB
Group Delay		tgd	-	10/Fs	-	s
De-emphasis Error (Note 4)	Fs = 44.1 kHz		-	-	+.05/-.25	dB
Combined Digital and On-chip Analog Filter Response			***Double Speed Mode***			
Passband (Note 2)	to -0.1 dB corner to -3 dB corner		0 0	- -	.4650 .4982	Fs Fs
Frequency Response 10 Hz to 20 kHz			-.05	-	+.2	dB
StopBand			.5770	-	-	Fs
StopBand Attenuation	(Note 3)		55	-	-	dB
Group Delay		tgd	-	5/Fs	-	s
Combined Digital and On-chip Analog Filter Response			***Quad Speed Mode***			
Passband (Note 2)	to -0.1 dB corner to -3 dB corner		0 0	- -	0.397 0.476	Fs Fs
Frequency Response 10 Hz to 20 kHz			0	-	+0.00004	dB
StopBand			0.7	-	-	Fs
StopBand Attenuation	(Note 3)		51	-	-	dB
Group Delay		tgd	-	2.5/Fs	-	s

Notes:
2. Response is clock-dependent and will scale with Fs.
3. For Single Speed Mode, the measurement bandwidth is 0.5465 Fs to 3 Fs.
   For Double Speed Mode, the measurement bandwidth is 0.577 Fs to 1.4 Fs.
   For Quad Speed Mode, the measurement bandwidth is 0.7 Fs to 1 Fs.
4. De-emphasis is available only in Single Speed Mode.
5. Amplitude vs. Frequency plots of this data are available in “Appendix” on page 21.

DIGITAL INPUT CHARACTERISTICS

Parameters	Symbol	Min	Typ	Max	Units
High-Level Input Voltage -all input Pins except RST (% of VL)	V_{IH}	70%	-	-	V
Low-Level Input Voltage -all input Pins except RST (% of VL)	V_{IL}	-	-	30%	V
High-Level Input Voltage -RST pin (Note 6) (% of VL)	V_{IH}	90%	-	-	V
Low-Level Input Voltage -RST pin (% of VL)	V_{IL}	-	-	10%	V
Input Leakage Current (Note 7)	I_{in}	-	-	±10	µA
Input Capacitance		-	8	-	pF

6. RST pin has an input threshold relative to VL but is VA tolerant.
7. I_{in} for LRCK is ±20 µA max.

POWER & THERMAL CHARACTERISTICS

Parameters	Symbol	5 V Nom			3.3 V Nom			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supplies								
Power Supply Current normal operation	I_A	-	66	90	-	48	63	mA
(Note 8)	I_L	-	0.1	1	-	0.1	1	mA
power-down state (Note 9)	I_A	-	300	-	-	180	-	µA
	I_L	-	26	-	-	24	-	µA
Power Dissipation normal operation		-	331	455	-	159	211	mW
power-down state (Note 9)		-	1.63	-	-	0.67	-	mW
Package Thermal Resistance	θ_{JA}	-	72	-	-	72	-	°C/Watt
Power Supply Rejection Ratio (Note 10) (1 kHz)	PSRR	-	60	-	-	60	-	dB
(60 Hz)		-	40	-	-	40	-	dB

8. Current consumption increases with increasing FS and increasing MCLK. Typ and Max values are based on highest FS and highest MCLK. Current variance between speed modes is small.
9. Power down mode is defined when all clock and data lines are held static.
10. Valid with the recommended capacitor values on VQ and FILT+ as shown in the typical connection diagram in Section 3.

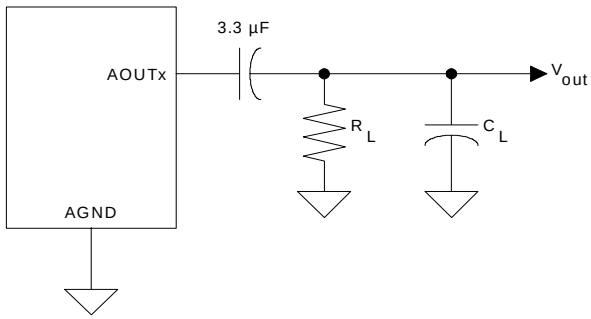


Figure 1. Equivalent Output Test Load

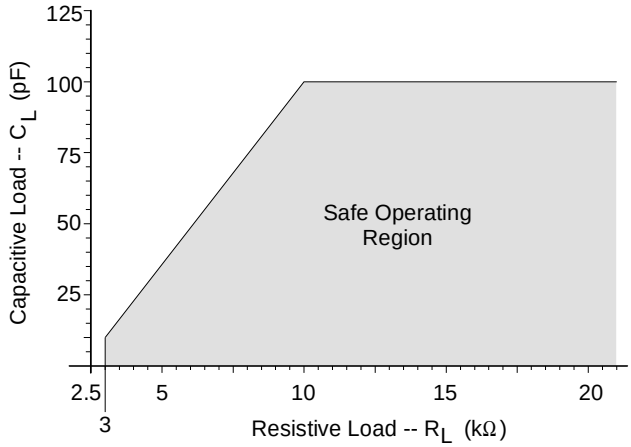


Figure 2. Maximum Loading

SWITCHING CHARACTERISTICS - SERIAL AUDIO INTERFACE

Parameters	Symbol	Min	Typ	Max	Units
MCLK Frequency		0.512	-	50	MHz
MCLK Duty Cycle		45	-	55	%
Input Sample Rate All MCLK/LRCK ratios combined	Fs	2		216	kHz
(Note 11) 256x, 384x, 1024x		2		54	kHz
256x, 384x		84		134	kHz
512x, 768x		42		67	kHz
1152x		30		34	kHz
128x, 192x		50		108	kHz
64x, 96x		100		216	kHz
128x, 192x		168		216	kHz
External SCLK Mode					
LRCK Duty Cycle (External SCLK only)		45	50	55	%
SCLK Pulse Width Low	t_{sclkl}	20	-	-	ns
SCLK Pulse Width High	t_{sclkh}	20	-	-	ns
SCLK Duty Cycle		45	50	55	%
SCLK rising to LRCK edge delay	t_{slrd}	20	-	-	ns
SCLK rising to LRCK edge setup time	t_{slrs}	20	-	-	ns
SDIN valid to SCLK rising setup time	t_{sdlrs}	20	-	-	ns
SCLK rising to SDIN hold time	t_{sdh}	20	-	-	ns
Internal SCLK Mode					
LRCK Duty Cycle (Internal SCLK only) (Note 12)		-	50	-	%
SCLK Period (Note 13)	t_{sclkw}	$\frac{10^9}{SCLK}$	-	-	ns
SCLK rising to LRCK edge	t_{sclkr}	-	$\frac{tsclkw}{2}$	-	µs
SDIN valid to SCLK rising setup time	t_{sdlrs}	$\frac{10^9}{(512)Fs} + 10$	-	-	ns
SCLK rising to SDIN hold time MCLK / LRCK =1152, 1024, 512, 256, 128, or 64	t_{sdh}	$\frac{10^9}{(512)Fs} + 15$	-	-	ns
SCLK rising to SDIN hold time MCLK / LRCK = 768, 384, 192, or 96	t_{sdh}	$\frac{10^9}{(384)Fs} + 15$	-	-	ns

Notes: 11. Not all sample rates are supported for all clock ratios. See table “Common Clock Frequencies” on page 12 for supported ratios and frequencies.

12. In Internal SCLK Mode, the duty cycle must be 50% ± 1/2 MCLK period.

13. The SCLK / LRCK ratio may be either 32, 48, 64, or 72. This ratio depends on data format and MCLK/LRCK ratio. (See figures 7-10)

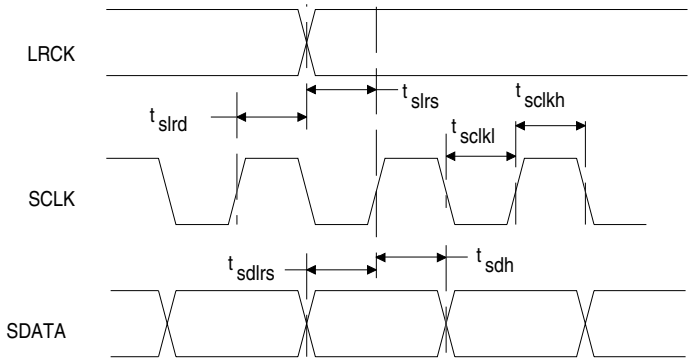


Figure 3. External Serial Mode Input Timing

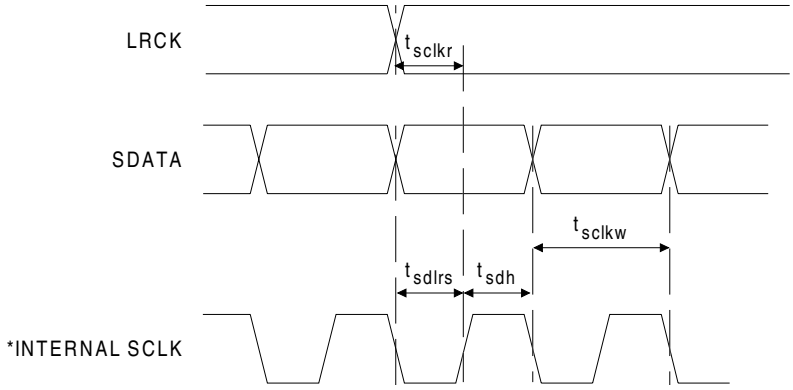


Figure 4. Internal Serial Mode Input Timing

* The SCLK pulses shown are internal to the CS4361.

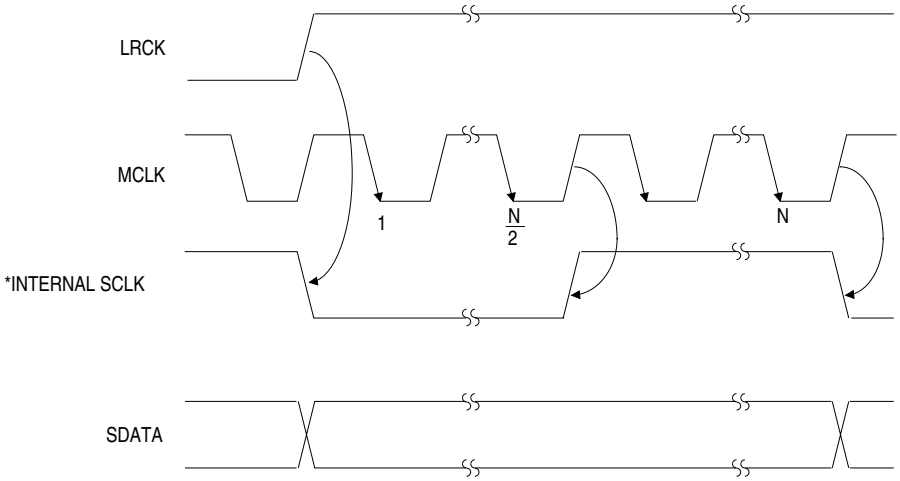


Figure 5. Internal Serial Clock Generation

* The SCLK pulses shown are internal to the CS4361.

N equals MCLK divided by SCLK

3. TYPICAL CONNECTION DIAGRAM

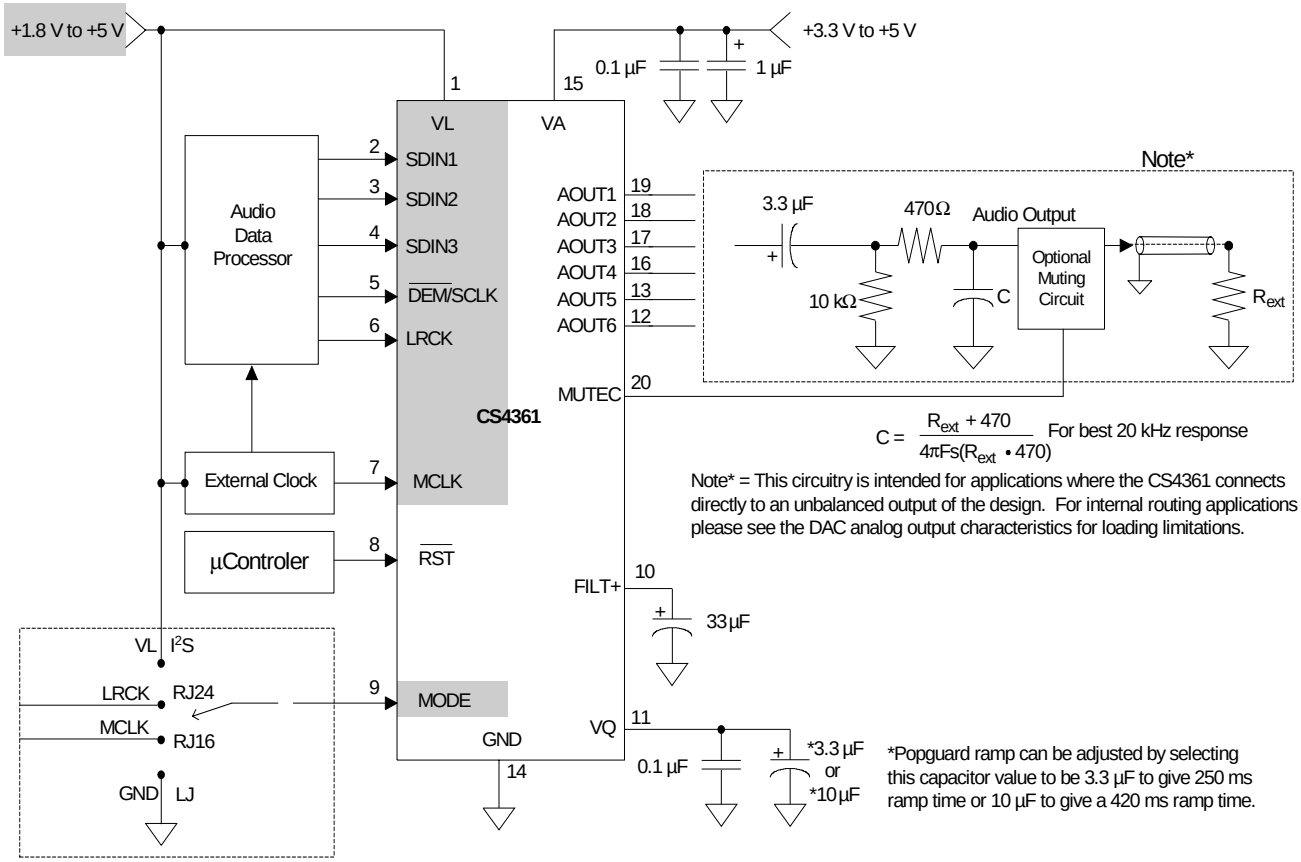


Figure 6. Recommended Connection Diagram

4.APPLICATIONS

The CS4361 accepts data at standard audio sample rates including 48, 44.1 and 32 kHz in SSM, 96, 88.2 and 64 kHz in DSM, and 192, 176.4 and 128 kHz in QSM. Audio data is input via the serial data input pin (SDIN). The Left/Right Clock (LRCK) determines which channel is currently being input on SDIN, and the optional Serial Clock (SCLK) clocks audio data into the input data buffer.

4.1 Master Clock

MCLK/LRCK must be an integer ratio as shown in Table 2. The LRCK frequency is equal to Fs, the frequency at which words for each channel are input to the device. The MCLK-to-LRCK frequency ratio and speed mode is detected automatically during the initialization sequence by counting the number of MCLK transitions during a single LRCK period and by detecting the absolute speed of MCLK. Internal dividers are set to generate the proper clocks. Table 2 illustrates several standard audio sample rates and the required MCLK and LRCK frequencies. Please note there is no required phase relationship, but MCLK, LRCK, and SCLK must be synchronous.

LRCK (kHz)	MCLK (MHz)									
	64x	96x	128x	192x	256x	384x	512x	768x	1024x	1152x
32	-	-	-	-	8.1920	12.2880	-	-	32.7680	36.8640
44.1	-	-	-	-	11.2896	16.9344	22.5792	33.8680	45.1580	-
48	-	-	-	-	12.2880	18.4320	24.5760	36.8640	49.1520	-
64	-	-	8.1920	12.2880	-	-	32.7680	49.1520	-	-
88.2	-	-	11.2896	16.9344	22.5792	33.8680	-	-	-	-
96	-	-	12.2880	18.4320	24.5760	36.8640	-	-	-	-
128	8.1920	12.2880	-	-	32.7680	49.1520	-	-	-	-
176.4	11.2896	16.9344	22.5792	33.8680	-	-	-	-	-	-
192	12.2880	18.4320	24.5760	36.8640	-	-	-	-	-	-
Mode	QSM				DSM		SSM			

Table 2. Common Clock Frequencies

4.2 Serial Clock

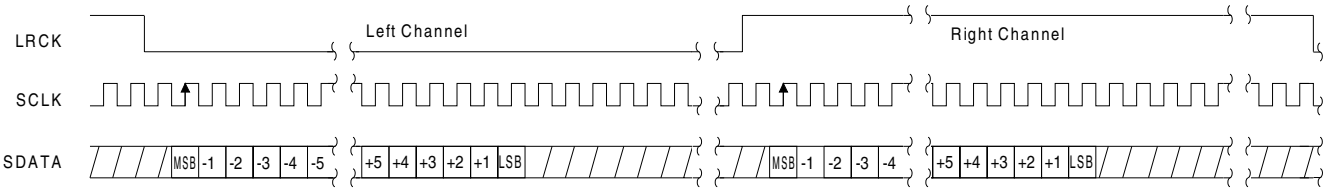
The serial clock controls the shifting of data into the input data buffers. The CS4361 supports both external and internal serial clock generation modes. Refer to Figures 7-10 for data formats.

4.2.1 External Serial Clock Mode

The CS4361 will enter the External Serial Clock Mode when 16 low-to-high transitions are detected on the DEM/SCLK pin during any phase of the LRCK period. When this mode is enabled, the Internal Serial Clock Mode and de-emphasis filter cannot be accessed. The CS4361 will switch to Internal Serial Clock Mode if no low-to-high transitions are detected on the DEM/SCLK pin for two consecutive frames of LRCK. Refer to Figure 12.

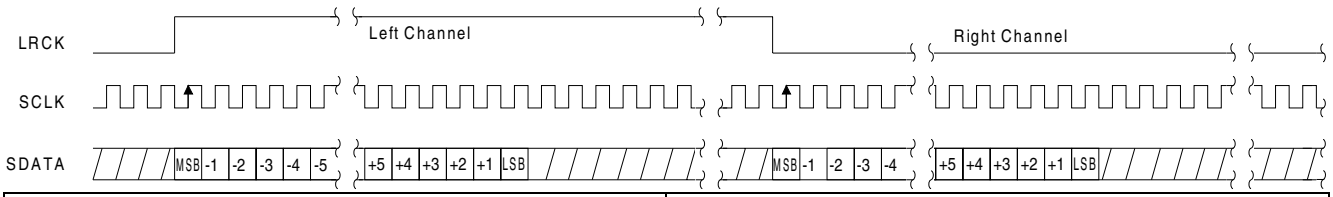
4.2.2 Internal Serial Clock Mode

In the Internal Serial Clock Mode, the serial clock is internally derived and synchronous with MCLK and LRCK. The SCLK/LRCK frequency ratio is either 32, 48, 64, or 72 depending upon data format. Operation in this mode is identical to operation with an external serial clock synchronized with LRCK. This mode allows access to the digital de-emphasis function. Refer to Figures 7 - 12 for details.



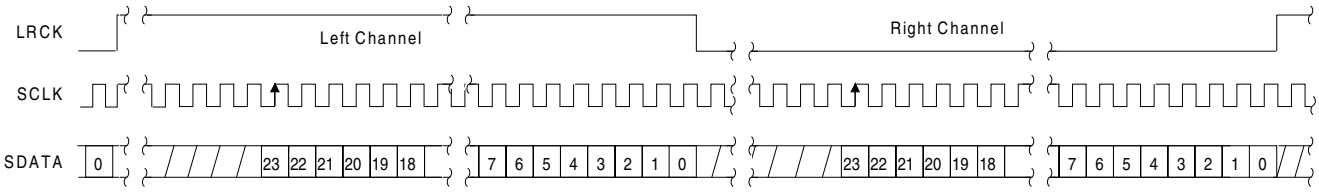
Internal SCLK Mode	External SCLK Mode
I^2S, 16-Bit data and INT SCLK = 32 Fs if MCLK/LRCK = 1024, 512, 256, 128, or 64 I^2S, Up to 24-Bit data and INT SCLK = 48 Fs if MCLK/LRCK = 768, 384, 192, or 96 I^2S, Up to 24-Bit data and INT SCLK = 72 Fs if MCLK/LRCK = 1152	I^2S, up to 24-Bit Data Data Valid on Rising Edge of SCLK

Figure 7. CS4361 Data Format (I^2S)



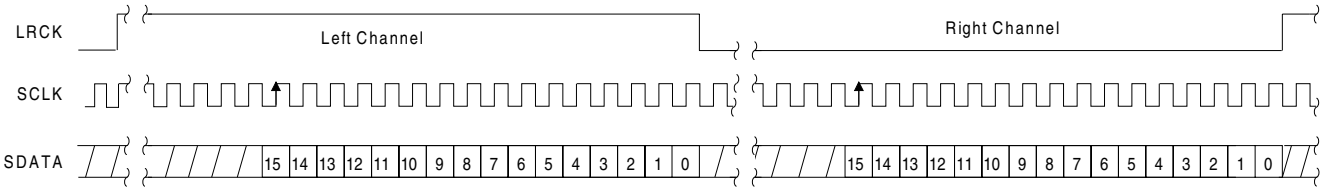
Internal SCLK Mode	External SCLK Mode
Left Justified, up to 24-Bit Data INT SCLK = 64 Fs if MCLK/LRCK = 1024, 512, 256, 128, or 64 INT SCLK = 48 Fs if MCLK/LRCK = 768, 384, 192, or 96 INT SCLK = 72 Fs if MCLK/LRCK = 1152	Left Justified, up to 24-Bit Data Data Valid on Rising Edge of SCLK

Figure 8. CS4361 Data Format (Left Justified)



Internal SCLK Mode	External SCLK Mode
Right Justified, 24-Bit Data INT SCLK = 64 Fs if MCLK/LRCK = 1024, 512, 256, 128, or 64 INT SCLK = 48 Fs if MCLK/LRCK = 768, 384, 192, or 96 INT SCLK = 72 Fs if MCLK/LRCK = 1152	Right Justified, 24-Bit Data Data Valid on Rising Edge of SCLK SCLK Must Have at Least 48 Cycles per LRCK Period

Figure 9. CS4361 Data Format (Right Justified 24)



Internal SCLK Mode	External SCLK Mode
Right Justified, 16-Bit Data INT SCLK = 32 Fs if MCLK/LRCK = 1024, 512, 256, 128, or 64 INT SCLK = 48 Fs if MCLK/LRCK = 768, 384, 192, or 96 INT SCLK = 72 Fs if MCLK/LRCK = 1152	Right Justified, 16-Bit Data Data Valid on Rising Edge of SCLK SCLK Must Have at Least 32 Cycles per LRCK Period

Figure 10. CS4361 Data Format (Right Justified 16)

4.3 De-Emphasis

The CS4361 includes on-chip digital de-emphasis. Figure 11 shows the de-emphasis curve for Fs equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs.

The de-emphasis filter is active (inactive) if the $\overline{\text{DEM}}$/SCLK pin is low (high) for five consecutive falling edges of LRCK. This function is available only in the internal serial clock mode when LRCK < 50 kHz.

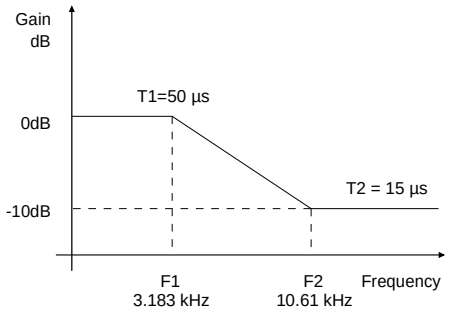


Figure 11. De-Emphasis Curve (Fs = 44.1kHz)

4.4 Mode Select

Mode selection is determined by the Mode Select pin. The value of this pin is locked 1024 LRCK cycles after $\overline{\text{RST}}$ is released. This pin requires a specific connection to supply, ground, MCLK, or LRCK as outlined in table 3.

.

Mode pin is:	Mode	Figure
Tied to VL	I2S	7
Tied to GND	Left Justified	8
Tied to LRCK	Right Justified - 24 bit	9
Tied to MCLK	Right Justified - 16bit	10

Table 3. Mode pin settings

4.5 Initialization and Power-Down

The initialization and power-down sequence flow chart is shown in Figure 12. The CS4361 enters the power-down state upon initial power-up. The interpolation filters and delta-sigma modulators are reset, and the internal voltage reference, multi-bit digital-to-analog converters, and switched-capacitor low-pass filters are powered down. The device will remain in the power-down mode until $\overline{\text{RST}}$ is released and MCLK and LRCK are present. Once MCLK and LRCK are detected, MCLK occurrences are counted over one LRCK period to determine the MCLK/LRCK frequency ratio. Power is then applied to the internal voltage reference. Finally, power is applied to the D/A converters and switched-capacitor filters, and the analog outputs will ramp to the quiescent voltage, VQ.

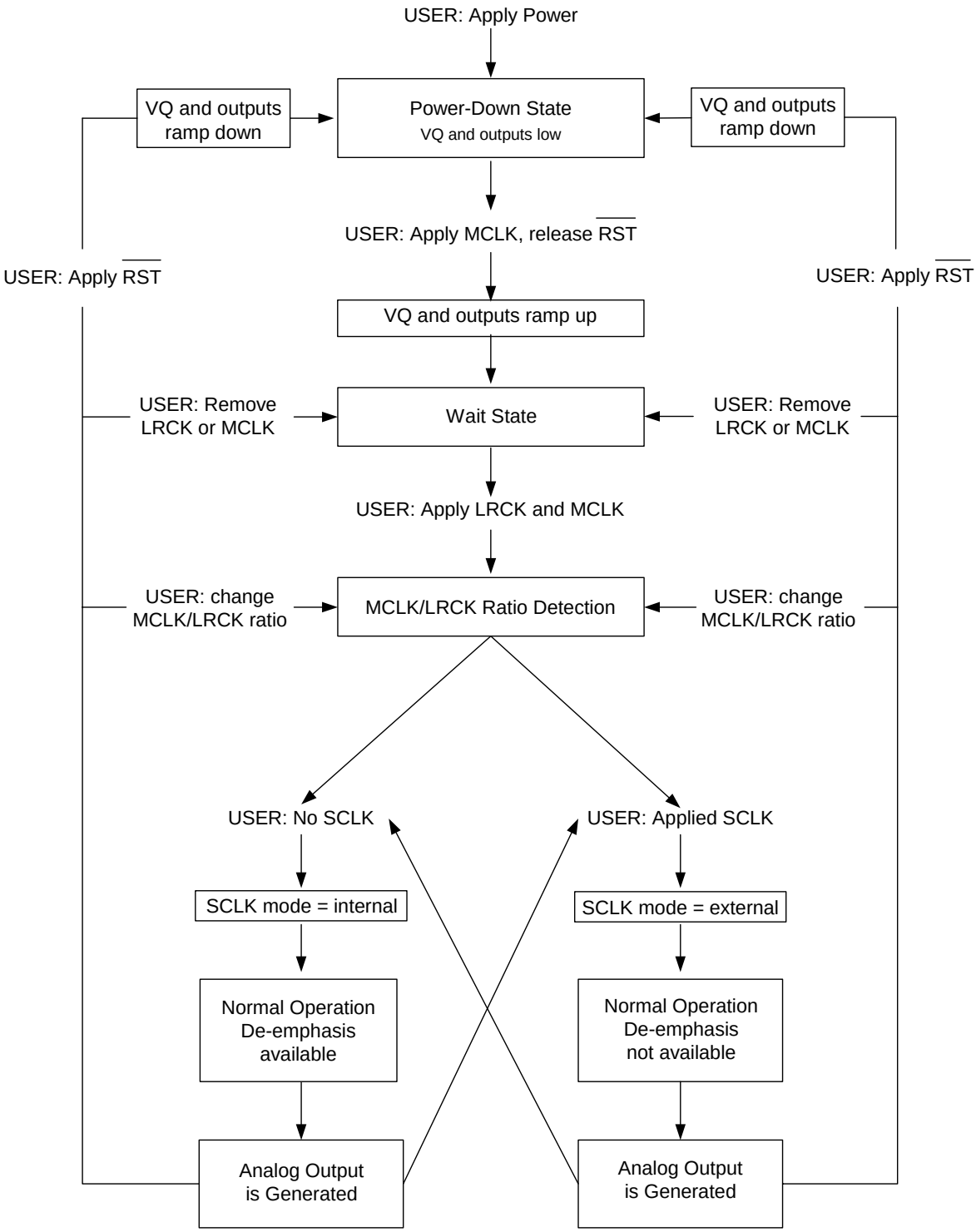


Figure 12. CS4361 Initialization and Power-Down Sequence

4.6 Output Transient Control

The CS4361 uses Popguard™ technology to minimize the effects of output transients during power-up and power-down. When implemented with external DC-blocking capacitors connected in series with the audio outputs, this feature eliminates the audio transients commonly produced by single-ended, single-supply converters. To make best use of this feature, it is necessary to understand its operation.

4.6.1 Power-up

When the device is initially powered-up, the audio outputs, AOUT1-6 are clamped to VQ which is initially low. After $\overline{RST}$ is released and MCLK is applied, the outputs begin to ramp with VQ towards the nominal quiescent voltage. This ramp takes approximately 200 ms to complete. The gradual voltage ramping allows time for the external DC-blocking capacitors to charge to VQ, effectively blocking the quiescent DC voltage. Audio output begins approximately 2000 sample periods after valid LRCK and SDIN are supplied (and SCLK, if used).

4.6.2 Power-down

To prevent audio transients at power-down, the DC-blocking capacitors must fully discharge before turning off the power. In order to do this $\overline{RST}$ should be held low for a period of about 250 ms before removing power. During this time voltage on VQ and the audio outputs discharge gradually to GND. If power is removed before this 250 ms time period has passed a transient will occur when the VA supply drops below that of VQ. There is no minimum time for a power cycle, power may be re-applied at any time.

When changing clock ratio or sample rate it is recommended that zero data (or near zero data) be present on SDIN for at least 10 LRCK samples before the change is made. During the clocking change the DAC outputs will always be in a zero data state. If non-zero audio is present at the time of switching, a slight click or pop may be heard as the DAC output automatically goes to its zero data state.

4.7 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS4361 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 6 shows the recommended power arrangement with VA connected to a clean +3.3 V or +5 V supply. For best performance, decoupling and filter capacitors should be located as close to the device package as possible, with the smallest capacitors placed closest.

4.8 Analog Output and Filtering

The analog filter present in the CS4361 is a switched-capacitor filter followed by a continuous-time, low-pass filter. Its response, combined with that of the digital interpolator, is given in Figures 14 - 21. The recommended external analog circuitry is shown in the “Typical Connection Diagram” on page 11.

The analog outputs are named AOUT1-6. The SDIN1 feeds AOUT1 as the ‘Left’ marked data and AOUT2 as the ‘Right’ marked data. The SDIN2 feeds AOUT3 as the ‘Left’ marked data and AOUT4 as the ‘Right’ marked data. The SDIN3 feeds AOUT5 as the ‘Left’ marked data and AOUT6 as the ‘Right’ marked data.

4.9 Mute Control

The MUTEC pin is intended to be used as control for an external mute circuit in order to add off-chip mute capability.

This pin becomes active under the following conditions.

1) during power-up initialization
2) upon reset
3) if the MCLK to LRCK ratio is incorrect
4) upon receipt of 8192 consecutive samples of zero
5) during power-down.

The MUTEC pin will only go active on static zero data only if all 6 channels satisfy the 8192 sample requirement. If any channel receives non-zero data then the mute pin will return low (inactive).

Use of the mute control function is not mandatory but is recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the mute control function can enable the system designer to achieve idle channel noise & signal-to-noise ratios which are only limited by the external mute circuit. The MUTEC pin is an active-high CMOS driver. See Figure 13 below for a suggested active-high mute circuit.

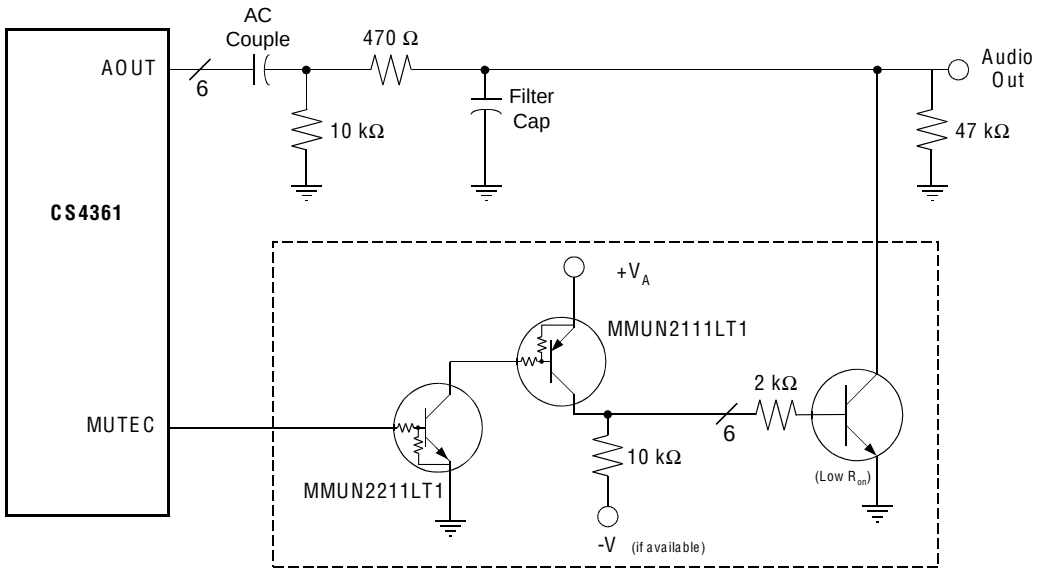


Figure 13. Suggested Active-low Mute Circuit

5.PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full scale analog output for a full scale digital input.

Gain Drift

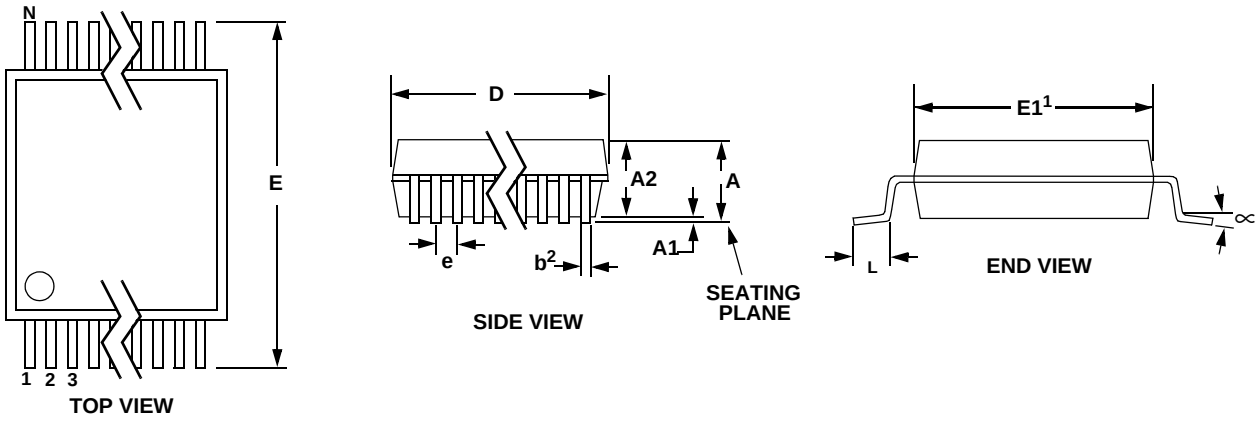
The change in gain value with temperature. Units in ppm/°C.

6.ORDERING INFORMATION

Model	Temperature	Package
CS4361-CZZ	-10 to +70 °C	20-pin Plastic TSSOP - Lead-Free
CS4361-DZZ	-40 to +85 °C	20-pin Plastic TSSOP - Lead-Free

7.PACKAGE DIMENSIONS

20L TSSOP (4.4 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.043	--	--	1.10	
A1	0.002	0.004	0.006	0.05	--	0.15	
A2	0.03346	0.0354	0.037	0.85	0.90	0.95	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.252	0.256	0.259	6.40	6.50	6.60	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	--	--	0.026	--	--	0.65	
L	0.020	0.024	0.028	0.50	0.60	0.70	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-153

Controlling Dimension is Millimeters.

Notes: 1. “D” and “E1” are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension “b” does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of “b” dimension at maximum material condition. Dambar intrusion shall not reduce dimension “b” by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

8.APPENDIX

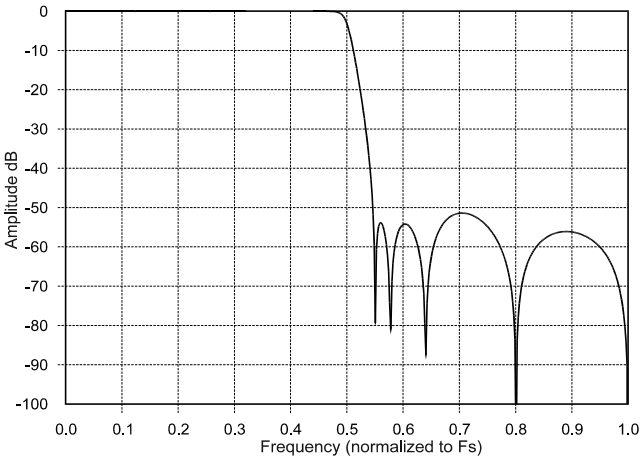


Figure 14. Single Speed Stopband Rejection

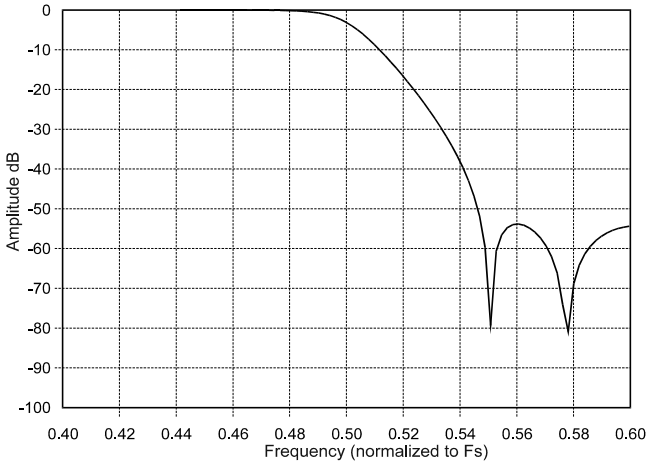


Figure 15. Single Speed Transition Band

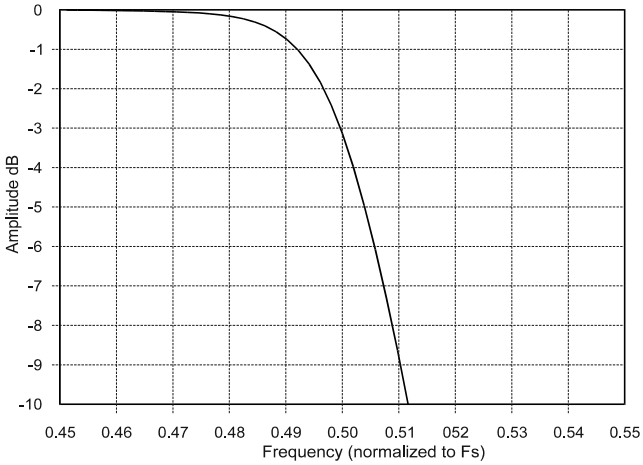


Figure 16. Single Speed Transition Band

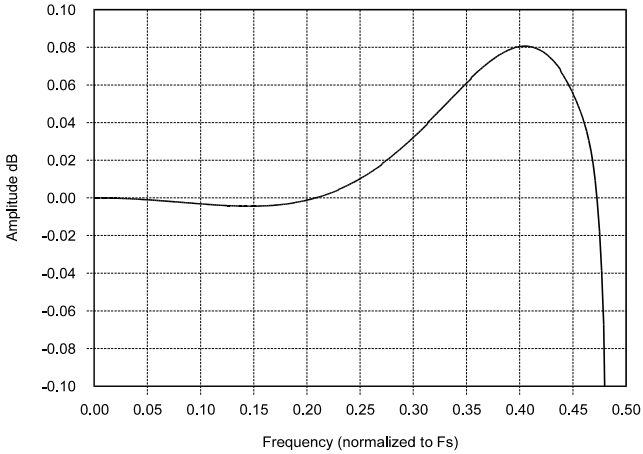


Figure 17. Single Speed Passband Ripple

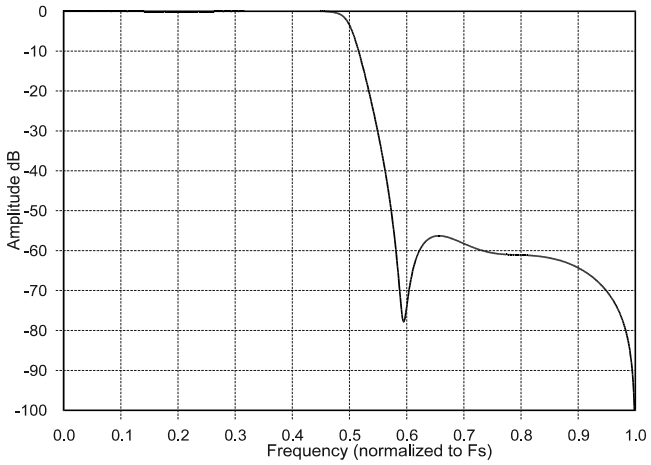


Figure 18. Double Speed Stopband Rejection

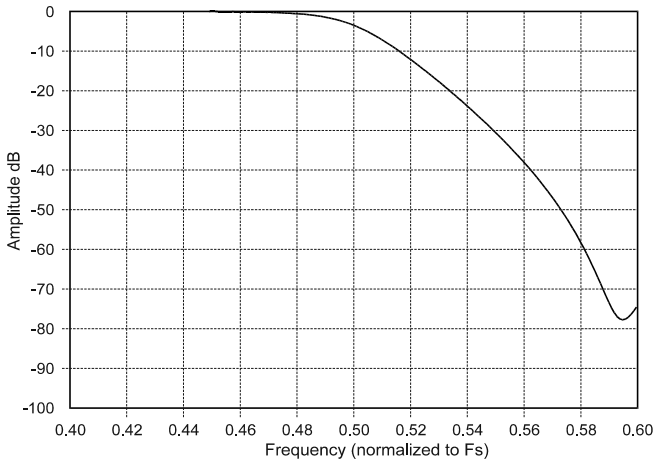


Figure 19. Double Speed Transition Band

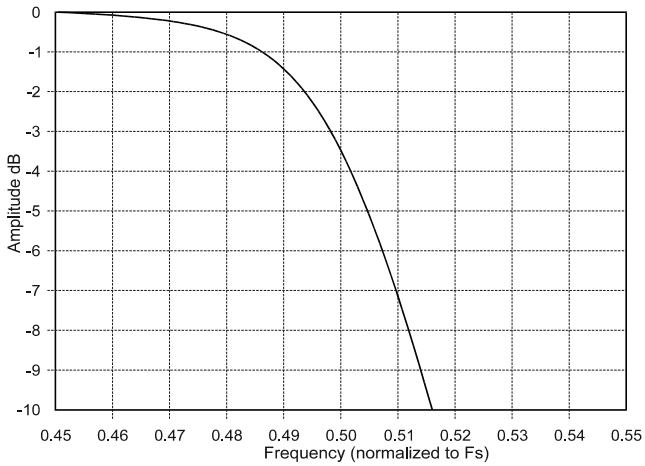


Figure 20. Double Speed Transition Band

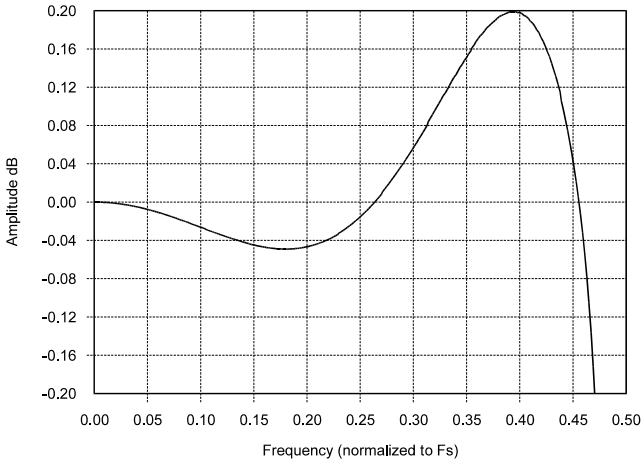


Figure 21. Double Speed Passband Ripple

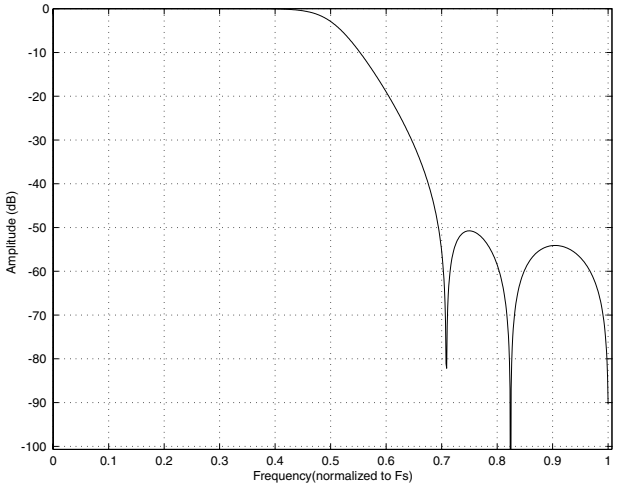


Figure 22. Quad Speed Stopband Rejection

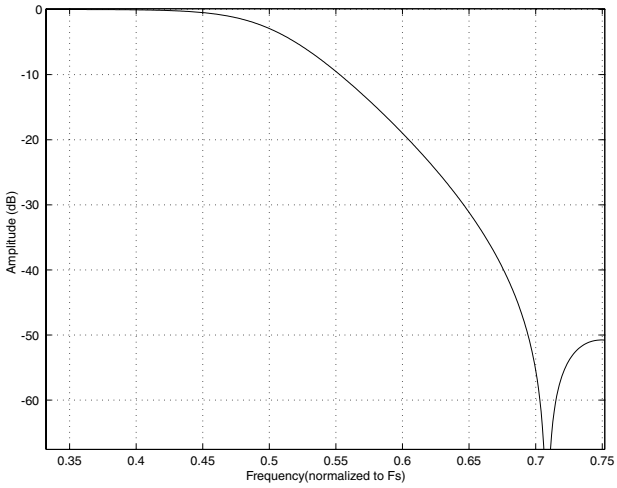


Figure 23. Quad Speed Transition Band

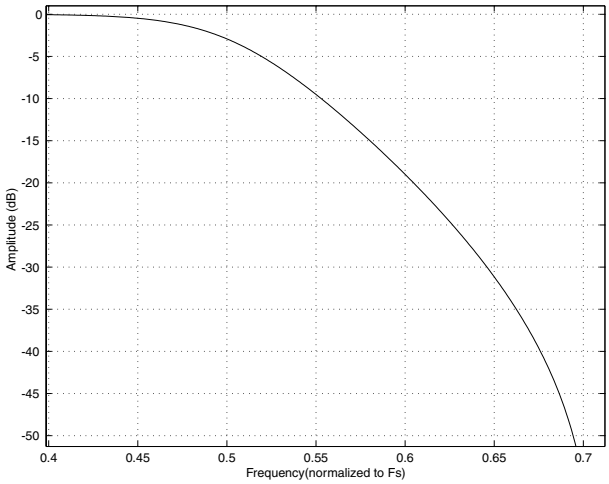


Figure 24. Quad Speed Transition Band

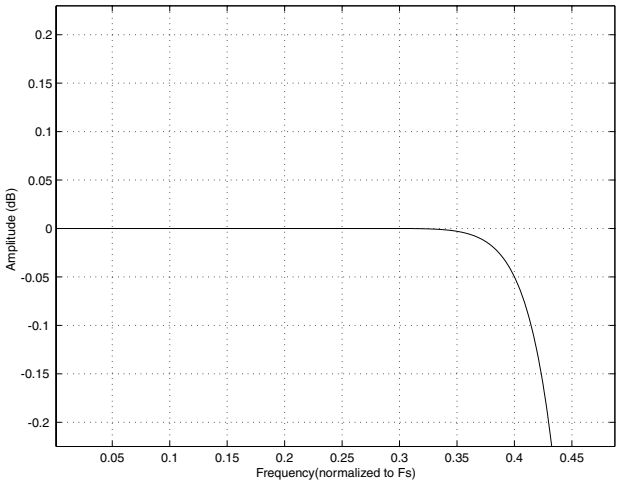


Figure 25. Quad Speed Passband Ripple