CS42406

24-Bit, 192 kHz 2-In 6-Out Audio CODEC

D/A Features

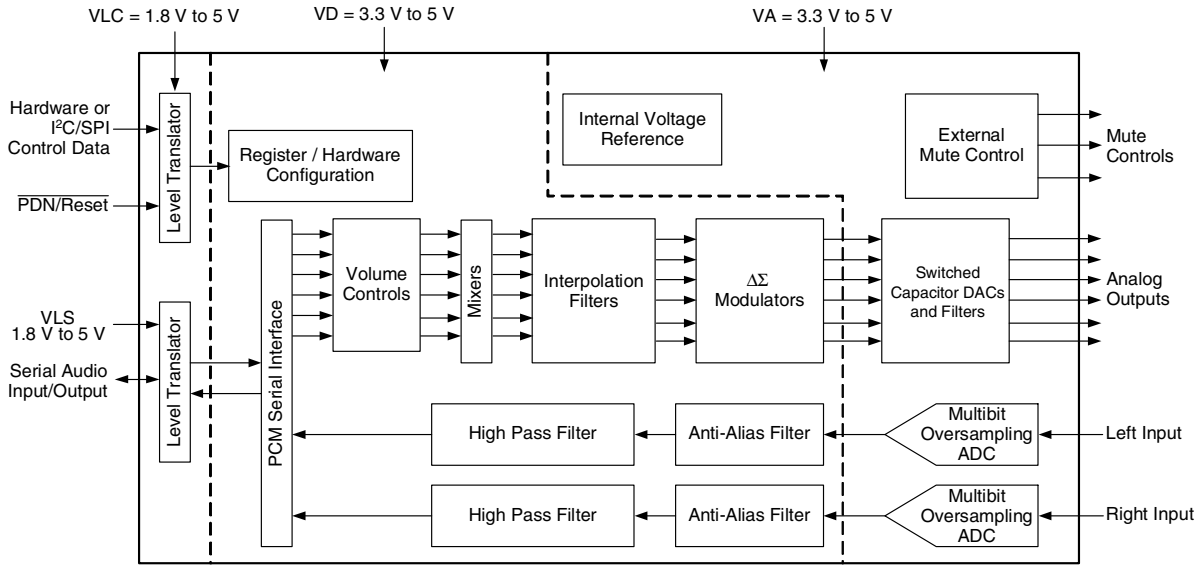
- 24-Bit Conversion
- 102 dB Dynamic Range at 5 V
- -91 dB THD+N
- Digital Volume Control with Soft Ramp
  - 119 dB Attenuation
  - 1 dB Step Size
  - Zero Crossing Click-Free Transitions
- I²C & SPI™ Host Control Port
- ATAPI Mixing
- Low Clock Jitter Sensitivity
- Popguard Technology® for Control of Clicks and Pops

A/D Features

- 24-Bit Conversion
- 105 dB Dynamic Range at 5 V
- -98 dB THD+N
- Advanced Multi-Bit Delta-Sigma Architecture
- High Pass Filter to Remove DC Offsets
- Auto-Mode Selection

System Features

- Direct interface with 5 V to 1.8 V logic levels
- Supports Independent, Synchronous ADC/DAC Sample Rates
- Operation as Clock Master or Slave
- Supports all Audio Sample Rates Including 192 kHz
- Single-Ended Inputs/Outputs
- Analog/Digital Core Supplies From 3.3 V to 5 V



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Stand Alone Mode Feature Set

- System features
  - ADC serial audio port master or slave operation
  - Independent ADC and DAC reset/power-down
  - 256x or 384x MCLK/LRCK ratio selectable
- D/A features
  - Auto-mute on static samples
  - 44.1 kHz 50/15 µs de-emphasis available
  - Selectable serial audio interface formats
    - Left justified up to 24-bit data
    - I²S up to 24-bit data
    - Right justified, 16-bit data
    - Right justified, 24-bit data
- A/D features
  - Serial audio port master or slave operation
  - Auto-mode select in slave mode
  - High-pass filter
  - Selectable serial audio interface formats
    - Left justified up to 24-bit
    - I²S up to 24-bit data

Control Port Mode Feature Set

- D/A features
  - Selectable auto-mute
  - Selectable 32, 44.1, and 48 kHz de-emphasis filters
  - Configurable ATAPI mixing functions
  - Configurable volume and muting controls
  - Selectable serial audio interface formats
    - Left justified up to 24-bit
    - I²S up to 24-bit
    - Right justified 16, 18, 20, and 24-bit

General Description

The CS42406 is a low cost, integrated audio CODEC. The CS42406 performs stereo analog-to-digital (A/D) conversion and six channels of digital-to-analog (D/A) conversion of up to 24-bit serial values at sample rates up to 200 kHz.

The D/A offers a volume control that operates with a 1 dB step size. It incorporates selectable soft ramp and zero crossing transition functions to eliminate clicks and pops.

The D/A's integrated digital mixing functions allow a variety of output configurations ranging from a channel swap to a stereo-to-mono down-mix.

Standard 50/15 µs de-emphasis is available for sampling rates of 32, 44.1, and 48 kHz for compatibility with digital audio programs mastered using the 50/15 µs pre-emphasis technique.

Integrated level translators allow easy interfacing between the CS42406 and other devices operating over a wide range of logic levels.

High-pass filters are available for the right and left channel of the A/D. This allows the A/D to remove unwanted DC offsets.

The CS42406's wide dynamic range, negligible distortion, and low noise make it ideal for applications such as A/V receivers, DVD receivers, and set-top box systems.

ORDERING INFORMATION

CS42406-CQZ	-10° to 70° C	48-pin LQFP
CDB42406	Evaluation Board	

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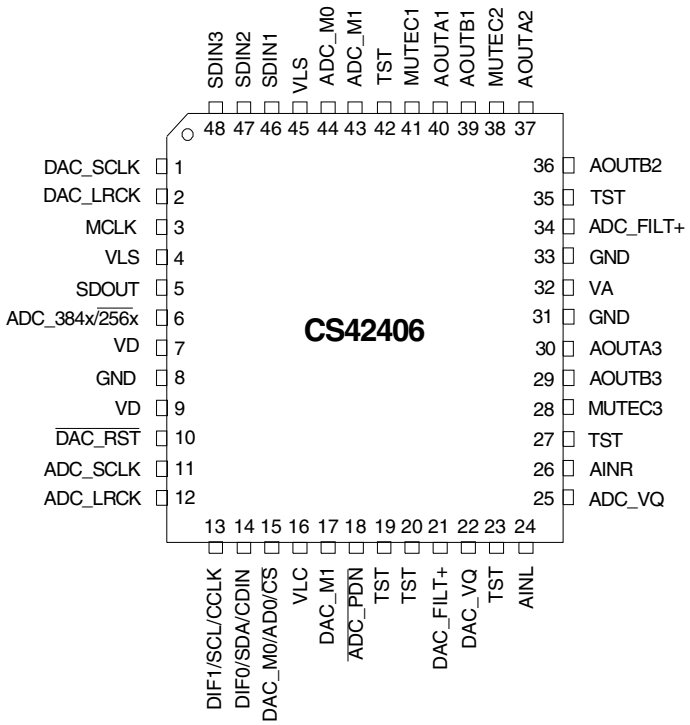
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1. PIN DESCRIPTION



Pin Name	#	Pin Description
DAC_SCLK	1	**DAC Serial Clock** (*Input*) - Serial clock for the DAC serial audio interface.
DAC_LRCK	2	**DAC Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the DAC serial audio data line.
MCLK	3	**Master Clock** (*Input*) - Clock source for the delta-sigma modulators and digital filters.
VLS	4 45	**Serial Audio Interface Power** (*Input*) **-** Positive power for the serial audio interface.
SDOUT	5	**Serial Audio Data Output** *(Output)* - Output for two's complement serial audio data.
ADC_384x/256x	6	**ADC MCLK/LRCK Ratio Select** *(Input)* - Selects the base MCLK/LRCK ratio for the ADC serial port.
VD	7 9	**Digital Power** (*Input*) **-** Positive power supply for the digital section.
GND	8 31 33	**Ground** (*Input*)
RST_DAC	10	**DAC Reset** (*Input*) - Powers down the DAC and resets all internal resisters to their default settings.
ADC_SCLK	11	**ADC Serial Clock** (*Input/Output*) - Serial clock for the ADC serial audio interface.
ADC_LRCK	12	**ADC Left Right Clock** (*Input/Output*) - Determines which channel, Left or Right, is currently active on the ADC serial audio data line.
VLC	16	**Control Port Interface Power** (*Input*) **-** Positive power for the control port interface.
ADC_PDN	18	**ADC Power-Down** *(Input)* - The ADC enters a low power mode when low.
TST	19,20 23,27 35,42	**Test Pin** *(Input)* - Connect to GND.

DAC_FILT+	21	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
DAC_VQ	22	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
AINL **AINR**	24 26	**Analog Inputs** *(Input)* - The full scale analog input level is specified in the "ADC Analog Characteristics (CS42406-CQZ)" on page 14.
ADC_VQ	25	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
AOUTB3 **AOUTA3** **AOUTB2** **AOUTA2** **AOUTB1** **AOUTA1**	29 30 36 37 39 40	**Analog Outputs** (*Output*) - The full scale analog line output level is specified in the "DAC Analog Characteristics (CS42406-CQZ)" on page 9.
MUTEC3 **MUTEC2** **MUTEC1**	28 38 41	**Mute Control** (*Output*) - Control signals for optional mute circuit.
VA	32	**Analog Power** (*Input*) **-** Positive power supply for the analog section.
ADC_FILT+	34	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
ADC_M1 **ADC_M0**	43 44	**ADC Mode Selection** (*Input*) - Determines the operational speed mode of the ADC.
SDIN1 **SDIN2** **SDIN3**	46 47 48	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
DAC Control Port Definitions		
SCL/CCLK	13	**Serial Control Port Clock** (*Input*) - Serial clock for the control port interface.
SDA/CDIN	14	**Serial Control Data I/O** (*Input/Output*) - Input/Output for I²C data. Input for SPI data.
AD0/$\overline{\text{CS}}$	15	**Address Bit / Chip Select** (*Input*) - Chip address bit in I²C Mode. Control signal used to select the chip in SPI mode.
DAC Stand Alone Definitions		
DIF1 **DIF0**	13 14	**Digital Interface Format** (*Input*) - Defines the required relationship between the Left Right Clock, Serial Clock and Serial Audio Data for the DAC.
DAC_M0 **DAC_M1**	15 17	**Mode Selection** (*Input*) - Determines the operational speed mode of the DAC.

2 CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS

(GND = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supplies	Analog (Note 3)	VA	3.1	(Note 1)	5.25	V
	Digital (Note 2, 3)	VD	3.1	3.3	5.25	V
	Logic/Serial Interface (Note 4)	VLS	1.7	3.3	5.25	V
	Control Port Interface	VLC	1.7	3.3	5.25	V
Ambient Temperature						
Commercial	-CQZ	T_A	-10	-	+70	°C

Notes: 1. This part is specified at typical analog voltages of 3.3 V and 5.0 V. See *DAC Analog Characteristics (CS42406-CQZ)* and *ADC Analog Characteristics (CS42406-CQZ)* for details.

2. Nominal VD supply must be less than or equal to the nominal VA supply.

3. In 384x Mode for the ADC, Quad-Speed Slave Mode operation is limited to a nominal VA and VD of 5 V.

4. In 384x Mode for the ADC, Double-Speed & Quad-Speed Mode operation is limited to a minimum VL of 2.5 V

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V, All voltages with respect to ground.) (Note 7)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Analog	VA	-0.3	+6.0	V
	Digital	VD	-0.3	+6.0	V
	Serial Audio Interface (SAI)	VLS	-0.3	+6.0	V
	Control Port Interface	VLC	-0.3	+6.0	V
Input Current	(Note 5)	I_{in}	-	±10	mA
Analog Input Voltage	(Note 6)	V_{IN}	GND-0.7	VA+0.7	V
Digital Input Voltage(Note 6)	Serial Audio Data Interface	V_{IND_S}	-0.3	VLS+0.4	V
	Control Port Interface	V_{IND_S}	-0.3	VLC+0.4	V
Ambient Operating Temperature (Power Applied)		T_A	-50	+95	°C
Storage Temperature		T_{stg}	-65	+150	°C

Notes: 5. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SRC latch-up.

6. The maximum over/under voltage is limited by the input current.

7. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

DAC ANALOG CHARACTERISTICS (CS42406-CQZ)

Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave at 0 dBFS; measurement bandwidth is 10 Hz to 20 kHz; test load R_L = 10 kΩ, C_L = 10 pF (see Figure 1).

Parameter		VA = 5.0 V			VA = 3.3 V			Unit
		Min	Typ	Max	Min	Typ	Max	
Single-Speed Mode	**Fs = 48 kHz**							
Dynamic Range	(Note 8)							
	unweighted	93	99	-	88	94	-	dB
	A-Weighted	96	102	-	91	97	-	dB
Total Harmonic Distortion + Noise	(Note 8)							
	0 dB	-	-91	-85	-	-91	-85	dB
	-20 dB	-	-79	-	-	-74	-	dB
	-60 dB	-	-39	-	-	-34	-	dB
Double-Speed Mode	**Fs = 96 kHz**							
Dynamic Range	(Note 8)							
	unweighted	93	99	-	88	94	-	dB
	A-Weighted	96	102	-	91	97	-	dB
40 kHz Bandwidth	A-Weighted	-	100	-	-	97	-	dB
Total Harmonic Distortion + Noise	(Note 8)							
	0 dB	-	-91	-85	-	-91	-85	dB
	-20 dB	-	-79	-	-	-74	-	dB
	-60 dB	-	-39	-	-	-34	-	dB
Quad-Speed Mode	**Fs = 192 kHz**							
Dynamic Range	(Note 8)							
	unweighted	93	99	-	88	94	-	dB
	A-Weighted	96	102	-	91	97	-	dB
40 kHz Bandwidth	A-Weighted	-	100	-	-	97	-	dB
Total Harmonic Distortion + Noise	(Note 8)							
	0 dB	-	-91	-85	-	-91	-85	dB
	-20 dB	-	-79	-	-	-74	-	dB
	-60 dB	-	-39	-	-	-34	-	dB

Notes: 8. One-half LSB of triangular PDF dither is added to data.

DAC ANALOG CHARACTERISTICS (CS42406-CQZ) (Continued)

Parameters		Symbol	Min	Typ	Max	Units
Dynamic Performance for All Modes						
Interchannel Isolation	(1 kHz)		-	102	-	dB
DC Accuracy						
Interchannel Gain Mismatch		ICGM	-	0.1	-	dB
Gain Drift			-	±100	-	ppm/°C
Analog Output Characteristics and Specifications						
Full Scale Output Voltage			0.60•VA	0.66•VA	0.72•VA	Vpp
Output Impedance		Z_{out}	-	100	-	Ω
Minimum AC-Load Resistance	(Note 7)	R_L	-	3	-	kΩ
Maximum Load Capacitance	(Note 7)	C_L	-	100	-	pF

9. See Figure 1-2. R_L and C_L reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. In this circuit topology, C_L will effectively move the dominant pole of the two-pole amp in the output stage. Increasing this value beyond the recommended 100 pF can cause the internal op-amp to become unstable.

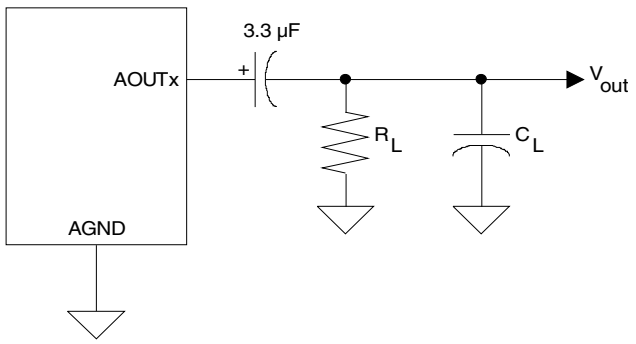


Figure 1. Output Test Load

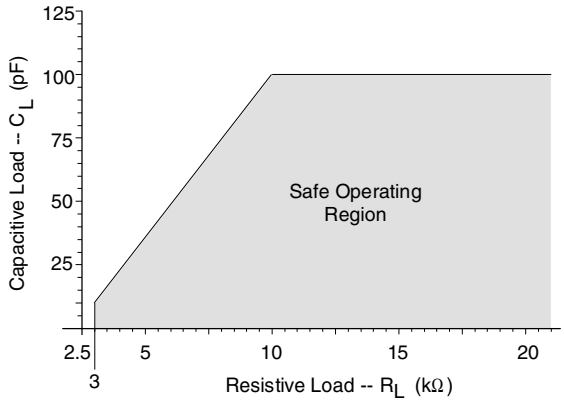


Figure 2. Maximum Loading

DAC FILTER RESPONSE The filter characteristics and the X-axis of the response plots have been normalized to the input sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs.

Parameter		Min	Typ	Max	Unit
Single-Speed Mode - (4 kHz to 50 kHz sample rates)					
Passband					
	to -0.05 dB corner	0	-	0.4535	Fs
	to -3 dB corner	0	-	0.4998	Fs
Passband Ripple		-0.02	-	+0.035	dB
StopBand		0.5465	-	-	Fs
StopBand Attenuation	(Note 10)	50	-	-	dB
Group Delay		-	9/Fs	-	s
De-emphasis Error (Relative to 1 kHz)	(Note 11)				
Control Port Mode	Fs = 32 kHz	-	-	+0.2/-0.1	dB
	Fs = 44.1 kHz	-	-	+0.05/-0.14	dB
	Fs = 48 kHz	-	-	+0/-0.22	dB
Stand-Alone Mode	Fs = 32 kHz	-	-	+1.5/-0	dB
	Fs = 44.1 kHz	-	-	+0.05/-0.14	dB
	Fs = 48 kHz	-	-	+0.2/-0.4	dB
Double-Speed Mode - (50 kHz to 100 kHz sample rates)					
Passband					
	to -0.1 dB corner	0	-	0.4621	Fs
	to -3 dB corner	0	-	0.4982	Fs
Passband Ripple		-0.1	-	0	dB
StopBand		0.577	-	-	Fs
StopBand Attenuation	(Note 10)	55	-	-	dB
Group Delay		-	4/Fs	-	s
Quad-Speed Mode - (100 kHz to 200 kHz sample rates)					
Passband					
	to -3 dB corner	0	-	0.25	Fs
Passband Ripple		-0.7	-	0	dB
Group Delay		-	1.5/Fs	-	s

Notes: 10. For Single-Speed Mode, the measurement bandwidth is 0.5465 Fs to 3 Fs.
For Double-Speed Mode, the measurement bandwidth is 0.577 Fs to 1.4 Fs.

11. De-emphasis is only available in Single-Speed Mode.

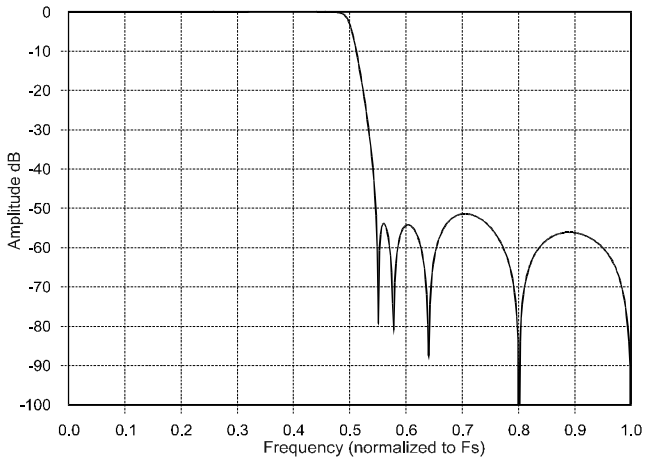


Figure 3. Single-Speed Stopband Rejection

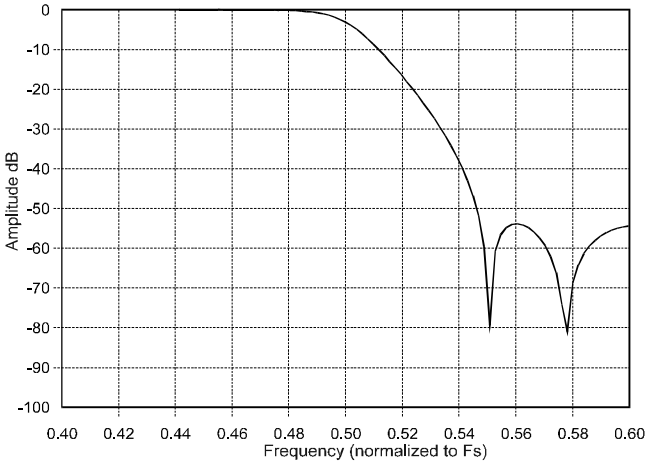


Figure 4. Single-Speed Transition Band

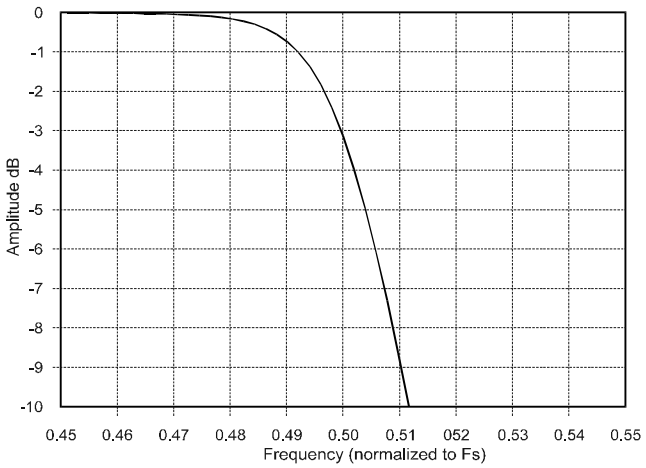


Figure 5. Single-Speed Transition Band (Detail)

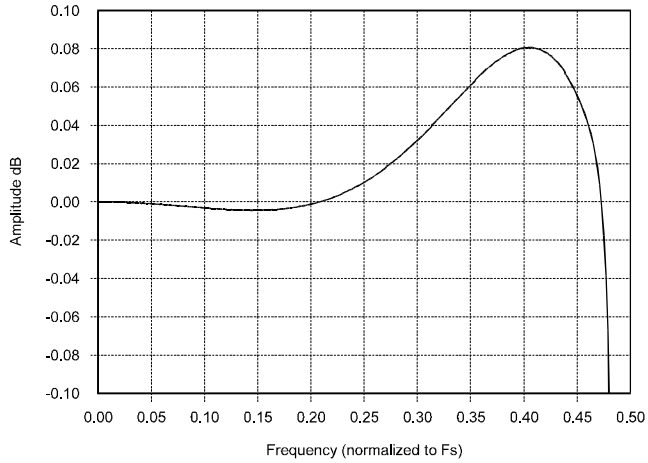


Figure 6. Single-Speed Passband Ripple

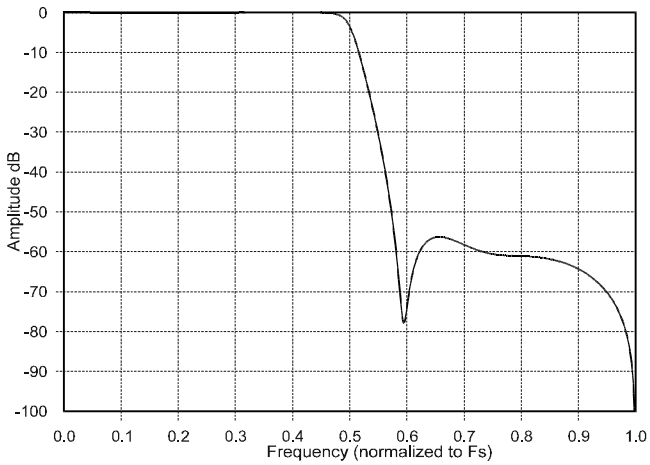


Figure 7. Double-Speed Stopband Rejection

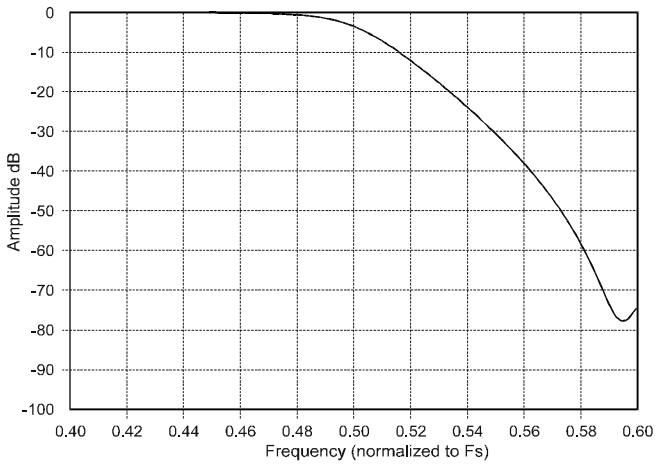


Figure 8. Double-Speed Transition Band

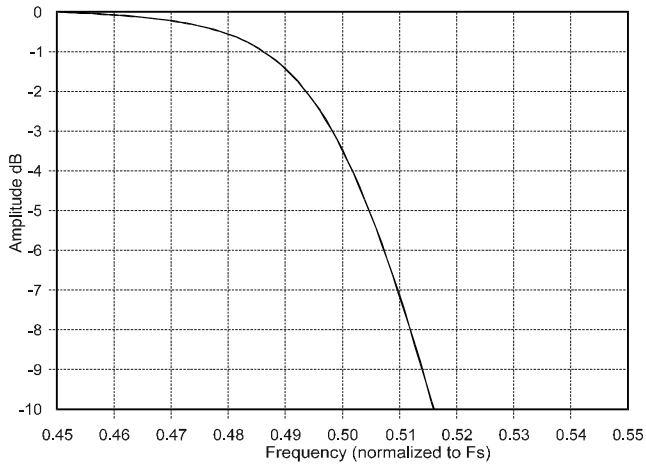


Figure 9. Double-Speed Transition Band (Detail)

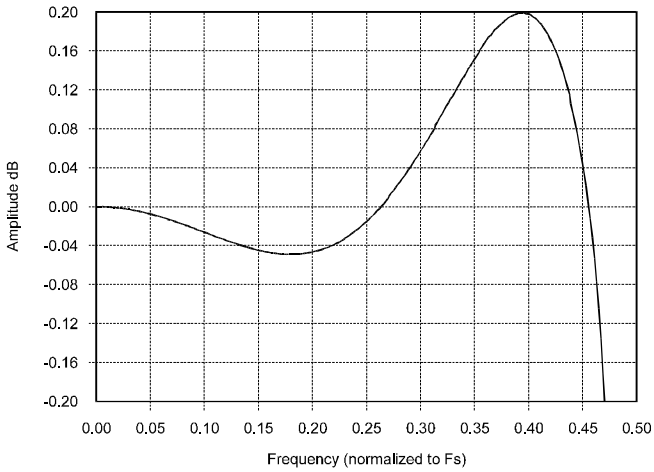


Figure 10. Double-Speed Passband Ripple

ADC ANALOG CHARACTERISTICS (CS42406-CQZ)

Test conditions (unless otherwise specified): Input test signal is a 1 kHz sine wave; measurement bandwidth is 10 Hz to 20 kHz.

Parameter		VA = 5.0 V			VA = 3.3 V			Unit
		Min	Typ	Max	Min	Typ	Max	
Single-Speed Mode	**Fs = 48 kHz**							
Dynamic Range	unweighted	96	102	-	93	99	-	dB
	A-Weighted	99	105	-	96	102	-	dB
Total Harmonic Distortion + Noise	(Note 12)							
	-1 dB	-	-98	-92	-	-95	-89	dB
	-20 dB	-	-82	-	-	-79	-	dB
	-60 dB	-	-42	-	-	-39	-	dB
Double-Speed Mode	**Fs = 96 kHz**							
Dynamic Range	unweighted	96	102	-	93	99	-	dB
	A-Weighted	99	105	-	96	102	-	dB
40 kHz Bandwidth	unweighted	-	99	-	-	96	-	dB
Total Harmonic Distortion + Noise	(Note 12)							
	-1 dB	-	-98	-92	-	-95	-89	dB
	-20 dB	-	-82	-	-	-79	-	dB
	-60 dB	-	-42	-	-	-39	-	dB
Quad-Speed Mode	**Fs = 192 kHz**							
Dynamic Range	unweighted	96	102	-	93	99	-	dB
	A-Weighted	99	105	-	96	102	-	dB
40 kHz Bandwidth	unweighted	-	99	-	-	96	-	dB
Total Harmonic Distortion + Noise	(Note 12)							
	-1 dB	-	-98	-92	-	-95	-89	dB
	-20 dB	-	-82	-	-	-79	-	dB
	-60 dB	-	-42	-	-	-39	-	dB

Note: 12. Referred to the typical full-scale input voltage

ADC ANALOG CHARACTERISTICS (CS42406-CQZ) (Continued)

Parameters	Min	Typ	Max	Units
Dynamic Performance for All Modes				
Interchannel Isolation	-	90	-	dB
DC Accuracy				
Interchannel Gain Mismatch	-	0.1	-	dB
Gain Error	-	-	±10	%
Gain Drift	-	±100	-	ppm/°C
Analog Input Characteristics				
Full Scale Input Voltage	0.53•VA	0.56•VA	0.59•VA	Vpp
Input Impedance	18	-	-	kΩ

ADC DIGITAL FILTER RESPONSE

The filter characteristics and the X-axis of the response plots have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs.

Parameter			Min	Typ	Max	Unit
Single-Speed Mode (4 kHz to 50 kHz sample rates)						
Passband		to -0.1 dB corner	0	-	0.49	Fs
Passband Ripple			-	-	0.035	dB
Stopband			0.57	-	-	Fs
Stopband Attenuation			70	-	-	dB
Total Group Delay			-	12/Fs	-	s
Double-Speed Mode (50 kHz to 100 kHz sample rates)						
Passband		to -0.1 dB corner	0	-	0.49	Fs
Passband Ripple			-	-	0.025	dB
Stopband			0.56	-	-	Fs
Stopband Attenuation			69	-	-	dB
Total Group Delay			-	9/Fs	-	s
Quad-Speed Mode (100 kHz to 200 kHz sample rates)						
Passband		to -0.1 dB corner	0	-	0.26	Fs
Passband Ripple			-	-	0.025	dB
Stopband			0.50	-	-	Fs
Stopband Attenuation			60	-	-	dB
Total Group Delay			-	5/Fs	-	s
High Pass Filter Characteristics						
Frequency Response	-3.0 dB		-	1	-	Hz
	-0.13 dB	(Note 13)		20	-	Hz
Phase Deviation	@ 20 Hz	(Note 13)	-	10	-	Deg
Passband Ripple			-	-	0	dB

Note: 13. Response shown is for Fs equal to 48 kHz.

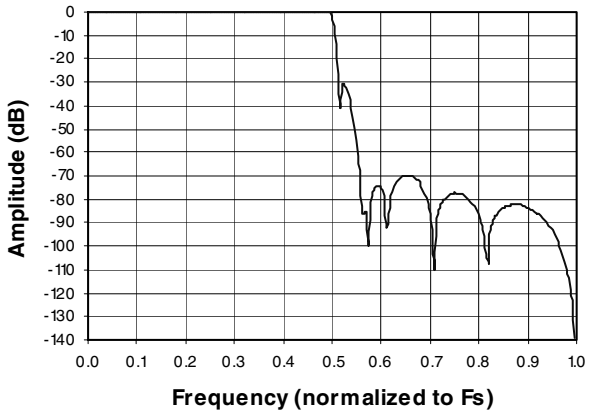


Figure 11. Single-Speed Mode Stopband Rejection

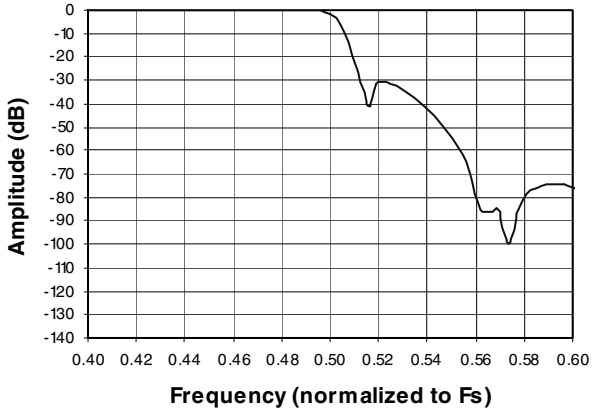


Figure 12. Single-Speed Mode Stopband Rejection

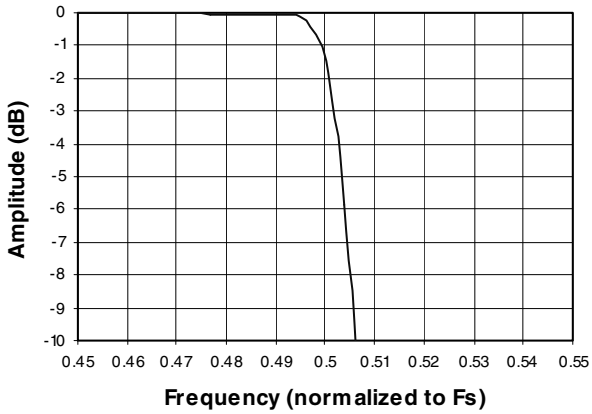


Figure 13. Single-Speed Mode Transition Band (Detail)

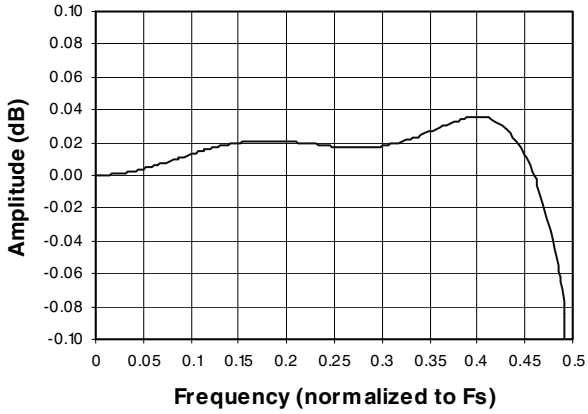


Figure 14. Single-Speed Mode Passband Ripple

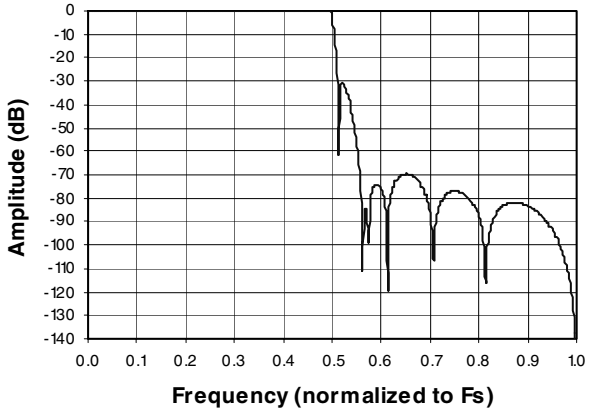


Figure 15. Double-Speed Mode Stopband Rejection

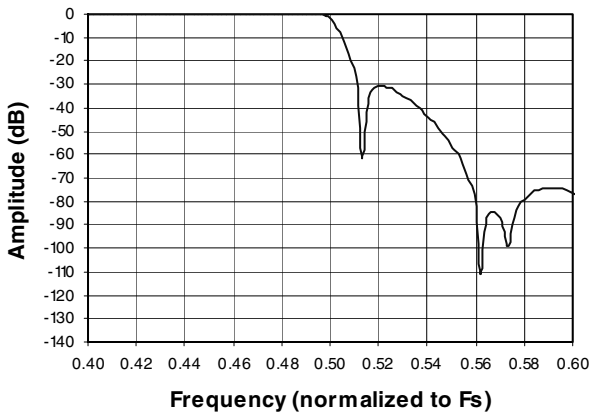


Figure 16. Double-Speed Mode Stopband Rejection

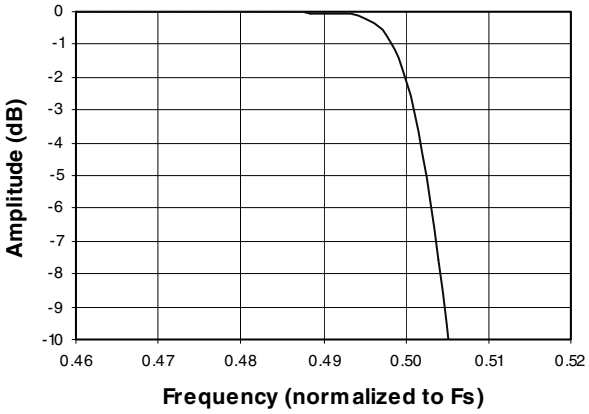


Figure 17. Double-Speed Mode Transition Band (Detail)

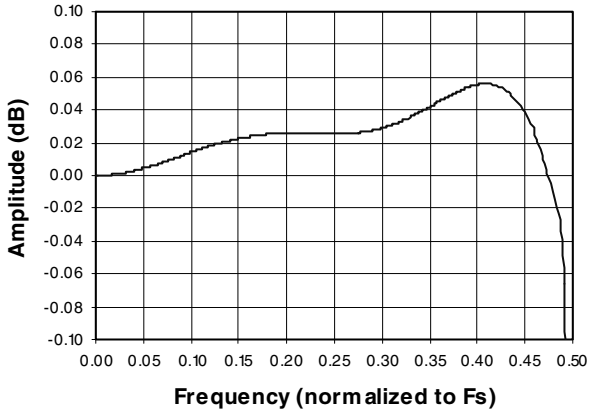


Figure 18. Double-Speed Mode Passband Ripple

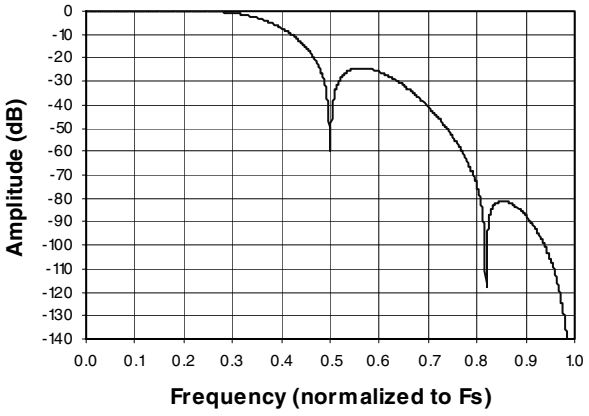


Figure 19. Quad-Speed Mode Stopband Rejection

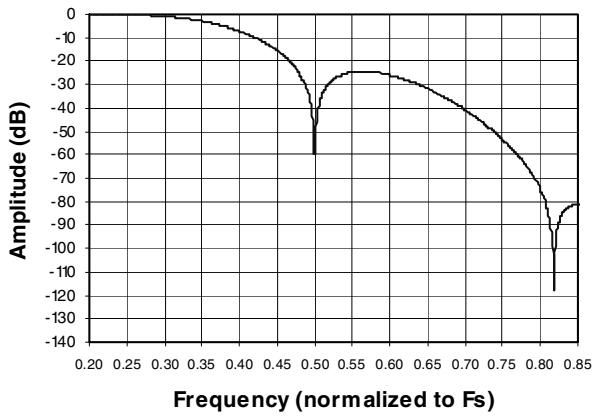


Figure 20. Quad-Speed Mode Stopband Rejection

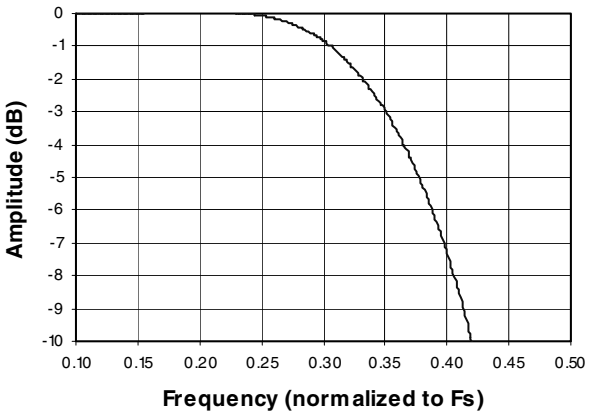


Figure 21. Quad-Speed Mode Transition Band (Detail)

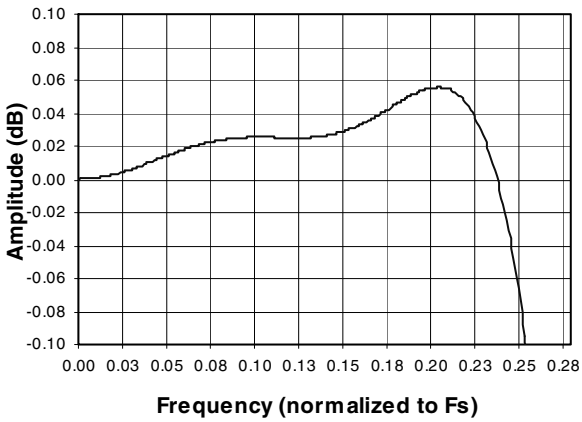


Figure 22. Quad-Speed Mode Passband Ripple

DC ELECTRICAL CHARACTERISTICS GND = 0 V; all voltages with respect to GND.

Parameters		Symbol	Min	Typ	Max	Units
Normal Operation (Note 14)						
Power Supply Current	VA = 5.0 V	I_A	-	43	48	mA
	VD, VLS, VLC = 5.0 V	I_{DT}	-	40	45	mA
	VA = 3.3 V	I_A	-	40	44	mA
	VD, VLS, VLC = 3.3 V (Note 15)	I_{DT}	-	25	26	mA
Power Dissipation	All Supplies = 5.0 V		-	415	465	mW
	All Supplies = 3.3 V		-	215	231	mW
Power-down Mode (Note 16)						
Power Supply Current	All Supplies = 5.0 V		-	2	-	mA
	All Supplies = 3.3 V		-	1	-	mA
Power Dissipation	All Supplies = 5.0 V		-	10	-	mW
	All Supplies = 3.3 V		-	3.3	-	mW
All Modes of Operation						
Power Supply Rejection Ratio (Note 17)	1 kHz	PSRR	-	60	-	dB
V_Q Nominal Voltage			-	0.5•VA	-	V
Output Impedance	DAC_VQ		-	250	-	kΩ
	ADC_VQ		-	25	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA
Filt+ Nominal Voltage			-	VA	-	V
MUTEC Low-Level Output Voltage			-	0	-	V
MUTEC High-Level Output Voltage			-	VA	-	V
Maximum MUTEC Drive Current			-	3	-	mA

Notes: 14. Normal operation is defined as $\overline{RST}$ = HI with a 997 Hz, 0 dBFS digital input sampled at the highest F_s for each speed mode, and open outputs, unless otherwise specified. Analog inputs are driven with a 1 kHz, -1 dBFS sine wave and sampled at the highest F_s for each speed mode.

15. I_{DT} measured with no external loading on pin 14 (SDA).

16. Power Down Mode is defined as $\overline{DAC_RST}$ = LO, $\overline{PDN_ADC}$ = LO, with all clocks and data lines held static.

17. Valid with the recommended capacitor values on FILT+ and VQ as shown in Figure 33.

DIGITAL CHARACTERISTICS GND = 0 V; all voltages with respect to GND.

Parameters		Symbol	Min	Typ	Max	Units
Input Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance			-	8	-	pF
High-Level Input Voltage	(% of VLS/VLC)	V_{IH}	70%	-	-	V
Low-Level Input Voltage	(% of VLS/VLC)	V_{IL}	-	-	13%	V
High-Level Output Voltage at I_o = 100 µA	(% of VLS/VLC)	V_{OH}	70%	-	-	V
Low-Level Output Voltage at I_o =100 µA	(% of VLS/VLC)	V_{OL}	-	-	15%	V

SWITCHING CHARACTERISTICS - DAC SERIAL AUDIO PORT (Logic "0" = GND = 0 V, Logic "1" = VLS)

Parameter	Symbol	Min	Typ	Max	Unit
MCLK Specifications					
MCLK Frequency		1.024	-	12.8	MHz
		22	-	25.6	MHz
MCLK Duty Cycle		45	-	55	%
Single-Speed*					
DAC_LRCK Duty Cycle		45	-	55	%
DAC_SCLK Frequency		-	-	128×Fs	Hz
DAC_SCLK Pulse Width Low	t_{sclkl}	20	-	-	ns
DAC_SCLK Pulse Width High	t_{sclkh}	20	-	-	ns
DAC_SCLK rising to DAC_LRCK edge delay	t_{slrd}	20			ns
DAC_SCLK rising to DAC_LRCK edge setup time	t_{slrs}	20			ns
SDINx valid to DAC_SCLK rising setup time	t_{sdlrs}	20			ns
DAC_SCLK rising to SDINx hold time	t_{sdh}	20			ns
Double-Speed*					
DAC_LRCK Duty Cycle		45	-	55	%
DAC_SCLK Frequency		-	-	64×Fs	Hz
DAC_SCLK Pulse Width Low	t_{sclkl}	20	-	-	ns
DAC_SCLK Pulse Width High	t_{sclkh}	20	-	-	ns
DAC_SCLK rising to DAC_LRCK edge delay	t_{slrd}	20			ns
DAC_SCLK rising to DAC_LRCK edge setup time	t_{slrs}	20			ns
SDINx valid to DAC_SCLK rising setup time	t_{sdlrs}	20			ns
DAC_SCLK rising to SDINx hold time	t_{sdh}	20			ns
Quad-Speed*					
DAC_LRCK Duty Cycle		45	-	55	%
DAC_SCLK Frequency		-	-	MCLK/2	Hz
DAC_SCLK Pulse Width Low	t_{sclkl}	20	-	-	ns
DAC_SCLK Pulse Width High	t_{sclkh}	20	-	-	ns
DAC_SCLK rising to DAC_LRCK edge delay	t_{slrd}	20			ns
DAC_SCLK rising to DAC_LRCK edge setup time	t_{slrs}	20			ns
SDINx valid to DAC_SCLK rising setup time	t_{sdlrs}	20			ns
DAC_SCLK rising to SDINx hold time	t_{sdh}	20			ns

* For a description of Speed Modes, please refer to Section 4.1.2 on page 30.

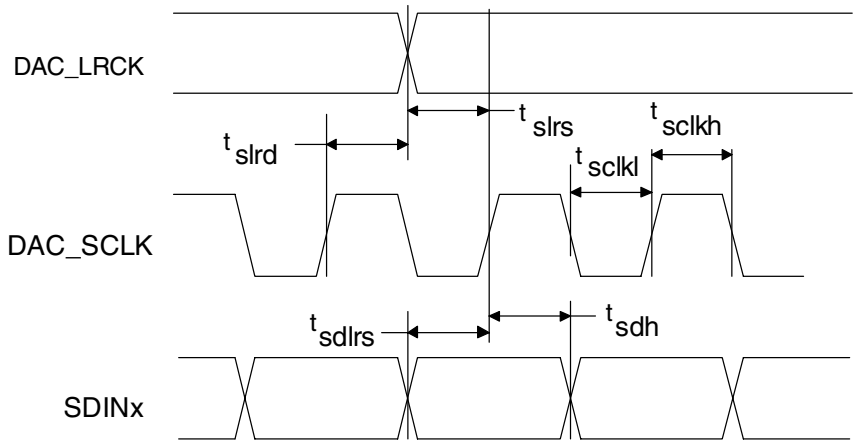


Figure 23. DAC Serial Audio Port

SWITCHING CHARACTERISTICS - ADC SERIAL AUDIO PORT

Logic "0" = GND = 0 V; Logic "1" = VLS, C_L = 20 pF.

NOTE: Certain parameters depend on the 256x/384x (pin6) mode setting and are separated below.

Parameter	Symbol	Min	Typ	Max	Unit
MCLK Duty Cycle		45	-	55	%
Master Mode					
ADC_SCLK falling to ADC_LRCK	t_{mslr}	-20	-	20	ns
ADC_SCLK falling to SDOUT valid	t_{sdo}	0	-	32	ns
Slave Mode					
Single-Speed*					
ADC_LRCK Frequency MCLK = 256, 384 Fs (÷1 or 1.5) (Note 18) MCLK = 512, 768 Fs (÷2 or 3)	Fs Fs	4 43	-	50 50	kHz kHz
ADC_LRCK Duty Cycle		40	-	60	%
SDOUT valid before ADC_SCLK rising	t_{stp}	10	-	-	ns
SDOUT valid after ADC_SCLK rising	t_{hld}	5	-	-	ns
ADC_SCLK falling to ADC_LRCK edge	t_{slrd}	-20	-	20	ns
Double-Speed*					
ADC_LRCK Frequency MCLK = 128, 192 Fs (÷1 or 1.5) (Note 18) MCLK = 256, 384 Fs (÷2 or 3)	Fs Fs	50 86	-	100 100	kHz kHz
ADC_LRCK Duty Cycle		40	-	60	%
SDOUT valid before ADC_SCLK rising	t_{stp}	10	-	-	ns
SDOUT valid after ADC_SCLK rising	t_{hld}	5	-	-	ns
ADC_SCLK falling to ADC_LRCK edge	t_{slrd}	-20	-	20	ns
Quad-Speed*					
ADC_LRCK Frequency (Note 18) MCLK = 128 Fs (÷2 or 3)	Fs	172	-	200	kHz
ADC_LRCK Duty Cycle		40	-	60	%
SDOUT valid before ADC_SCLK rising	t_{stp}	10	-	-	ns
SDOUT valid after ADC_SCLK rising	t_{hld}	5	-	-	ns
ADC_SCLK falling to ADC_LRCK edge	t_{slrd}	-8	-	8	ns

256x Mode *(pin 6 = LO)*						
MCLK Frequency (Note 18)	Internal ÷1		1.024	-	12.8	MHz
	Internal ÷2		22.016	-	25.6	MHz
Master Mode						
ADC_SCLK Duty Cycle	Single-Speed Mode		-	50	-	%
	Double-Speed Mode		-	50	-	%
	Quad-Speed Mode		-	50	-	%
ADC_LRCK Frequency (Note 18) MCLK = 64 Fs (÷1)	Quad-Speed Mode	Fs	100	-	200	kHz
Slave Mode						
ADC_SCLK Period	Single-Speed Mode	t_{sclkw}	156	-	-	ns
	Double-Speed Mode		156	-	-	ns
	Quad-Speed Mode		78	-	-	ns
ADC_SCLK Duty Cycle	Single-Speed Mode		45	-	55	%
	Double-Speed Mode		45	-	55	%
	Quad-Speed Mode		45	-	55	%
384x Mode *(pin 6 = HI)*						
MCLK Frequency (Note 18)	Internal ÷1.5		1.536	-	19.2	MHz
	Internal ÷3		33.024	-	38.4	MHz
Master Mode						
ADC_SCLK Duty Cycle	Single-Speed Mode		-	50	-	%
	Double-Speed Mode		-	50	-	%
	Quad-Speed Mode		-	33	-	%
ADC_LRCK Frequency (Note 18) MCLK = 96 Fs (÷1.5)	Quad-Speed Mode	Fs	100	-	200	kHz
Slave Mode						
ADC_SCLK Period	Single-Speed Mode	t_{sclkw}	290	-	-	ns
	Double-Speed Mode		193	-	-	ns
	Quad-Speed Mode		104	-	-	ns
ADC_SCLK Duty Cycle	Single-Speed Mode		45	-	55	%
	Double-Speed Mode		45	-	55	%
	Quad-Speed Mode		45	-	50	%

* For a description of Speed Modes, please refer to Table 1 on page 30.

18. Internal ÷ is automatically determined when operating within the specified limits.

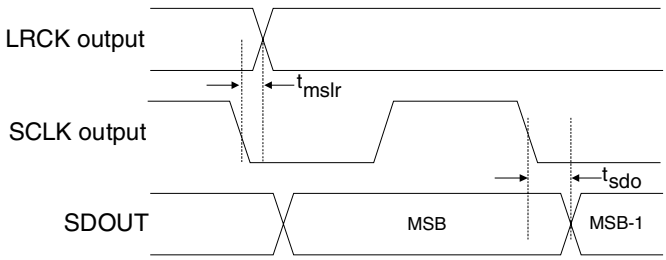


Figure 24. Master Mode, Left Justified SAI

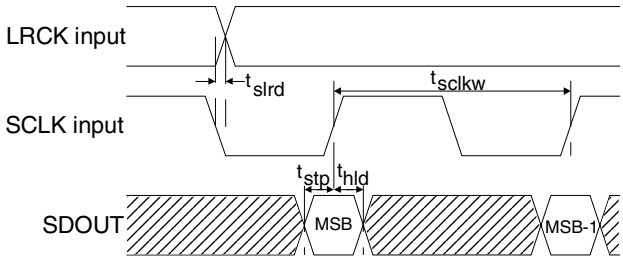


Figure 25. Slave Mode, Left Justified SAI

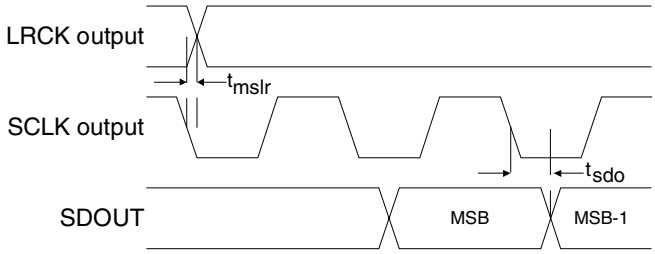


Figure 26. Master Mode, I²S SAI

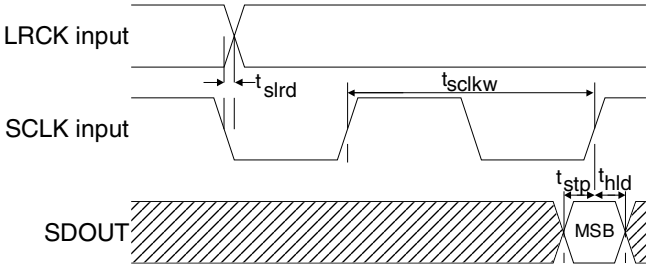


Figure 27. Slave Mode, I²S SAI

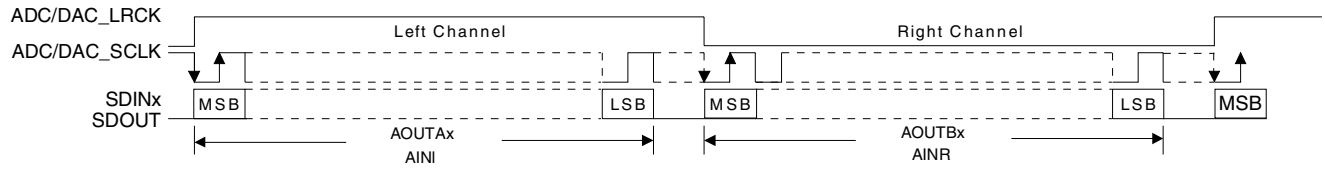


Figure 28. Left Justified up to 24-Bit Data

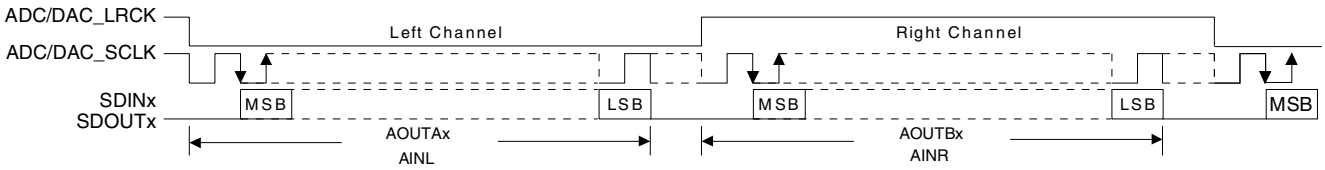


Figure 29. I²S, up to 24-Bit Data

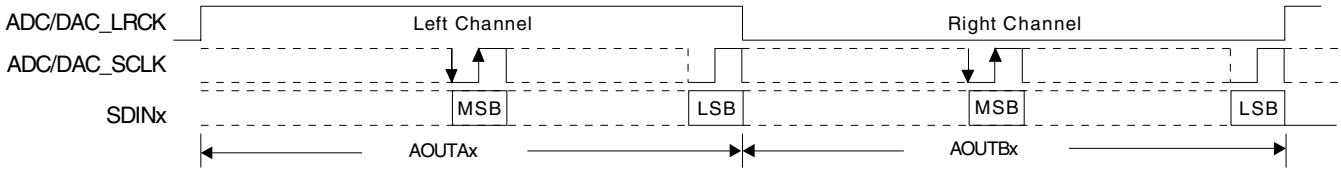


Figure 30. Right Justified Data

SWITCHING SPECIFICATIONS - CONTROL PORT INTERFACE Inputs: Logic 0 = GND, Logic 1 = VLC

Parameter		Symbol	Min	Max	Unit
I²C Mode					
SCL Clock Frequency		f_{scl}	-	100	kHz
$\overline{\text{DAC_RST}}$ Rising Edge to Start		t_{irs}	500	-	ns
Bus Free Time Between Transmissions		t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)		t_{hdst}	4.0	-	µs
Clock Low time		t_{low}	4.7	-	µs
Clock High Time		t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition		t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling	(Note 19)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising		t_{sud}	250	-	ns
Rise Time of SCL and SDA		t_{rc}, t_{rc}	-	1	µs
Fall Time SCL and SDA		t_{fc}, t_{fc}	-	300	ns
Setup Time for Stop Condition		t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	(Note 20)	t_{ack}	-	(Note 21)	ns

Notes: 19. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

20. The acknowledge delay is based on MCLK and can limit the maximum transaction speed.

21. $\frac{5}{256 \times Fs}$ for Single-Speed Mode, $\frac{5}{128 \times Fs}$ for Double-Speed Mode, $\frac{5}{64 \times Fs}$ for Quad-Speed Mode.

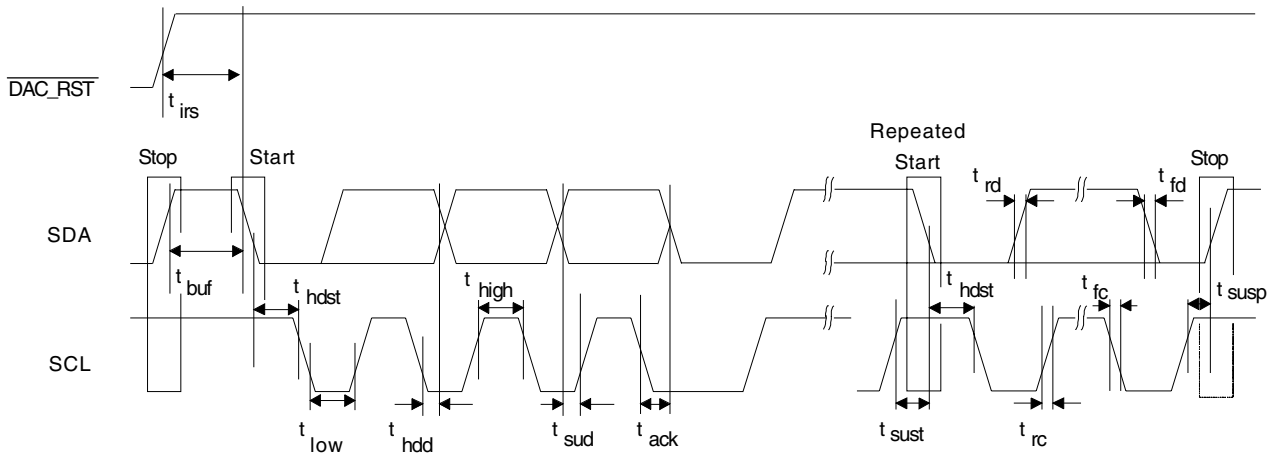


Figure 31. Control Port Timing - I²C Mode

SWITCHING SPECIFICATIONS - CONTROL PORT INTERFACE (Continued)

Parameter		Symbol	Min	Max	Unit
SPI Mode					
CCLK Clock Frequency		f_{sclk}	-	6	MHz
$\overline{\text{DAC_RST}}$ Rising Edge to $\overline{\text{CS}}$ Falling		t_{srs}	500	-	ns
CCLK Edge to $\overline{\text{CS}}$ Falling	(Note 22)	t_{spi}	500	-	ns
$\overline{\text{CS}}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
$\overline{\text{CS}}$ Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	$\frac{1}{\text{MCLK}}$	-	ns
CCLK High Time		t_{sch}	$\frac{1}{\text{MCLK}}$	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 23)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 24)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 24)	t_{f2}	-	100	ns

Notes: 22. t_{spi} only needed before first falling edge of $\overline{\text{CS}}$ after $\overline{\text{DAC_RST}}$ rising edge. t_{spi} = 0 at all other times.

23. Data must be held for sufficient time to bridge the transition time of CCLK.

24. For f_{sclk} < 1 MHz.

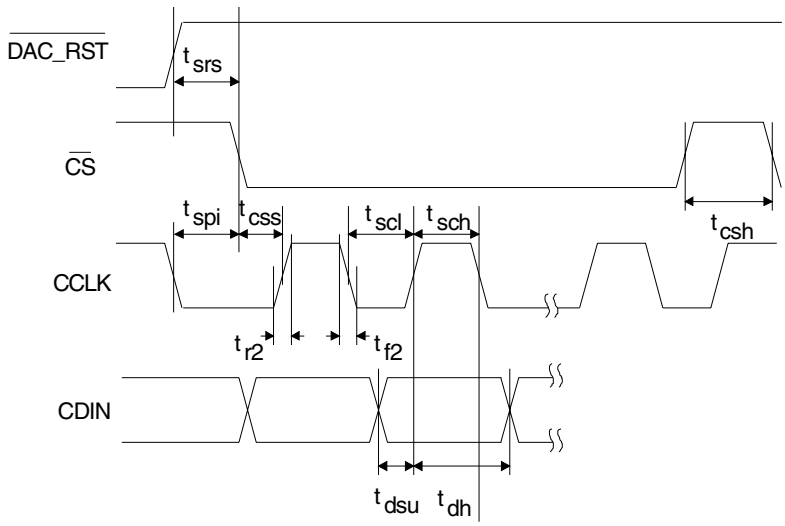


Figure 32. Control Port Timing - SPI Mode

3. TYPICAL CONNECTION DIAGRAM

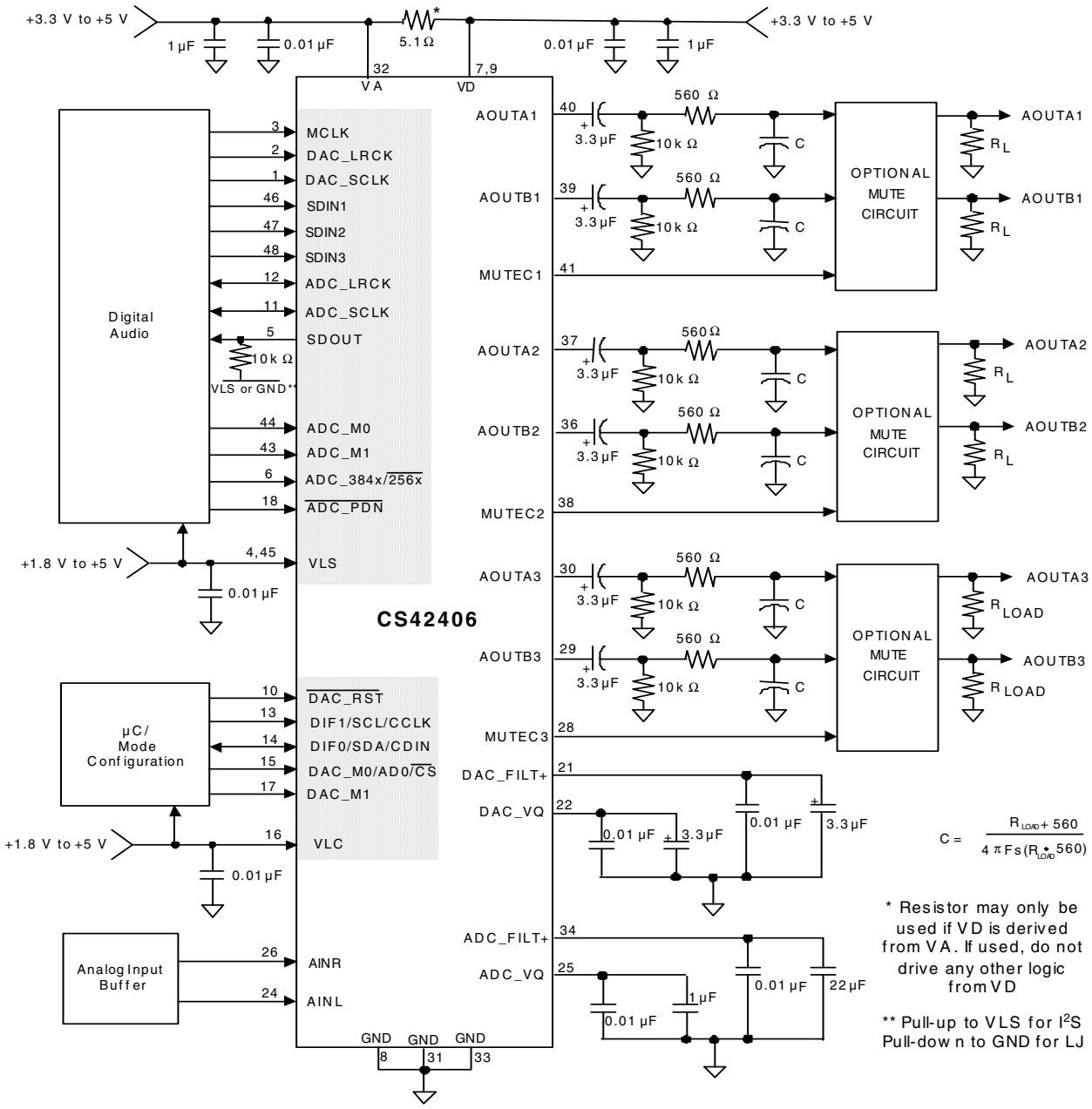


Figure 33. Typical Connection Diagram

4. APPLICATIONS

4.1 Single, Double, and Quad-Speed Modes

4.1.1 ADC Serial Port

The ADC's internal to the CS42406 can support output sample rates from 2 kHz to 200 kHz, and a base MCLK/ADC_LRCK ratio of either 256x or 384x. The proper speed mode can be determined by the desired output sample rate and the external MCLK/ADC_LRCK ratio, as shown in Table 1 and Table 2. Please see section 4.2 for a discussion on how to select the desired speed mode.

Speed Mode	MCLK / ADC_LRCK Ratio	ADC_SCLK / ADC_LRCK Ratio	Output Sample Rate Range (kHz)
Single-Speed Mode	512x	32x, 48x, 64x	43 - 50
	256x	32x, 48x, 64x	2 - 50
Double-Speed Mode	256x	32x, 48x, 64x	86 - 100
	128x	32x, 48x, 64x	50 - 100
Quad-Speed Mode	128x	32x, 48x, 64x	172 - 200
	64x*	64x	100 - 200

* Quad-Speed Mode, 64x only available in Master Mode.

Table 1. ADC Speed Modes and the Associated Output Sample Rates (Fs) for 256x Mode

Speed Mode	MCLK/ADC_LRCK Ratio	ADC_SCLK/ADC_ LRCK Ratio	Output Sample Rate Range (kHz)
Single-Speed Mode	768x	32x, 48x, 64x	43 - 50
	384x	32x, 48x, 64x	2 - 50
Double-Speed Mode	384x	32x, 48x	86 - 100
	192x	32x, 48x	50 - 100
Quad-Speed Mode	192x	32x, 48x	172 - 200
	96x*	48x	100 - 200

* Quad Speed Mode, 96x only available in Master Mode.

Table 2. ADC Speed Modes and the Associated Output Sample Rates (Fs) for 384x Mode

4.1.2 DAC Serial Port

4.1.2a Stand Alone Mode

The DAC's internal to the CS42406 operate in one of four operational modes determined by the DAC_Mx pins when in Stand Alone Mode. Sample rates outside the specified range for each mode are not supported. Refer to Table 3.

DAC_M1	DAC_M0	Input Sample Rate (Fs)	MODE
0	0	4 kHz - 50 kHz	Single-Speed Mode (without De-emphasis)
0	1	32 kHz - 48 kHz	Single-Speed Mode (with De-emphasis)
1	0	50 kHz - 100 kHz	Double-Speed Mode
1	1	100 kHz - 200 kHz	Quad-Speed Mode

Table 3. CS42406 Stand Alone DAC Operational Modes

4.1.2b Control Port Mode

The DAC's operate in one of three operational modes determined by the FM bits (see section 6.1.4) in Control Port mode. Sample rates outside the specified range for each mode are not supported.

FM1	FM0	Input Sample Rate (Fs)	MODE
0	0	4 kHz - 50 kHz	Single-Speed Mode
0	1	50 kHz - 100 kHz	Double-Speed Mode
1	0	100 kHz - 200 kHz	Quad-Speed Mode
1	1	Reserved	Reserved

Table 4. CS42406 Control Port DAC Operational Modes

4.2 ADC Serial Port Operation as Either a Clock Master or Slave

The CS42406 ADC serial port supports operation as either a clock master or slave. As a clock master, the ADC_LRCK and ADC_SCLK pins are outputs with the left/right and serial clocks synchronously generated on-chip. As a clock slave, the ADC_LRCK and ADC_SCLK pins are inputs and require the left/right and serial clocks to be externally generated. The selection of clock master or slave is made via the ADC_Mx pins as shown in Table 5.

ADC_M1	ADC_M0	MODE
0	0	Clock Master, Single-Speed Mode
0	1	Clock Master, Double-Speed Mode
1	0	Clock Master, Quad-Speed Mode
1	1	Clock Slave, All Speed Modes

Table 5. CS42406 ADC Serial Port Mode Control

4.2.1 Operation as a Clock Master

As a clock master, ADC_LRCK and ADC_SCLK operate as outputs. The left/right and serial clocks are internally derived from the master clock with the left/right clock equal to Fs and the serial clock equal to 64x Fs, as shown in Figure 34.

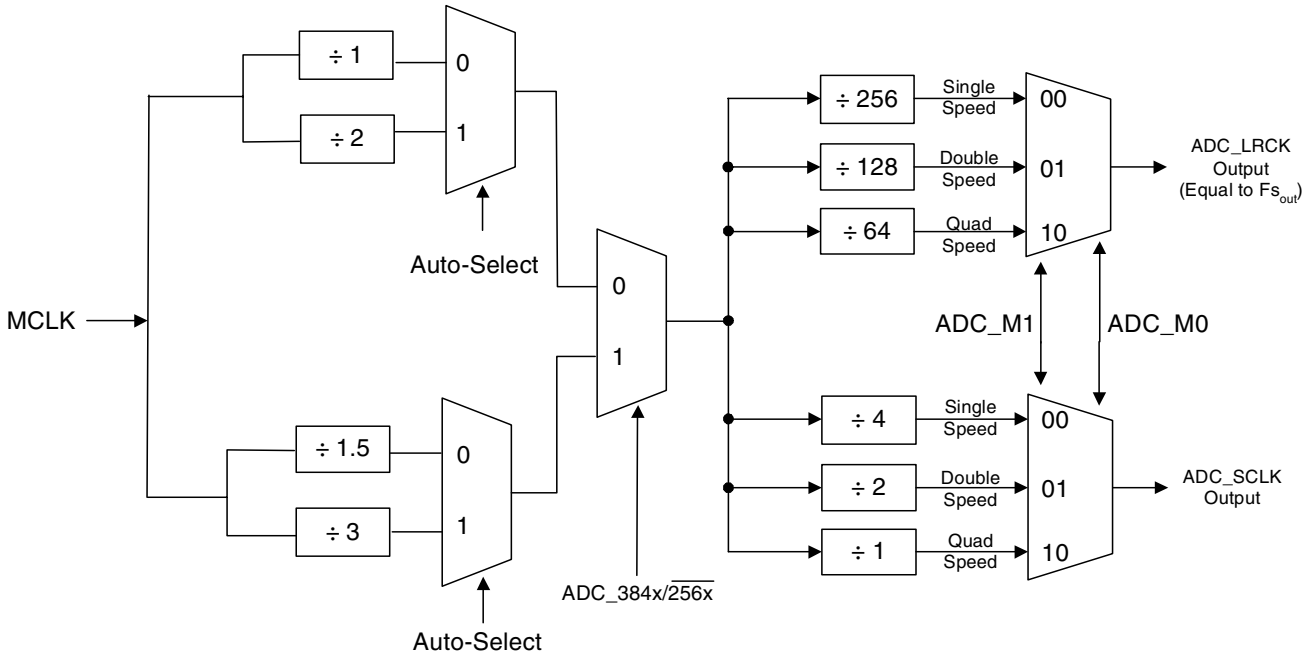


Figure 34. ADC Serial Port, Master Mode Clocking

4.2.2 Operation as a Clock Slave

ADC_LRCK and ADC_SCLK operate as inputs in clock slave mode. It is recommended that the left/right clock be synchronously derived from the master clock and must be equal to Fs. It is also recommended that the serial clock be synchronously derived from the master clock and be equal to 64x Fs to maximize system performance. Please refer to Table 1 and Table 2 for supported SCLK ratios.

A unique feature of the CS42406 ADC serial port is the automatic selection of either Single, Double or Quad-Speed Mode when operating as a clock slave. The auto-mode selection feature supports all standard audio sample rates from 2 to 200 kHz. However, there are ranges of non-standard audio sample rates that are not supported when operating with a fast MCLK (512x/768x, 256x/384x, 128x/192x for Single, Double, and Quad-Speed Modes, respectively). Please refer to Table 1 and Table 2 for supported sample rate ranges.

4.3 Digital Interface Format

4.3.1 DAC Serial Port

The CS42406 DAC serial port will accept audio samples in 1 of 4 digital interface formats in Stand Alone Mode (as illustrated in Table 6), and 1 of 6 formats in Control Port mode (as illustrated in Table 7 on page 41).

4.3.1a Stand Alone Mode

The desired format for the DAC serial port is selected via the DIF1 and DIF0 pins. For an illustration of the required relationship between the DAC_LRCK, DAC_SCLK and SDINx, see Figures 28-30.

DIF1	DIF0	DESCRIPTION	FORMAT	FIGURE
0	0	Left Justified, up to 24-bit Data	0	29
0	1	I²S, up to 24-bit Data	1	28
1	0	Right Justified, 16-bit Data	2	30
1	1	Right Justified, 24-bit Data	3	30

Table 6. DAC Digital Interface Format - Stand Alone Mode

4.3.1b Control Port Mode

The desired format for the DAC serial port is selected via the DIF2, DIF1 and DIF0 bits in the Mode Control 2 register (see section 6.1.2). For an illustration of the required relationship between DAC_LRCK, DAC_SCLK and SDINx, see Figures 28-30.

4.3.2 ADC Serial Port

The CS42406 ADC serial port supports both I²S and Left Justified serial audio formats. Upon start-up, the CS42406 will detect the logic level on SDOUT. A 10 kΩ pull-up resistor to VLS is needed to select I²S format, and a 10 kΩ pull-down resistor to GND is needed to select Left Justified format. Please see Figures 28 and 29 for an illustration of the required relationship between ADC_LRCK, ADC_SCLK, and SDOUT.

4.4 De-Emphasis Control

The CS42406 includes on-chip digital de-emphasis. Figure 35 shows the de-emphasis curve for Fs equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs.

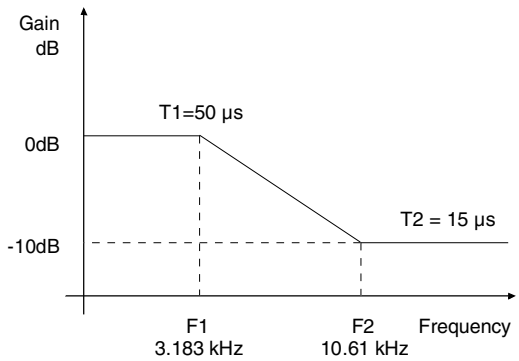


Figure 35. De-Emphasis Curve

Notes: De-emphasis is only available in Single-Speed Mode.

4.4.1 Stand Alone Mode

The operational mode pins, DAC_M1 and DAC_M0, selects the 44.1 kHz de-emphasis filter. Please see section 4.1.2a for the desired de-emphasis control.

4.4.2 Control Port Mode

The Mode Control bits selects either the 32, 44.1, or 48 kHz de-emphasis filter. Please see section 6.1.3 for the desired de-emphasis control.

4.5 Analog Connections

The analog modulator samples the input at 6.144 MHz. The digital filter will reject signals within the stop-band of the filter. However, there is no rejection for input signals which are multiples of the input sampling frequency (n * 6.144 MHz), where n=0, 1, 2, ... Refer to Figure 36 which shows the suggested filter that will attenuate any noise energy at 6.144 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these can degrade signal linearity.

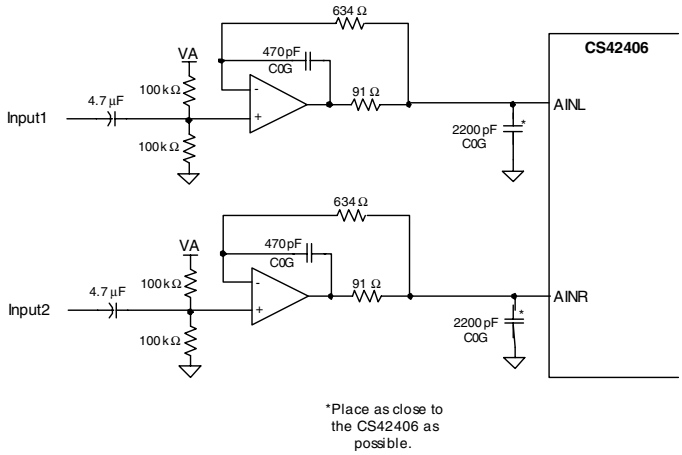


Figure 36. CS42406 Recommended Analog Input Buffer

4.5.1 Capacitor Size on the Reference Pin (FILT+)

The CS42406 requires an external capacitance on the internal reference voltage pin, ADC_FILT+. The size of this decoupling capacitor will affect the low frequency distortion performance as shown in Figure 37, with larger capacitor values used to optimize low frequency distortion performance.

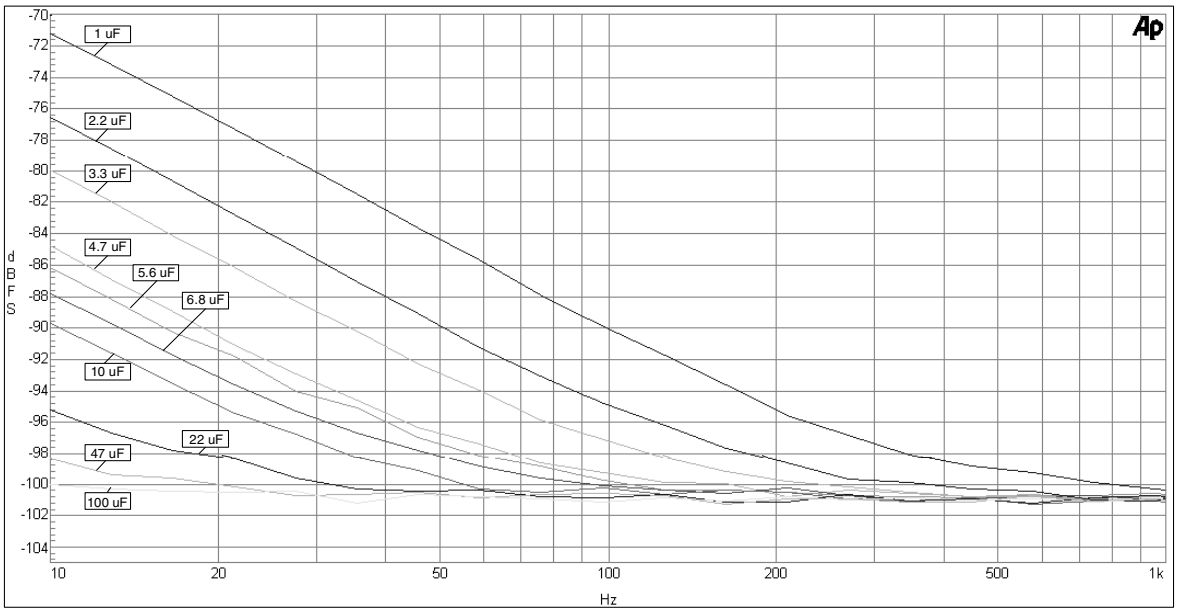


Figure 37. CS42406 ADC: THD+N versus Frequency

4.6 Recommended Power-up Sequence

4.6.1 Stand Alone Mode

1) Hold $\overline{\text{DAC_RST}}$ and $\overline{\text{ADC_PDN}}$ low until the power supplies and configuration pins are stable, and the master and left/right clocks are locked to the appropriate frequencies. In this state, the control port is reset to its default settings.
2) Bring $\overline{\text{DAC_RST}}$ and $\overline{\text{ADC_PDN}}$ high. The CS42406 DAC will remain in a low power state with DAC_VQ low and will initiate the Stand Alone power-up sequence after approximately 512 DAC_LRCK cycles in Single-Speed Mode (1024 DAC_LRCK cycles in Double-Speed Mode, and 2048 DAC_LRCK cycles in Quad-Speed Mode). The CS42406 ADC will begin the power-up sequence immediately following $\overline{\text{ADC_PDN}}$ going high.

4.6.2 Control Port Mode

1) Hold $\overline{\text{DAC_RST}}$ and $\overline{\text{ADC_PDN}}$ low until the power supplies are stable, and the master and left/right clocks are locked to the appropriate frequencies. In this state, the control port is reset to its default settings.
2) Bring $\overline{\text{DAC_RST}}$ and $\overline{\text{ADC_PDN}}$ high. The CS42406 DAC will remain in a low power state with DAC_VQ low.
3) Load the desired register settings while keeping the PDN bit set to 1.
4) Set the PDN bit to 0. This will initiate the power-up sequence for the DAC, which lasts approximately 50 µs when the POPG bit is set to 0. If the POPG bit is set to 1, see Section 4.7 for a complete description of power-up timing.

4.7 Popguard® Transient Control

The CS42406 uses a technique to minimize the effects of output transients during power-up and power-down. This technology, when used with external DC-blocking capacitors in series with the audio outputs, minimizes the audio transients commonly produced by single-ended single-supply converters. It is activated inside the CS42406 when the $\overline{\text{DAC_RST}}$ pin or PDN bit is enabled/disabled and requires no other external control, aside from choosing the appropriate DC-blocking capacitors.

4.7.1 Power-up

When the device is initially powered-up, the audio outputs, AOUTAx and AOUTBx, are clamped to GND. Following a delay of approximately 1000 DAC_LRCK cycles, each output begins to ramp toward the quiescent voltage. Approximately 10,000 DAC_LRCK cycles later, the outputs reach DAC_VQ and audio output begins. This gradual voltage ramping allows time for the external DC-blocking capacitors to charge to the quiescent voltage, minimizing the power-up transient.

4.7.2 Power-down

To prevent transients at power-down, the CS42406 must first enter its power-down state. When this occurs, audio output ceases and the internal output buffers are disconnected from AOUTAx and AOUTBx. In their place, a soft-start current sink is substituted which allows the DC-blocking capacitors to slowly discharge. Once this charge is dissipated, the power to the device may be turned off and the system is ready for the next power-on.

4.7.3 Discharge Time

To prevent an audio transient at the next power-on, the DC-blocking capacitors must fully discharge before turning on the power or exiting the power-down state. If full discharge does not occur, a transient will occur when the audio outputs are initially clamped to GND. The time that the device must remain in the

power-down state is related to the value of the DC-blocking capacitance and the output load. For example, with a 3.3 µF capacitor, the minimum power-down time will be approximately 0.4 seconds.

4.8 Mute Control

The Mute Control pins go high during power-up initialization, reset, muting (see section 6.1.1 and 6.4.1), or if the MCLK to DAC_LRCK ratio is incorrect. These pins are intended to be used as control for external mute circuits to prevent the clicks and pops that can occur in any single-ended single supply system.

Use of the Mute Control function is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle channel noise/signal-to-noise ratios which are only limited by the external mute circuit. Please see the CDB42406 data sheet for a suggested mute circuit.

4.9 Grounding and Power Supply Arrangements

As with any high resolution converter, the CS42406 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 33 shows the recommended power arrangements, with VA, VD, VLS and VLC connected to clean supplies. If the ground planes are split between digital ground and analog ground, the GND pins of the CS42406 should be connected to the analog ground plane.

All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The CDB42406 evaluation board demonstrates the optimum layout and power supply arrangements.

4.9.1 Capacitor Placement

Decoupling capacitors should be placed as close to the CS42406 as possible, with the low value ceramic capacitor being the closest. To further minimize impedance, these capacitors should be located on the same layer as the converter. If desired, all supply pins may be connected to the same supply, but a decoupling capacitor should still be placed on each supply pin and referenced to analog ground. Due to the proximity of the two VD pins (pins 7 and 9), one set of decoupling capacitors will be sufficient for the digital supply. Please refer to Figure 33.

4.10 Control Port Interface

The control port is used to load all the internal register settings (see section 6). The operation of the control port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port operates in one of two modes: I²C or SPI.

Notes: MCLK must be applied during all I²C communication.

4.10.1 Memory Address Pointer (MAP)

The MAP byte precedes the control port register byte during a write operation and is not available again until after a start condition is initiated. During a read operation the byte transmitted after the $\overline{ACK}$ will contain the data of the register pointed to by the MAP (see sections 4.10.2a and 4.10.2b for write/read details).

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	Reserved	MAP3	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	0

4.10.1a INCR (Auto Map Increment)

The CS42406 has MAP auto increment capability enabled by the INCR bit (the MSB) of the MAP. If INCR is set to 0, MAP will stay constant for successive I²C writes or reads and SPI writes. If INCR is set to 1, MAP will auto increment after each byte is written, allowing block reads or writes of successive registers.

Default = '0'
0 - Disabled
1 - Enabled

4.10.1b MAP0-3 (Memory Address Pointer)

Default = '0000'

4.10.2 I²C Mode

In the I²C mode, data is clocked into and out of the bi-directional serial control data line, SDA, by the serial control port clock, SCL. There is no $\overline{CS}$ pin. Pin AD0 enables the user to alter the chip address (001000[AD0][R/$\overline{W}$]) and should be tied to VLC or GND as required, before powering up the device. If the device ever detects a high to low transition on the AD0/$\overline{CS}$ pin after power-up, SPI mode will be selected.

4.10.2a I²C Write

To write to the device, follow the procedure below while adhering to the control port timing as described in "Switching Specifications - Control Port Interface" on page 27.

1) Initiate a START condition to the I²C bus followed by the address byte. The upper 6 bits must be 001000. The seventh bit must match the setting of the AD0 pin, and the eighth must be 0. The eighth bit of the address byte is the R/$\overline{W}$ bit.
2) Wait for an acknowledge (ACK) from the part, then write to the memory address pointer, MAP. This byte points to the register to be written.
3) Wait for an acknowledge (ACK) from the part, then write the desired data to the register pointed to by the MAP.
4) If the INCR bit (see section 4.10.1a) is set to 1, repeat the previous step until all the desired registers are written, then initiate a STOP condition to the bus.
5) If the INCR bit is set to 0 and further I²C writes to other registers are desired, it is necessary to repeat the procedure detailed from step 1. If no further writes to other registers are desired, initiate a STOP condition to the bus.

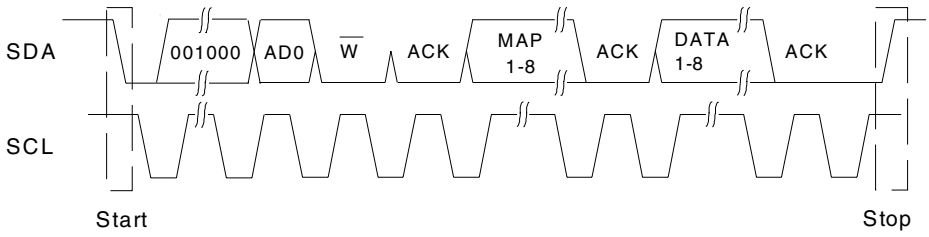


Figure 38. I²C Write

4.10.2b I²C Read

To read from the device, follow the procedure below while adhering to the control port Switching Specifications. During this operation it is first necessary to write to the device, specifying the appropriate register through the MAP.

1) After writing to the MAP (see section 4.10.1), initiate a repeated START condition to the I²C bus followed by the address byte. The upper 6 bits must be 001000. The seventh bit must match the setting of the AD0 pin, and the eighth must be 1. The eighth bit of the address byte is the R/$\overline{W}$ bit.
2) Signal the end of the address byte by *not* issuing an acknowledge. The device will then transmit the contents of the register pointed to by the MAP. The MAP will contain the address of the last register written to the MAP.
3) If the INCR bit is set to 1, the device will continue to transmit the contents of successive registers. Continue providing a clock but do not issue an ACK on the bytes clocked out of the device. After all the desired registers are read, initiate a STOP condition to the bus.
4) If the INCR bit is set to 0 and further I²C reads from other registers are desired, it is necessary to repeat the procedure detailed from step 1. If no further reads from other registers are desired, initiate a STOP condition to the bus.

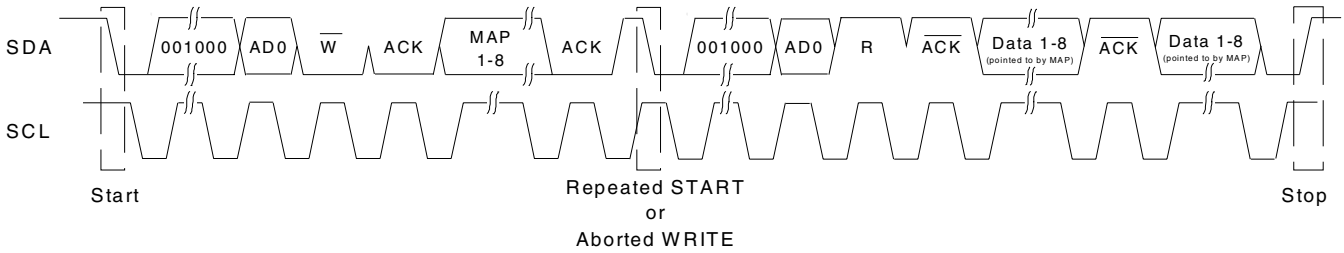


Figure 39. I²C Read

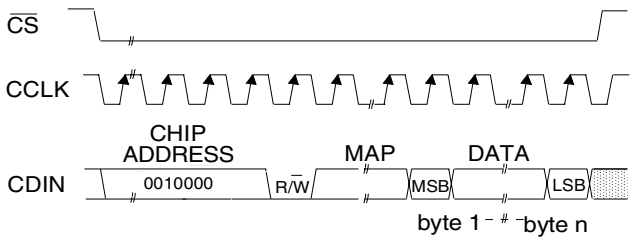
4.10.3 SPI Mode

In SPI mode, data is clocked into the serial control data line, CDIN, by the serial control port clock, CCLK (see Figure 40 for the clock to data relationship). There is no AD0 pin. Pin $\overline{CS}$ is the chip select signal and is used to control SPI writes to the control port. When the device detects a high to low transition on the AD0/$\overline{CS}$ pin after power-up, SPI mode will be selected. All signals are inputs and data is clocked in on the rising edge of CCLK.

4.10.3a SPI Write

To write to the device, follow the procedure below while adhering to the control port Switching Specifications.

1) Bring $\overline{CS}$ low.
2) The address byte on the CDIN pin must then be 00100000.
3) Write to the memory address pointer, MAP. This byte points to the register to be written.
4) Write the desired data to the register pointed to by the MAP.
5) If the INCR bit (see section 4.10.1a) is set to 1, repeat the previous step until all the desired registers are written, then bring $\overline{CS}$ high.
6) If the INCR bit is set to 0 and further SPI writes to other registers are desired, it is necessary to bring $\overline{CS}$ high, and repeat the procedure detailed from step 1. If no further writes to other registers are desired, bring $\overline{CS}$ high.



MAP = Memory Address Pointer

Figure 40. SPI Write

5. REGISTER QUICK REFERENCE

Addr	Function	7	6	5	4	3	2	1	0
1h	Mode Control 1	AMUTE	DIF2	DIF1	DIF0	DEM1	DEM0	FM1	FM0
	default	1	0	0	0	0	0	0	0
2h	Invert Signal	Reserved	Reserved	INV_B3	INV_A3	INV_B2	INV_A2	INV_B1	INV_A1
	default	0	0	0	0	0	0	0	0
3h	Mixing Control P1	Reserved	Reserved	Reserved	Reserved	P1ATAPI3	P1ATAPI2	P1ATAPI1	P1ATAPI0
	default	0	0	0	0	1	0	0	1
4h	Mixing Control P2	Reserved	Reserved	Reserved	Reserved	P2ATAPI3	P2ATAPI2	P2ATAPI1	P2ATAPI0
	default	0	0	0	0	1	0	0	1
5h	Mixing Control P3	Reserved	Reserved	Reserved	Reserved	P3ATAPI3	P3ATAPI2	P3ATAPI1	P3ATAPI0
	default	0	0	0	0	1	0	0	1
6h	Volume Control A1	A1_MUTE	A1_VOL6	A1_VOL5	A1_VOL4	A1_VOL3	A1_VOL2	A1_VOL1	A1_VOL0
	default	0	0	0	0	0	0	0	0
7h	Volume Control B1	B1_MUTE	B1_VOL6	B1_VOL5	B1_VOL4	B1_VOL3	B1_VOL2	B1_VOL1	B1_VOL0
	default	0	0	0	0	0	0	0	0
8h	Volume Control A2	A2_MUTE	A2_VOL6	A2_VOL5	A2_VOL4	A2_VOL3	A2_VOL2	A2_VOL1	A2_VOL0
	default	0	0	0	0	0	0	0	0
9h	Volume Control B2	B2_MUTE	B2_VOL6	B2_VOL5	B2_VOL4	B2_VOL3	B2_VOL2	B2_VOL1	B2_VOL0
	default	0	0	0	0	0	0	0	0
0Ah	Volume Control A3	A3_MUTE	A3_VOL6	A3_VOL5	A3_VOL4	A3_VOL3	A3_VOL2	A3_VOL1	A3_VOL0
	default	0	0	0	0	0	0	0	0
0Bh	Volume Control B3	B3_MUTE	B3_VOL6	B3_VOL5	B3_VOL4	B3_VOL3	B3_VOL2	B3_VOL1	B3_VOL0
	default	0	0	0	0	0	0	0	0
0Ch	Mode Control 2	SZC1	SZC0	CPEN	PDN	POPG	FREEZE	Reserved	SNGLVOL
	default	1	0	0	1	1	0	0	0

6. REGISTER DESCRIPTIONS

Note: All registers are read/write in I²C mode and write only in SPI, unless otherwise stated.

6.1 MODE CONTROL 1 (ADDRESS 01H)

7	6	5	4	3	2	1	0
AMUTE	DIF2	DIF1	DIF0	DEM1	DEM0	FM1	FM0
1	0	0	0	0	0	0	0

6.1.1 AUTO-MUTE (AMUTE) BIT 7

Default = 1
0 - Disabled
1 - Enabled

Function:

The CS42406 DAC output will mute following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting is done independently for each channel. The quiescent voltage on the output will be retained and the Mute Control pin will go active during the mute period. The muting function is affected, similar to volume control changes, by the Soft and Zero Cross bits in the Power and Muting Control register.

6.1.2 DIGITAL INTERFACE FORMAT (DIF) BIT 6-4

Default = 000 - Format 0 (Left Justified, up to 24-bit data)

Function:

The required relationship between the DAC_LRCK, DAC_SCLK, and SDINx is defined by the Digital Interface Format and the options are detailed in Figures 28-30.

DIF2	DIF1	DIF0	DESCRIPTION	Format	FIGURE
0	0	0	Left Justified, up to 24-bit data	0	28
0	0	1	I²S, up to 24-bit data	1	29
0	1	0	Right Justified, 16-bit data	2	30
0	1	1	Right Justified, 24-bit data	3	30
1	0	0	Right Justified, 20-bit data	4	30
1	0	1	Right Justified, 18-bit data	5	30
1	1	0	Reserved	-	-
1	1	1	Reserved	-	-

Table 7. Digital Interface Formats - Control Port Mode

6.1.3 DE-EMPHASIS CONTROL (DEM) BIT 3-2

Default = 00
00 - Disabled
01 - 44.1 kHz
10 - 48 kHz
11 - 32 kHz

Function:

Selects the appropriate digital filter to maintain the standard 15 µs/50 µs digital de-emphasis filter response at 32, 44.1 or 48 kHz sample rates. (See Figure 35.)

Note: De-emphasis is only available in Single-Speed Mode.

6.1.4 FUNCTIONAL MODE (FM) BIT 1-0

Default = 00
00 - Single-Speed Mode (4 to 50 kHz sample rates)
01 - Double-Speed Mode (50 to 100 kHz sample rates)
10 - Quad-Speed Mode (100 to 200 kHz sample rates)
11 - Reserved

Function:

Selects the required range of input sample rates.

6.2 INVERT SIGNAL (ADDRESS 02H)

7	6	5	4	3	2	1	0
Reserved	Reserved	INV_B3	INV_A3	INV_B2	INV_A2	INV_B1	INV_A1
0	0	0	0	0	0	0	0

6.2.1 INVERT SIGNAL POLARITY (INV_XX) BIT 5-0

Default = 0
0 - Disabled
1 - Enabled

Function:

When enabled, these bits invert the signal polarity for each of their respective channels.

6.3 MIXING CONTROL PAIR 1 (CHANNELS A1 & B1) (ADDRESS 03H) MIXING CONTROL PAIR 2 (CHANNELS A2 & B2) (ADDRESS 04H) MIXING CONTROL PAIR 3 (CHANNELS A3 & B3) (ADDRESS 05H)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	PxATAPI3	PxATAPI2	PxATAPI1	PxATAPI0
0	0	0	0	1	0	0	1

6.3.1 ATAPI CHANNEL MIXING AND MUTING (ATAPI) BIT 3-0

Default = 1001 - AOUTAx = L, AOUTBx = R (Stereo)

Function:

The CS42406 implements the channel mixing functions of the ATAPI CD-ROM specification. Refer to Table 8 and Figure 41 for additional information.

Note: All mixing functions occur prior to the digital volume control. Mixing only occurs in channel pairs.

ATAPI3	ATAPI2	ATAPI1	ATAPI0	AOUTAx	AOUTBx
0	0	0	0	MUTE	MUTE
0	0	0	1	MUTE	R
0	0	1	0	MUTE	L
0	0	1	1	MUTE	[(L+R)/2]
0	1	0	0	R	MUTE
0	1	0	1	R	R
0	1	1	0	R	L
0	1	1	1	R	[(L+R)/2]
1	0	0	0	L	MUTE
1	0	0	1	L	R
1	0	1	0	L	L
1	0	1	1	L	[(L+R)/2]
1	1	0	0	[(L+R)/2]	MUTE
1	1	0	1	[(L+R)/2]	R
1	1	1	0	[(L+R)/2]	L
1	1	1	1	[(L+R)/2]	[(L+R)/2]

Table 8. ATAPI Decode

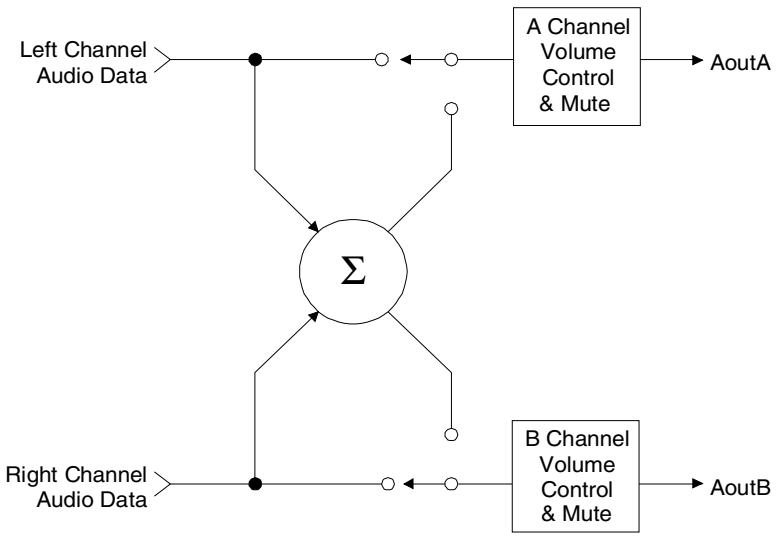


Figure 41. ATAPI Block Diagram

6.4 VOLUME CONTROL (ADDRESSES 06H - 0BH)

7	6	5	4	3	2	1	0
xx_MUTE	xx_VOL6	xx_VOL5	xx_VOL4	xx_VOL3	xx_VOL2	xx_VOL1	xx_VOL0
0	0	0	0	0	0	0	0

6.4.1 MUTE (MUTE) BIT 7

Default = 0

0 - Disabled

1 - Enabled

Function:

The CS42406 DAC output converter output will mute when enabled. The quiescent voltage on the output will be retained. The muting function is affected, similar to attenuation changes, by the Soft and Zero Cross bits. The MUTECx pins will go active during the mute period if the Mute function is enabled for both channels in the pair.

6.4.2 DAC VOLUME CONTROL (XX_VOL) BIT 6-0

Default = 0

Function:

The Digital Volume Control registers allow independent control of the signal levels in 1 dB increments from 0 to -119 dB. Volume settings are decoded as shown in Table 9. The volume changes are implemented as dictated by the Soft Ramp and Zero Cross bits. All volume settings less than -119 dB are equivalent to enabling the MUTE bit.

Binary Code	Decimal Value	Volume Setting
0001010	10	-10 dB
0010100	20	-20 dB
0101000	40	-40 dB
0111100	60	-60 dB
1011010	90	-90 dB

Table 9. Example Digital Volume Settings

6.5 MODE CONTROL 2 (ADDRESS 0CH)

7	6	5	4	3	2	1	0
SZC1	SZC0	CPEN	PDN	POPG	FREEZE	RESERVED	SNGLVOL
1	0	0	1	1	0	0	0

6.5.1 SOFT RAMP AND ZERO CROSS CONTROL (SZC) BIT 7-6

Default = 10

00 - Immediate Change

01 - Zero Cross

10 - Soft Ramp

11 - Soft Ramp and Zero Cross

Function:

Immediate Change

When Immediate Change is selected all level changes will be implemented immediately in one step.

Zero Cross

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz input sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 DAC_LRCK periods.

Soft Ramp and Zero Cross

Soft Ramp and Zero Cross dictates that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and will be implemented on successive signal zero crossings. The 1/8 dB level changes will occur after timeout periods between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz input sample rate) if the signal does not encounter zero crossings. The zero cross function is independently monitored and implemented for each channel.

6.5.2 CONTROL PORT ENABLE (CPEN) BIT 5

Default = 0
0 - Disabled
1 - Enabled

Function:

The Control Port will become active and reset to the default settings when this function is enabled.

6.5.3 POWER DOWN (PDN) BIT 4

Default = 1
0 - Disabled
1 - Enabled

Function:

The DAC will enter a low-power state when this function is enabled, but the contents of the control registers will be retained in this mode. The power-down bit defaults to 'enabled' on power-up and must be disabled before normal operation in Control Port mode can occur.

6.5.4 POPGUARD® TRANSIENT CONTROL (POPG) BIT 3

Default = 1
0 - Disabled
1 - Enabled

Function:

The PopGuard® Transient Control allows the quiescent voltage to slowly ramp to and from 0 volts to the quiescent voltage during power-on or power-off when this function is enabled. Please see section 4.7 for implementation details.

6.5.5 FREEZE CONTROLS (FREEZE) BIT 2

Default = 0
0 - Disabled
1 - Enabled

Function:

This function allows modifications to be made to the registers without the changes taking effect until the FREEZE is disabled. To have multiple changes in the control port registers take effect simultaneously, enable the FREEZE bit, make all register changes, then disable the FREEZE bit.

6.5.6 SINGLE VOLUME CONTROL (SNGLVOL) BIT 0

Default = 0
0 - Disabled
1 - Enabled

Function:

The individual channel volume levels are independently controlled by their respective Volume Control Bytes when this function is disabled. When enabled, the volume on all channels is determined by the A1 Channel Volume Control Byte, and the other Volume Control Bytes are ignored.

7 PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog input for a full-scale digital output.

Gain Drift

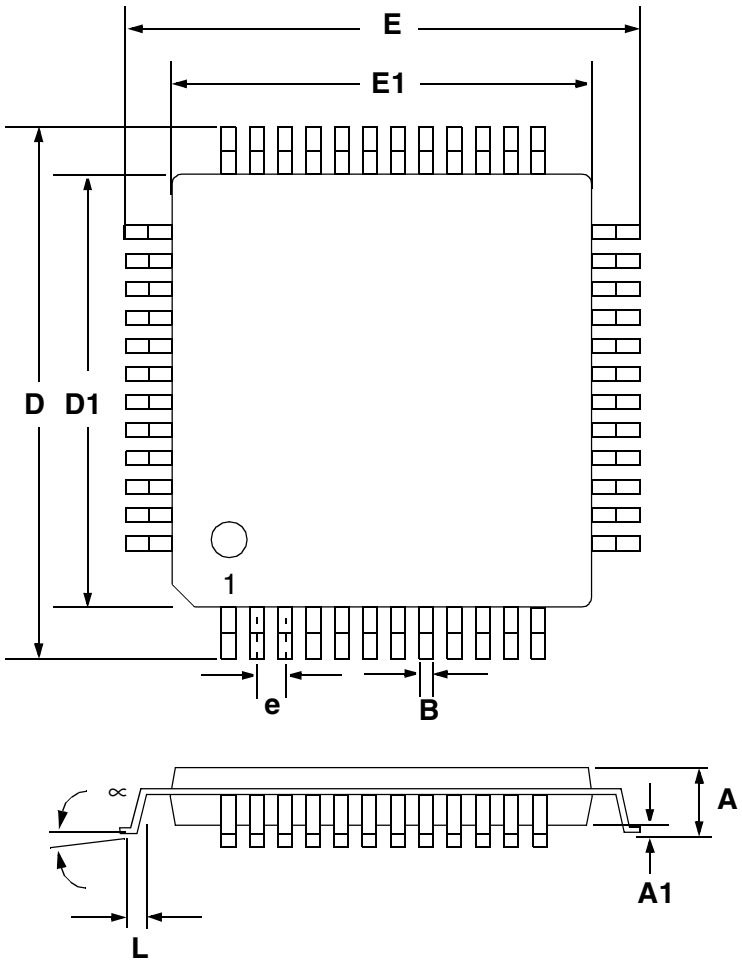
The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

8. PACKAGE DIMENSIONS

48L LQFP PACKAGE DRAWING



	INCHES			MILLIMETERS		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	---	0.055	0.063	---	1.40	1.60
A1	0.002	0.004	0.006	0.05	0.10	0.15
B	0.007	0.009	0.011	0.17	0.22	0.27
D	0.343	0.354	0.366	8.70	9.0 BSC	9.30
D1	0.272	0.28	0.280	6.90	7.0 BSC	7.10
E	0.343	0.354	0.366	8.70	9.0 BSC	9.30
E1	0.272	0.28	0.280	6.90	7.0 BSC	7.10
e*	0.016	0.020	0.024	0.40	0.50 BSC	0.60
L	0.018	0.24	0.030	0.45	0.60	0.75
∝	0.000°	4°	7.000°	0.00°	4°	7.00°

* Nominal pin pitch is 0.50 mm

Controlling dimension is mm.
JEDEC Designation: MS026

9. REVISION HISTORY

Revision	Date	Changes
PP1	August 2003	Initial Release
PP2	March 2004	***Added*** Revision History Table. ***Changed*** "Gain Error" from ±5% to ±10% in the ADC Analog Characteristics. ***Removed*** "Inter Channel" and "Intra Channel Phase Deviation" specification on page 11 and page 16. ***Removed*** ADC & DAC FILT+ "Output Impedance" and "Current Source Sink" specification on page 19. ***Changed*** maximum V_{OL} from 13% to 15% on page 20. ***Changed*** MCLK min/max duty cycle from 40/60% to 45/55% on page 23. ***Added*** Figure 37 on page 34.
PP3	August 2004	***Added*** lead free part numbers.
PP4	December 2004	***Corrected*** typographical errors.
PP5	December 2004	***Removed*** automotive part *CS42406-DQZ* ordering availability and performance specifications. ***Added*** Note 3 to 4 on page 8 limiting VA, VD and VL operation. ***Modified*** table "Switching Characteristics - ADC Serial Audio Port" on page 23 to highlight 256x and 384x mode. ***Added*** "ADC_LRCK Frequency", "SCLK Duty Cycle (Slave Mode)" and setup & hold timing specifications in "Switching Characteristics - ADC Serial Audio Port" on page 23. ***Removed*** ADC_SCLK high/low timing and the "ADC_SCLK falling to SDOUT valid" specifications from "Switching Characteristics - ADC Serial Audio Port" on page 23. ***Modified*** Figures 24 to 27 on page 25 to reflect timing specifications. ***Corrected*** Typical Connection Diagram, Figure 33 on page 29. ***Added*** ADC_SCLK/ADC_LRCK ratio parameters in Table 1 to 2 on page 30. ***Changed*** recommended anti-aliasing capacitor value from 2700 pF to 2200 pF in Figure 36 "CS42406 Recommended Analog Input Buffer" on page 34.

Table 10. Revision History

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to **http://www.cirrus.com/**

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