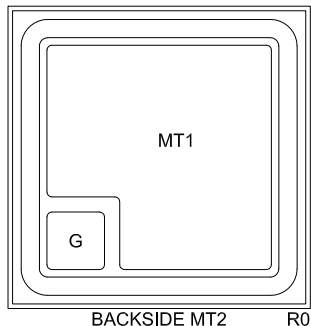


CPQ114-CQD-8M3

Three Quadrant TRIAC Die

8.0 Amp, 600 Volt

The CPQ114-CQD-8M3 is a silicon TRIAC designed for full wave AC control applications featuring gate triggering in three quadrants.



MECHANICAL SPECIFICATIONS:

Die Size	114 x 114 MILS
Die Thickness	8.3 MILS
Gate Bonding Pad Size	21.7 x 21.7 MILS
MT1 Bonding Pad Size	84.6 x 84.6 MILS
Top Side Metalization	Al – 45,000Å
Back Side Metalization	Al/Ti/Ni/Ag – 36,600Å
Scribe Alley Width	3.0 MILS
Wafer Diameter	4 INCHES
Gross Die Per Wafer	787

MAXIMUM RATINGS: ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

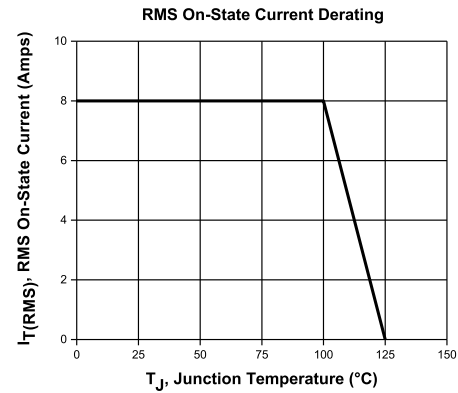
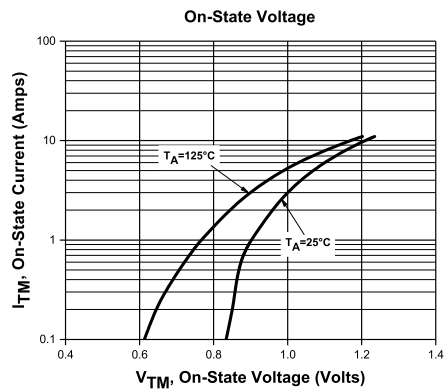
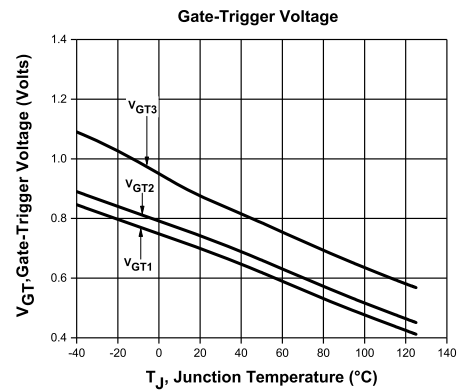
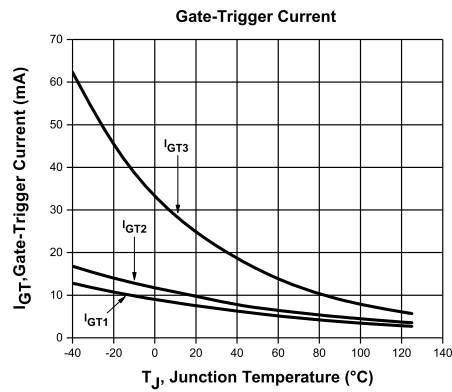
	SYMBOL		UNITS
Peak Repetitive Off-State Voltage	V_{DRM}	600	V
RMS On-State Current ($T_J=100^{\circ}\text{C}$)	$I_{\text{T(RMS)}}$	8.0	A
Peak One Cycle Surge Current, 50Hz	I_{TSM}	70	A
I^2t Value for Fusing, $t=10\text{ms}$	I^2t	32	A^2s
Peak Gate Current, $t_p=20\mu\text{s}$ ($T_J=125^{\circ}\text{C}$)	I_{GM}	4.0	A
Critical Rate of Rise of On-State Current Repetitive, $f=100\text{Hz}$ ($T_J=125^{\circ}\text{C}$)	di/dt	50	$\text{A}/\mu\text{s}$
Operating Junction Temperature	T_J	-40 to +125	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	-40 to +150	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS: ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

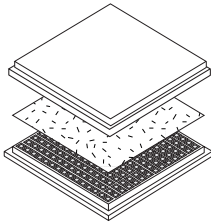
SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
$I_{\text{DRM}}, I_{\text{RRM}}$	$V_{\text{DRM}}, V_{\text{RRM}}=600\text{V}$		5.0	μA
I_{GT}	$V_{\text{D}}=12\text{V}, R_{\text{L}}=30\Omega$, QUAD I, II, III		50	mA
I_{H}	$V_{\text{D}}=12\text{V}, I_{\text{T}}=100\text{mA}$		50	mA
V_{GT}	$V_{\text{D}}=12\text{V}, R_{\text{L}}=30\Omega$, QUAD I, II, III		1.3	V
V_{TM}	$I_{\text{TM}}=11\text{A}, t_p=380\mu\text{s}$		1.55	V
dv/dt	$V_{\text{D}}=2/3 V_{\text{DRM}}, R_{\text{GK}}=\infty, T_J=125^{\circ}\text{C}$		1000	$\text{V}/\mu\text{s}$

CPQ114-CQD-8M3

Typical Electrical Characteristics



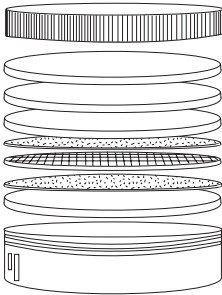
BARE DIE PACKING OPTIONS



BARE DIE IN TRAY (WAFFLE) PACK

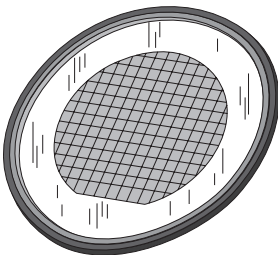
CT: Singulated die in tray (waffle) pack.
(example: CP211-PART NUMBER-CT)

CM: Singulated die in tray (waffle) pack 100% visually inspected as per MIL-STD-750, (method 2072 transistors, method 2073 diodes).
(example: CP211-PART NUMBER-CM)



UNSAWN WAFER

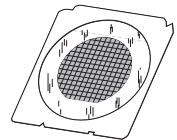
WN: Full wafer, unsawn, 100% tested with reject die inked.
(example: CP211-PART NUMBER-WN)



SAWN WAFER ON PLASTIC RING

WR: Full wafer, sawn and mounted on plastic ring,
100% tested with reject die inked.
(example: CP211-PART NUMBER-WR)

Please note: Sawn Wafer on Metal Frame (WS) is possible as a special order. Please contact your Central Sales Representative at 631-435-1110.



Visit the Central website for a complete listing of specifications:
www.centrasemi.com/bdspecs

OUTSTANDING SUPPORT AND SUPERIOR SERVICES



PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

REQUESTING PRODUCT PLATING

1. If requesting Tin/Lead plated devices, add the suffix " TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
2. If requesting Lead (Pb) Free plated devices, add the suffix " PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

CONTACT US

Corporate Headquarters & Customer Support Team

Central Semiconductor Corp.
145 Adams Avenue
Hauppauge, NY 11788 USA
Main Tel: (631) 435-1110
Main Fax: (631) 435-1824
Support Team Fax: (631) 435-3388
www.centrasemi.com

Worldwide Field Representatives:
www.centrasemi.com/wwreps

Worldwide Distributors:
www.centrasemi.com/wwdistributors

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