CPLD I/O User Guide

UG445 (v1.2) January 14, 2014

XILINX®



DISCLAIMER

The information disclosed to you hereunder (the “Materials”) is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx’s limited warranty, please refer to Xilinx’s Terms of Sale which can be viewed at www.xilinx.com/legal.htm#tos; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx’s Terms of Sale which can be viewed at www.xilinx.com/legal.htm#tos.

© Copyright 2007–2014 Xilinx, Inc. Xilinx, the Xilinx logo, Artix, ISE, Kintex, Spartan, Virtex, Vivado, Zynq, and other designated brands included herein are trademarks of Xilinx in the United States and other countries. All other trademarks are the property of their respective owners.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
6/26/2007	1.0	Initial Xilinx release.
11/27/2007	1.1	• Added “JTAG Termination,” page 12. • Updated Figure 4. • Added sentence at the end of first paragraph after Figure 5.
01/14/2014	1.2	JTAG pin information changed in “JTAG Termination,” page 12. Values in “Maximum I/O Power Dissipation,” page 15 under “When sourcing 40 mA, the voltage at the output of the CPLD will be 2.3V...” changed.

Table of Contents

Preface: About This Guide

Guide Contents 5
Additional Resources 5
Additional Documentation 5
Conventions 6
Typographical 6
Online Document 7

CPLD I/O User Guide

Terminations 9
Termination Options 9
Setting Termination Modes in Software 10
Termination Mode for Outputs 10
Bus-hold/Keeper 10
Impedance of the Bus-hold, Keeper, or Pull-up 11
Half Latch 11
CoolRunner XPLA3 11
CoolRunner-II 12
XC9500, XC9500XL, and XC9500XV 12
JTAG Termination 12
Thresholds 12
I/V Curves 12
Reading I/V Curves 13
Maximum I/O Power Dissipation 15
Drive Strength 16
Power, Sequencing, and Slew Rates 17
Hot-Swappable 17
Powering CPLDs 17
Power Sequencing 17
Current Consumption 20
5V Tolerance 20
I/O Standards 22
Simultaneous Switching Output Limits 22
Decoupling Guidelines 22
Schmitt Trigger 22
Slew Rate 23

About This Guide

The *CPLD I/O User Guide* describes the behavior of the I/Os under various operating conditions. It describes how to use the different termination modes, how to understand thresholds, and how loading affects the I/Os.

Guide Contents

This manual contains the following topics:

- "Terminations" provides a brief description of the different terminations available in Xilinx CPLDs. It also contains details on how to use termination.
- "Thresholds" describes in detail the conditions that affect the threshold levels. It gives examples on how to use the I/V curves to understand what thresholds are under nominal operating conditions.
- "Power, Sequencing, and Slew Rates" describes effects of powering, sequencing, and slew rates on I/Os. It includes details on how much voltage can be driven into a Xilinx CPLD and the behavior of the I/Os in different operating conditions.

Additional Resources

To find additional documentation, see the Xilinx Web site at:

www.xilinx.com/support/documentation/index.htm.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx Support Web site at:

www.xilinx.com/support.

Additional Documentation

Xilinx ISE Software Manuals are available for download at:

www.xilinx.com/support/software_manuals.htm.

The following documents are also available:

- DS012 *CoolRunner™ XPLA3 CPLD Data Sheet*

  This data sheet contains the electrical and functional specifications of the CoolRunner XPLA3 CPLD.

- DS090 *CoolRunner-II CPLD Family Data Sheet*

  This data sheet contains the electrical and functional specifications of the CoolRunner-II CPLD.

- DS054 *XC9500XL High-Performance CPLD Family Data Sheet*

  This data sheet describes the XC9500XL 3.3V CPLD Family, including architecture, basic family device descriptions, and package options.

- DS049 *XC9500XV High-Performance CPLD Family Data Sheet**

  This data sheet describes the XC9500XV 2.5V CPLD Family, including architecture, basic family device descriptions, and package options.

  *Please note that this family has been discontinued and is not recommended for use in new designs. For further information, please see XCN07010.

- UG112 *Device Package User Guide*

  This guide discusses thermal, electrical, moisture, and soldering characteristics of Xilinx device packages.

- XAPP150 *I/V Curves for Xilinx FPGA and CPLD Families*

  This application note describes the output sink and source current for average processing, nominal supply voltage, and room temperature.

- XAPP342 *XPLA3 I/O Cell Characteristics Application Note*

  This application note describes the features and benefits of the I/O cells provided by Xilinx CoolRunner XPLA3 CPLDs.

- XAPP382 *CoolRunner-II I/O Characteristics Application Note*

  This document is a comprehensive description of the I/O structure of the CoolRunner-II CPLD family.

- XAPP429 *5V Tolerance Techniques for CoolRunner-II Devices Application Note*

  This application note describes several different methods for interfacing 5V signals to CoolRunner-II devices.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *design_name*
Italic font	References to other manuals	See the *Development System Reference Guide* for more information.

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. In the example in Figure 2, if the Volmax is 0.5V, you can sink 21 mA.
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

CPLD I/O User Guide

Terminations

Terminations are a vital aspect of a robust transmission line. The on-chip termination of the CPLD I/Os eliminate the need for external termination. It is strongly recommended not to float CMOS inputs as this increases power. The on-chip termination of the CPLDs can be used to minimize power without the need for external components. The following section discusses the termination options available in the different CPLD families and how to utilize the features.

Termination Options

The user can select the termination type for the unused I/Os and the Input and Tristate I/Os separately.

For the Input and Tristate I/O termination mode, the options are (default in parentheses):

Note: Bus-hold and Keeper terms can be used interchangeably.

- XC9500 XL/ XV: Float, Keeper (keeper)
- CoolRunner™ XPLA3: Float, Pull-up (pull-up)
- CoolRunner™-II: Float, Pull-up, Keeper (keeper)

For the unused I/Os, the options are (default in parentheses):

- XC9500 /XL/XV: Float, Ground (float)
- CoolRunner XPLA3: Float, Pull-up (pull-up)
- CoolRunner-II: Float, Ground, Pull-up, Keeper (ground)

For CoolRunner-II devices, it is possible to have a combination of multiple termination modes for used and unused I/Os. However, not all combinations are possible. Table 1 lists permitted combinations.

Table 1: **Input Termination Schemes**

Possible Input Termination Schemes
All Pull-up
All Bus-hold
Combination of Pull-up and Float
Combination of Bus-hold and Float
All Float

Table 2: **Unused I/O Termination Schemes**

Unused I/O Termination Schemes
All Pulled-up (not possible if Bus-hold is selected for input termination)
All Bus-hold (not possible if Pull-up is selected for input termination)
All Configurable Ground
All Float

It is not recommended to float a CPLD I/O, as it consumes extra current than if held in a known state. You should select float as a termination mode only if the pin has external terminations.

Setting Termination Modes in Software

The termination modes can either be selected globally, as CPLDFit options, or on a pin-by-pin basis using constraints.

If you are using the ISE tools GUI:

1. Select the top level in the Sources window.
2. In the Processes window, select CPLDFit.
3. Right-click and select Properties. The Fit Properties dialog box appears.

There is a drop-down menu for the Input and Tristate I/O termination mode. For the CoolRunner-II and CoolRunner XPLA3, there is a drop-down menu for the Unused I/O Pad termination. However, if the design targets an XC9500, XC9500XL, or XC9500XV, there are only two options for the unused termination; by default, this is float. The user has the option to Create Programmable Ground pins on Unused I/Os; if this check box is ticked, the pin can be considered as outputs driving low.

To constrain the termination on a pin-by-pin basis, use the following UCF example:

```
NET "My_NET" KEEPER;
```

For more information on the constraints syntax, see the Constraints Guide in the software manuals, found at:

www.xilinx.com/support/software_manuals.htm.

Termination Mode for Outputs

It is not possible or necessary to select a termination mode for output pins. The output of a macro cell, which drives the output, is always at logic 1 or logic 0. Therefore, there is no need to terminate the output. Outputs that are in a Tristate condition can be terminated.

Bus-hold/Keeper

The bus-hold or keeper is present in the CoolRunner-II, XC9500, XC9500XL, and XC9500XV families. It is internal circuitry that drives the last known value on the I/O into the device. The bus-hold circuit is only on when the device is in user mode and keeper termination mode is selected. Therefore, if the device is unconfigured or in the In-System-

Programming (ISP) mode, the bus-hold is not active. If the device loses V_{CCINT}, the I/Os are in a pull-up state. The Bus-hold is enabled by Vccint, but pulls to Vccio.

Impedance of the Bus-hold, Keeper, or Pull-up

The values given in this section are typical numbers that cannot be guaranteed as the impedance varies over process, voltage, and temperature.

CoolRunner-II

The effective resistance of the termination circuitry varies with V_{CCIO}.

At V_{CCIO} = 1.8V, the effective resistance is typically 100 kΩ.

As V_{CCIO} increases, the effective resistance decreases. Typical for V_{CCIO} =3.3V is 42 kΩ.

The minimum resistance value presented by the termination circuitry is 20 kΩ.

CoolRunner XPLA3

The CoolRunner does not have a bus-hold. It does have an internal pull-up that has been characterized at approximately 60 to 150 kΩ.

XC9500, XC9500XL, and XC9500XV

The bus hold impedance is approximately 25 kΩ, with a range of 15 kΩ to 70 kΩ (the lower range at lower temperatures).

Half Latch

CoolRunner XPLA3

The CoolRunner XPLA3 has a half latch feature on the I/Os. The half latch is essentially a pull-up that turns on only when the I/O pin voltage is in the linear region (not a 0, not a 1). So, when the voltage at the pin is in the trip-point region or higher, the half latch is enabled. The idea is that it prevents signals from floating, and therefore, saves power. This half latch cannot be disabled.

The device data sheet states the following: “The I/O is configured as an input (or 3-stated output), a half latch feature exists. This half latch pulls the input high (through a weak pull-up) if the input should float and cross the threshold.”

This means that the half latch feature exists even when the pull-up is not selected. If you want to pull down the input, a resistor strong enough to overcome the half latch must be used. Xilinx recommends that any pull-down resistor value be 10 kΩ or less. Xilinx does not recommend using CoolRunner XPLA3 devices in any design that requires I/O pins to truly float.

Some CoolRunner XPLA3 devices appear to have a pull-up on the I/O pins when there is no pull-up specified, this is due to the CoolRunner XPLA3 half latch circuitry. The range of the trip-point is from 0.9V to 1.6V. There was a change in the trip-point when Xilinx changed fabs. The change in fab locations is documented in PCNs, and is available on the Xilinx Customer Notices page:

www.xilinx.com/support/documentation/customer_notices.htm.

The trip-point for the newer devices (part marking of *MN) is lower than the trip-point for the older devices (part marking of APN); this can result in the half latch circuitry being “turned on” sooner than in the older devices. If this occurs, a pull-down resistor of a value stronger than 10 kΩ is required to overcome the half latch pull-up resistance; a value of

4.7 kΩ is recommended. If the incorrect value of a pull-down is used, a voltage divider is created at the input.

More information on the half latch is available in the *XPLA3 I/O Cell Characteristics Application Note* (XAPP342).

CoolRunner-II

The CoolRunner-II I/Os have a half latch feature enabled by default. Half latch occurs only in cases when the CoolRunner-II I/Os are configured as LVCMOS18 and the Schmitt trigger is disabled. If the Schmitt trigger is used, the half latch is disabled. When using LVCMOS18, the only way to turn the half latch off is to enable the Schmitt trigger on that input.

XC9500, XC9500XL, and XC9500XV

The XC9500 families do not have a half latch.

The XC9500XL and XC9500XV have internal circuitries that function in a similar manner to a half latch. To overcome this circuitry, ensure that a pull-down of 4.7 kΩ or stronger is used. (The effective resistance of the internal circuitry is between 30 to 60 kΩ.)

JTAG Termination

XC9500, XC9500XL, XC9500XV, and CoolRunner XPLA3 have internal pull-ups on TDI and TMS.

CoolRunner-II devices have internal pull-ups on TDI, TMS, and TCK.

It is recommended to place external pull-up resistors on the JTAG input pins TDI, TMS, and TCK. For a single device, the resistor value of 4.7 kΩ is suggested. This value may be adjusted depending on the number of devices in the JTAG chain or the application. External pull-down termination is not recommended as it would conflict with the internal pull-ups.

Thresholds

I/V Curves

The I/V curve is a graphical representation of the nominal amount of current that an I/O can source or sink at different voltage levels. The range of voltage levels, and therefore, the current, is dependent on the I/O voltage used. The I/V curves provide details on thresholds.

The I/V curves for the CoolRunner-II and CoolRunner XPLA3 devices can be found in the family data sheets and in the *I/V Curves for Xilinx FPGA and CPLD Families Application Note* (XAPP150) for the XC9500, XC9500XL and XC9500XV families.

Questions often asked by users are:

- How much current can an I/O source or sink?
- If I am driving a certain load, what voltage levels can I expect?

Reading I/V Curves

Customers who need to understand what threshold their outputs will have can use the I/V curve (for example, if you are using an I/O standard powered at 3.3V, and need to know how much current can be sourced from the I/O). The threshold that the CPLD drives out can be determined by the Vihmin of the downstream device (i.e., if the downstream device requires a Vihmin of 3.0V, then you must ensure that the CPLD can drive out this voltage with its current loading). If the Vohmin is 3.0V, then you can extrapolate from the curve in Figure 1; under typical conditions, the device can source 18 mA of current without dropping below the required threshold.

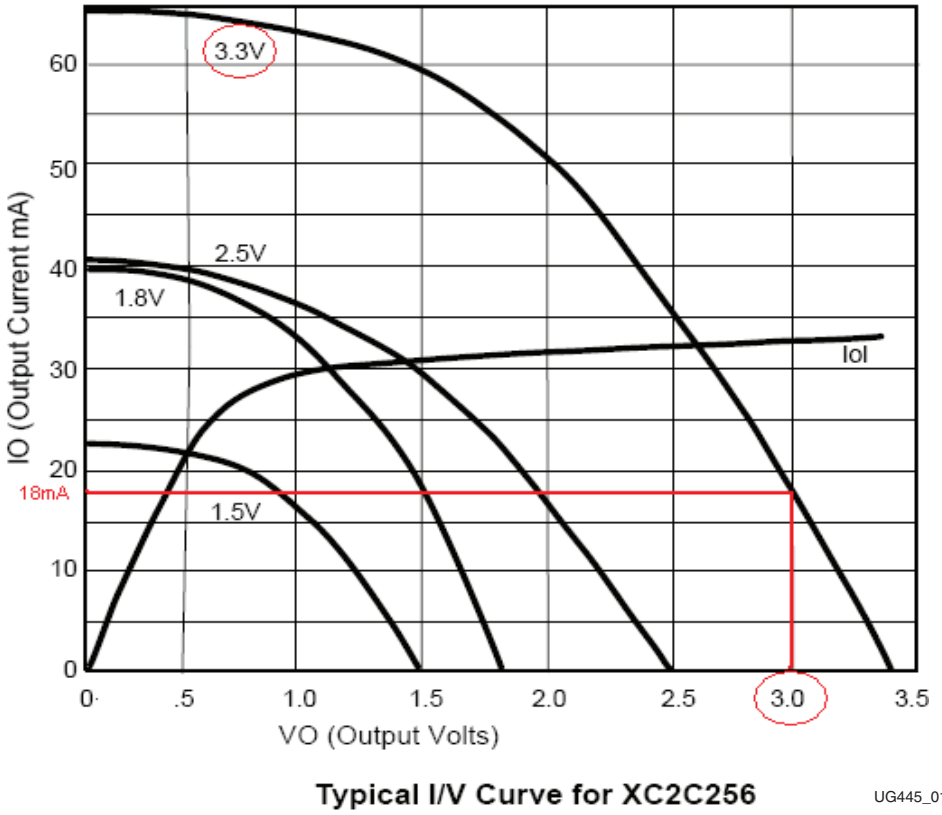


Figure 1: **I/V Curve Example 1**

If you want to find out how much current an I/O can sink before you raise the voltage level above Volmax, you can look at the Iol (output low current) curve in Figure 2, the Volmax and trace to the corresponding current value.

In the example in Figure 2, if the Volmax is 0.5V, you can sink 21 mA.

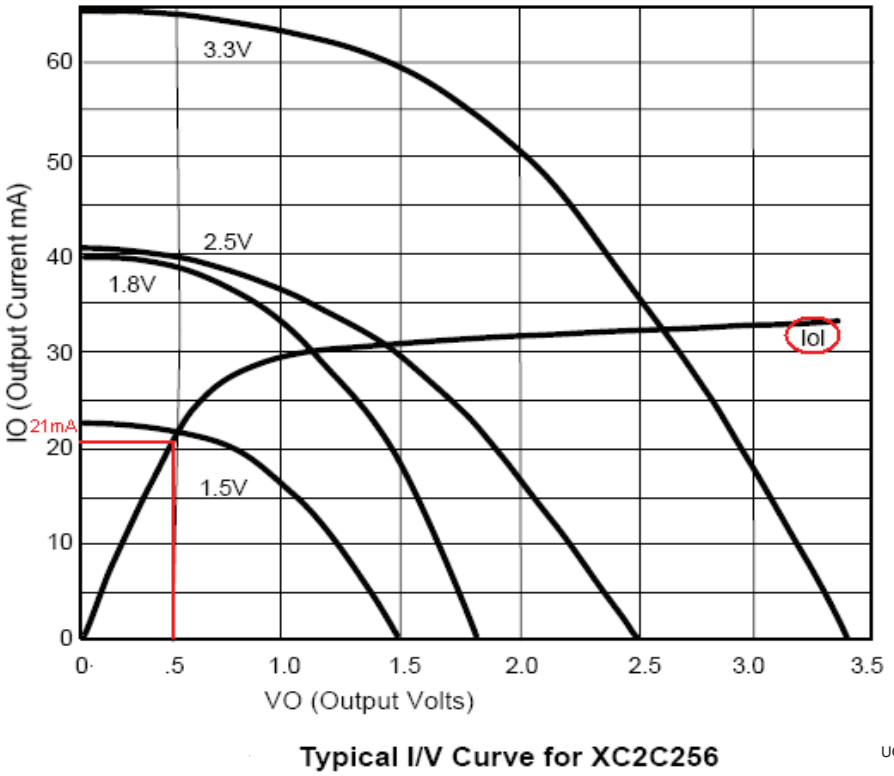


Figure 2: **I/V Curve Example 2**

Another common use of the I/V curve is to determine the voltage at the IOB depending on the load.

For example, if you are driving a 24 mA load from CPLD, will you violate the input thresholds?

From the curve (see Figure 3), you can see that when you drive 24 mA, the nominal output is 2.8V, which is above the Vohmin requirement for both the LVCMOS33 and LVTTL standards.

The user must ensure that the Vohmin requirement meets the Vihmin of the downstream device.

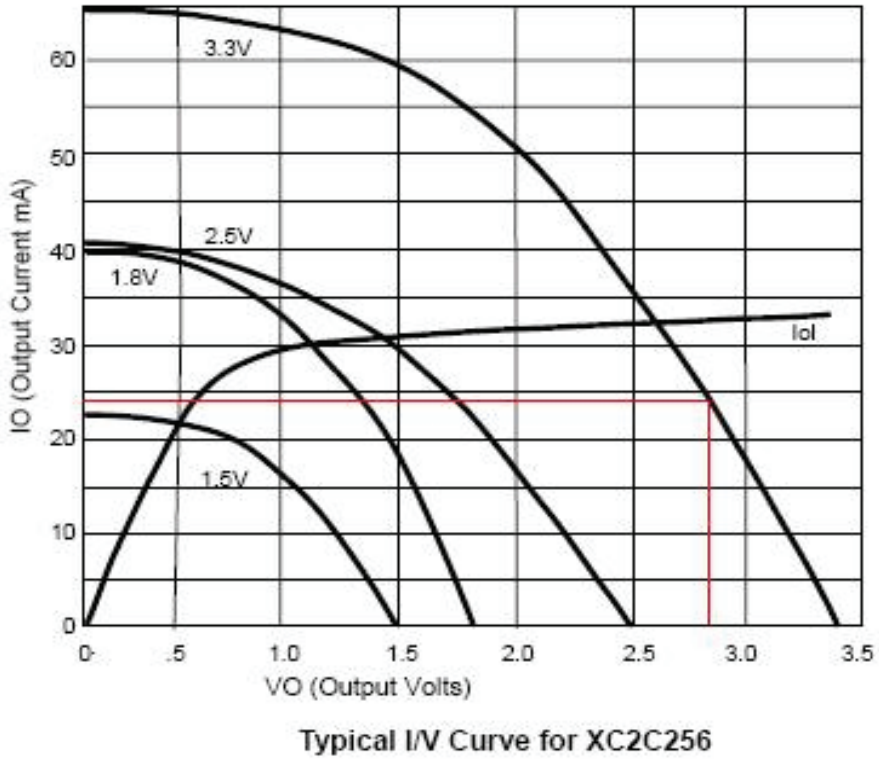


Figure 3: **I/V Curve Example 3**

Maximum I/O Power Dissipation

As an example, you might want to know how to calculate the maximum number of I/Os one device can sink or source before damaging the device.

In this example, you calculate how many I/Os one device can sink or source current before you violate the acceptable Ta range. If you want to keep the device within the recommended limits to prevent long-term reliability implications, adjust the TjMax so that it is equal to the maximum Ta for the temperature grade you are using (i.e., Commercial = 70°C, Industrial = 85°C). This ensures that the 20-year data retention limit is preserved, as well as guarantee the specified timing delays in the data sheet.

If you sink or source lots of current with one device, you risk heating it so much that it is destroyed. So, you need to know the maximum permissible temperature of the package. If you want to perform the calculations to see how much current will be sourced or sunk before the device is compromised, adjust the Tjmax in the calculation to the Tjmax of the package (i.e., Tjmax = 125°C for a plastic package).

Tjmax > (ThetaJC * Pd) + Ta

- Where Tjmax = Tamax of 70°C
- ThetaJC is available in the *Device Package User Guide* (UG112)
- Pd is the power dissipated (use XPower, or measure the design power)
- Ta is the ambient temperature at which the device will run

For example, if you want to know how many output loads you could drive that each require 40 mA with one device, the selected device is XCR3064XL-PC44:

- Tjmax is 70°C for a plastic package
- ThetaJC is 12.4°C/Watt for PC44 package
- Ta will not exceed 50°C

  70 = (12.4*Pd) + 50

  Pd = 1.613W

You need to expand Pd to take into account Pd of the design and the I/O:

(Pddesign + PdIO) = 1.613W

Pddesign is 66 mW from measurement; doubled to 132 mW for safety cushion.

When sourcing 40 mA, the voltage at the output of the CPLD is 2.3V (information obtained from the I/V curve).

X * (3.3V – 2.3V) = 1.613W – 0.132W

X = 1.48W/(1)V

X = 1.48A

You will have 1480 mA to use to drive the I/O pins.

1480 mA/40 mA = 37 output loads can be driven by this device before you exceed the acceptable temperature range.

How many 40 mA output loads can the device sink?

When sinking 40 mA, the voltage at the output of the CPLD is 0.7V.

(X*0.7V) = 1.613W - 0.132W

X = 1.481W/0.7V

X = 2.12A

You should have 2116 mA to use to drive the I/O pins.

2116 mA/40 mA = 53 LEDs can be driven by this device before before you exceed the acceptable temperature range.

Drive Strength

You cannot select the drive strength for CPLDs. The drive strength must be read from the I/V curve.

Power, Sequencing, and Slew Rates

The maximum voltage that you can you drive into an I/O with the device powered or unpowered, is limited to the Vi/Vin parameter in the family data sheet.

- **XC9500:** You can drive into an unpowered I/O, provided Vin does not exceed the Vin limits of the CPLD.
- **XC9500XL:** You can drive into an unpowered I/O, provided Vin does not exceed V_{CCINT} by more than 4.0V.
- **XC9500XV:** You can drive into an unpowered I/O, provided Vin does not exceed the Vin limits of the CPLD.
- **CoolRunner XPLA3:** You can drive into an unpowered I/O, provided Vin does not exceed V_{CCINT} by more than 4.0V.
- **CoolRunner-II:** You can drive into an unpowered I/O, provided Vin does not exceed the Vin limits of the CPLD.

In terms of current, the absolute maximum current that should be applied to an unpowered part is 100mA to the whole part.

Before the device is configured and for unprogrammed devices, the status of the I/Os are disabled and terminated with a weak pull-up.

Hot-Swappable

The following list indicates whether or not devices are hot-swappable:

- CoolRunner-II: Yes
- CoolRunner XPLA3: Yes
- XC9500XL: Yes
- XC9500XV: Yes
- XC9500: No

XC9500 has clamp diodes to V_{CC} (5V); the XC9500XL, XC9500XV, CoolRunner XPLA3 and CoolRunner-II devices do not.

Powering CPLDs

Some of the CPLD families have multiple voltage rails. V_{CCINT} supplies power to internal logic and to the configuration circuit. V_{CCIO} only supplies power to I/O buffers. V_{CCAUX} supplies power to JTAG pins on the CoolRunner-II. In previous families the JTAG pins were powered by V_{CCIO}.

CoolRunner-II CPLDs have three separate voltage rails: V_{CCINT}, V_{CCIO}, and V_{CCAUX}.

XC9500, XC9500XL, and XC9500XV have two separate voltage rails; V_{CCINT} and V_{CCIO}.

Power Sequencing

CoolRunner-II devices are guaranteed to work under all power sequences. However, the order in which V_{CCINT} and V_{CCIO} are applied might cause the CPLD to function differently. V_{CCAUX} can be powered at any time, independent of V_{CCINT} and V_{CCIO}.

V_{CCINT} and V_{CCIO} are most important because they determine whether the CPLD logic comes alive before the I/Os, or if the I/Os are to come alive before the CPLD logic.

There are three basic scenarios:

- V_{CCINT} and V_{CCIO} rise together (both tied to the same 1.8V rail)
- V_{CCIO} before V_{CCINT} (I/O comes alive before logic)
- V_{CCINT} before V_{CCIO} (logic comes alive before I/O)

During configuration, the I/Os are placed in a Tristate condition with a weak pull-up to V_{CCIO}. If V_{CCIO} voltage is either rising with V_{CCINT} or is well established before V_{CCINT} begins rising (i.e., scenario 1 and 2), the I/Os will track V_{CCIO} before the logic that drives the I/Os is active. This may be seen as Logic High to a downstream device. If the output should be driving low at power-up, then the tracking of the I/O to V_{CCIO} might appear as a glitch. However, this is the intended behavior as specified in the data sheet. An example of the tracking of V_{CCIO} by the output is shown in Figure 4.

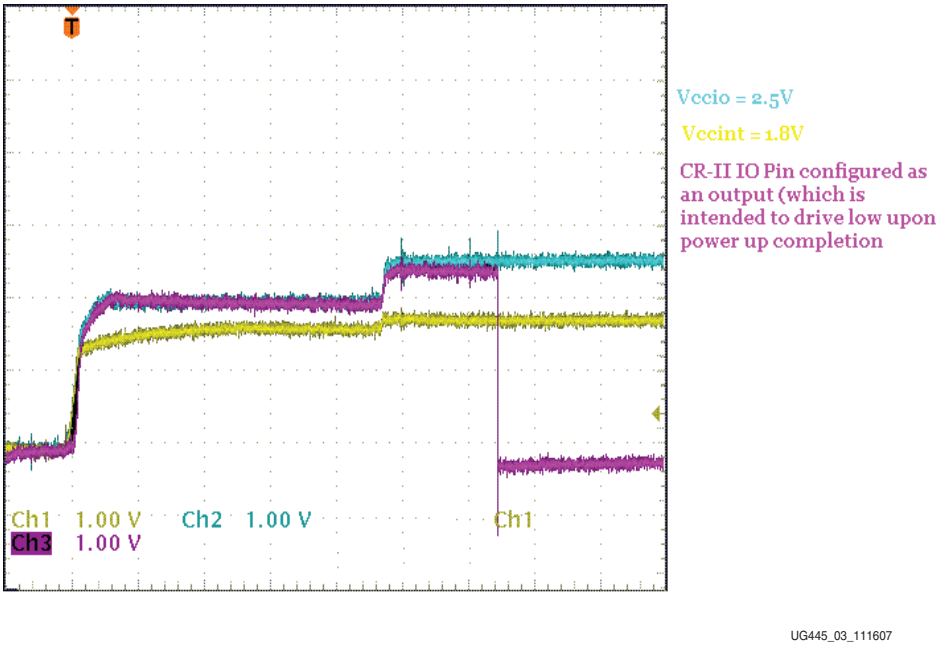


Figure 4: **V_{CCINT} is powered after V_{CCIO}**

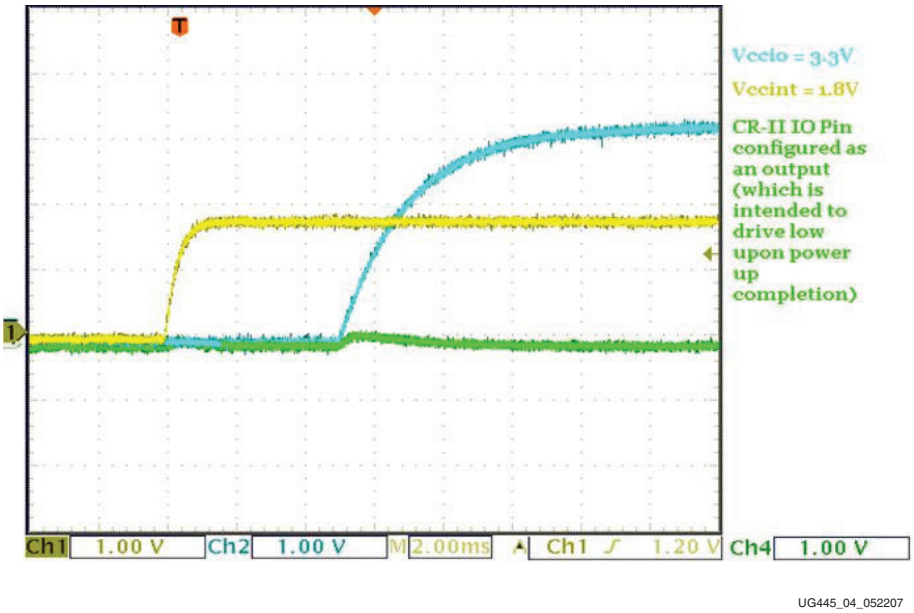


Figure 5: **V_{CCINT} is powered before V_{CCIO}**

For best results (with multiple power rails), Xilinx recommends that V_{CCINT} be applied before V_{CCIO} (see Figure 5); this ensures that the internal logic is correct before the I/Os are active. If V_{CCIO} is powered before V_{CCINT}, this does not damage the device, but there might be glitches on the I/O as the internal circuitry is initialized. Xilinx recommends not leaving V_{CCIO} floating while V_{CCINT} is ramping.

During power-up, all Xilinx CPLDs employ internal circuitry which keeps the devices in the quiescent state (weak pull-up) until the V_{CCINT} supply voltage is at a safe level.

The approximate "safe level" for each device is listed below:

- CoolRunner-II: 1.3V
- CoolRunner XPLA3: 2.1V
- XC9500XL: 2.5V
- XC9500XV: 1.9V
- XC9500: 3.8V

V_{CCIO} can be removed without damaging the part, but the exact behavior under these conditions is not characterized, and therefore, not recommended. When power is removed from V_{CCIO} with the core powered, the I/Os still try to drive and read their pins. Transistors are in an unknown state, which results in more current than if the I/Os were disabled or held in a known state.

V_{CCIO} is not required for programming of the non-volatile memory of a CoolRunner-II. However, it is strongly recommended to power V_{CCIO} during programming. For the XC9500, XC9500XL, XC9500XV, and CoolRunner XPLA3 devices, V_{CCIO} is required for configuration and programming.

V_{CCAUX} is used to power the JTAG circuitry. This leads to a common question, can V_{CCAUX} be safely removed after configuration. This is not recommend. V_{CCAUX} should be powered even after configuration. If there are no JTAG instructions, the power consumed on

V_{CCAUX} is minimal. However, if you remove power from V_{CCAUX}, the state of the TAP controller cannot be guaranteed.

Current Consumption

Programming is defined as the process of programming the non-volatile memory.

Configuration is defined as the process of the CPLD self-configuring upon power-up (Tconfig).

Programming current:

- **CoolRunner-II**

  Typical: 5 mA increasing up to 15 mA for the largest device (512 macro cell).

  Max: 30 mA for the family.

- **CoolRunner XPLA3**

  The current required for ISP programming is 30 mA. This information is taken from the CoolRunner XPLA3 CPLD Data Sheet (DS012), see Programming Specifications (I_{CCP}), Table 7.

- **XC9500, XC9500XL, and XC9500XV**

  Tests show that the 95144XL requires approximately 16 mA.

  Tests show that the 95288XL requires between 19 mA to 40 mA.

- **Tconfig**

  Can be found in the device specific data sheet.

Leakage current is the amount of current consumed when the voltage at the pin is at one of the rails, (i.e., either Logic High or Logic Low). This is specified in the density specific data sheets (IL).

Crowbar current is the amount of current consumed when both the "p" and the "n" transistor are on and there is a path from V_{CCIO} to ground; this is when the voltage at the pin is in between the voltage rails.

The amount of crowbar current is not specified by Xilinx, as the transition rate plays a large role in the amount of current.

5V Tolerance

CoolRunner XPLA3 devices are 5V-tolerant. Also, the XC9500, XC9500XL, and XC9500XV families are 5V-tolerant.

CoolRunner-II devices are not 5V-tolerant. The *5V Tolerance Techniques for CoolRunner-II Devices Application Note* (XAPP429) discusses methods of adding external circuitry to allow CoolRunner-II to operate in a 5V environment. If you drive 5V into the CoolRunner-II, the long-term reliability of the device is compromised. Below is an equation to estimate how the reliability is affected (this is strictly for illustrative purposes). Customers should not exceed the recommended operating conditions given in the device data sheet.

- I/O Gate Oxide Lifetime to be:

  Lifetime = $C_0 10^{-\beta E} \exp(E_a / KT)$

- Based on the above equation, Oxide Lifetime at 5.0V is 3313X smaller than Lifetime at 3.3V

- Oxide Lifetime for 65Å gate oxide is ~2.66 years at 5.0V
- Oxide Lifetime for 65Å gate oxide is ~0.24 years at 5.5V
- Oxide Lifetime for 65Å gate oxide is ~10 minutes at 7.5V

Driving 5V with a CPLD

First, determine if 5V is truly necessary for the downstream device. LVTTL, a 5V standard, can be driven by a LVCMOS33 device and function properly. This is because the input thresholds for the 5V device are met by the output thresholds for the LVCMOS33 I/O standard. The information below applies if you still need 5V outputs.

CoolRunner-II devices are not 5V-tolerant.

For other CPLDs, the basic strategy is to configure the I/O structure so that it drives either a 0, or is high-Z. Then, use an external pull-up resistor (500 Ω to 1 kΩ) to 5V. To do this, run the output signal logic to the enable of the OBUFT. The logic input of the OBUFT is connected to ground. In this way, when the signal is low, the output is grounded.

When the signal is high, the output is placed in a Tristate condition, and the external pull-up pulls the output up to 5V.

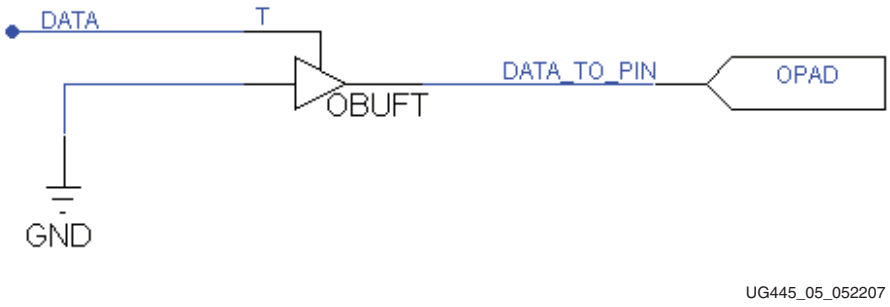


Figure 6: **Simplified Method of Driving 5V**

The following expands upon the first solution. Using a feedback loop allows the output to drive up to 3.3V (or 2.5V) for a short period of time before being placed in a Tristate condition and allowing the external pull-up resistor take care of the rest. The advantage of this is that it has a faster rise, from 0 to 3.3V (or 2.5V), than the first solution.

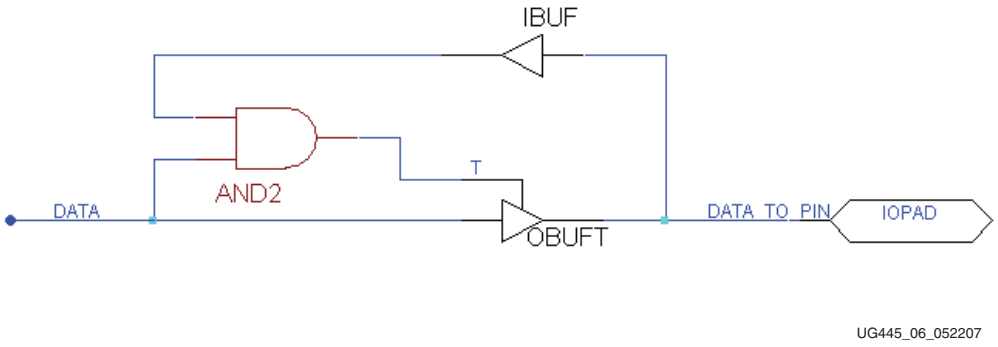


Figure 7: **Fast Rise Time Method of Driving 5V**

The following is sample code for how to achieve the fast rise in VHDL:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity top is
    Port ( data : in std_logic;  data_to_pin : inout std_logic);
end top;
architecture Behavioral of top is
begin
 data_to_pin<= data  when ((data and data_to_pin) ='0') else 'Z';
end Behavioral;
```

Code for Verilog:

```
module top(data, data_to_pin );
    input data;
    inout data_to_pin ;
assign data_to_pin = ((data & data_to_pin) == 0)? data : 1'bz;
endmodule
```

I/O Standards

The supported I/O standards for the different CPLD families are as follows:

- XC9500, XC9500XL, and XC9500XV: LVTTL, LVCMOS33
- CoolRunner XPLA3: LVCMOS33
- CoolRunner-II: LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, HSTL_1, SSTL2_1, SSTL3_1, and LVCMOS15 require use of Schmitt trigger inputs.

Simultaneous Switching Output Limits

Xilinx does not characterize the CPLD device packages to estimate the maximum number of Simultaneous Switching Outputs (SSOs) before ground bounce. However, Xilinx recommends that you not have more than 8 SSOs on the entire chip (all banks included).

If you need to have more than 8 SSOs, Xilinx recommends that you consider altering the slew rate setting on these outputs to skew the outputs relative to each other. By following this recommendation, you can avoid ground bounce due to SSOs.

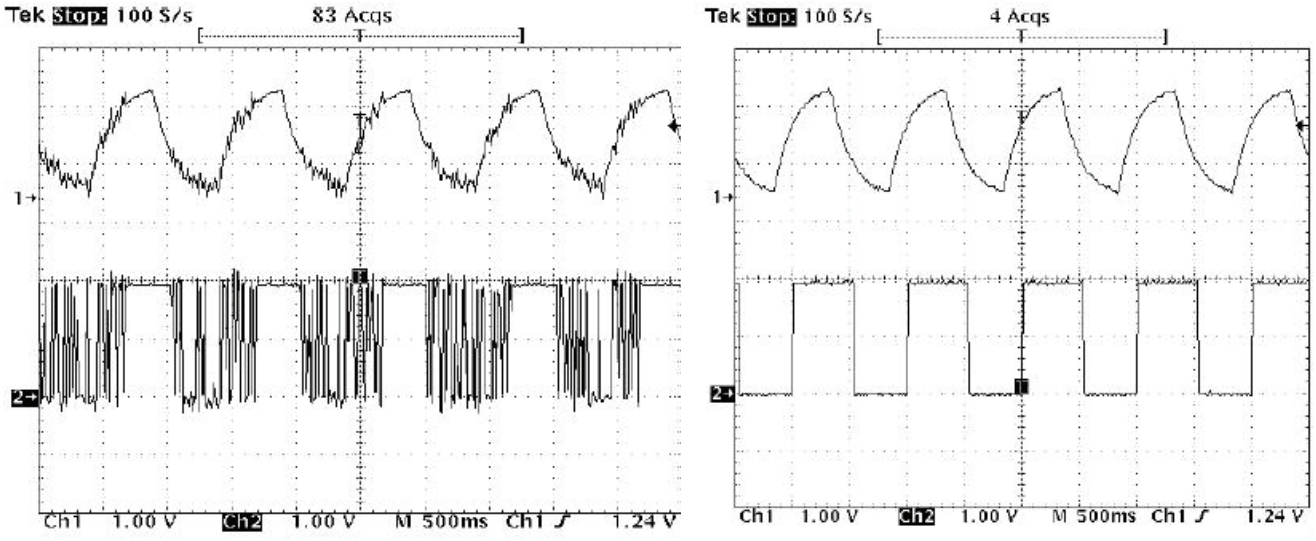
Decoupling Guidelines

The minimum decoupling recommendations for CPLD devices are to provide both 0.1 and 0.01 uF capacitors at every V_{CC} point of the chip and attach them directly to the nearest ground.

Schmitt Trigger

CoolRunner-II is the only family to have the Schmitt trigger feature. A Schmitt trigger is an input circuit used to reduce noise on the input signal. In CoolRunner-II devices, there is a Schmitt trigger available on all I/Os, but only with the I/O standards that do not require a VREF.

In Figure 8 are two waveforms of a signal with and without the Schmitt Trigger, it is the noise from the outputs that make the non-Schmitt Trigger input appear jagged.



Non-Schmitt Waveforms

Schmitt Waveforms

UG445_07_052207

Figure 8: **Before and After Schmitt Trigger Waveforms**

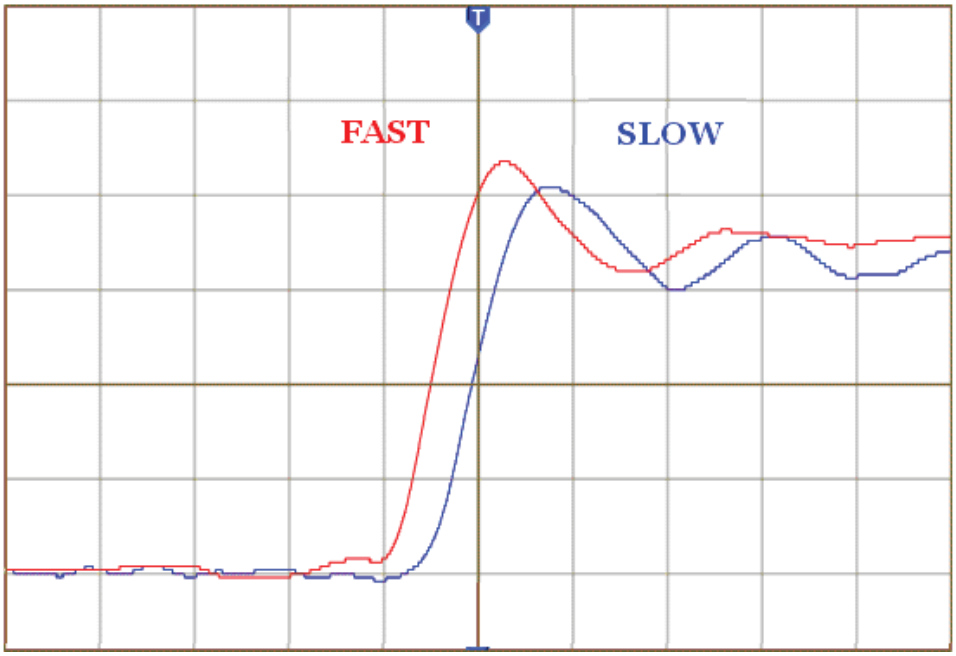
When the input is higher than a certain chosen threshold, the output is high; when the input is below another (lower) threshold, the output is low; when the input is between the two, the output retains its value. Thus, the output retains its value until the input changes sufficiently to trigger a change. This dual-threshold action is called “hysteresis”.

The hysteresis for the CoolRunner-II Schmitt trigger is reported in the data sheet. One point to note is that the Vt+ min and Vt- max are equal. However, this combination does not happen together as the Vt levels track each other. When looking at the Vt max of one characteristic, you must look at the Vt max of the other.

For more information on the CoolRunner-II Schmitt trigger, see the *CoolRunner-II I/O Characteristics Application Note* (XAPP382).

Slew Rate

The slew rate for outputs can be selected as either fast or slow. A slow slew rate is a delayed version of the fast slew rate. The change in the slew rate is achieved by delaying the fast slew rate output.



UG445_08_052207

Figure 9: **Slew Rate**