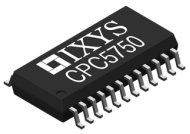
IXYS
INTEGRATED CIRCUITS DIVISION



CPC5750
Single-Channel Voice Band CODEC

PRELIMINARY

Features

- μ-law and A-law ITU G.711 Companding Codec
- Operates on +3.3V Power
- Differential Analog Signal Paths
- Programmable Transmit and Receive Gain, +/-12dB in 0.1dB increments
- Transmit Path 60Hz Rejection Filter
- Differential amplifier drives +3.2dBm into 600Ω
- Stable Gain over temperature
- PCM and IOM-2 GCI telecommunication interfaces
- Short and Long Frame Syncs Supported
- Independent Transmit and Receive Programmable Time Slots
- Accepts PCLK from 512kHz to 8.192MHz
- SPI Serial Interface for control in PCM Mode
- Programmable Power Down Mode, I_{DD} = 20μA
- Analog and Digital Loopback Modes for testing

Description

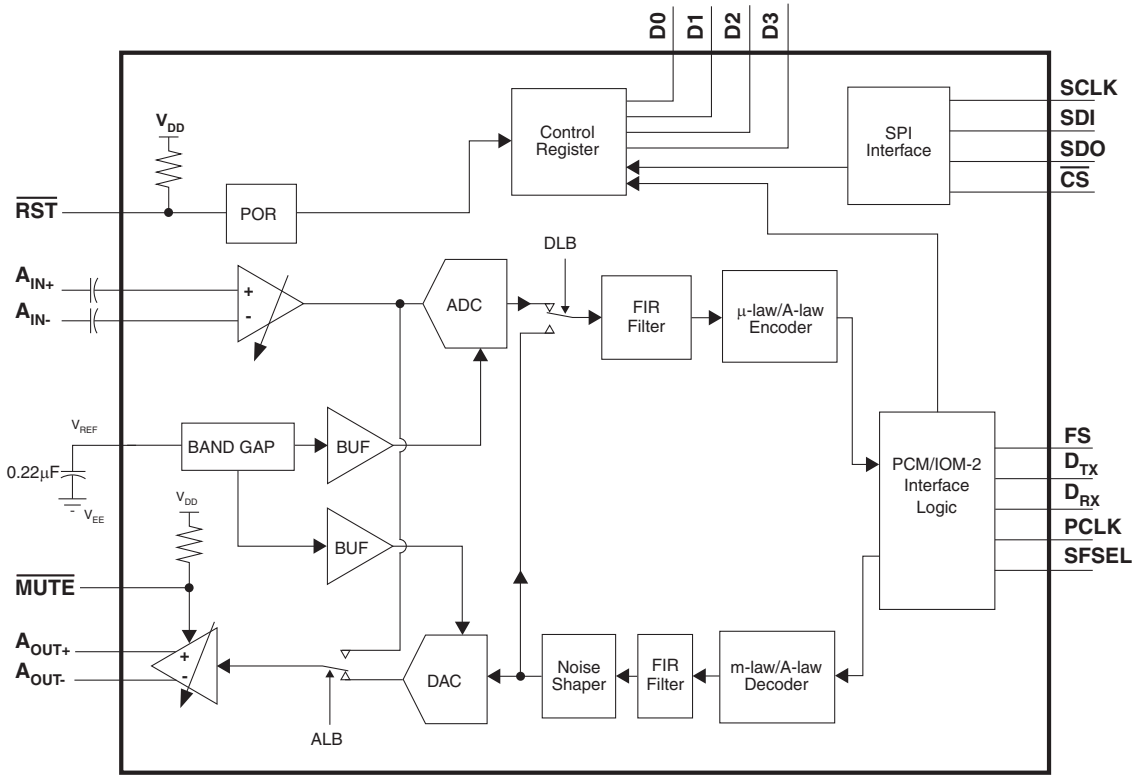
The CPC5750 is a voice-band CODEC with pin-selectable PCM or IOM-2 (GCI) digital interfaces. Clock frequencies for the PCM Mode range from 512kHz to 8.192MHz while the GCI interface allows clocking at 2.048MHz and 4.096MHz. While the GCI interface utilizes the integrated data link to read and write the control registers, a four-wire Serial Peripheral Interface (SPI) bus provides register access while in PCM Mode.

The CODEC provides the necessary A/D and D/A functions with pin-selectable μ-law or A-law companding. A low-noise internal reference is used to keep signal gains well controlled over supply and temperature variations. Programmable gain of ±12dB for both transmit and receive allow the CPC5750 to accept differential input signals as large as +8dBm, and to source +3.2dBm differential signals into 600Ω while operating from a single 3.3V supply.

Ordering Information

Part	Description
CPC5750U	SSOP-24 Package 50/Tube
CPC5750UTR	SSOP-24 Package 2000/Reel

CPC5750 Block Diagram



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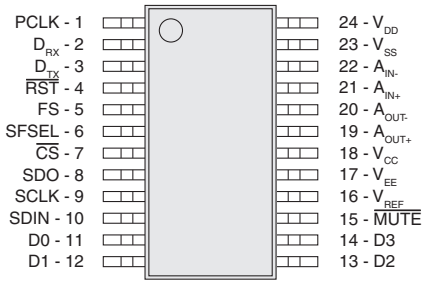
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1. Specifications

1.1 Pinout



1.2 Pin Descriptions

Pin Name	Pin #	Pin Type	Description
Power and Ground			
V_{DD}	24	Power In	Digital Supply Voltage
V_{SS}	23	Power In	Digital Ground
V_{CC}	18	Power In	Analog Supply Voltage
V_{EE}	17	Power In	Analog Ground
V_{REF}	16	Power Out	Analog Reference Voltage - C_{REF} = 0.22µF (From V_{REF} to V_{EE})
Control Interface			
$\overline{RST}$	4	Digital Input - PU	Active low digital input with internal pull-up (PU). When asserted low, all logic is asynchronously reset.
$\overline{CS}$	7	Digital Input (Dual Purpose)	1) Companding selection during Power-Up or $\overline{RST}$. Hold for 40µs after Power-Up or $\overline{RST}$: $\overline{CS}$ = low, Companding = µ-law; $\overline{CS}$ = high, Companding = A-law. Can be modified via programming. 2) PCM Mode: SPI bus Chip Select, active low.
D0	11	Digital Input/Output	General purpose input/output pin.
D1	12	Digital Input/Output	General purpose input/output pin.
D2	13	Digital Input/Output	General purpose input/output pin.
D3	14	Digital Input/Output	General purpose input/output pin.
$\overline{MUTE}$	15	Digital Input - PU	Active low digital input with internal pull-up. When asserted low, the analog output amplifier is disabled and it's outputs A_{OUT+} and A_{OUT-} are held at a nominal ½ V_{CC}.
SCLK	9	Digital Input (Dual Purpose)	1) PCM Mode: SPI bus clock. 2) GCI Mode: Input, MSB address bit to select sub-frame.
SDI	10	Digital Input (Dual Purpose)	1) Transmission Mode select during Power-Up or Reset. Hold for 40µs after Power-Up or $\overline{RST}$: SDI = low, Mode = IOM-2 GCI; SDI = high, Mode = PCM. 2) PCM Mode: SPI bus data input. Connects to the SPI bus master SDO output.
SDO	8	Digital Input/Output Tri-State (Dual Purpose)	1) PCM Mode: SPI bus data output. Connects to the SPI bus master SDI input. 2) GCI Mode: Input, address bit to select sub-frame used.
SFSEL	6	Digital Input	GCI Mode: Input LSB address bit to select sub-frame. PCM Mode: Not used.
PCM/IOM-2 Digitized Voice Interface			
D_{RX}	2	Digital Input	Receive data for PCM Interface or GCI bus.
D_{TX}	3	Digital Output Tri-State	Transmit data for PCM Interface or GCI bus.
FS	5	Digital Input	Frame synchronization signal for GCI or PCM Interface bus.
PCLK	1	Digital Input	Master clock signal for GCI or PCM Interface bus as well as signal processing.
Analog Interface			
A_{IN+}	21	Analog Input	Differential amplifier Non-inverting input.
A_{IN-}	22	Analog Input	Differential amplifier Inverting input.
A_{OUT+}	19	Analog Output	Positive amplifier output, differential 600Ω driver.
A_{OUT-}	20	Analog Output	Negative amplifier output, differential 600Ω driver.

1.3 Absolute Maximum Ratings

Unless otherwise noted, Absolute Maximum Ratings are provided over the operational temperature range and all voltages are referenced to $V_{EE} = V_{SS} = 0V$.

Parameter	Symbol	Min	Max	Units
DC Supply Voltages				
Analog Supply	V_{CC}	- 0.4	3.7	V
Digital Supply	V_{DD}			
Input Voltage				
Analog Pins	V_{IN}	- 0.4	V_{CC} + 0.4	V
Digital Pins			V_{DD} + 0.4	
Output Current				
Analog Pins	I_O		±10	mA
Digital Pins				
Operational Temperature	T_A	- 40	+85	°C
Storage Temperature	T_{STG}	- 40	+150	°C

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied. Exposure to absolute-maximum rated conditions for extended periods of time may affect device reliability.

1.4 Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units
DC Supply Voltages					
Analog Supply	V_{CC}	3.0	3.3	3.6	V
Digital Supply	V_{DD}				
Input Voltage					
Analog Pins	V_{IN}	0		V_{CC}	V
Digital Pins				V_{DD}	
Ambient Temperature	T_A	- 40		+85	°C

1.5 Specifications: General Conditions

Unless otherwise specified:

The characteristics provided in the following tables cover the Operating Ambient Temperature Range -40°C to +85°C; $V_{CC} = V_{DD} = 3.0V$ to 3.6V, $V_{EE} = V_{SS} = 0V$.

Additionally, transmission characteristics cover the programmable gain settings; analog input and output specifications are differential; the test signal and reference signal is 0dBm0 at 1020Hz; and the companding is set to μ-law. Signal power given in dBm is referenced to 600 ohms.
NOTE: Characteristics over the transmission gain settings are bounded by the limitations of the companding and the analog amplifier's input and output capabilities.

Typical values are for 25°C with nominal supplies and are provided for reference purposes only.

1.6 Analog Interface Characteristics

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Inputs						
Input Offset Voltage: A_{IN+} and A_{IN-}	PD = 0	V_{IN}		½ V_{CC}		V
	PD = 1			0		
Input Impedance						
Differential	-	$R_{AIN+/-}$	160	200	240	kΩ
Input to Ground (V_{EE})	-	R_{AIN}	-	100	-	kΩ
Maximum Differential Input Signal	Referenced to 600Ω	-	-	-	+8	dBm
Differential Common Mode Rejection Ratio	Relative to -26dBm0, 0 to 3.6kHz	-	60	-	-	dB
Differential Power Supply Rejection Ratio [1]	$R_{AIN+/-}$ = Open 0 to 3.6kHz	-	60			dB
Outputs						
Output Offset Voltage: A_{OUT+} and A_{OUT-}	PD = 0, $\overline{MUTE}$ = x	V_{OUT}		½ V_{CC}		V
	PD = 1			0		
Output drive	R_L = 500Ω		3.2			mA_p
Maximum Output Signal	Referenced to 600Ω	-	-	-	3.2	dBm
Differential Load Impedance	-	-	500	600	-	Ω
Load Capacitance						
Differential	-	C_{LD}	-	-	250	pF
To GND	-	C_L	-	-	50	pF
Differential Power Supply Rejection Ratio [1]	0 to 3.6kHz	-	60	-	-	dB

[1] Not tested, guaranteed by design. Power supply rejection is evaluated for sample parts.

1.7 Digital Interface Characteristics

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Inputs: All logic inputs and all GPIO provisioned as inputs are Schmitt trigger inputs.						
Input Voltage						
Logic 1 Threshold	-	V_{IH}	-	1.65	2	V
Logic 0 Threshold	-	V_{IL}	0.8	1.1	-	
Hysteresis	-	V_{HYS}	0.3	0.55	0.7	
Input Leakage (Inputs without Pull-Up Resistors and D_x when provisioned as inputs.)	$V_{IN} = V_{SS}$ to V_{DD}	I_{IN}			± 10	µA
Pull-Up Resistors: Pins $\overline{RST}$ & $\overline{MUTE}$		R_{PU}	24	33	42	kΩ
Outputs						
Output Voltage						
Logic 1	I_{OH} = -4mA	V_{OH}	V_{DD}-0.3	V_{DD}-0.17	-	V
Logic 0	I_{OL} = 4mA	V_{OL}	-	0.12	0.3	
Leakage: 3-State Off (Hi-Z)	$V_{OZ} = V_{SS}$ to V_{DD}	I_{OZ}			± 10	µA

1.8 Transmit Path: Analog Inputs (A_{IN+} and A_{IN-}) to Digital Output (D_{TX}) - AC Characteristics

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Gain						
Absolute	0 dBm0, 1020 Hz	-	-0.3	-	0.3	dB
Variation with Frequency (Frequency Response)	Relative to 0 dBm0, 1020 Hz					
	≤ 60 Hz	-	-	-	- 29	dB
	< 200 Hz		-	-	0	
	200 Hz to 300 Hz		-	-	0.25	
	300 Hz to 3000 Hz		-0.25	-	0.25	
	3000 Hz to 3400 Hz		- 0.9	-	0.25	
	3400 Hz to 3600 Hz		-	-	0.25	
	3600 Hz to 4600 Hz		-	-	0	
	> 4.6kHz		-	-	- 25	
Variation with Signal Level (Amplitude Tracking)	Relative to 0 dBm0, 1020Hz					
	+3 dBm0 to -40 dBm0					dB
	-40 dBm0 to -50 dBm0					
	-50 dBm0 to -55 dBm0					
Idle Channel Noise						
C Message Weighted, μ-law	Transmit Gain = 0dB		-	-	12	dBrnC0
P Message Weighted, A-law			-	-		dBm0p
Signal to Total Distortion	3.2 dBm0	-	30	-	-	dB
	0dBm0 to -30dBm0		36	-	-	
	- 40 dBm0		30	-	-	
	- 45 dBm0		25	-	-	
Single Frequency Distortion: Receive any single frequency distortion product.	Any frequency 300 Hz to 3400 Hz				-46	dB
Intermodulation Distortion	300 Hz to 3400 Hz, any two frequencies.				-41	dB
Envelope Delay Distortion						
Absolute	1600 Hz				315	μs
Variation with Frequency	Relative to 1600 Hz					
	500 Hz to 600 Hz				210	μs
	600 Hz to 800 Hz				130	
	800 Hz to 1000 Hz				70	
	1000 Hz to 1600 Hz				35	
	1600 Hz to 2600 Hz				70	
	2600 Hz to 2800 Hz				95	
	2800 Hz to 3000 Hz				145	
Crosstalk - Receive Path to Transmit Path	0dBm0, 300 Hz to 3400 Hz,				-75	dB

1.9 Receive Path: Digital Input (D_{RX}) to Analog Outputs (A_{OUT+} and A_{OUT-}) - AC Characteristics

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Gain						
Absolute	0 dBm0 @1020Hz		-0.3	-	0.3	dB
Variation with Frequency (Frequency Response)	Relative to 0 dBm0, 1020Hz					
	< 200 Hz	-	-	-	0	
	200 Hz to 300 Hz		-	-	0.25	dB
	300 Hz to 3000 Hz		-0.25	-	0.25	
	3000 Hz to 3400 Hz		- 0.9	-	0.25	
	3400 Hz to 3600 Hz		-	-	0.25	
	3600 Hz to 4600 Hz		-	-	0	
	> 4.6kHz		-	-	- 25	
Variation with Signal Level (Amplitude Tracking)	Relative to 0 dBm0, 1020Hz					
	+3 dBm0 to -40 dBm0					dB
	-40 dBm0 to -50 dBm0					
	-50 dBm0 to -55 dBm0					
Idle Channel Noise	Transmit Gain = 0dB					
C Message Weighted, μ-law	Alternating positive and negative PCM zero codes		-	-	12	dBrnC0
P Message Weighted, A-law	Positive zero PCM code		-	-		dBm0p
Signal to Distortion	3.2 dBm0	-	30	-	-	dB
	0dBm0 to -30dBm0		36	-	-	
	- 40 dBm0		30	-	-	
	- 45 dBm0		25	-	-	
Single Frequency Distortion: Receive any single frequency distortion product.	Any frequency 300 Hz to 3400 Hz				-46	dB
Intermodulation Distortion	300 Hz to 3400 Hz, any two frequencies.				-41	dB
Envelope Delay Distortion						
Absolute	1600 Hz				200	μs
Variation with Frequency	Relative to 1600 Hz					
	500 Hz to 1000 Hz		-40			μs
	1000 Hz to 1600 Hz		-30			
	1600 Hz to 2600 Hz				90	
	2600 Hz to 2800 Hz				125	
	2800 Hz to 3000 Hz				175	
Spurious Out of Band Signals	0dBm0, 300 Hz to 3400 Hz					
	4600 Hz to 7600 Hz					dB
	7600 Hz to 8400 Hz					
	8400 Hz to 50 kHz					
Crosstalk - Transmit Path to Receive Path	0dBm0, 300 Hz to 3400 Hz, PCM D_{RX} = Positive zero code				-75	dB
$\overline{\text{Mute}}$ Signal Attenuation	Input 0dBm0, 1020Hz		90	-	-	dB

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Noise Single Frequency	Tie D_{TX} to D_{RX}, 0 Hz to 100kHz, V_{IN} = 1V_{rms},	V_{OUT}			-53	dB

1.10 Power Characteristics

$I_{DC} = I_{CC} + I_{DD}$

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Power-On Reset						
Power-On Reset Voltage (Voltage at Which Reset is Active)	V_{DD} Rising	V_{POR}	-	1.3	2	V
Reference Voltage		V_{REF}				V
Power Supply Current						
Total Supply Current, Device Shut Down	PD = 1	I_{DC}	-	1	20	µA
Total Supply Current, Device Active	PD = 0, No AC transmission	I_{DC}	-	7.5		mA

1.11 Power-On Reset

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Power-On Reset Period	-	T_{POR}	-	20	40	µs
De-Bounce Time	-	T_{RST}	-	20	-	

NOTE: With V_{DD} rising, $V_{IH} = V_{DD}$ for $V_{DD} < V_{POR_MAX}$.

2. Control Registers

The control registers are used to set up operating characteristics, transmit/receive gains, PCM time slot assignments and GPIO control. Access to these registers is dependent on the transmission mode set by the logical state of SDI (pin 10) during a Reset or Power-Up event. With SDI held at a logic high, the device is configured for PCM Mode and register access is only available via the SPI bus. When SDI is held at a logic low, the device is configured for IOM-2 GCI Mode and register access is only available through the GCI data link.

NOTE: PCLK and FS must be active before a write command is issued to the control registers, otherwise the written values will not be retained.

Power Up and Reset events set the device's Power Down bit (PD) to a logic high which disables the input and output analog amplifiers and if configured for PCM Mode, disables the upstream digital signal and places the D_{TX} output into a high impedance state. After provisioning the control registers and if necessary, assigning the PCM interface to the proper time slot, PD can be set low to begin operation. The GCI Mode does not allow changing the time slot of the digitized voice data.

The table below shows the CPC5750 control register names, the bit names, and the register address. Access to the registers is only available via read or write commands. The structure of a register command consists of two parts; first is the command type nibble which is followed immediately by the register address nibble. Write commands will be followed by the data word to be stored in the addressed register. The first four bits (nibble) of a read command are 1010 (0xA) while the write command's first four bits (nibble) are 1011 (0xB). Following the command type nibble is the register address nibble as provided in the table below. As an example, the command to read back the value provisioned into the PCM Transmit Time Slot register is: 0xA7. Detailed discussions of each register are provided in the following sections.

Table 1: Control Registers

Register Name	(MSB) Bits							(LSB)	Address	
	7	6	5	4	3	2	1	0	Dec	Hex
Mode Control	Companding	Not Used	ALB	DLB	PD	CPB	TXZ	TM	0	0x0
TX Gain: ±1dB Steps	Not Used			[4:0]					1	0x1
TX Gain: ±0.1dB Steps	Not Used				[3:0]				2	0x2
RX Gain: ±1dB Steps	Not Used			[4:0]					3	0x3
RX Gain: ±0.1dB Steps	Not Used				[3:0]				4	0x4
PCM D_{RX} Time Slot	Not Used	[6:0]							5	0x5
PCM D_{RX} Bit Delay	Not Used					[2:0]			6	0x6
PCM D_{TX} Time Slot	Not Used	[6:0]							7	0x7
PCM D_{TX} Bit Delay	Not Used					[2:0]			8	0x8
Reserved	0	0	0	0	0	0	0	0	9	0x9
GPIO Control	DIR(3)	DIR(2)	DIR(1)	DIR(0)	D(3)	D(2)	D(1)	D(0)	10	0xA

NOTE: All registers are Read / Write and all user defined bits are Read / Write.

2.1 Mode Control Register

This register allows the programmable control of the Companding, analog and digital loop backs for debug testing, Power Down mode, and custom control of the PCM interface.

Register	7	6	5	4	3	2	1	0	Address
Mode Control	Companding	Not Used	ALB	DLB	PD	CPB	TXZ	TM	0x0
Default	($\overline{CS}$ Level at Reset)	0	0	0	1	0	0	0	-

2.1.1 Companding (bit 7)

This bit determines the data compression method to be used. The value of this bit during Power Up or Reset is determined by the level on $\overline{CS}$ (pin 7) when the chip reset goes inactive. During either of these events the logical level on $\overline{CS}$ must be maintained for a minimum duration of 40µs. For Power Up, the hold time begins with a valid V_{DD} level and a logic high at $\overline{RST}$ (pin 4). For an external reset ($\overline{RST}$ = 0) the hold time begins with a logic high at $\overline{RST}$. Once active, this bit can be modified using the SPI interface (PCM Mode) or the GCI link (IOM-2 GCI Mode). The bit values to set the compression method are:

Logic '0': µ-law
Logic '1': A-law

2.1.2 ALB (bit 5)

The Analog Loop Back (ALB) bit is used to test the analog interface of the CPC5750 by connecting the output of the analog input amplifier to the input of the analog output amplifier. To prevent received digital information from interfering with the test, the connection between the DAC and the input of the analog output amplifier is opened. This provides an all-analog test path from the A_{IN+} and A_{IN-} inputs to the A_{OUT+} and A_{OUT-} outputs. Additionally the analog to digital transmit path remains intact, allowing the means to monitor the analog input gain. The bit values to activate and de-activate the Analog Loop Back are:

Logic '0': Normal Operation (Analog Loop Back disabled)
Logic '1': Analog Loop Back Mode

2.1.3 DLB (bit 4)

The Digital Loop Back (DLB) bit is used to test the digital interfaces, (PCM or GCI) and the DSP sections of the CPC5750 by separating the transmit path analog input section and ADC from the transmit DSP section and connecting the digital output of the receive path DSP to the digital input of the transmit path DSP. This provides an all-digital test path through the receive path's DAC filters and Noise Shaper and back out through ADC digital filters. The DLB configuration retains the connection between the receive path's digital and analog sections providing the means to monitor the converted receive digital signal at the A_{OUT+} and A_{OUT-} analog outputs. The bit values to control the Digital Loop Back function are:

Logic '0': Normal Operation (Digital Loop Back disabled)
Logic '1': Digital Loop Back Mode

2.1.4 PD (bit 3)

The Power-Down (PD) bit is used to put the CPC5750 in a standby mode where it draws very little current.

Logic '0': Normal Operation
Logic '1': Device is Powered Down. The SPI bus interface (PCM Mode) and GCI link (GCI Mode) are still functional to allow enabling the part. The GCI interface will draw current if clocked externally. In PCM Mode, D_{TX} is set to high impedance (Hi-Z).

2.1.5 CPB (bit 2)

The Clocks Per Bit (CPB) selection bit is used to set the number of PCM clock cycles per bit of transmit and receive data transfer at either 1 clock-per-bit or 2 clocks-per-bit. This programmable option is only used in PCM Mode as the clock rate is auto-detected in GCI Mode.

Logic '0': 1 Clock cycle Per data Bit
Logic '1': 2 Clock cycles Per data Bit

2.1.6 TXZ (bit 1)

The PCM data Tri-state (TXZ) selection bit is used to set when the PCM transmit output driver, D_{TX}, goes high impedance.

Logic '0': Tri-State on the first PCLK Rising Edge following the LSB of the time slot.
Logic '1': Tri-State on the PCLK Falling Edge during the LSB of the time slot. (The second falling edge of PCLK when CPB = 1.)

2.1.7 TM (bit 0)

Reserved: This bit is not user defined and it's value should not be modified. The default power up and reset value of this bit is 0 and must not be changed.

2.2 TX Path Gain: ±1dB Steps Register

FIve bits of this register determine the analog input amplifier gain in 1 dB steps as shown in the following table.

Register	7	6	5	4	3	2	1	0	Address
TX Path Gain: ±1dB Steps	-	-	-	TXG(4)	TXG(3)	TXG(2)	TXG(1)	TXG(0)	0x1
Default Value	0	0	0	0	0	0	0	0	-

2.2.1 TXG (bits [4:0])

TXG is a 5-bit, 2's complement number between -12 and 12. This value sets the transmit path gain in 1 dB increments. Values of TXG larger than +12 set a gain of +12dB. Values of TXG less than -12 set a gain of -12dB.

2.3 TX Path Gain: +0.1dB Steps Register

Four bits of this register determine the analog input amplifier gain in 0.1 dB steps as shown in the following table.

Register	7	6	5	4	3	2	1	0	Address
TX Path Gain: +0.1dB Steps	-	-	-	-	TXB(3)	TXB(2)	TXB(1)	TXB(0)	0x2
Default Value	0	0	0	0	0	0	0	0	-

2.3.1 TXB (bits [3:0])

TXB is a 4-bit number between 0 and +9. This value increases the transmit path gain in 0.1dB increments. These bits are used in conjunction with the TXG bits to define a 9-bit gain value from -12dB to +12.9dB in 0.1dB steps. For example, to set the transmit gain to -0.1dB, the TXG bits are set for -1dB (11111) and the TXB bits are set for +0.9dB (1001). The nine bit value 111111001(binary) provides for a transmit gain = -1dB + 0.9dB = -0.1dB; EX2: 111110000 = -1dB; EX3: 001110011 = +7.3dB. Values of TXB are always positive and values greater than 9 continue to define the gain as +0.9dB.

2.4 RX Path Gain: ±1dB Steps Register

FIve bits of this register determine the analog output amplifier gain in 1 dB steps as shown in the following table.

Register	7	6	5	4	3	2	1	0	Address
RX Path Gain: ±1dB Steps	-	-	-	RXG(4)	RXG(3)	RXG(2)	RXG(1)	RXG(0)	0x3
Default Value	0	0	0	0	0	0	0	0	-

2.4.1 RXG (bits [4:0])

RXG is a 5-bit, 2's complement number between -12 and 12. This value sets the receive path gain in 1dB increments. Values of RXG larger than +12 set a gain of +12dB. Values of RXG less than -12 set a gain of -12dB.

2.5 RX Path Gain: +0.1dB Steps Register

Four bits of this register determine the analog output amplifier gain 0.1 dB steps as shown in the following table.

Register	7	6	5	4	3	2	1	0	Address
RX Path Gain: +0.1dB Steps	-	-	-	-	RXB(3)	RXB(2)	RXB(1)	RXB(0)	0x4
Default Value	0	0	0	0	0	0	0	0	-

2.5.1 RXB (bits [3:0])

RXB is a 4-bit number between 0 and +9. This value increases the receive path gain in 0.1 dB increments. These bits are used in conjunction with the RXG bits to define a 9-bit gain value from -12 to +12.9dB in 0.1 steps. For example, to set the receive gain to -3.1dB, the RXG bits are set for -4dB (11100) and the RXB bits are set for +0.9dB (1001). The nine bit value 111001001(binary) provides for a receive gain = -4dB + 0.9dB = -3.1dB; EX2: 110110011 = -5dB + 0.3dB = -4.7dB; EX3: 010011000 = +9.8dB. Values of RXB are always positive and values greater than 9 continue to define the gain as +0.9dB.

2.6 PCM Interface D_{RX} Time Slot Assignment Register

The lower seven bits of this register determine which of the available 8-bit time slots the CPC5750 uses to receive data when in the PCM Mode.

Register	7	6	5	4	3	2	1	0	Address
PCM D_{RX} Time Slot	-	PRC(6)	PRC(5)	PRC(4)	PRC(3)	PRC(2)	PRC(1)	PRC(0)	0x5
Default Value	0	0	0	0	0	0	0	0	-

2.7 PCM Interface D_{RX} Bit Delay Register

The lower three bits of this register delay the receiver from reading the selected time slot by 0 to 7 bits.

Register	7	6	5	4	3	2	1	0	Address
PCM D_{RX} Bit	-	-	-	-	-	PRB(2)	PRB1)	PRB(0)	0x6
Default Value	0	0	0	0	0	0	0	0	-

2.8 PCM Interface D_{TX} Time Slot Assignment Register

The lower seven bits of this register determine which of the available 8-bit time slots the CPC5750 uses to transmit data when in the PCM Mode.

Register	7	6	5	4	3	2	1	0	Address
PCM D_{TX} Channel	-	PTC(6)	PTC(5)	PTC(4)	PTC(3)	PTC(2)	PTC(1)	PTC(0)	0x7
Default Value	0	0	0	0	0	0	0	0	-

2.9 PCM Interface D_{TX} Bit Delay Register

The lower three bits of this register delay the transmit data in the selected time slot by 0 to 7 bits.

Register	7	6	5	4	3	2	1	0	Address
PCM D_{TX} Bit	-	-	-	-	-	PTB(2)	PTB1)	PTB(0)	0x8
Default Value	0	0	0	0	0	0	0	0	-

2.10 Reserved Register

The Reserved register is not user defined and it's value should not be modified. The default power up and reset value of this register is 0 and must not be changed.

Register	7	6	5	4	3	2	1	0	Address
Reserved	0	0	0	0	0	0	0	0	0x9

2.11 GPIO Control Register

The CPC5750 has four General Purpose I/O pins that can be programmed as inputs or outputs and whose values can be examined or controlled by the user. This register allows for control and monitoring of external digital nets using these I/O pins.

Register	7	6	5	4	3	2	1	0	Address
GPIO Control	DIR(3)	DIR(2)	DIR(1)	DIR(0)	D(3)	D(2)	D(1)	D(0)	0xA
Default Value	0	0	0	0	0	0	0	0	-

2.11.1 DIR(x) (bits [3:0])

Setting a DIR(x) bit to 1, configures the corresponding CPC5750 I/O pin as an output. When the DIR(x) bits are cleared, i.e. DIR(x) = 0, the corresponding I/O pin will be configured as an input. Following a Power Up or Reset the CPC5750 configures all four I/O pins as inputs thereby eliminating any possibility of an I/O pin back driving another output.

2.11.2 D(x) (bits [3:0])

When an I/O is configured as an input, then reading the corresponding D(x) bit of this register gives the logical state of that input pin. Writing to the D(x) bits of inputs performs no function while writing to the D(x) bit of an I/O configured as an output determines the state of that output pin. Reading this register returns the current value of the bits. For an I/O pin configured as an output, reading this register returns the last value written to it's D(x) bit.

3. Digital Transmission Modes: PCM or IOM-2 GCI

The CPC5750 was designed to be used in communication systems utilizing either the traditional PCM bus method of digital transmission flow or the newer IOM-2 GCI bus. Both operational modes make use of the 4-wire digital transmission bus consisting of the data clock (PCLK), an 8kHz Frame Synchronization clock (FS), an upstream transmit data signal (D_{TX}) and a downstream receive data signal (D_{RX}). Although both modes use this 4-wire bus, the data structure within the digital transmit and receive streams is dissimilar.

One major difference between the PCM Mode and the GCI Mode of operation is how provisioning, control and status is implemented. When operating in the PCM Mode a serial (SPI) bus is utilized to perform these functions. In the GCI Mode these functions are embedded in the transmit and receive data streams, thereby eliminating the need for an additional bus for command and control.

3.1 Digital Transmission Mode Selection

Configuring the CPC5750 to operate in PCM or GCI Mode is performed during either a Power Up or Reset event using the level at the SDI input pin to determine the mode. Holding SDI high will cause the CPC5750 to be placed into the PCM Mode of operation while holding SDI low will result in the GCI Mode.

For PCM applications, the voltage available at SDI during power up may not satisfy the specified logic high threshold voltage stated in **Section 1.7 Digital Interface Characteristics on page 6**. To ensure a logic high is recognized at the SDI input during power up, the input should be biased to V_{DD}. As the V_{DD} supply rises towards the Power On Reset threshold, the CPC5750 will accept the V_{DD} voltage level at SDI as a logic high.

Because the GCI Mode does not utilize the SPI bus, those applications should tie the SDI input low and the $\overline{CS}$ input to the appropriate logic level dependent on the desired companding. The companding method set by $\overline{CS}$ during Power Up or Reset can be overridden by provisioning bit 7 of the Mode Control register.

3.2 PCLK Frequencies and Time Slot Selection

The clocking circuits use the Frame Sync (FS) signal from the PCM or IOM-2 bus to automatically determine the PCLK frequency and divides or multiplies the clock as necessary to generate an on-chip 1.024MHz clock.

The table below shows the allowed PCLK frequencies for both the PCM and GCI Modes and the time slot allocations. For the PCM Mode there are eight allowed PCLK frequencies while the IOM-2 GCI Mode has only two. When using the PCM Mode, the maximum number of available time slots is dependent on the number of eight bit channels that can be transferred within one period of the 8kHz Frame Sync clock. For all systems, the maximum number of time slots is the PCLK frequency divided by the Frame Sync frequency divided by the number of clock bits (pulses) per channel. A system that uses one clock bit for each transmission bit, the number of time slots is the PCLK frequency divided by 8kHz divided by 8 clock pulses which is PCLK / 64kHz. PCM systems using two PCLK pulses per transmission bit will need to set bit 2 of the Mode Control register to a logic 1. Calculating the number of time slots is now PCLK frequency / 128kHz. The table below provides a quick reference.

Assignment of the specific time slot to be used when in PCM Mode is done by provisioning the PCM transmit and receive time slot assignment registers described in **Section 2.8** and **Section 2.6 beginning on page 13**.

Only two PCLK frequencies are allowed for the IOM-2 GCI Mode and the number of available time slots is independent of the clock frequency. Because the number of time slots in GCI Mode is fixed and the higher allowed frequency is twice the lower allowed frequency, the CPC5750 will use two PCLK bits per transmission bit when it detects the higher allowed PCLK frequency. This is shown in the following table.

Available time slots for the IOM-2 GCI Mode is based on the number of available sub-frames. The IOM-2 GCI definition provides for eight sub-frames within a single frame defined by the time period of the Frame Sync clock.

Although the IOM-2 specification provides for two digitized voice time slots per sub-frame, the CPC5750 only uses the B1 time slot. This allows for a total of eight available time slots when operating in the GCI Mode.

Selection of the sub-frame is not a provisioning option. It is done by applying the appropriate logic levels at pins: SCLK, SDO, and SFSEL. See **Section 6 IOM-2 (GCI) Interface beginning on page 23** and **Table 4 on page 23** for more details.

Table 2: PCLK Frequencies and Available PCM Time Slots

Frequency	Available PCM Time Slots CPB = 0 (1 Clock per bit)	Available PCM Time Slots CPB = 1 (2 Clocks per bit)	GCI Frequency
512kHz	8	4	No
1.024MHz	16	8	No
1.536MHz	24	12	No
2.048MHz	32	16	Yes: 1 Clock per bit
3.072MHz	48	24	No
4.096MHz	64	32	Yes: 2 Clocks per bit
6.144MHz	96	48	No
8.192MHz	128	64	No

3.3 Hardware Configuration For Transmission Mode Selection

To ensure correct initialization of the CPC5750 following a Power Up or Reset event, the appropriate inputs must be properly conditioned.

PCM Mode: SDI = 1 and $\overline{CS}$ = x

GCI Mode: SDI = 0 and $\overline{CS}$ = x;
Also, the sub-frame selection using SCLK, SDO, and SFSEL must be made at this time.

Failure to condition and hold these inputs at the appropriate logic level for the specified duration during Power Up or Reset will require a Reset to re-initialize the device.

While the input $\overline{CS}$ may be conditioned to configure the CPC5750 for the desire companding method, this can be modified via provisioning once the part becomes active.

Special Notes:

1) SDI and $\overline{CS}$ are not used in normal operation of the GCI Mode, therefore it is recommended that these unused inputs be fixed to a stable logic level.
2) For the PCM Mode, SFSEL is an unused input and should be fixed to a stable logic level.

4. Functional Description - To Do

5. PCM Bus Interface

The PCM bus consists of four signals: PCLK, FS, D_{TX}, and D_{RX} which are used to transmit and receive one byte each (eight bits) of μ-law or A-law companded audio data every cycle of the 8kHz Frame Sync (FS) clock. This provides for a 64k bit per second data rate in each direction. Provided within each frame (cycle of the FS clock) are a number of 8-bit time slots determined by the frequency of PCLK and the value assigned to the CPB bit in the Mode Control register. The number of available time slots is calculated as the PCLK frequency (variable) divided by the FS frequency (fixed at 8kHz) divided by the number of PCLK cycles per data byte (variable, 8 or 16 controlled by CPB). The relationship between the PCLK frequency and CPB to the number of available PCM time slots is shown in **Table 2: PCLK Frequencies and Available PCM Time Slots**.

Capable of transmitting (upstream) and receiving (downstream) in separate time slots, the CPC5750 PCM upstream and downstream data paths can be provisioned independently to any of the available time slots within the frame. Additionally, the upstream and downstream paths can be provisioned independently for bit delays within the time slot. While the non-delayed timing mode does not have bit delays, the delayed timing mode does. To provide for bit delays within the system, the CPC5750 allows the user to provision the time slot starting point to any of the possible bits within the 125μs frame. This requires 10 bits to accommodate the device's 128 maximum time slots. The lower 3 bits used to modify the start bit (MSB) position within a time slot is in a separate register from the time slot assignment register to ease provisioning for applications that require setting only the 8-bit time slot or just the bit delay, allowing the other register to be ignored.

The CPC5750 PCM bus is a 4-wire full duplex digital transmission medium using two data wires, D_{TX} and D_{RX}, so data can be transmitted and received simultaneously. The D_{TX} transmit signal used to send data upstream is output onto a common bus. Since other devices assigned to different time slots transmit their upstream data onto this same bus, the CPC5750 must tri-state D_{TX} during all non-assigned time slots. Determination of when D_{TX} tri-states after it outputs 8-bits of data is contingent upon the value set in the Mode Control register's TXZ bit. For provisioning details see **Section 2.1.6 TXZ (bit 1)** and **Section 2.1.5 CPB (bit 2) beginning on page 12**.

Time slot locations within the transmit and receive data bit streams are defined by the location of the Frame Synchronization (FS) pulse and the value set in bit delay registers as described in **Section 2.9 PCM Interface DTX Bit Delay Register** and **Section 2.7 PCM Interface DRX Bit Delay Register beginning on page 13**. Historically, timing of data bit streams was defined by two modes, Non-delayed Timing Mode and Delayed Timing Mode by means of a Long Frame Sync pulse and a Short Frame Sync pulse to establish a reference point for the first bit of the first time slot of the frame.

The Non-delayed Timing Mode used the Long Frame Sync as an enable to define the location of the time slot. The first data bit of the Long Frame Sync time slot was defined as the first concurrent logic high of the PCM clock and the frame sync pulse. In this configuration there is no requirement for the rising edge of the clock or the sync pulse to precede the other. Because the Long Frame Sync pulse is an enable, the width of pulse needs to be sufficient to ensure data transfer of all eight bits.

The Delayed Timing Mode used the Short Frame Sync to establish the beginning of the first time slot within the frame. This method used the first falling edge of the PCM clock to register the frame synchronization pulse marking the end of the current frame. With the conclusion of the current frame, the first bit of the next frame begins with the next rising edge of the PCM clock. Because this method provides an indicator prior to the beginning of the frame it is ideal for use in systems wishing to delay data transfer.

The CPC5750 uses a timing mode that is compatible with both of these legacy techniques. Interoperability is assured by the internal timing circuitry and the device's ability to access the data bit stream at any point within the frame. In the CPC5750, the first bit of the frame is defined as coincident with the PCLK rising edge preceding the falling PCLK edge used to detect the active FS pulse.

Because the first transmitted data bit is in the same bit time as the FS pulse, the D_{TX} driver must be enabled with the correct data before the FS signal is detected. For this to happen, the CPC5750 must count the PCLK cycles in the first complete frame to determine the number of 8-bit time slots per frame so it can predict when to drive the D_{TX} bus. If the FS pulse does not arrive as predicted, then the CPC5750 will re-synchronize, and recount the time slots in the frame. For this reason the data in the first two received frames after connection to a PCM bus will be ignored and no data will be transmitted upstream.

Detection of the FS pulse with the PCLK falling edge eliminates the rigid FS pulse width constraints and the required synchronization of the FS rising edge with the PCLK rising edge. The minimum FS pulse width is the sum of the setup and hold times while the maximum pulse width must allow for a minimum of one FS low detect by the falling PCLK edge.

Assuring the first upstream data bit is available with the rising edge of FS and allowing the FS pulse to persist for multiple PCLK cycles provides compatibility with the legacy Long Frame Sync, Non-delayed Timing Mode when the time slot and bit delay setting registers are configured for the first bit of the first time slot, (Time Slot 0 {zero} and no bit delay) of the frame. Additionally, since the CPC5750 is designed to accept small FS pulses and can be provisioned for the transfer of data delayed by one or more bits it is compatible with the legacy Short Frame Sync Delayed Timing Mode. As with the legacy data bit stream formats, the Most Significant Bit (MSB) will be the first bit received and the first bit transmitted in the data byte.

Figure 1: PCM Time Slot 0, Short FS, No Bit Delay (PTC=PRC=0, PTB=PRB=0, CPB=0, TXZ=1)

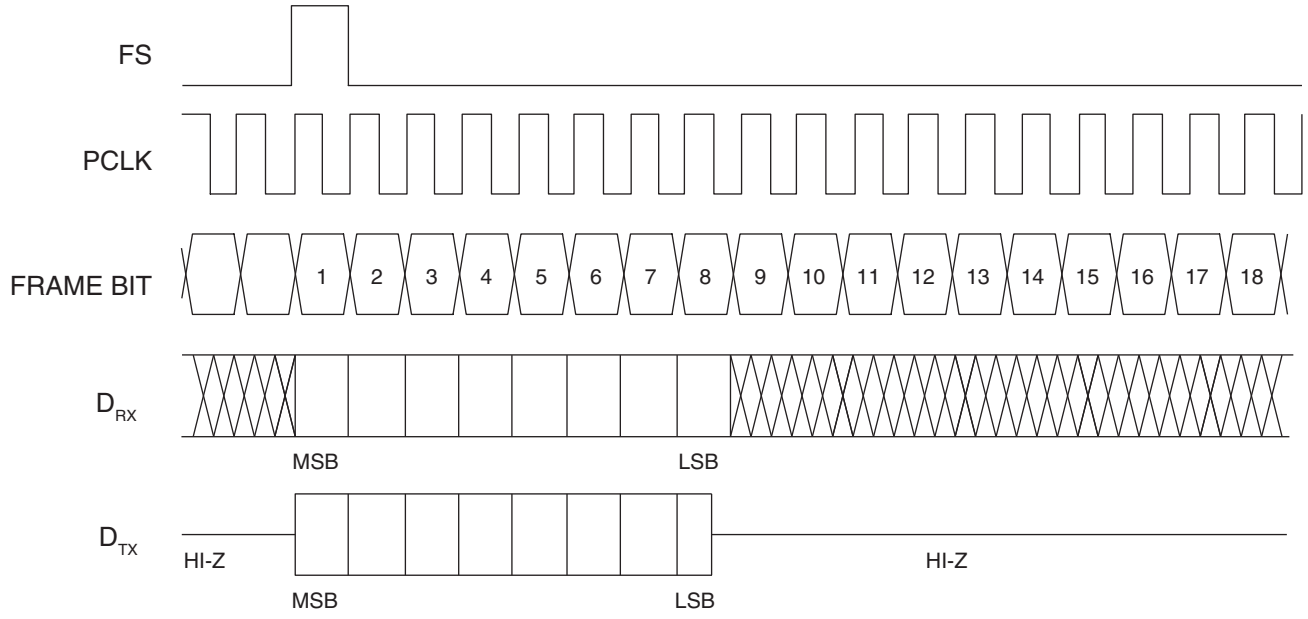


Figure 2: PCM Time Slot 0, Long FS, No Bit Delay (PTC=PRC=0, PTB=PRB=0, CPB=0, TXZ=1)

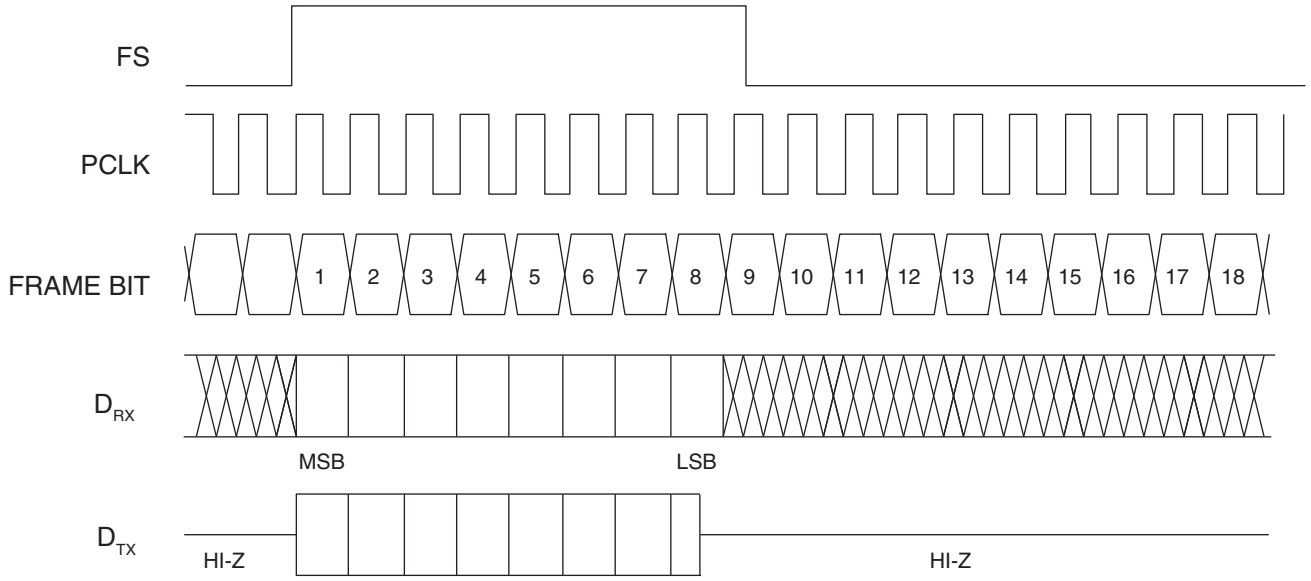


Figure 3: PCM Time Slot 1, Long FS, 2 Bit Delay (PTC=PRC=1, PTB=PRB=2, CPB=0, TXZ=1)

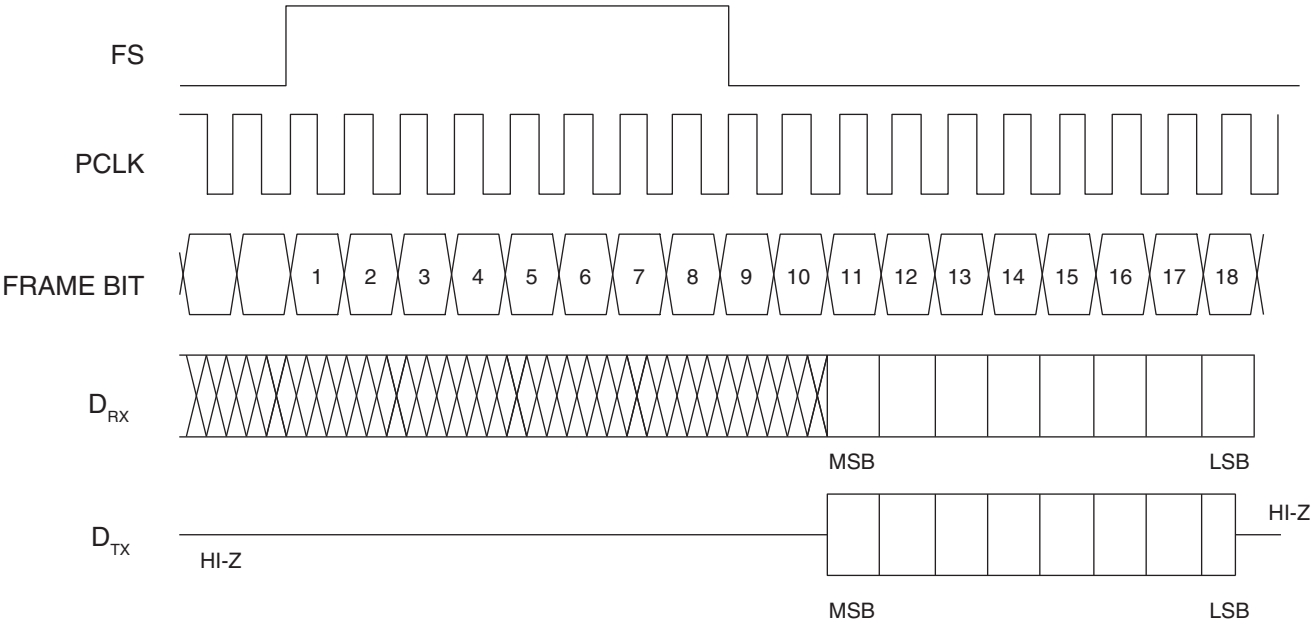


Figure 4: PCM Time Slot 0, Short FS, No Bit Delay, 2x PCLK (PTC=PRC=0, PTB=PRB=0, CPB=1, TXZ=1)

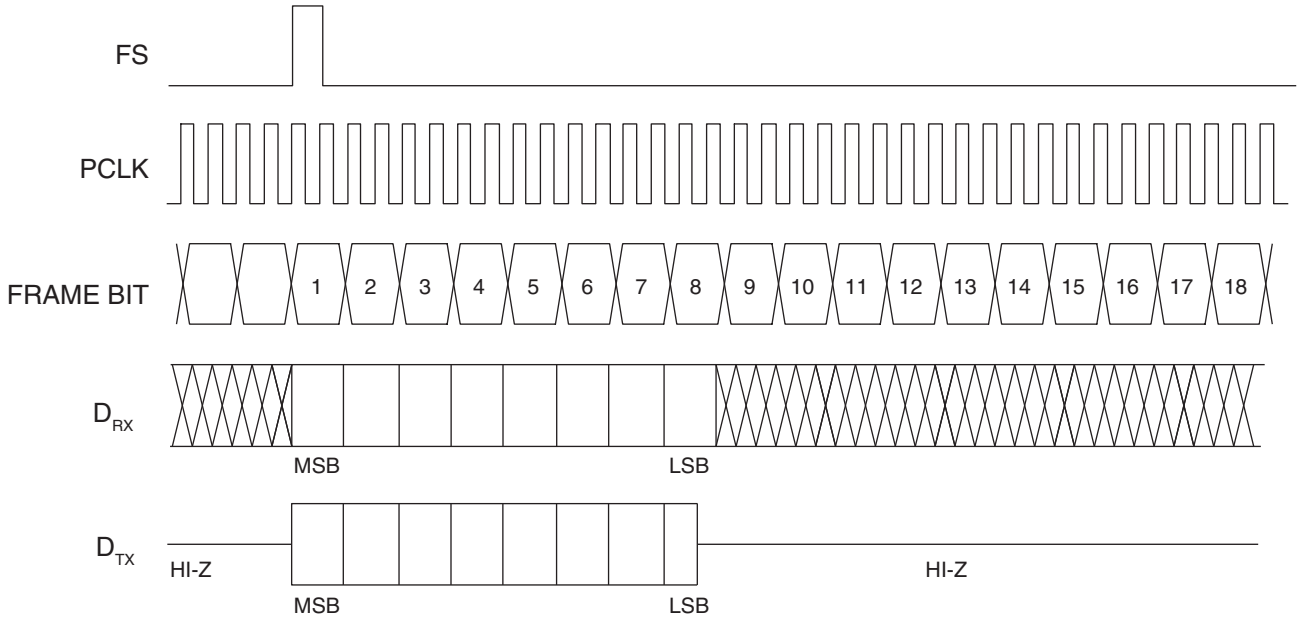


Table 3: PCM Interface AC Characteristics

Ambient temperature range -40°C to +85°C; V_{CC}=V_{DD}=3V to 3.6V

Parameter	Test Condition	Symbol	Min	Typ	Max	Units
FS Period	-	t_{FP}	-	125	-	µs
FS Jitter	-	t_{FJ}	-	-	100	ns
PCLK Cycle Time	-	t_{PC}	122	-	1955	
PCLK Duty Cycle	-		40	50	60	%
PCLK Jitter	-	t_{PJ}	-	-	±2	
PCLK Rise Time	20% to 80%	t_{PR}	-	-	25	
PCLK Fall Time	20% to 80%	t_{PF}	-	-	25	
D_{TX} Data Access Valid from PCLK Rising	-	t_{TXDA}	-	-	20	
D_{TX} Tri-State from PCLK Rising	TXZ = 0	t_{TRIR}	-	-	20	
D_{TX} Tri-State from PCLK Falling	TXZ = 1	t_{TRIF}	-	-	20	
FS Setup Time to PCLK Falling	-	t_{FSU}	25	-	-	
FS Hold Time from PCLK Falling	-	t_{FHD}	20	-	-	
D_{RX} Data Setup Time to PCLK Falling	-	t_{RXSU}	25	-	-	
D_{RX} Data Hold Time from PCLK Falling	-	t_{RXHD}	20	-	-	

Figure 5: AC Timing for PCM Time Slot 0, 1 Bit Delay (PTC=PRC=0, PTB=PRB=1, CPB=0)

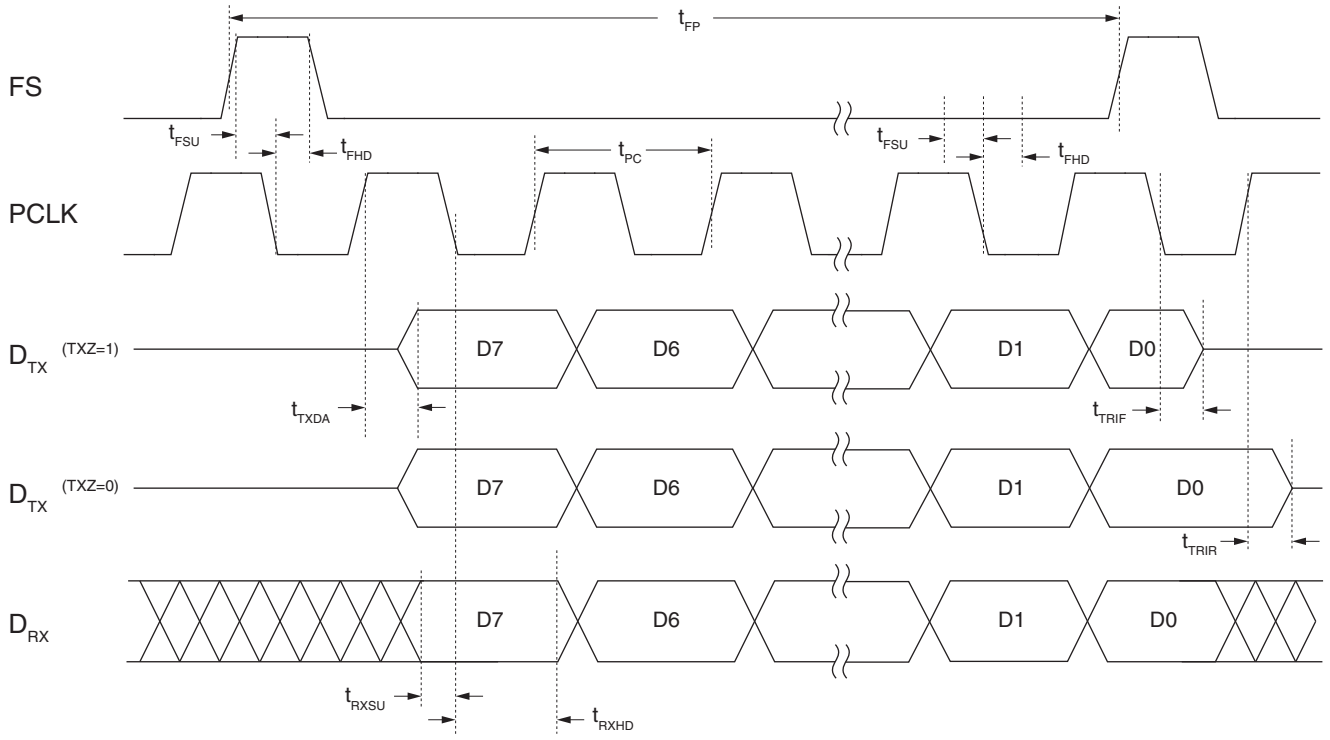
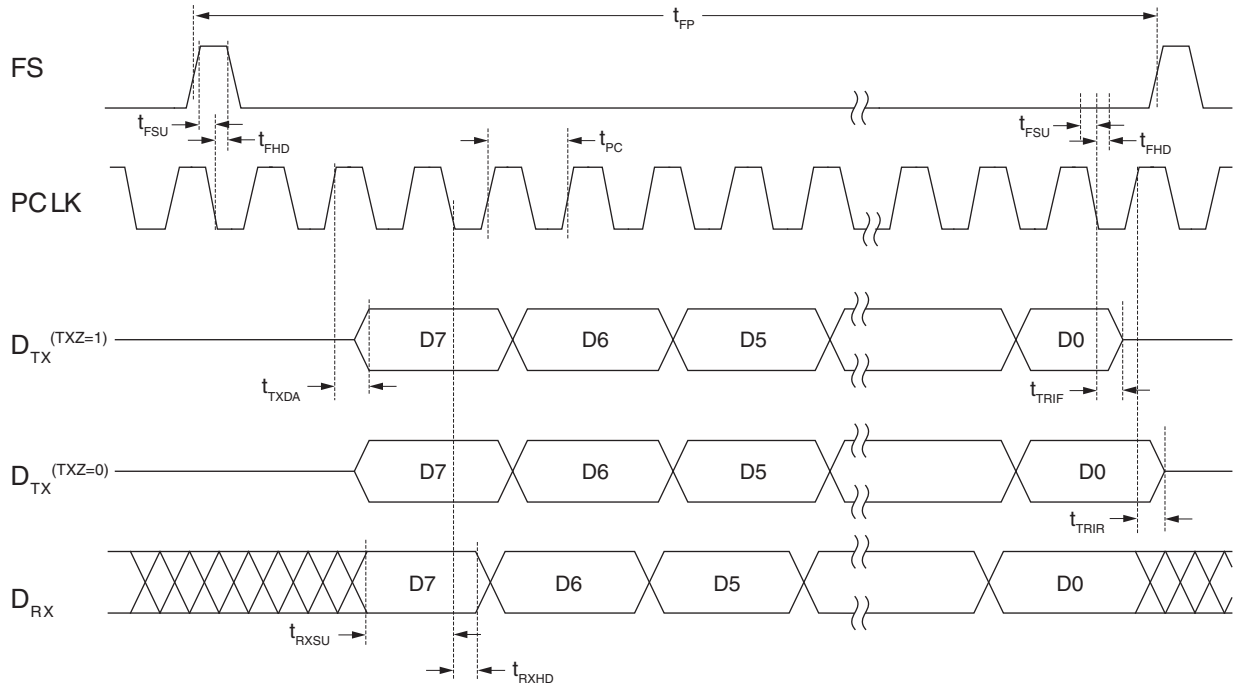


Figure 6: AC Timing for PCM Time Slot 0, 1 Bit Delay, 2x PCLK (PTC=PRC=0, PTB=PRB=1, CPB=1)



6. IOM-2 (GCI) Interface

IOM-2 is a superset specification that includes the General Circuit Interface (GCI), the line card portion of the specification. The CPC5750 implements the GCI part of this bus as specified in the Advanced Micro Devices document, IOM-2 Interface Reference Guide.

The GCI bus has an 8kHz frame sync pulse that indicates the start of each frame. Each frame consists of 8 sub-frame locations with 4 bytes per sub-frame. The CPC5750 can be configured to transmit and receive on any of these sub-frames. The selection of which sub-frame to use is done with the three pins; SCLK, SDO and SFSEL. The SPI pins SCLK and SDO are utilized since the SPI bus is not used when in the GCI Mode. The logical value of these three inputs when reset is complete sets the sub-frame assignment. Sub-Frame assignments are shown in logic table below.

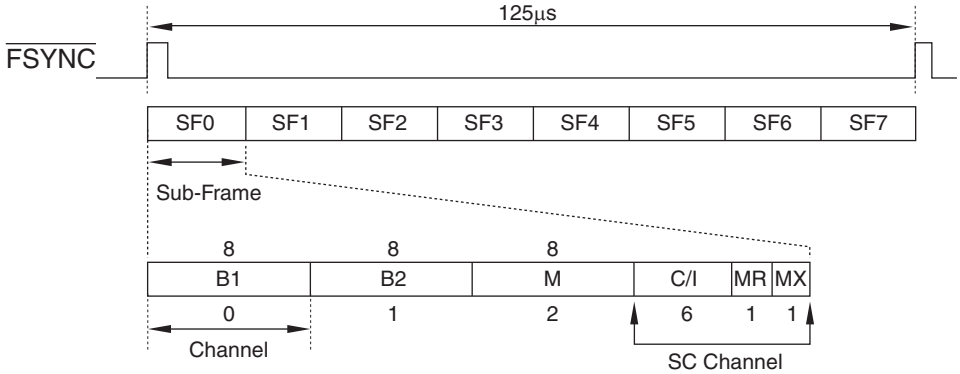
Table 4: GCI Mode Sub-Frame Selection

SCLK	SDO	SFSEL	Sub-Frame
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

The 4 bytes within each sub-frame are considered communication channels. The 32 bits of the sub-frame are designated for specific use by the standard. Each sub-frame can support a pair of codecs, one each for channels B1 & B2. Although the CPC5750 uses the entire sub-frame, only B1 is used.

(32 bits per sub-frame) x (8 sub-frames) x (8kHz frame rate) x (2 clocks per bit) = 4.096MHz clock. There is also a mode that uses 1 clock per bit for a 2.048MHz clock rate.

Figure 7: GCI Sub-Frame Makeup



Time-Multiplexed GCI Frame Structure

B1: Channel slot used to transmit and receive audio data by CPC5750

M: Channel used to read and write CPC5750 control registers

SC: Channel used to control CPC5750 register access

Figure 8 and **Figure 9** show the timing relationships between the GCI bus signals used to transmit and receive PCM data and register data when in the GCI Mode. The single-clock or double-clock mode is detected automatically by the CPC5750 in GCI Mode.

Table 5: GCI Interface AC Timing

Parameter	Test Condition	Symbol	Min	Typ	Max	Units
FS Period	-	t_{FP}	-	125	-	µs
FS Jitter	-	t_{FJ}	-	-	±120	
PCLK Cycle Time - Single-Clocking Mode	-	t_{PC}	-	488	-	
PCLK Cycle Time - Double-Clocking Mode	-	t_{PC}	-	244	-	
PCLK Jitter	-	t_{PJ}	-	-	±2	
PCLK Rise Time	20% to 80%	t_{PR}	-	-	25	
PCLK Fall Time	20% to 80%	t_{PF}	-	-	25	
TX Data Access Valid from PCLK Rising	-	t_{TXDA}	-	-	20	ns
D_{TX} Tri-State from PCLK Rising	TXZ = 0	t_{TRIR}	-	-	20	
D_{TX} Tri-State from PCLK Falling	TXZ = 1	t_{TRIF}	-	-	20	
FS Setup Time to PCLK Falling	-	t_{FSU}	25	-	-	
FS Hold Time from PCLK Falling	-	t_{FHD}	20	-	-	
D_{RX} Data Setup Time to PCLK Falling	-	t_{RXSU}	25	-	-	
D_{RX} Data Hold Time from PCLK Falling	-	t_{RXHD}	20	-	-	

Figure 8: GCI Interface AC Timing with 1x PCLK

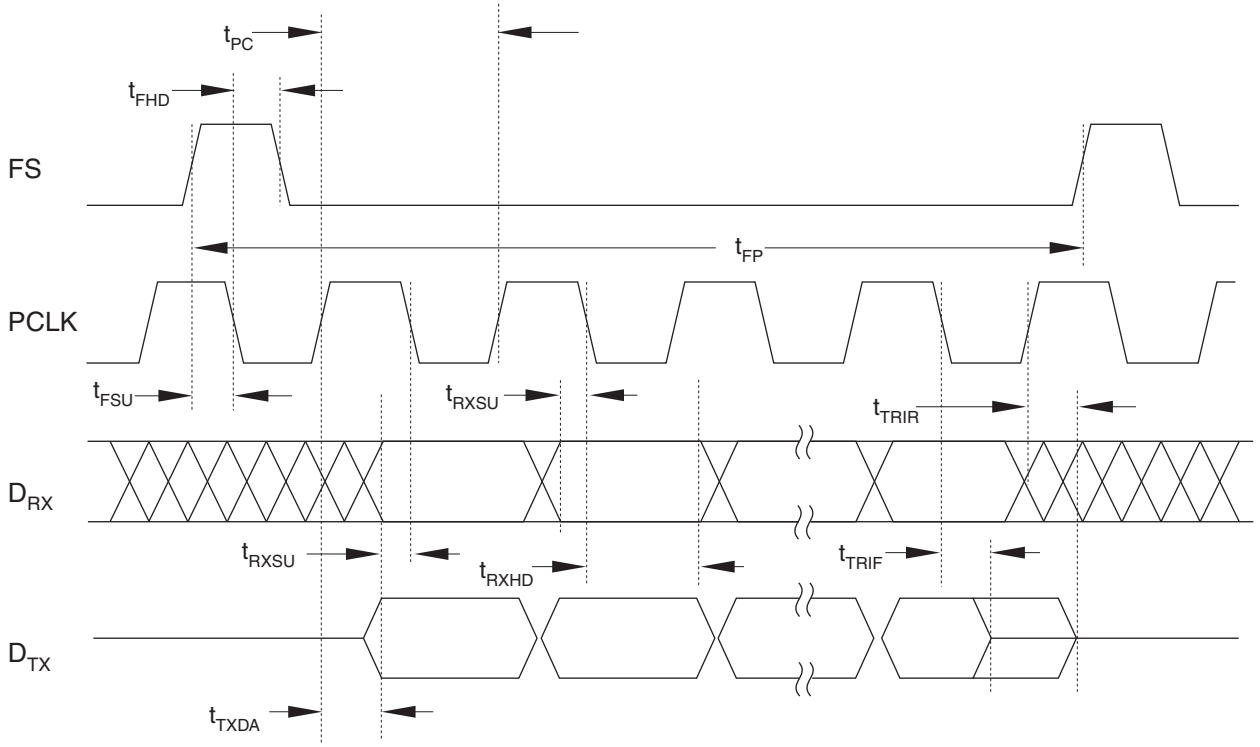
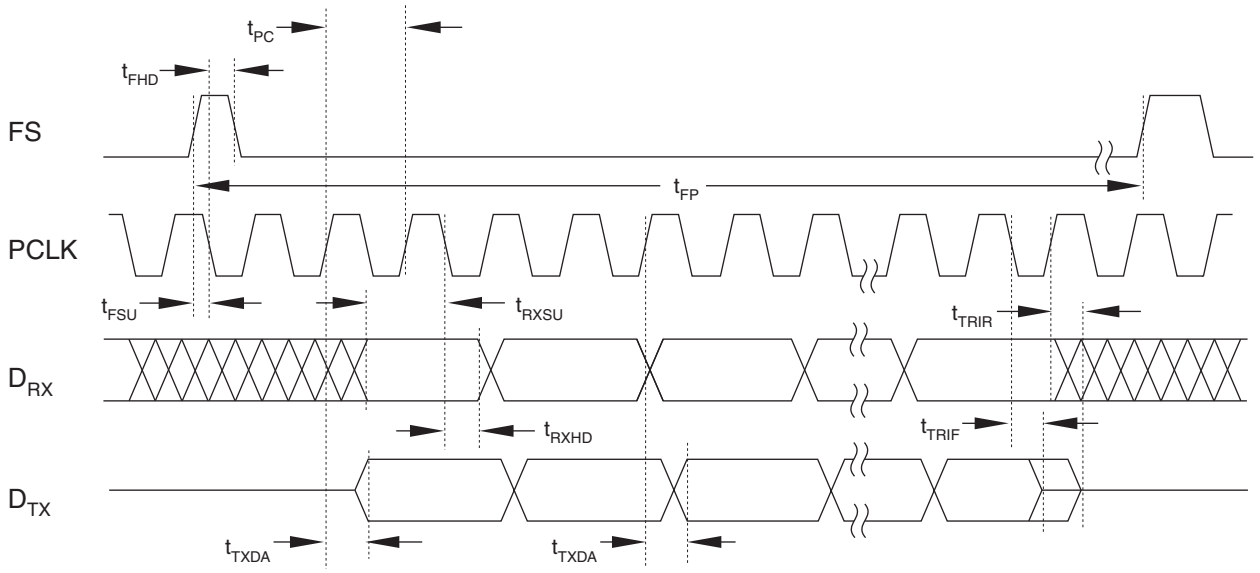


Figure 9: GCI Interface Timing with 2x PCLK



6.1 Monitor Channel Operations

The Monitor (M) channel is used for reading and writing the CPC5750's registers. The Monitor channel requires the use of the MR and MX bits in the SC channel for handshaking.

All Monitor channel transfers are in the following format:

1. Device Address: 0x91 for normal transfers, 0x90 for the special “Channel Identification Command”

2. Command: 0x81 for a read, 0x01 for a write, 0x00 for the “Channel Identification Command”

3. Address: 0x0 - 0xA corresponding to register address in **Table 1: Control Registers** (Not sent for “Channel Identification Command”)

4a. Write commands follow the address with up to 11 data bytes

4b. Read commands terminate after the address, and are followed by a write sequence (controlled by the CPC5750) that transfers data to the host device

4c. The special “Channel Identification Command” is terminated after the command byte is sent (The CPC5750 responds by controlling a write sequence to the host of two fixed bytes: 0x90, 0xB8)

Before a Monitor channel command can be started by the host device, the MX and MR bits must be inactive (high) for at least two frames. To initiate a transfer of data by the host device, the MX bit should be set active by the external controller. This signals the CPC5750 to look for a transmission on the Monitor channel. To confirm that the data was received, the CPC5750 asserts the MR bit. Once confirmation is complete, the external controller makes the MX inactive for one frame, then, if it is to continue to transmit, it sets the MX bit active again; otherwise, it ends the message by leaving the MX bit inactive for another frame.

When writing data, an initial address must be specified. Once the data is written to that address, the CPC5750 automatically increments the address after every register access so that in one transmission multiple consecutive registers can be written (see **Figure 11**). The transmission can continue until either an invalid memory location is reached or the host device sends two frames with MX inactive.

When the host device wants to read a register or registers, it begins by controlling the MX bit, and the CPC5750 controls the MR bit exactly as in a write command except that the second byte sent is the read command code 0x81. The third byte sent is the register address to be read first. The CPC5750 responds by controlling its MX bit to begin a write transfer to the host device. This transfer begins with the contents of the register addressed in the read command, and auto-increments the register address for each byte read (see **Figure 10**). When the CPC5750 is not executing a read command from the host, it transmits 0xFF on the monitor byte.

The CPC5750 can also signal an abort by sending two frames with the MR bit inactive. The CPC5750 will signal an abort if:

- The host device attempts to read or write from an invalid memory location
- The CPC5750 does not recognize the command it received
- The data byte received was not held for at least two consecutive frames
- A collision occurs on the monitor data bytes while the CPC5750 is transmitting (see **Figure 12**, **Figure 13**, and **Figure 15**).

If an invalid command is received, the state of the CPC5750 does not change. If the host device attempts to read or write to an invalid memory address, the previous reads or writes to the memory are still valid. If the abort signal is detected before a command has been sent, the CPC5750 returns to an idle state and no changes are made.

Figure 10: Example GCI Read from Mode Control and RX Gain ±1dB Registers

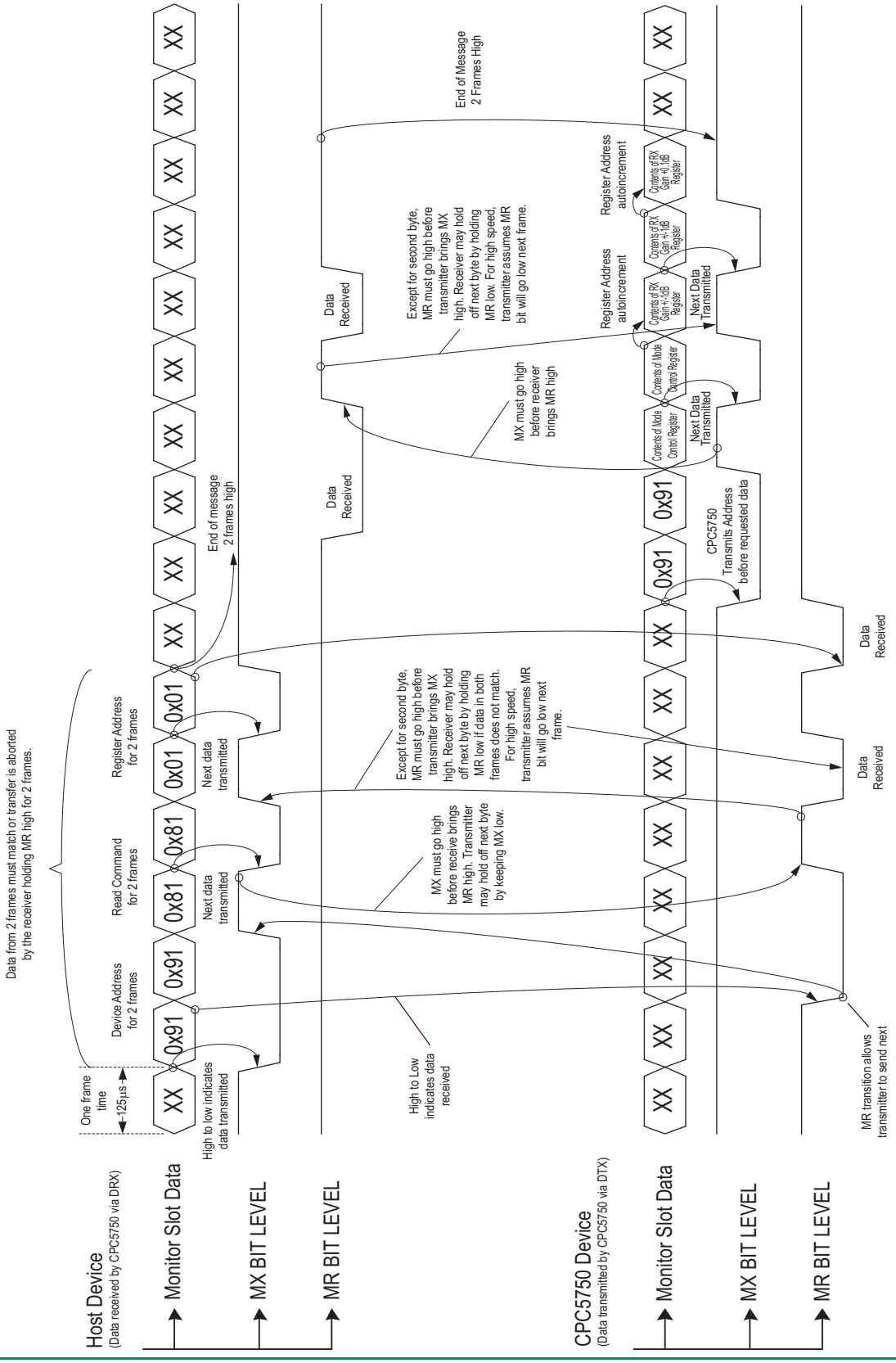


Figure 11: Example GCI Write to Mode Control and RX Gain ±1dB Registers

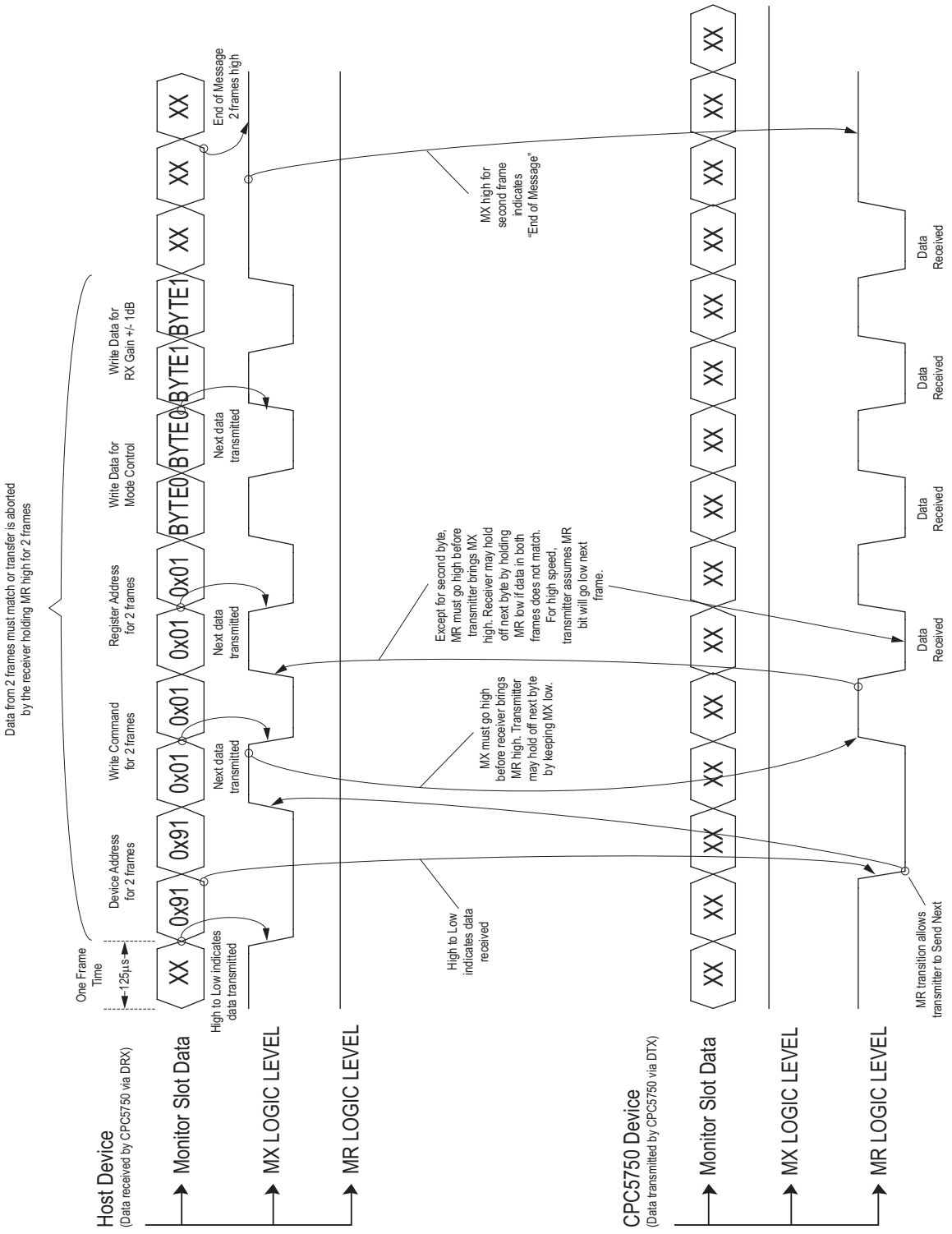


Figure 12: Example GCI Write Command Aborted Due to Invalid Address

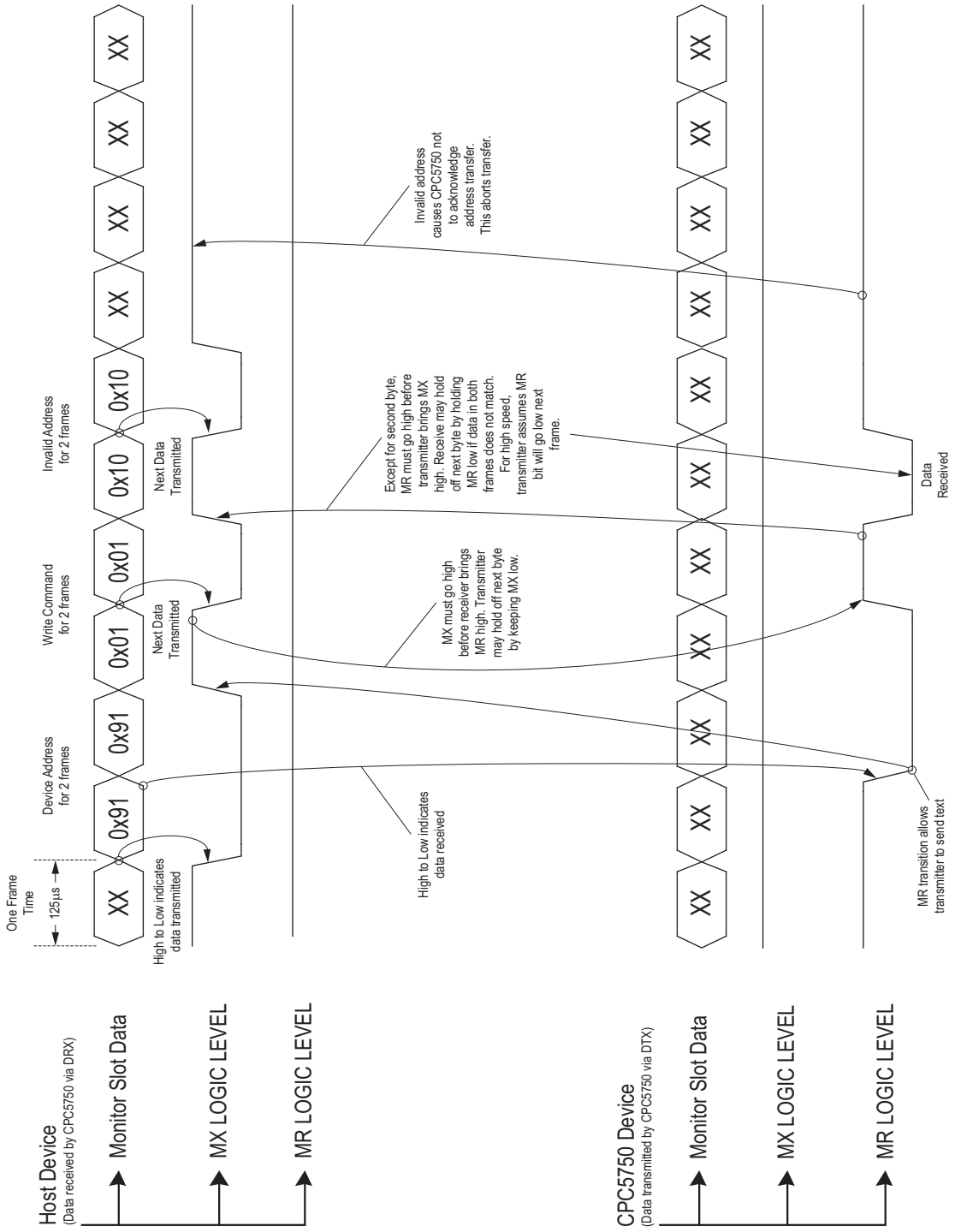


Figure 13: Example GCI Write Command Aborted Due to Frame Mismatch

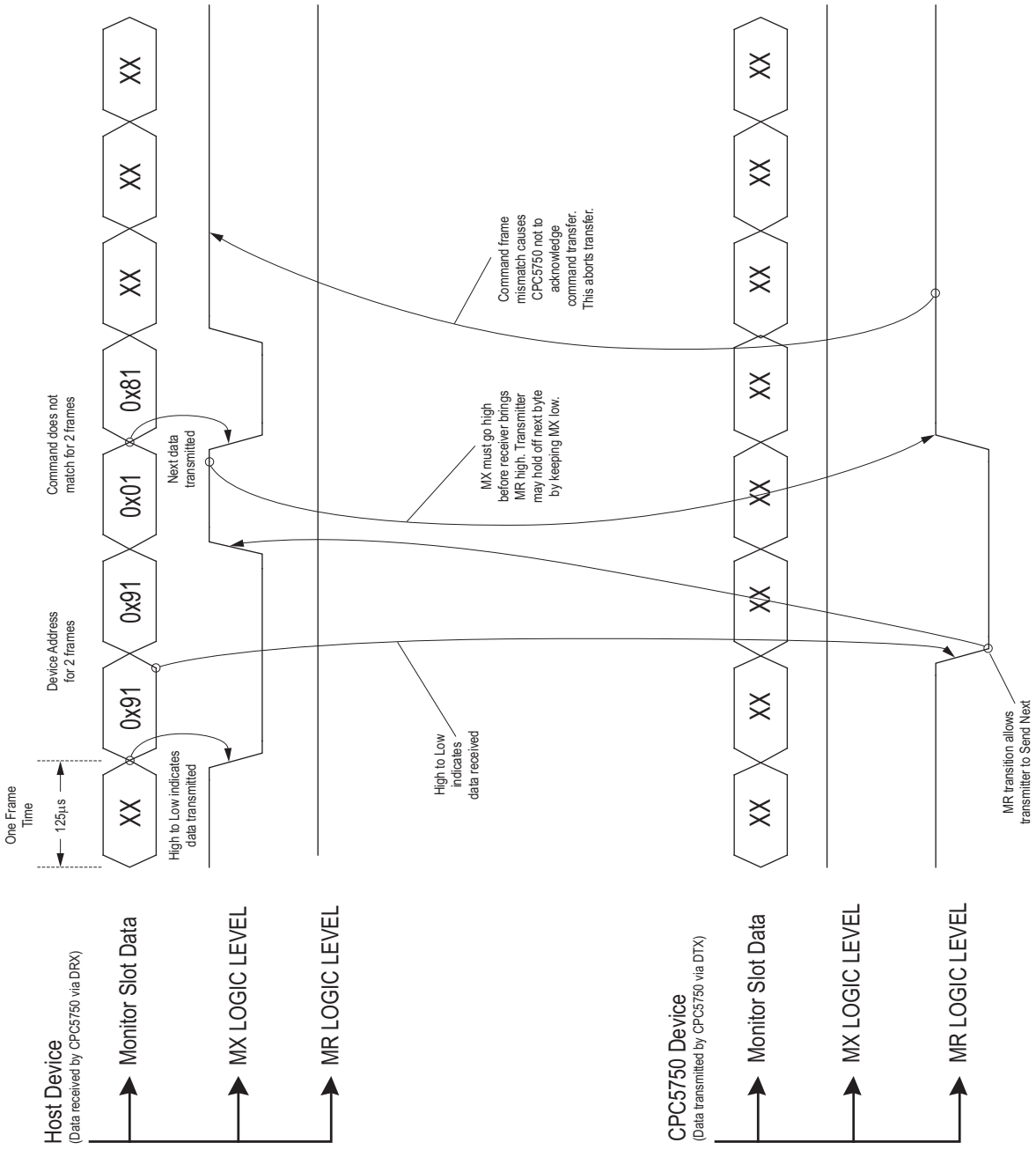


Figure 14: Example GCI Channel Identification Command

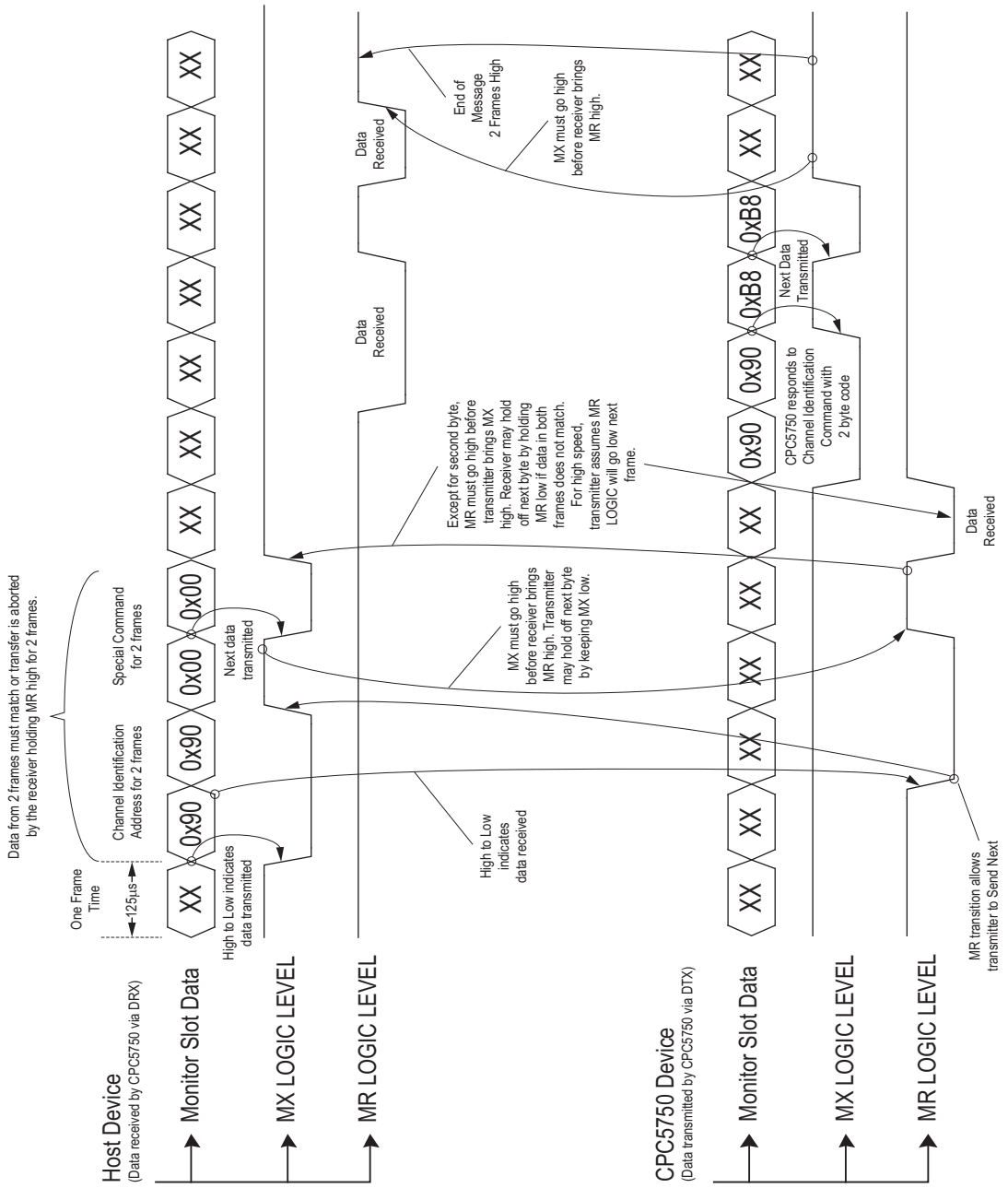
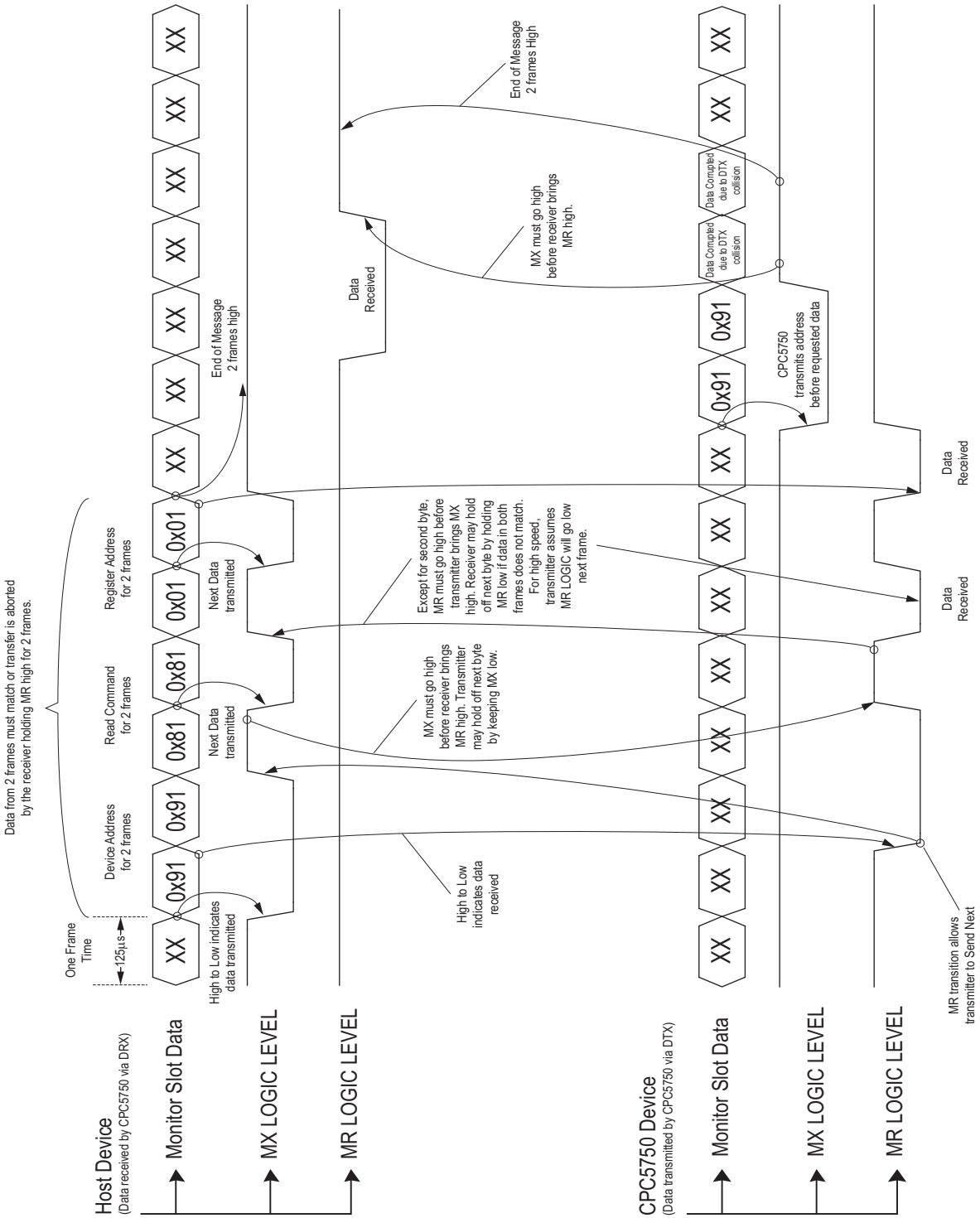


Figure 15: Example GCI Read Command Aborted Due to Bus Contention



7. 4-Wire SPI (Serial Peripheral Interface)

A 4-wire, bidirectional serial interface is used for control and status monitoring when the CPC5750 is configured for the PCM transmission mode. Typical hardware implementation of a SPI bus consists of a single master with one or more slave devices where the role of the master is generally performed by the system controller. In PCM voice circuit applications where a configurable CODEC is utilized such as the CPC5750, the CODEC is a slave. Data is passed between the master and slave(s) by means of four logic signals. They are: SCLK (the serial clock); SDO (the serial data out); SDI (the serial data in); and $\overline{CS}$ (the chip select line). Of these four logical signals, three are output by the SPI bus master. The SPI bus master drives the CPC5750 serial data pins SCLK, SDI and $\overline{CS}$. For the SPI bus to function properly, the bus master's input and output nodes must be cross connected to the SPI bus slave's output and input nets. This means, the master's SDO output must be connected to the slave's SDI input and the slave's SDO output must be connected to the master's SDI input. In order to connect multiple slave devices onto the SPI bus, all slaves must set their SDO output to high impedance (HI-Z) when not actively driving the common SDO net and each slave must have it's own dedicated $\overline{CS}$ connection back to the SPI bus master.

SPI bus commands issued by the system controller to the CPC5750 are eight bits in length (MSB first) and are constructed by appending the command nibble (4 bits) with the register address nibble. The CPC5750 SPI bus circuitry recognizes only two commands; they are READ and WRITE. For the system controller to issue a command via the SPI bus it must drive the three SPI bus slave inputs; SCLK, $\overline{CS}$ and SDI.

Write commands are the means by which the system controller places data into one the CPC5750 control registers. Each packet of a single register write sequence contains an 8-bit command byte appended by the 8-bit data byte to be stored in the register listed in the command byte. The CPC5750 inputs eight bits of SDI data beginning with the first rising edge of SCLK after $\overline{CS}$ goes active (low). When the input data byte is 0xB (1011) followed by a legitimate four bit register address, the command is accepted and the second data byte is written into the appropriate register. This sequence is illustrated in **Figure 16**.

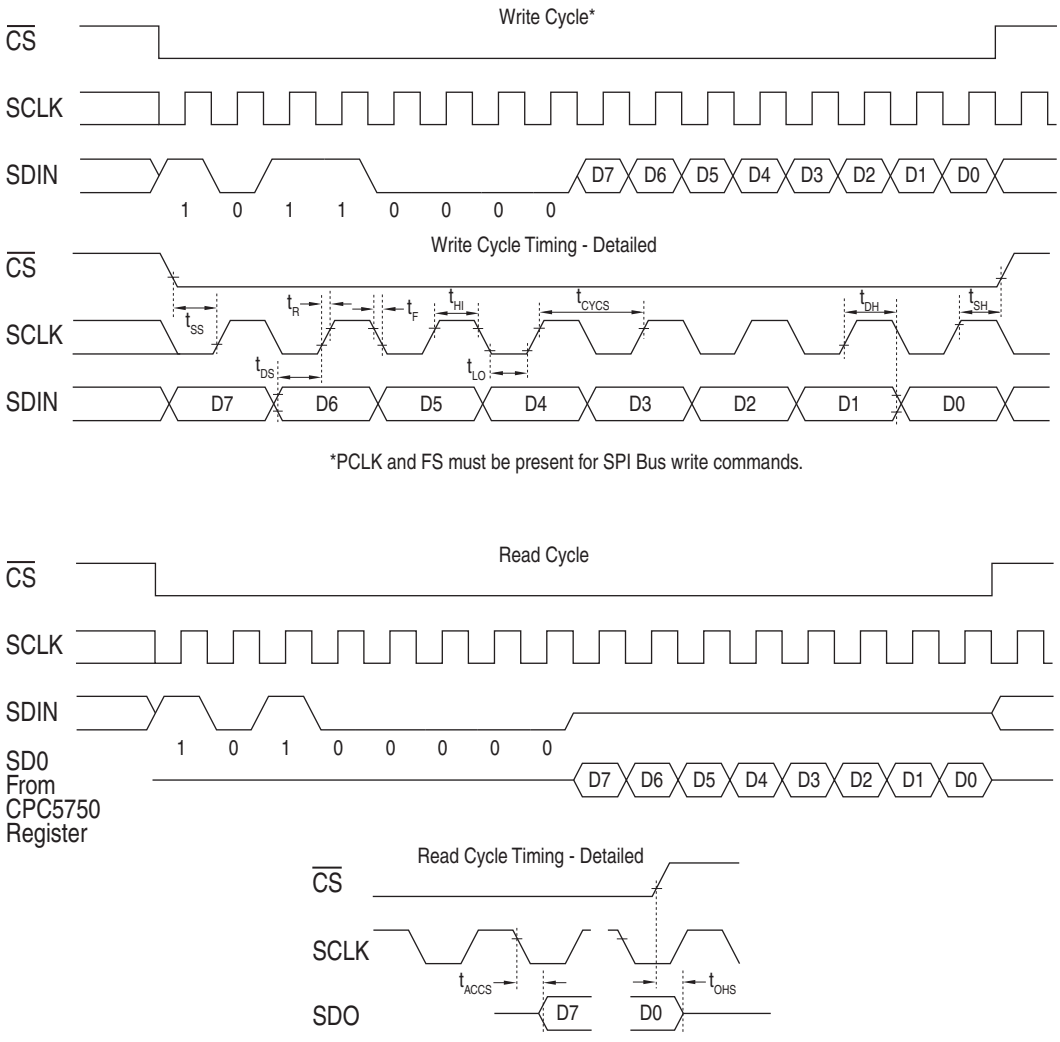
Read commands are used by the system controller to validate the values written into the configuration registers and to query the logical values applied to the GPIO ports configured as inputs. The read command byte sequence is the same as described above for the write mode. The CPC5750 recognizes and accepts read commands when the input data byte is 0xA (1010) followed by a legitimate four bit register address. With a valid read command, the CPC5750 will output the eight data bits contained in the register listed in the command byte. This data is output onto the SDO net beginning with the MSB of the register's contents on the first falling edge of SCLK after the rising edge of SCLK used to clock in the LSB of the command byte. In this manner, the first control register bit will be available to the system controller on the next rising edge of SCLK. Reliable data transfer from the CPC5750 to the system controller requires $\overline{CS}$ to remain low while the CPC5750 is outputting data, going high only after satisfying the controller's input data setup and hold time requirements to ensure the last output bit is received. This sequence is illustrated in **Figure 16**.

Multi-byte writes and reads are supported for single write or read commands. The register address automatically increments after each data byte for as long as $\overline{CS}$ is active.

Table 6: SPI Timing

Parameter	Condition	Symbol	Min	Max	Units
Cycle Time	-	t_{CYCS}	250	-	ns
Pulse Width	-	t_{HI}, t_{LO}	50	-	
Pulse Edge Rise Time	-	t_R		50	
Pulse Edge Fall Time	-	t_F		50	
Data Setup Time	-	t_{DS}	50	-	
Data Hold Time	-	t_{DH}	30	-	
$\overline{CS}$ Setup Time, Write	-	t_{SS}	30	-	
$\overline{CS}$ Hold Time, Write	-	t_{SH}	30	-	
Read Access Time	C_L=100pF	t_{ACCS}	-	30	
Read Output Disable Time	C_L=100pF	t_{OHS}	-	30	

Figure 16: 4-Wire SPI



7.1 Data Compression/Expansion

The differential analog signal on $A_{IN+/-}$ is converted and filtered as 14-bit data internally. This digital data is compressed to 8 bits as specified by the ITU G.711 standard before being transmitted in 8-bit words via the PCM bus.

8-bit data received via the PCM interface is decompressed as specified by ITU G.711 to 14-bit data before being converted to a differential analog signal, and output on the $A_{OUT+/-}$ signals.

7.2 Power On Reset (POR)

The power-on-reset circuit will be active when power is first applied to the device. This power up active reset signal will go inactive after 20µs nominally. Additionally, a hardware reset pin ($\overline{RST}$) is supplied to force an internal reset. The hardware reset pin is also de-bounced by the same nominal 20µs delay.

8. Manufacturing Information

8.1 Moisture Sensitivity



All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits Division classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL) rating** as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Rating
CPC5750U	MSL 1

8.2 ESD Sensitivity



This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

8.3 Reflow Profile

This product has a maximum body temperature and time rating as shown below. All other guidelines of **J-STD-020** must be observed.

Device	Maximum Temperature x Time
CPC5750U	260°C for 30 seconds

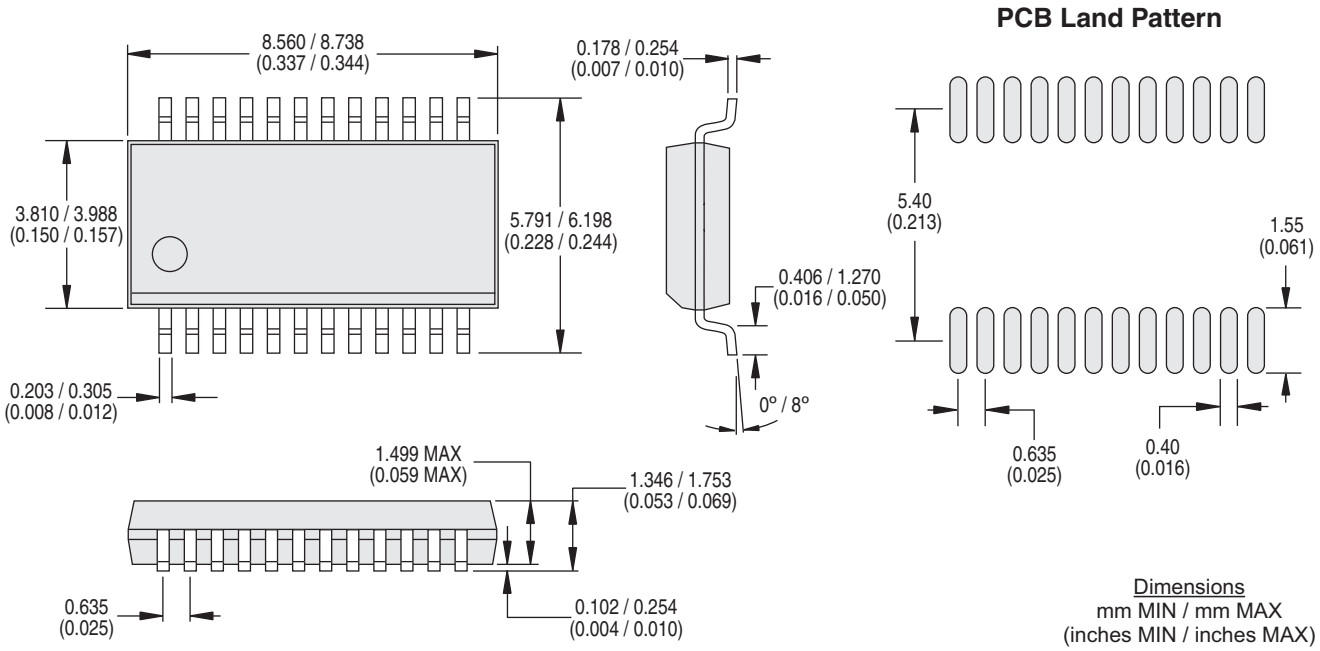
8.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. However, board washing to remove flux residue is acceptable, and the use of a short drying bake may be necessary. Chlorine-based or Fluorine-based solvents or fluxes should not be used. Cleaning methods that employ ultrasonic energy should not be used.

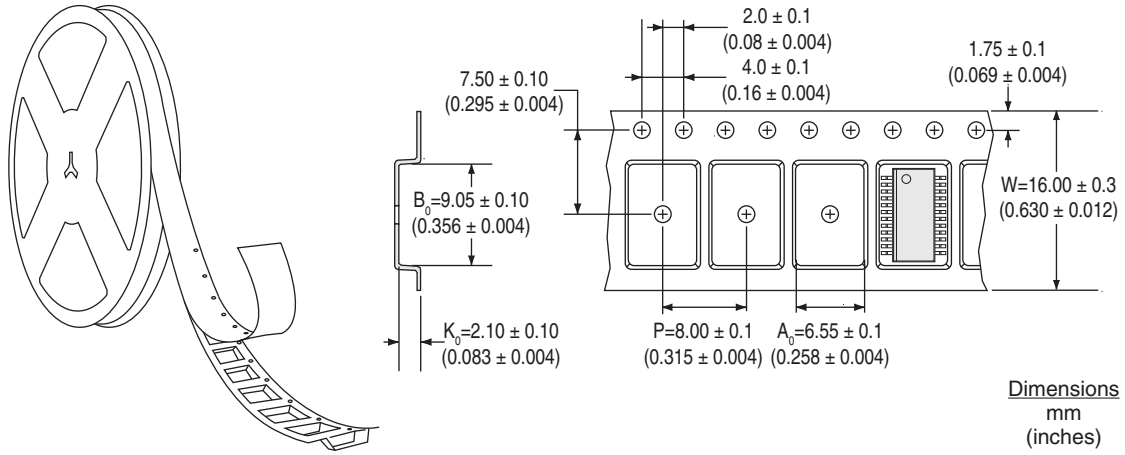


8.5 Mechanical Dimensions

8.5.1 CPC5750U - 24-Pin SSOP Package



8.5.2 Tape and Reel Drawing



For additional information please visit our website at: www.ixysic.com

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Specification: DS-CPC5750-Rev F
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6/8/2015