PROCESS CP705

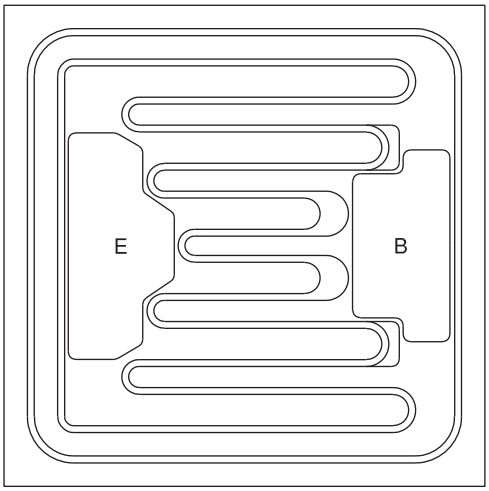
Small Signal Transistor

PNP - High Current Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	31 x 31 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	5.9 x 11.8 MILS
Emitter Bonding Pad Area	6.5 x 13.8 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

GEOMETRY



BACKSIDE COLLECTOR R2

GROSS DIE PER 4 INCH WAFER

11,212

PRINCIPAL DEVICE TYPES

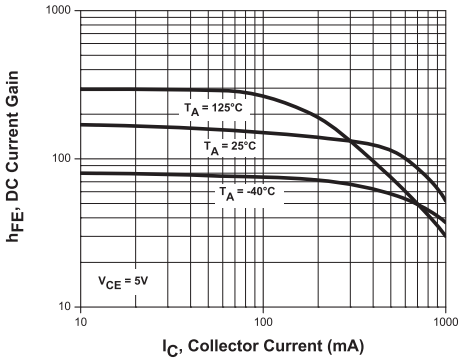
2N4033
CMPT4033
CXT4033
CZT4033

R4 (22-March 2010)

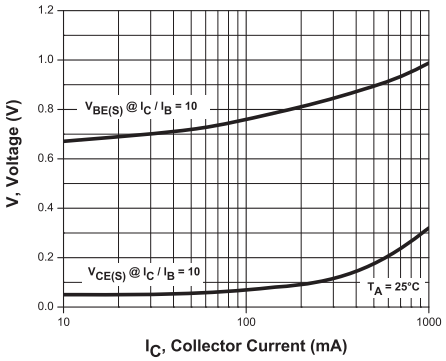
PROCESS CP705

Typical Electrical Characteristics

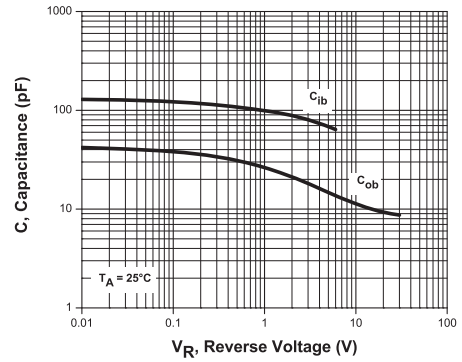
DC Current Gain



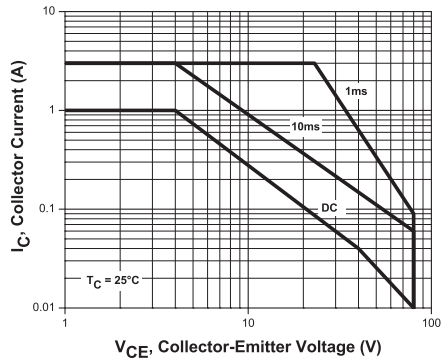
"ON" Voltage



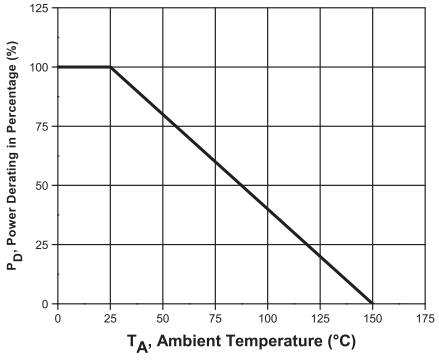
Capacitance



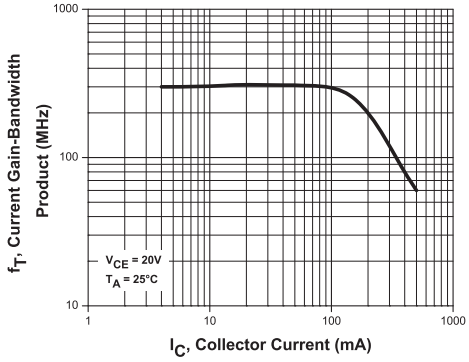
Safe Operating Area



Normalized Power Derating



Current Gain-Bandwidth Product



R4 (22-March 2010)