# PROCESS CP341V

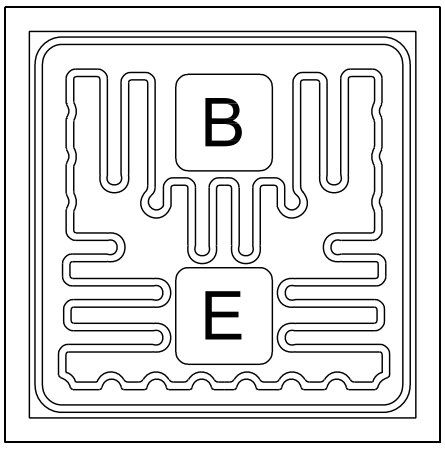
## Small Signal Transistors

### NPN - Low $V_{CE(SAT)}$ Transistor Chip

**PROCESS DETAILS**

| | |
|---|---|
| Process | Epitaxial Planar |
| Die Size | 18 x 18 MILS |
| Die Thickness | 7.1 MILS |
| Base Bonding Pad Area | 3.8 x 3.8 MILS |
| Emitter Bonding Pad Area | 3.8 x 3.8 MILS |
| Top Side Metalization | Al/Si - 30,000Å |
| Back Side Metalization | Au - 12,000Å |

**GEOMETRY**




BACKSIDE COLLECTOR R0

**GROSS DIE PER 5 INCH WAFER**

54,330

**PRINCIPAL DEVICE TYPES**

CMLT3410
CMPT3410
CMST3410
CMUT3410

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R0 (5- January 2006)