USB Peripheral Power Management

Features

- 3.3V regulated output up to 500mA
- Quiescent current 35µA (typical)
- Shutdown mode current 7µA (typical)
- 30ms active LOW Power-On Reset (POR) pulse
- Thermal overload protection
- Foldback current limiting protection
- Reverse-current protection
- 8 pin SOIC power package

Applications

- Bus-powered USB peripherals
- Self-powered USB peripherals
- Portable/battery-powered devices
- Critical power monitoring, hot-insertion devices

The SmartOR™ CMPWR160 combines a Low Dropout Regulator (LDO) with a Power-On Reset (POR) pulse generator, and is intended for Universal Serial Bus (USB) peripherals. To meet the specification requirements of both USB 1.0 and USB 2.0, the CMPWR160 draws a very low quiescent current (35µA), and delivers up to 500mA of load current at a fixed 3.3V output.

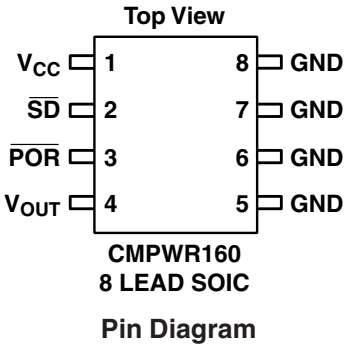
The POR pulse (active LOW) has a typical duration of 30ms after the output has exceeded and stabilized above 2.9V. Thus a new POR pulse is developed each time the regulator power is interrupted and restored, which occurs often on USB buses when cables are connected (or disconnected) by the user. It is not necessary to have a V_{CC} supply for POR to operate, allowing the CMPWR160 to work in Wired-ORed power systems.

When V_{CC} is powered down, the device will automatically enter reverse-current protection mode and maintain isolation between V_{OUT} and V_{CC}. This is useful for applications that can use power from the USB port in addition to internal batteries or an AC adapter supply (Wired-ORed power systems). In the event of V_{CC} collapsing below V_{OUT}, the device will automatically enter shutdown mode and fully isolate the V_{CC} power source from the output.

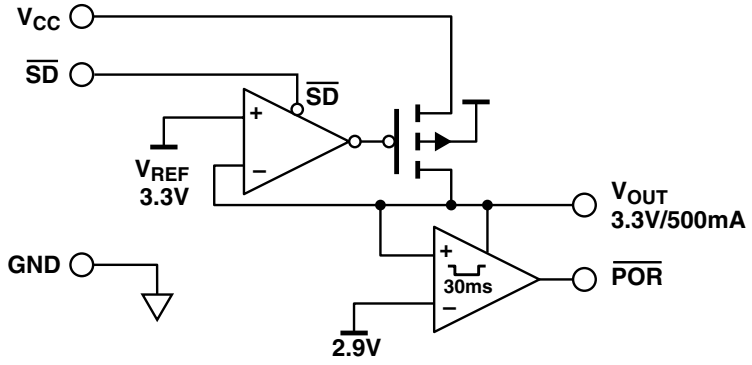
A ShutDown input ($\overline{SD}$) forces the regulator to be powered down on demand. While in shutdown mode the POR circuitry will remain active, making the device suitable for systems which contain backup or alternative power sources.

The CMPWR160 is available in an 8-pin SOIC thermally enhanced package, ideal for applications where space is tight.

Block Diagram



Pin Diagram



Simplified Electrical Schematic

Standard Part Ordering Information

Package		Ordering Part Number		
Pin	Style	Tubes	Tape & Reel	Part Marking
8	Power SOIC	CMPWR160SA/T	CMPWR160SA/R	CMPWR160SA

C1571000

Absolute Maximum Ratings		
Parameter	**Rating**	**Unit**
ESD Protection (HBM)	2000	V
V_{CC}/V_{OUT} Voltage	6.0, GND –0.5	V
$\overline{SD}$ Logic Input Voltage	V_{CC} + 0.5, GND –0.5	V
$\overline{POR}$ Logic Output Voltage	V_{OUT} + 0.5, GND –0.5	V
Temperature: Storage Operating Ambient Operating Junction	–40 to 150 0 to 70 0 to 125	°C
Power Dissipation Note 1	Internally Limited	

Operating Conditions		
Parameter	**Range**	**Unit**
V_{CC}	4.2 to 5.5	V
Temperature (Ambient)	0 to 70	°C
Load Current	0 to 500	mA
C_{EXT}	10 ± 10%	µF

Electrical Operating Characteristics
(over operating conditions unless specified otherwise)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
V_{OUT}	Regulator Output Voltage	0mA < I_{LOAD} < 500mA	3.135	3.30	3.465	V
I_{LIM}	Regulator Current Limit		550			mA
$I_{S/C}$	Short-Circuit Current Limit			300		mA
$V_{R\ LOAD}$	Load Regulation	V_{CC} = 5V, I_{LOAD} = 5mA to 500mA		75		mV
$V_{R\ LINE}$	Line Regulation	V_{CC} = 4.2V to 5.5V, I_{LOAD} = 5mA		2		mV
V_{DO}	Regulator Dropout Voltage	MIN $V_{CC} - V_{OUT}$ for I_{LOAD} = 500mA		0.6	0.9	V
I_Q	Quiescent Supply Current	Regulator Enabled (No Load)		35	50	µA
I_{SD}	Shutdown Supply Current	Regulator Disabled		7	10	µA
I_{RCC}	V_{CC} Pin Reverse Leakage	V_{OUT} = 3.3V, V_{CC} = 0V		1	10	µA
$V_{IH\ SD}$	Shutdown High Detect	V_{CC} = 5V		3.0		V
$V_{IL\ SD}$	Shutdown Low Detect	V_{CC} = 5V		1.0		V
V_{POR}	POR Detect Threshold	4.2V < V_{CC} < 5.5V	2.8	2.9	3.0	V
T_{POR}	POR Pulse Duration		20	30	40	ms
R_{POR}	POR Output Impedance	After POR Threshold Detected Sinking to GND/Sourcing from V_{CC}	0.2	0.5	2	kΩ
$T_{DISABLE}$	Shutdown Temperature			160		°C
T_{HYST}	Thermal Hysteresis			20		°C

Note 1: The SOIC package used is thermally enhanced through the use of a fused integral leadframe. The power rating is based on a printed circuit board heat spreading capability equivalent to 2 square inches of copper connected to the GND pins. Typical multi-layer boards using power plane construction will provide this heat spreading ability without the need for additional dedicated copper area. (Please consult with factory for thermal evaluation assistance.)

Interface Signals

V_{CC} is the input power source for the Low Drop Out Regulator, capable of delivering 3.3V/500mA output current even when the input is as low as 4.2V.

Internal loading on this pin is typically 35µA when the regulator is enabled, which reduces to only 7µA whenever the regulator is shutdown ($\overline{SD}$ taken Low). In the event of V_{CC} collapsing below V_{OUT}, the loading at V_{CC} will immediately reduce to less than 0.1µA.

If the V_{CC} pin is within a few inches of the main input filter, a capacitor may not be necessary. Otherwise an input filter capacitor in the range of 1µF to 10µF will ensure adequate filtering.

$\overline{SD}$ is the regulator shutdown input logic signal which is Active Low. This is a true CMOS input signal referenced to V_{CC} supply. When the pin is tied High (V_{CC}) the regulator operates fully. When the pin is taken to GND, the device enters shutdown mode and the regulator is fully disabled. In this mode all critical $\overline{POR}$ circuitry remains fully powered consuming less than 7µA (typical).

V_{OUT} is the regulator output voltage used to power the load. An output capacitor of 10µF is used to provide the necessary phase compensation, thereby preventing oscillation. The capacitor also helps to minimize the peak output disturbance during line or load transients. Whenever V_{CC} collapses below the output the device immediately enters reverse protection mode to prevent any current flow back into the regulator pass transistor. Under these conditions V_{OUT} will also be used to provide the necessary quiescent current for the internal reference and $\overline{POR}$ circuits. This ensures excellent start-up characteristics for the regulator.

$\overline{POR}$ is the Power-On-Reset output pin (Active Low).

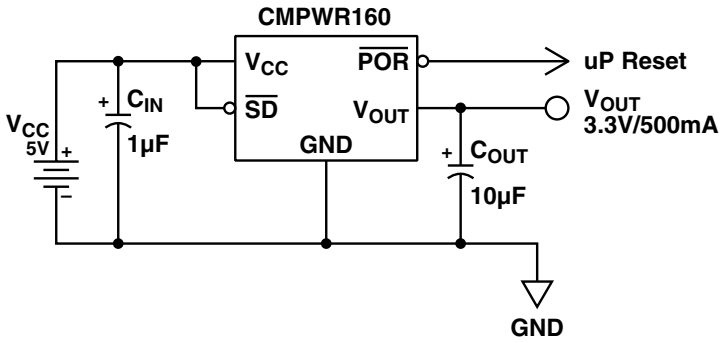
When V_{OUT} rises above the $\overline{POR}$ threshold voltage (typically 2.9V), the pin is forced to logic low (GND). The pin remains logic low for 30ms then it is forced logic high (3.3V). If V_{OUT} falls below the $\overline{POR}$ threshold voltage during this 30ms interval $\overline{POR}$ will remain logic low. If it falls below the voltage threshold and then recovers the 30ms time will reset.

If V_{OUT} falls below the $\overline{POR}$ threshold voltage $\overline{POR}$ is immediately forced to logic low.

The power-on reset circuitry is designed to remain active under all conditions and will produce a valid output even when V_{CC} is not present. A very low quiescent current (7µA typical) ensures continuous operation of the POR circuit.

GND is the negative reference for all voltages. This current that flows in the ground connection is very low (35µA typical with the regulator enabled and 7µA typical with the regulator disabled).

Pin Functions	
Symbol	**Description**
V_{CC}	Positive supply input for regulator. When V_{CC} falls below V_{OUT} the regulator is disabled.
SD	Shutdown control input signal (Active Low) to disable internal voltage regulator and current supply to less than 7µA.
POR	Power-On-Reset output signal is held Low until the output has been stable (>2.9V) for at least 30ms.
V_{OUT}	Regulator voltage ouput (3.3V) capable of delivering 500mA when device is enabled (SD is High). Whenever the output exceeds 2.9V (TYP) the POR pulse is triggered.
GND	Negative reference for all voltages



Typical Application Circuit

Typical DC Characteristics

Unless stated otherwise, all DC characteristics were measured at room temperature with a nominal V_{CC} supply voltage of 5V and an output capacitance of 10µF. Resistive load conditions were used.

Line Regulation Characteristics of the regulator are shown in Figure 1. At maximum rated load conditions (500mA), a 100mV drop in regulation occurs when the line voltage has collapses below 3.8V. For light load conditions (5mA), regulation is maintained for line voltages as low as 3.3V.

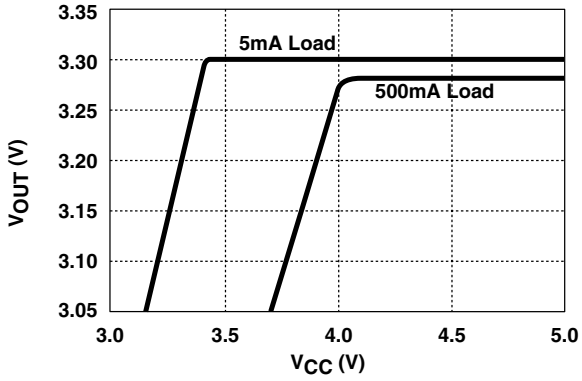


Figure 1. Line Regulation

Load Regulation performance is shown from zero to maximum rated load in Figure 2. A 10% to 100% change of rated load, results in an output voltage change of less than 10mV. This translates into an effective output impedance of approximately 0.02Ω.

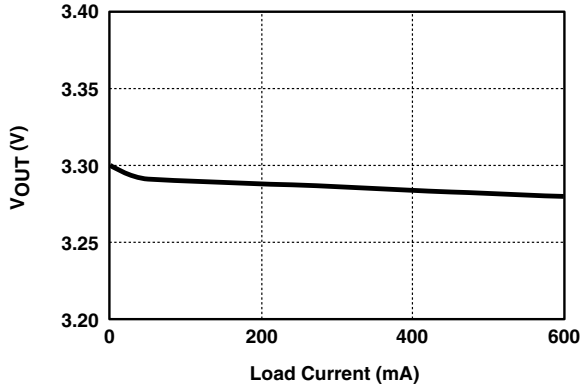


Figure 2. Load Regulation

Ground Current is shown across the entire range of load conditions in Figure 3. The ground current increases by 40µA across the range of load conditions. This increase is due to the current limiting protective circuitry becoming active.

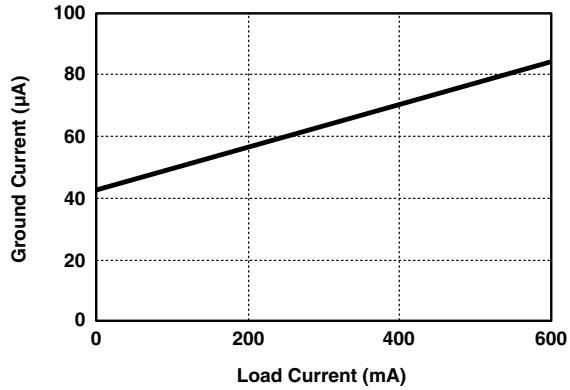


Figure 3. Ground Current

Typical DC Characteristics continued

V_{cc} Operating Current (no load, $\overline{SD}$ high) is shown across a range of V_{CC} supply voltages with the regulator enabled in Figure 4. The graph shows that the operating current is 35µA typical and changes by less than 1µA across this range.

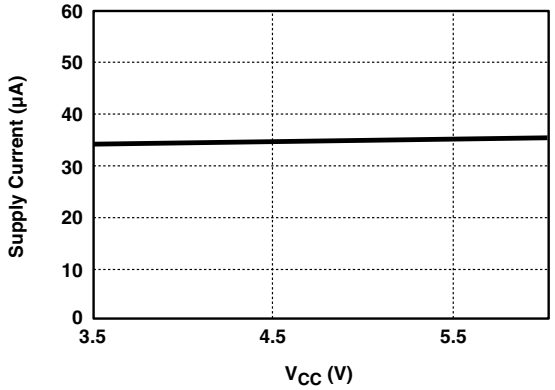


Figure 4. V_{cc} Operating Current (no load)

V_{cc} Shutdown Current variation with the V_{CC} supply voltage is shown in Figure 5.

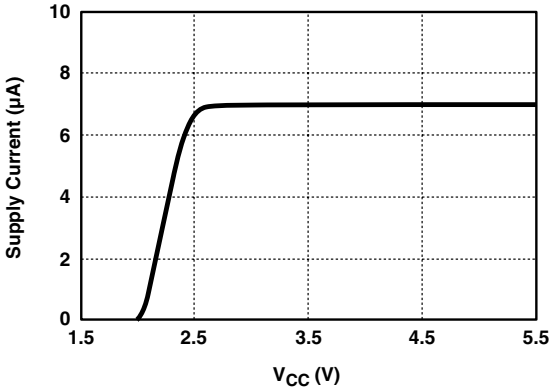


Figure 5. V_{cc} Shutdown Current

Typical Transient Characteristics

The transient characterization test setup is shown in Figure 6. It was the setup used for the transient tests unless specified otherwise.

A maximum rated load current of 6.6Ω (500mA @ 3.3V) was used during characterization along with a nominal V_{CC} supply voltage of 5V DC, unless specified otherwise.

The load transient characterization was done by switching between 6.6 and 660Ω load resistors. This switched the load between 500 and 5mA respectively.

For the V_{CC} power-up and power-down characterizations V_{CC} supply was ramped between 0 and 5V. Both the rise and fall times for the V_{CC} power-up/down pulses were controlled to be 15ms.

In the line transient characterizations the V_{CC} supply voltage was controlled to step between 4.5 to 5.5V.

For the $\overline{POR}$ response characterization V_{CC} and $\overline{SD}$ were tied to ground and the V_{OUT} voltage was directly driven between 2.7 and 3.1V. This was done by connecting a function generator directly to the output of the device. These voltage values were picked because it drove V_{OUT} directly across the typical $\overline{POR}$ threshold voltage of 2.9V. V_{CC} was tied to ground to show that the $\overline{POR}$ circuitry will operate even when the V_{CC} supply voltage is not present.

The oscilloscope traces show the full bandwidth response at the $\overline{SD}$, $\overline{POR}$, V_{CC} and V_{OUT} pins depending on the characterization.

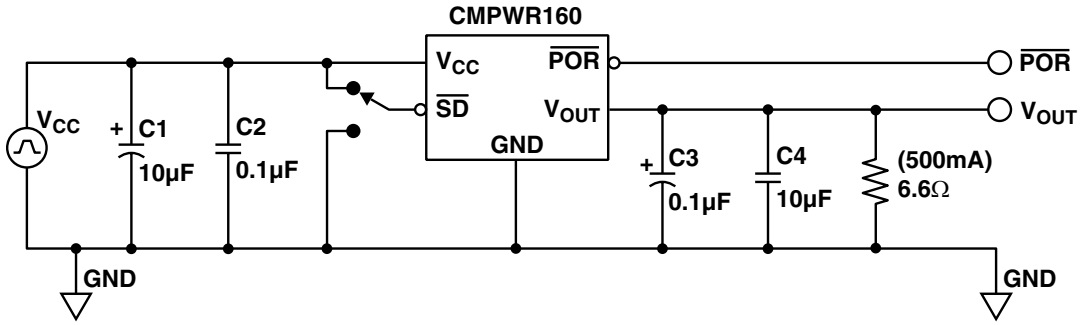


Figure 6. Transient Characterization Test Setup

V_{CC} power-up Cold Start

Figure 7 shows the output response during an initial V_{CC} power up with $\overline{SD}$ tied to V_{CC}. When V_{CC} reaches a particular threshold, the regulator turns on. The uncharged output capacitor causes maximum inrush current to flow. At this point the device sees the output as a short circuit and the device enters a protective current limiting mode. The output capacitor quickly charges and V_{OUT} rises. Once this voltage rises to just below V_{CC} the inrush current stops flowing and the output rises with the input. V_{OUT} continues to rise with the input until it reaches 3.3V.

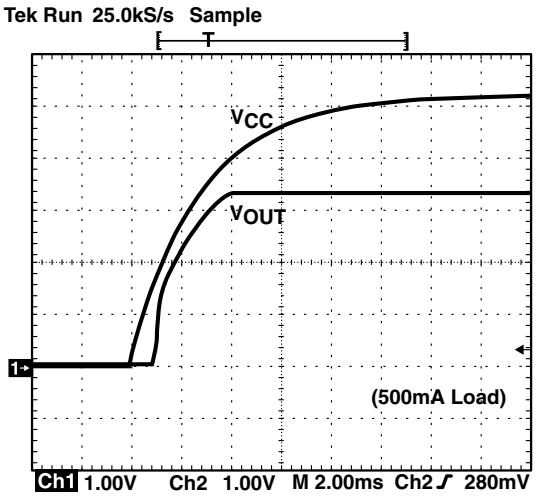


Figure 7. V_{CC} Power-up Cold Start

Typical Transient Characteristics continued

V_{CC} Power down

Figure 8 shows the output response of the regulator during a complete power down situation under full load conditions with $\overline{SD}$ tied to V_{CC}.

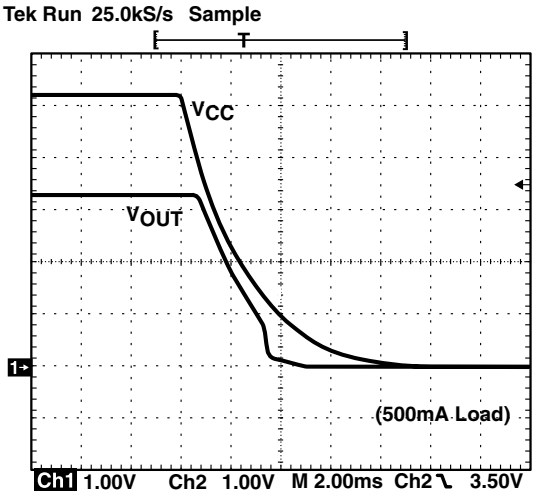


Figure 8. V_{CC} Power Down

Shutdown Transient Response

The transient response of the output voltage to the $\overline{SD}$ pin is shown in Figure 9. The graph shows that a rising edge on the $\overline{SD}$ pin enables the regulator and a falling edge disables the regulator.

The rise and fall time for the output voltages are 100µs and 200µs respectively.

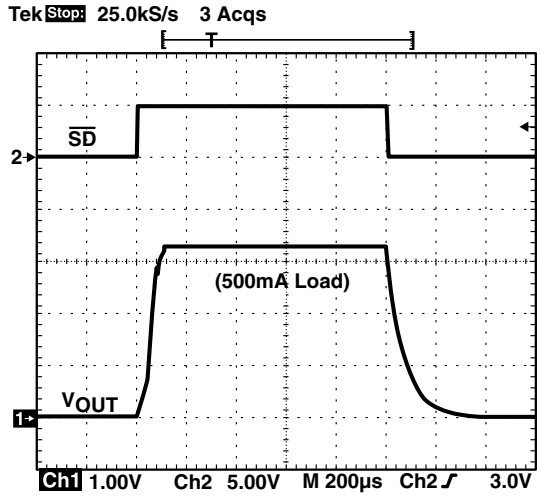


Figure 9. Shutdown Transient Response

$\overline{POR}$ Response

The transient response of the active low POR pin to V_{OUT} is shown in Figure 10. When V_{OUT} rises above the $\overline{POR}$ threshold voltage (typically 2.9V), the pin is forced to logic low (0V). The pin remains at logic low for 30ms then it is forced to logic high (3.3V). If V_{OUT} falls below the $\overline{POR}$ threshold voltage during this 30ms interval $\overline{POR}$ will remain logic low. If it falls below the voltage threshold and then recovers the 30ms time will reset.

When V_{OUT} falls below the $\overline{POR}$ threshold voltage $\overline{POR}$ is immediately forced to logic low.

V_{CC} is tied to ground to show that the $\overline{POR}$ circuitry will work without V_{CC} present.

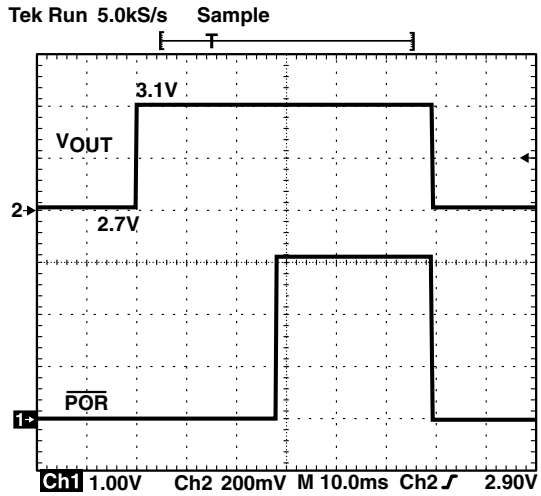


Figure 10. $\overline{POR}$ Response

Typical Transient Characteristics continued

Load Step response

Figure 11 shows the output voltage (Ch1) response of the regulator during a step load change between 5mA and 500mA (represented on Ch2). For the 5mA to 500mA transition an initial transient overshoot of 60mV occurs and then the output settles to its final voltage within 20µs. For the 500mA to 5mA transition there is also an initial overshoot of 60mV however it takes approximately 250µs to settle to its final voltage.

The overall DC voltage disturbance on the output is approximately 25mV, which demonstrates the regulator output impedance of 50mΩ.

V_{OUT} offset = 3.3V

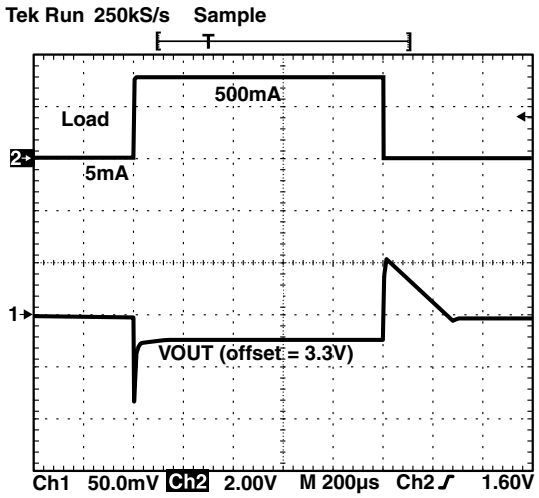


Figure 11. Load Step Response

Line Step Response

Figure 12 shows the output response of the regulator to a V_{CC} line voltage transient between 4.5V and 5.5V (1Vpp as shown on Ch2). The load condition during this test is 5mA. The output response produces less than 10mV of disturbance on both edges indicating a line rejection of better than 40dB at high frequencies.

V_{OUT} offset = 3.3V

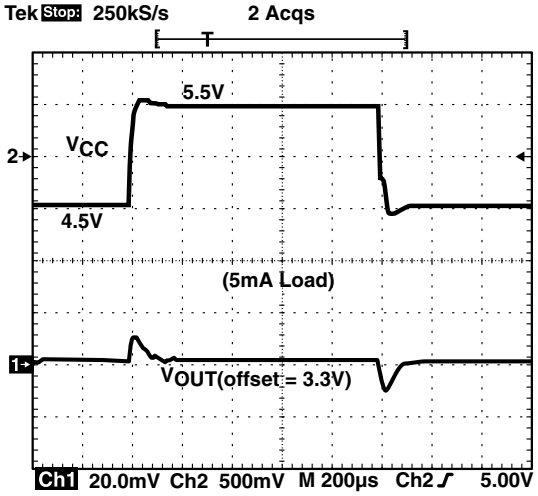


Figure 12. Line Step Response

Reset response time with overdrive

Figure 13 shows the time it takes for the $\overline{POR}$ signal to reset when the output voltage is driven below the $\overline{POR}$ trigger threshold by varying amounts. The amount the voltage is driven below the POR trigger threshold is the overdrive voltage.

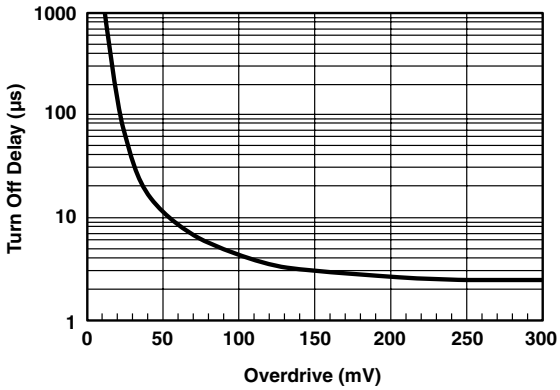


Figure 13. Reset Response Time with Overdrive

Typical Thermal Characteristics

Thermal dissipation of junction heat consists primarily of two paths in series. The first path is the junction to the case (θ_{JC}) thermal resistance which is defined by the package style, and the second path is the case to ambient (θ_{CA}) thermal resistance, which is dependent on board layout.

The overall junction to ambient (θ_{JA}) thermal resistance is equal to:

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

For a given package style and board layout, the operating junction temperature is a function of junction power dissipation P_{JUNC}, and the ambient temperature, resulting in the following thermal equation:

$$T_{JUNC} = T_{AMB} + P_{JUNC}(\theta_{JC}) + P_{JUNC}(\theta_{CA})$$
$$= T_{AMB} + P_{JUNC}(\theta_{JA})$$

The CMPWR160SA is housed in a thermally enhanced package where all the GND pins (5 through 8) are integral to the leadframe (fused leadframe). When the device is mounted on a double sided printed circuit board with two square inches of copper allocated for "heat spreading", the resulting θ_{JA} is 50°C/W.

Based on a maximum power dissipation of 1.0W (2Vx500mA) with an ambient of 70°C the resulting junction temperature will be:

$$T_{JUNC} = T_{AMB} + P_{JUNC}(\theta_{JA})$$
$$= 70°C + 1.0W\ (50°C/W)$$
$$= 70°C + 50°C = 120°C$$

All thermal characteristics of the CMPWR160SA were measured using a double sided board with two square inches of copper area connected to the GND pins for "heat spreading".

Measurements showing performance up to junction temperature of 125°C were performed under light load conditions (5mA). This allows the ambient temperature to be representative of the internal junction temperature.

Note: The use of multi-layer board construction with power planes will further enhance the thermal performance of the package. In the event of no copper area being dedicated for heat spreading, a multi-layer board construction, using only the minimum size pad layout, will typically provide the CMPWR160SA with an overall θ_{JA} of 70°C/W which allows up to 780mW to be safely dissipated.

Output Voltage vs. Temperature

Figure 14 shows the regulator V_{OUT} performance up to the maximum rated junction temperature. A 125°C variation in junction temperature from –25°C causes an output voltage variation of about 50mV, reflecting a voltage temperature coefficient of approximately ±50ppm/°C.

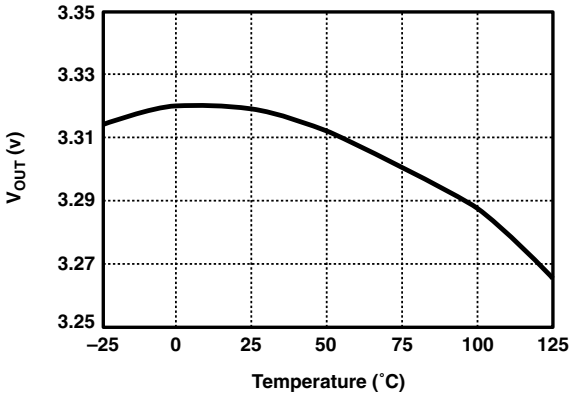


Figure 14. V_{OUT} Temperature Variation (5mA)

Typical Thermal Characteristics continued

Output Voltage (Rated) vs. Temperature

Figure 15 shows the regulator steady state performance when fully loaded (500mA) from –25°C up to the rated maximum temperature of 70°C. The output variation at maximum load is approximately 20mV across the shown operating temperature. This translates to a temperature coefficient of approximately ±30ppm/°C.

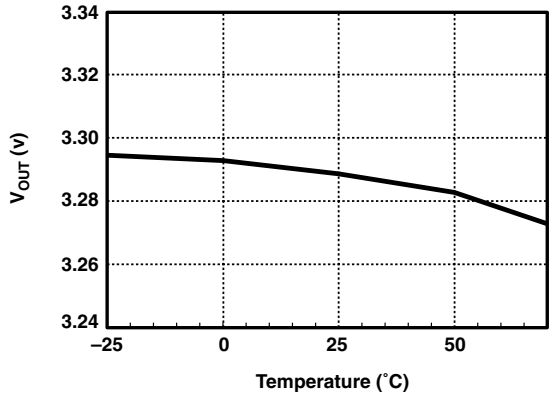


Figure 15. V_{OUT} Temperature Variation (500mA)

$\overline{POR}$ Voltage Threshold Temperature Variation

Figure 16 shows the $\overline{POR}$ threshold voltage variation from –25°C up to the maximum rated junction temperature. The overall 150°C change in junction temperature causes less than a 5mV variation in the $\overline{POR}$ threshold voltage. This translates to a temperature coefficient of ±6ppm/°C.

The POR pulse duration does not vary with temperature.

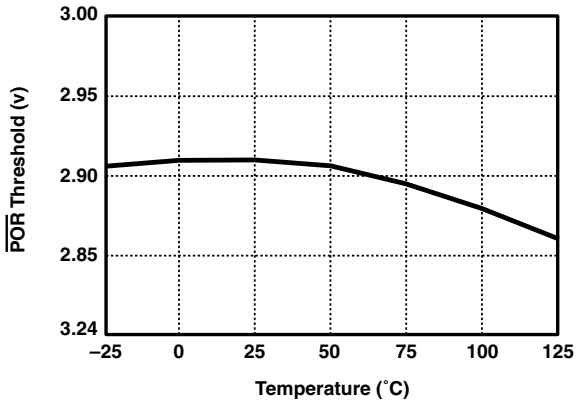


Figure 16. $\overline{POR}$ Threshold Temperature Variation

V_{CC} Supply Current Temperature Variation

Figure 17 shows the V_{CC} supply current variation with temperature from –25°C to the maximum rated junction temperature with no load on the device. The supply current changes less than 1µA over the entire 150°C range shown in the plot.

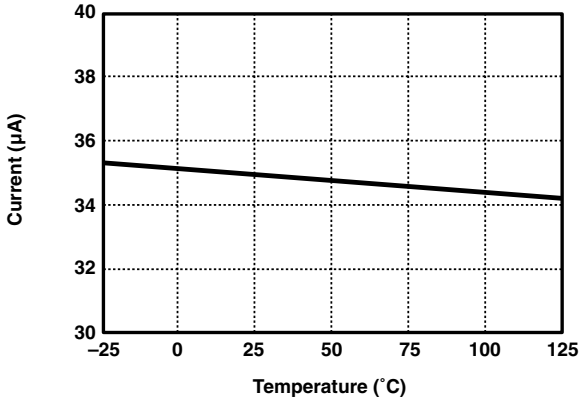


Figure 17. V_{CC} Supply Current vs. Temperature