GENERAL DESCRIPTION

The CM8500 is a switching regulator designed to provide a desired output voltage or termination voltage for various applications by converting voltage supplies ranging from 2.0V to 4.0V. The CM8500 can be implemented to produce regulated output voltages in two different modes. In the default mode, when the VIN/2 pin is open, the output voltage is 50% of the VCCQ. The CM8500 can also be used to produce various user-defined voltages by forcing a voltage on the VIN/2 pin. In this case, the output voltage follows the VIN/2 pin input voltage. The switching regulator is capable of sourcing or sinking up to 3A of current while regulating an output V_{TT} voltage to within 3% or less.

The CM8500, used in conjunction with series termination resistors, provides an excellent voltage source for active termination schemes of high speed transmission lines as those seen in high speed memory buses and distributed backplane designs.

The voltage output of the regulator can be used as a termination voltage for other bus interface standards such as SSTL, CMOS, Rambus ™ ,GTL+, VME, LV-CMOS, LV-TTL, and PECL.

FEATURES

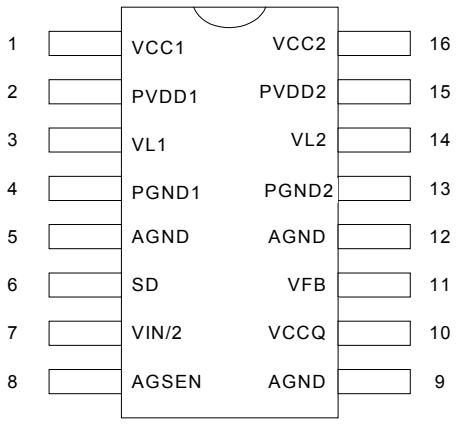
- Patent Filed #6,452,366
- 16 pin PTSSOP and PSOP package
- Source and sink up to 3A, no heat sink required
- Peak Current to 6A
- Integrated Power MOSFETs
- Output voltage can be programmed by external resistors
- Separate voltages for VCCQ and PVDD
- V OUT of ±3% or less at 3A
- Minimum external components
- Shutdown for standby or suspend mode operation
- Thermal shutdown protection
- Soft start

APPLICATIONS

- Mother Board
- PCI / AGP Graphics
- Game / Play Station
- Set Top Box
- IPC
- SCSI-III Bus terminator
- Buck Converter

PIN CONFIGURATION

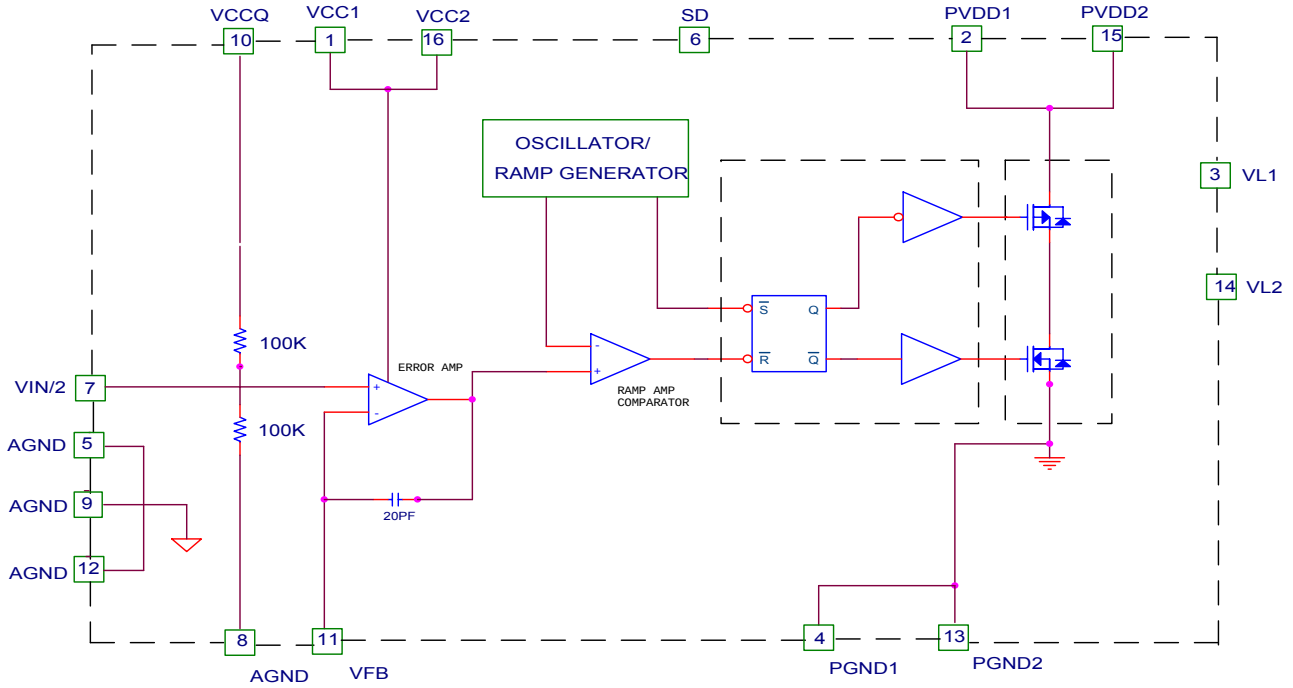
PSOP-16 (PS16)/PTSSOP-16 (PT16)
Top View



PIN DESCRIPTION

Pin No.	Symbol	Description	Operating Rating			
			Min.	Typ.	Max.	Unit
1,16	VCC1,VCC2	Voltage supply for internal circuits	2	2.5	4	V
2,15	PVDD1,PVDD2	Voltage supply for output power transistors	2	2.5	4	V
3,14	VL1,VL2	Output voltage/inductor connection (IDD1+IDD2, Output RMS current)	-3		3	A
4,13	PGND1,PGND2	Ground for output power transistors				
5,9,12	AGND	Ground for internal reference voltage divider				
8	AGSEN	Ground for remote sensing				
6	SD	Shutdown active high. CMOS input level	0.75 X VCC		VCC + 0.3V	V
7	VIN/2	Input for external reference voltage		VCCQ/2		V
10	VCCQ	Voltage reference for external voltage divider		2.5		V
11	VFB	Feedback node for the V_{TT}		VCCQ/2		V

BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Temperature Range	Package
CM8500IT	-40℃ to 85℃	16-Pin PTSSOP (PT16)
CM8500IS	-40℃ to 85℃	16-Pin PSOP (PS16)
CM8500GIT*	-40℃ to 85℃	16-Pin PTSSOP (PT16)
CM8500GIS*	-40℃ to 85℃	16-Pin PSOP (PS16)
CM8500TEVAL		Evaluation Board (T16)

*Note: G : Suffix for Pb Free Product

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged.

PVDD/VCC/VCCQ .....-0.3V to 4.0V
Voltage on Any Other Pin …….. GND – 0.3V to VCC + 0.3V
Output RMS Current, Source or Sink .....……..…….....3.0A

Junction Temperature ...…… ……150°C
Storage Temperature ……..…….. -65°C to 125°C
Lead Temperature (Soldering, 10 sec)…….. 300°C
Thermal Resistance (θ_{JA})….. …….. .40°C/W

OPERATING CONDITIONS

Temperature Range ..... -40°C to 85°C
P_{VDD} Operating Range .....2.0V to 4.0V

ELECTRICAL CHARACTERISTICS **(Unless otherwise stated, these specifications apply T_A=25°C; VCC=+3.3V and PVDD=+3.3V)** maximum ratings are stress ratings only and functional device operation is not implied. (Note 1)

Symbol	Parameter	Test Conditions		CM8500 Min.	CM8500 Typ.	CM8500 Max.	Unit
SWITCHING REGULATOR							
VL	Output Voltage, SSTL_2	IOUT = 0, V_{IN}/2 = open Note 2	VCCQ = 2.3V	1.12	1.15	1.18	V
			VCCQ = 2.5V	1.22	1.25	1.28	V
			VCCQ = 2.7V	1.32	1.35	1.38	V
		IOUT = ±3A, V_{IN}/2 = open Note 3	VCCQ = 2.3V	1.09	1.15	1.21	V
			VCCQ = 2.5V	1.19	1.25	1.31	V
			VCCQ = 2.7V	1.28	1.35	1.42	V
V_{IN}/2	Internal Resistor Divider	IOUT = 0 Note 2	VCCQ = 2.3V	1.139	1.15	1.162	V
			VCCQ = 2.5V	1.238	1.25	1.263	V
			VCCQ = 2.7V	1.337	1.35	1.364	V
Z_{IN}	V_{IN}/2 Reference Pin Input Impedance	Note 2	VCCQ = 0		50		KΩ
fsw	Switching Frequency	CM8500		510	600	690	KHz
$I_{OUT(RMS)}$	Maximum Output RMS Current	CM8500				3	A
$I_{OUT(PEAK)}$	Maximum Output Peak Current	CM8500				6	A
MOSFETs							
$RDS_{(ON)}$	Drain to Source on-State Resistance	PVDD=5V			150	180	mΩ
SUPPLY							
I_{VCCA}	Quiescent Current	VFB = 1.4V LC unconnected			200		μA
I_{PVDD}		VFB = 1.4V LC unconnected			500		μA

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions

Note 2: VCC, PVDD = 3.3V ±10%

Note 3: It's not 100% test

FUNCTIONAL DESCRIPTION

The CM8500 is a switching regulator that is capable of sinking and sourcing 3A of current without an external heat sink. CM8500 uses a standard surface mount PTSSOP and PSOP package with bottom metal exposed and the heat can be piped through the bottom of the device and onto the PCB.

The CM8500 integrates power MOSFETs that are capable of source and sink 3A of current while maintaining excellent voltage regulation. The output voltage can be regulated within 3% or less by using the external feedback. Separate voltage supply inputs have been added to fit applications with various power supplies for the databus and power buses.

OUPUTS

The output voltage pins (VL1, VL2) are tied to the databus, address, or clock lines via an external inductor. Output voltage is determined by the VCCQ or VIN/2 inputs.

INPUTS

The input voltage pins (VCCQ or VIN/2) determine the output voltages (VL1 or VL2). In the default mode, when the VIN/2 pin is open, the output voltage is 50% of the VCCQ input.
If a specific voltage is forced at the VIN/2 pin, the output voltage follows the voltage at the VIN/2 pin. VCCQ suggested connecting to VCCQ of memory module for better tracking with memory VCCQ.

OTHER SUPPLY VOLTAGES

Several inputs are provided for the supply voltages: PVDD1, PVDD2, VCC1, and VCC2.

The PVDD1 and PVDD2 provide the power supply to the power MOSFETs. VCC1 and VCC2 provide the voltage supply to the logic section and internal error amplifiers.

FEEDBACK

The VFB pin is an input that can be used for closed loop compensation. This input is derived from the voltage output. AGSEN pin is a contact node of internal resistor divider for remote sense.

APPLICATIONS

USING THE CM8500 FOR SSTL BUS TERMINATION

Figure 1 is the typical schematic of the CM8500TEVAL that shows the recommended approach for bus terminating solutions for SSTL-2 bus. This circuit can be used in PC memory and Graphics memory applications as shown in Figure 2 and Figure 3.
Figure 4 shows the PCB layout of the CM8500TEVAL.
Table 1details the key parameters of SSTL_2 specification.
Figure 5 shows two different approach of SSTL_2 Terminated Output. (Refer to page 8 for detail description.)

APPLICATION CIRCUIT

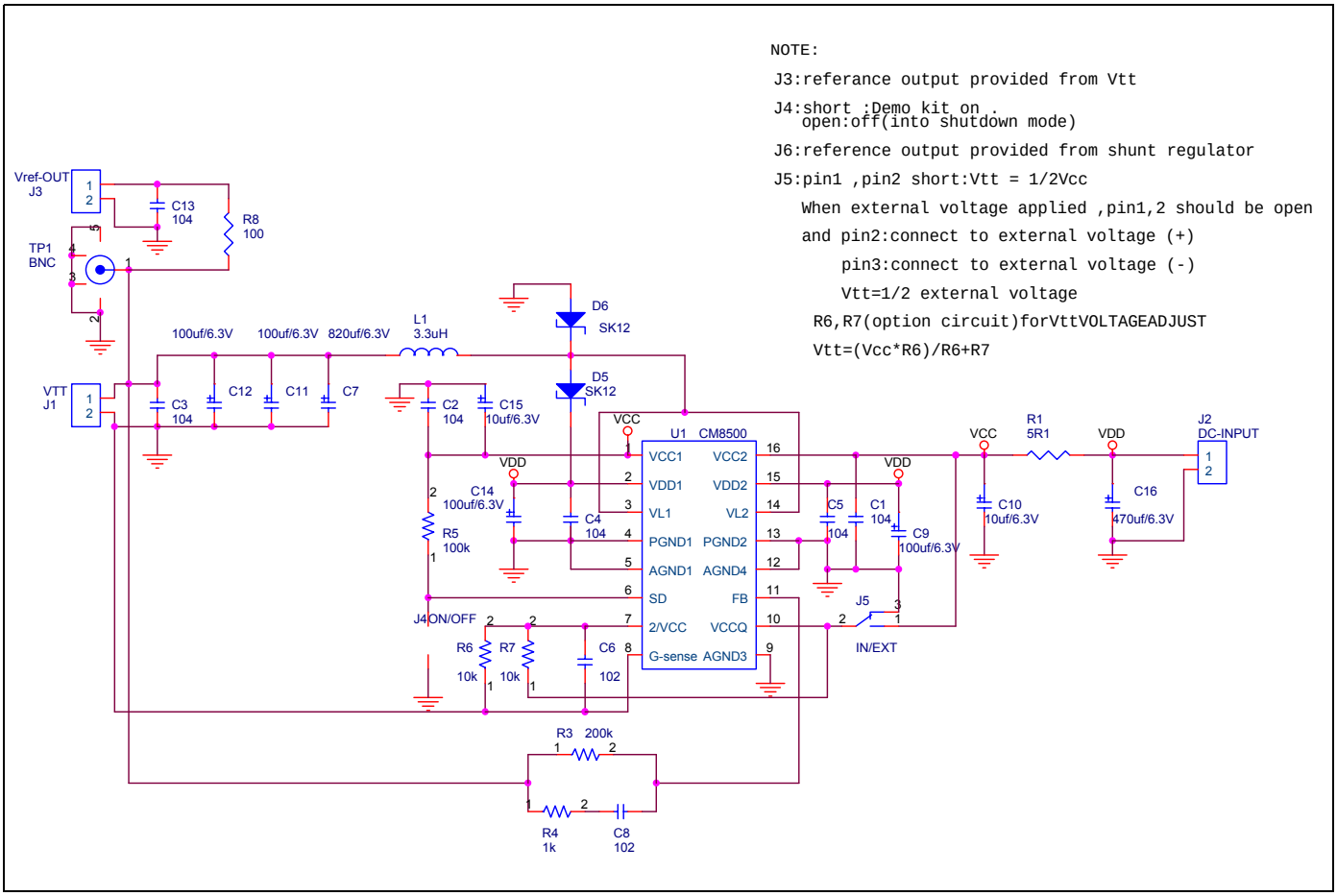


Figure 1. CM8500 Typical Application
(Schematic of CM8500TEVAL)

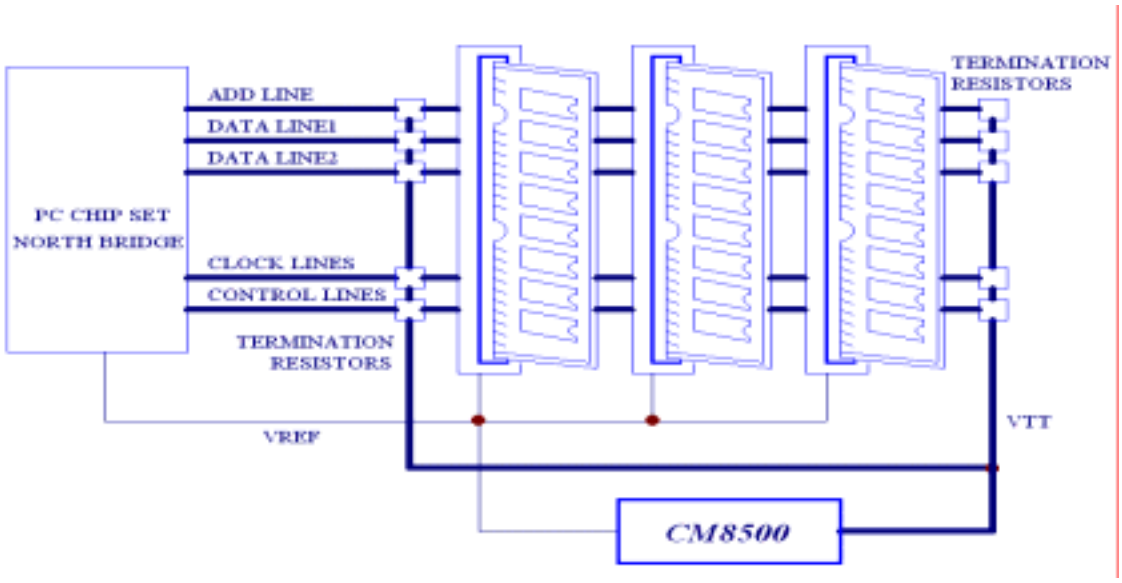


Figure 2. Termination Solution for PC Main Memory (Mother Boards)

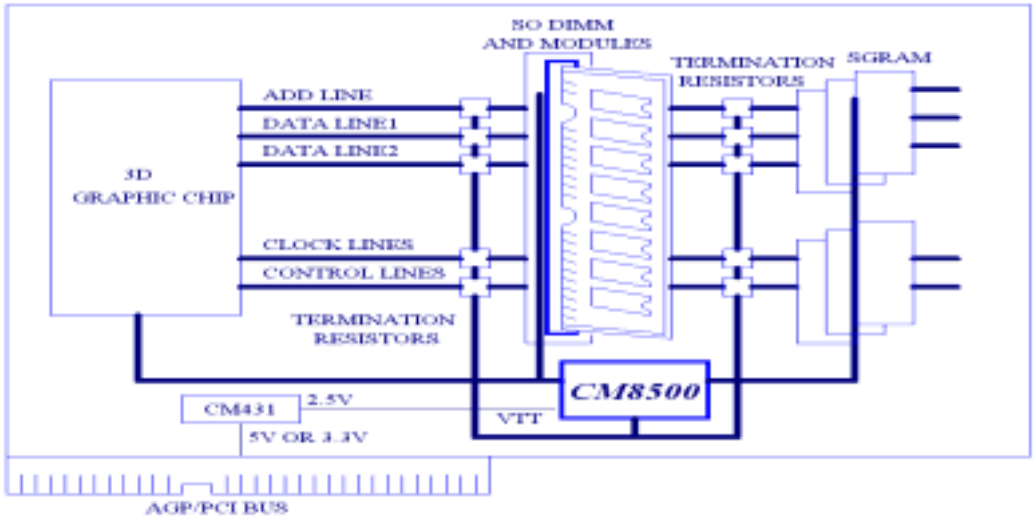


Figure 3. Termination Solution for Graphic Memory (AGP Graphics)

CM8500TEVAL PART LIST

Item	Q'ty	Description	Designator	Manufacturer
	Resistors			
1	1	0805, 5Ω, 1/8W	R1	
2	1	0805, 100Ω, 1/8W	R8	
3	1	0805, 470Ω, 1/8W	R9 (option)	
4	1	0805, 1KΩ, 1/8W	R4	
5	2	0805, 100KΩ, 1/8W	R3, R5	
	Capacitors			
6	1	0805, 1nF/ 16V (102)	C6, C8	
7	6	0805, 0.1µF/ 16V (104)	C1, C2, C3, C4, C5	
8	1	0805, 1µF/ 16V (105)	C13	
9	1	CE 10φ, 820uF/ 6.3V	C7	Sanyo OSCON
10	2	B Size, Tant 10uF/ 6.3V	C10, C15	
11	4	D Size, Tant 100uF/ 6.3V	C9, C11, C12, C14	
	Magnetics			
12	1	3.3uH 5A Inductor	L1	Bipolar Electronic Corp.
	IC's			
13	1	CM8500IT	U1	Champion Microelectronic Corp.
14	1	CM431L	U2 (option)	Champion Microelectronic Corp.
	Connectors			
15	1	2-pin, 2.54mm	J2	
16	4	2-pin Jumper, 2.54mm	J1, J3, J4, J6 (option)	
17	1	3-pin Jumper, 2.54mm	J5	
	PCBs			
18	1	CM8500TEVAL PCB		Champion Microelectronic Corp.

Vendor Information

Bipolar Electronic Corp. Phn: +886-3-360 8892
Sanyo

CM8500TEVAL PCB LAYOUT

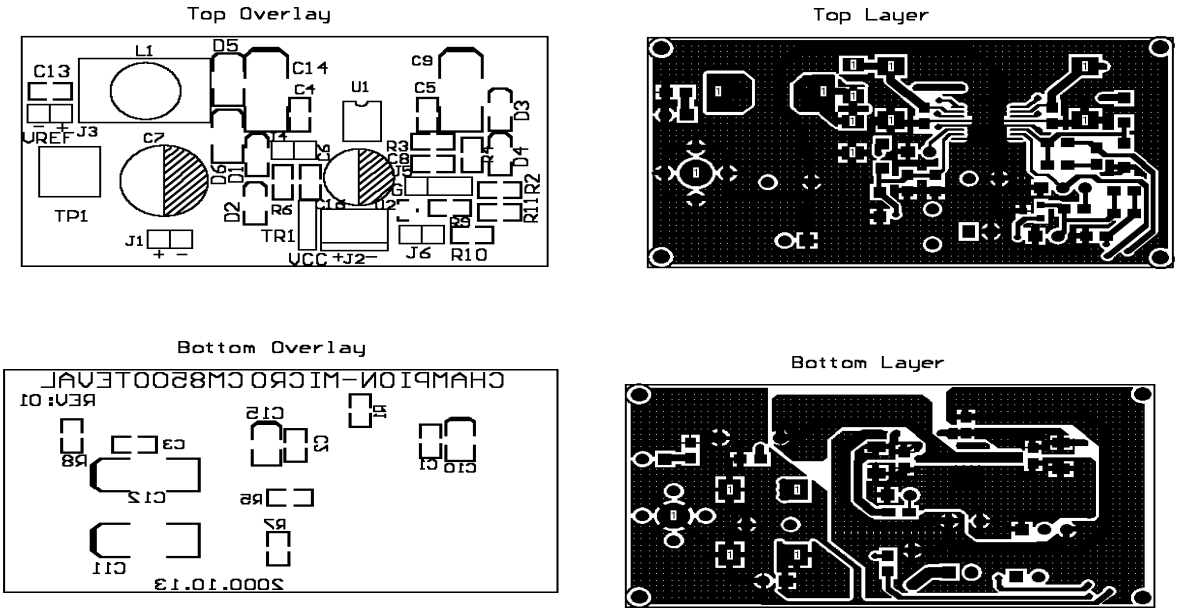


Figure 4. CM8500EVAL PCB Layout

SSTL-2 SPECIFICATIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{DD}	Device Supply Voltage	V_{DDQ}		N/A	V
V_{DDQ}	Output Supply Voltage	2.3	2.5	2.7	V
V_{REF}	Input Reference Voltage	1.15	1.25	1.35	V
V_{TT}	Termination Voltage	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V
INPUT DC LOGIC LEVELS					
V_{IH} (DC)	DC Input Logic High	V_{REF} + 0.18		V_{DDQ} + 0.3	V
V_{IL} (DC)	DC Input Logic Low	- 0.3		V_{REF} - 0.18	V
INPUT AC LOGIC LEVELS					
V_{IH} (AC)	AC Input Logic High	V_{REF} + 0.35			V
V_{IL} (AC)	AC Input Logic Low			V_{REF} - 0.35	V
OUTPUT DC CURRENT DRIVE					
I_{OH} (DC)	Output Minimum Source DC Current	- 15.2			mA
I_{OL} (DC)	Output Minimum Sink DC Current	15.2			mA

Notes: V_{REF} and V_{TT} must track variations in V_{DDQ}
Peak-to-peak AC noise on V_{REF} may not exceed ±2% V_{REF} (DC)
V_{TT} of transmitting device must track V_{REF} of receiving device

Table 1. Key Specifications for SSTL_2

SSTL_2 TERMINATED OUTPUT



Single Terminated Output

Double Terminated Output

Figure 5. SSTL_2 Terminated Output

Note.

The SSTL_2 specification requires adequate output current drive so that parallel termination schemes can be used. The use of parallel termination is important for high-speed signaling, since it allows proper termination of the bus transmission lines, which reduces signal reflections. The result will be improved settling, lower EMI emissions, and higher possible clock rates. A minimum termination resistance of 23Ω to V_{TT} can be used and still comply with the minimum output voltages and output currents of the SSTL_2 specification.

Two choices for implementing the parallel termination are shown in Figure 5.

Double Terminated Output

The bus is terminated at both ends with a 50Ω resistor, for a combined parallel resistance of 25Ω.

Single Terminated Output

The bus is terminated at the far end from the controller with a single 25Ω resistor.

It is strongly recommended that the single resistor termination scheme be used for best performance. The benefits of this approach include reduced cost, simpler signal routing, reduced reflections, and better signal bandwidth and settling.

CM8500EVAL TESTING DIAGRAM

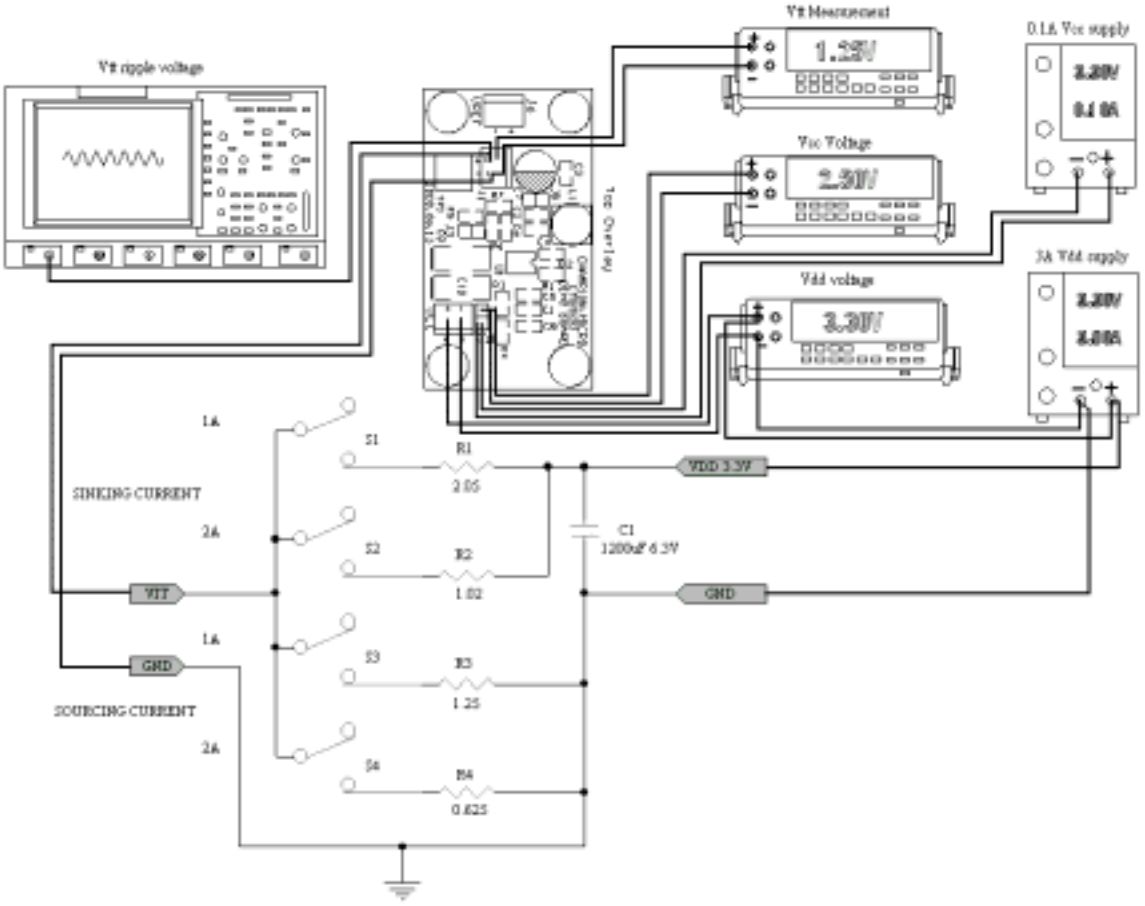
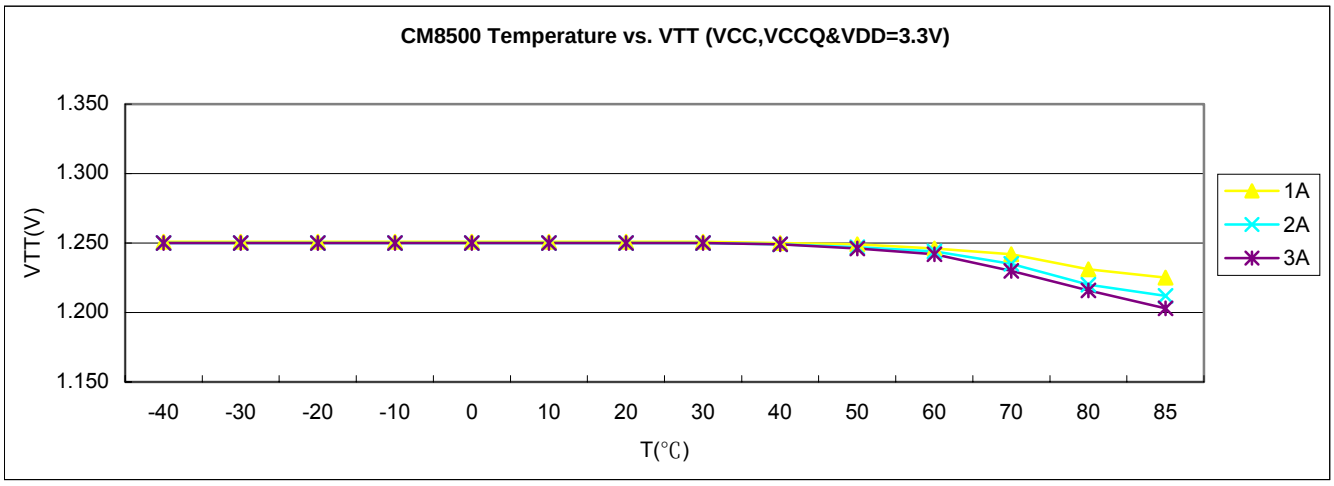
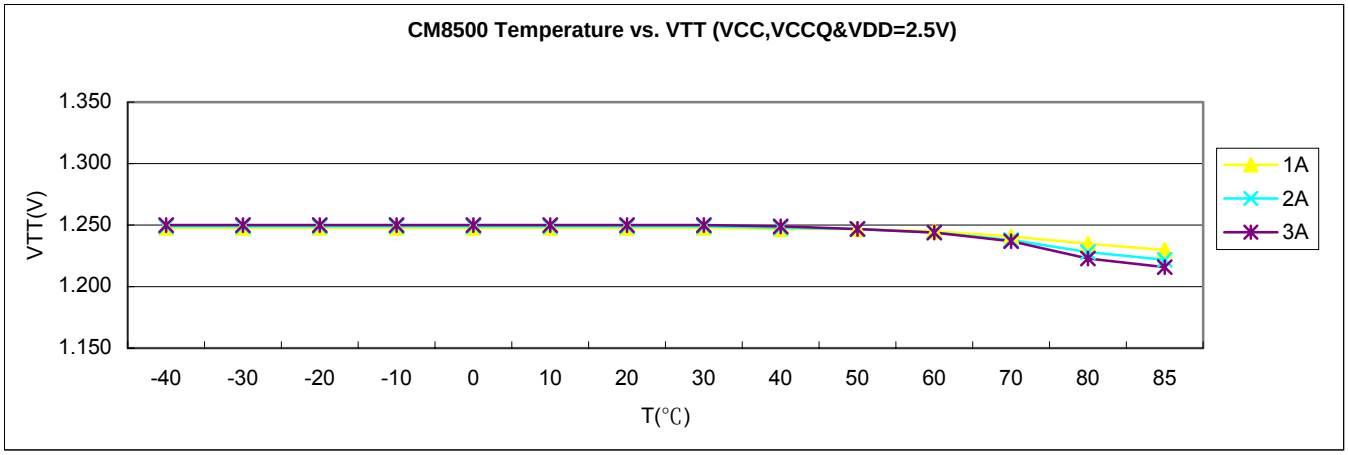


Figure 6. CM8500EVAL Typical Testing Diagram

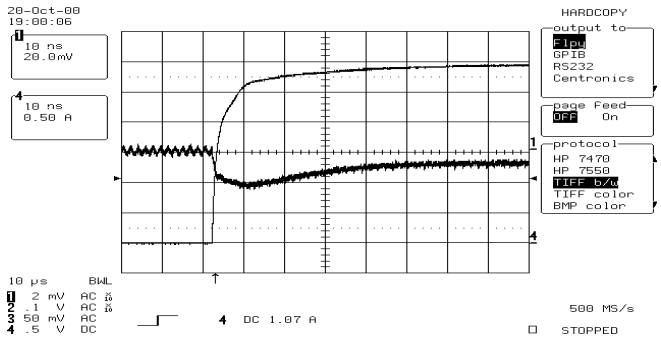
TYPICAL CHARACTERISTICS



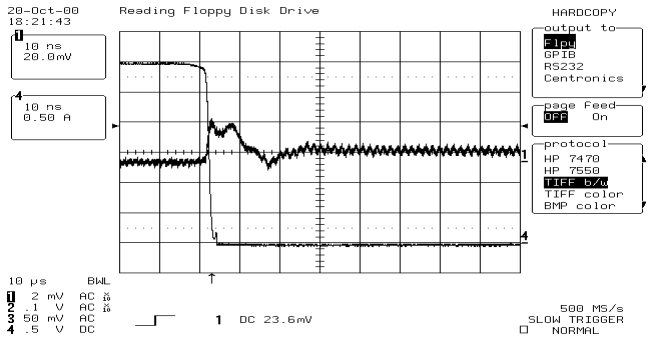
Temperature vs. VTT VCC, VCCQ & VDD=3.3V



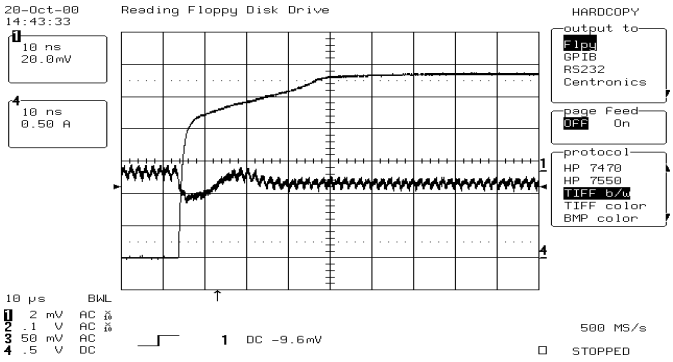
Temperature vs. VTT VCC, VCCQ & VDD=2.5V



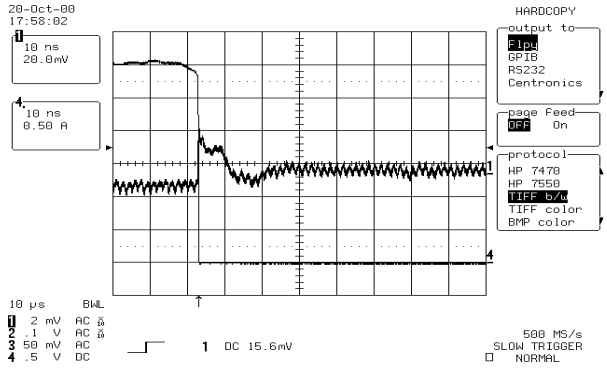
2V INPUT LOAD: 0A - 3A



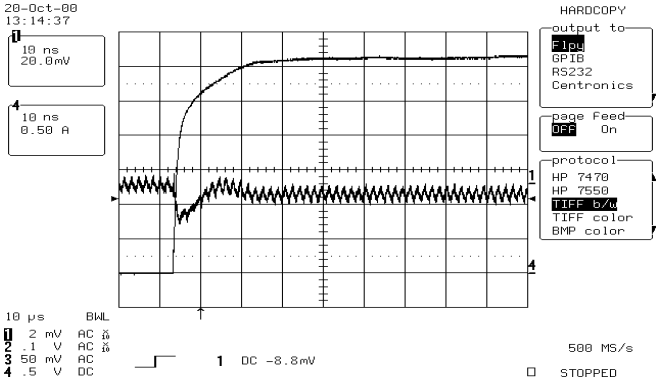
2V INPUT LOAD: 3A - 0A



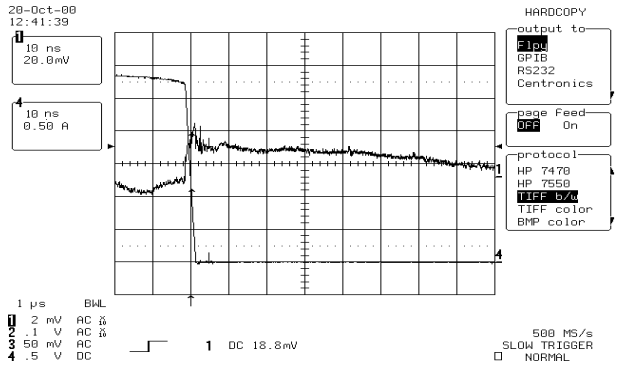
2.5V INPUT LOAD: 0A - 3A



2.5V INPUT LOAD: 3A - 0A



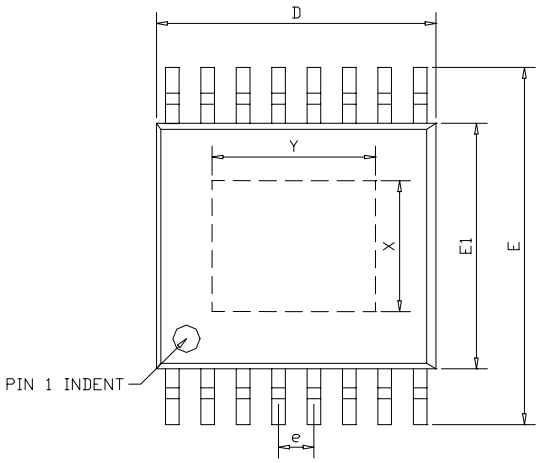
3.3V INPUT LOAD: 0A - 3A



3.3V INPUT LOAD: 3A - 0A

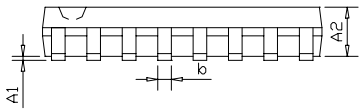
PACKAGE DIMENSION

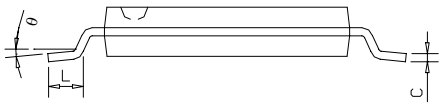
16-PIN PTSSOP (PT16)



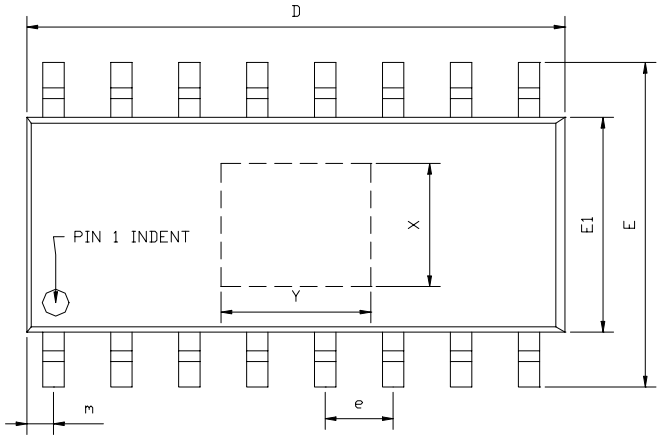
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX	MIN	NOM	MAX
A1	0.05	---	0.15	0.002	---	0.006
A2	0.84	---	0.94	0.033	---	0.037
b	0.20	---	0.30	0.008	---	0.012
C	0.10	---	0.20	0.004	---	0.008
D	4.88	---	5.13	0.192	---	0.202
E	6.25	---	6.55	0.246	---	0.258
E1	4.29	---	4.50	0.169	---	0.177
e	---	0.65	---	---	0.026	---
L	0.51	---	0.71	0.020	---	0.028
θ	0°	---	8°	0°	---	8°

EXPOSED PAD DIMENSION : (mm)
PAD SIZE: X=2.4; Y=3.0



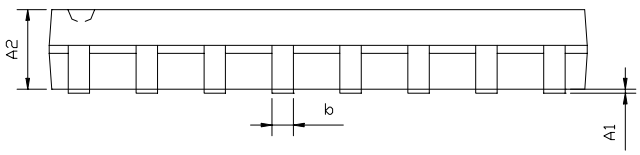


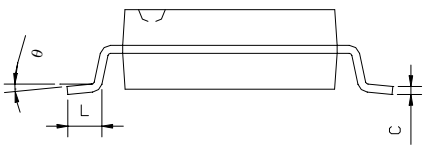
16-PIN PSOP (PS16)



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX	MIN	NOM	MAX
A1	0.05	---	0.15	0.002	---	0.006
A2	1.40	---	1.55	0.055	---	0.061
b	0.30	---	0.51	0.012	---	0.020
C	0.15	---	0.26	0.006	---	0.010
D	9.80	---	10.06	0.386	---	0.396
E	5.79	---	6.20	0.228	---	0.244
E1	3.76	---	4.01	0.148	---	0.158
e	---	1.27	---	---	0.050	---
L	0.38	---	0.69	0.015	---	0.035
m	0.43	---	0.69	0.017	---	0.027
θ	0°	---	8°	0°	---	8°

EXPOSED PAD DIMENSION : (mm)
PAD SIZE: X=2.3 ; Y=2.8





IMPORTANT NOTICE

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A few applications using integrated circuit products may involve potential risks of death, personal injury, or severe property or environmental damage. CMC integrated circuit products are not designed, intended, authorized, or warranted to be suitable for use in life-support applications, devices or systems or other critical applications. Use of CMC products in such applications is understood to be fully at the risk of the customer. In order to minimize risks associated with the customer's applications, the customer should provide adequate design and operating safeguards.

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