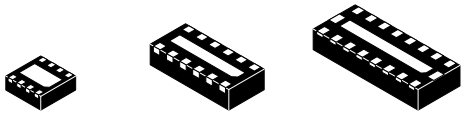
CM1460

Praetorian® C-L-C LCD and Camera EMI Filter Array with ESD Protection

ON Semiconductor®

http://onsemi.com



WDFN8
DE SUFFIX
CASE 511BE

WDFN12
DE SUFFIX
CASE 511AZ

WDFN16
DE SUFFIX
CASE 511AU

Product Description

The CM1460 is a family of pi−style EMI filter arrays with ESD protection, which integrates four, six and eight filters (C−L−C) in small form factor WDFN 0.50 mm pitch packages. Each EMI filter channel of the CM1460 is implemented as a 3−pole L−C filter where the component values are 15 pF − 17 nH − 15 pF. The CM1460's roll−off frequency at −6 dB attenuation is 350 MHz and can be used in applications where the data rates are as high as 140 Mbps while providing greater than 30 dB over the 800 MHz to 2.7 GHz frequency range.

The parts include ESD diodes on every pin, which provide a very high level of protection for sensitive electronic components that may be subjected to electrostatic discharge (ESD). The ESD protection diodes connected to the filter ports are designed and characterized to safely dissipate ESD strikes of ±15 kV, beyond the maximum requirement of the IEC61000−4−2 international standard. Using the MIL−STD−883 (Method 3015) specification for Human Body Model (HBM) ESD, the pins are protected for contact discharges at greater than ±30 kV.

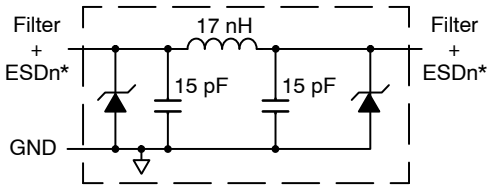
This device is particularly well suited for wireless handsets, mobile LCD modules and PDAs because of its small package format and easy−to−use pin assignments. In particular, the CM1460 is ideal for EMI filtering and protecting data and control lines for the LCD display and camera interface in mobile handsets.

The CM1460 is housed in space saving, low profile, 0.50 mm pitch WDFN packages and is available in lead−free format.

Features

- Four, Six and Eight Channels of EMI Filtering with Integrated ESD Protection
- Pi−Style EMI Filters in a Capacitor−Inductor−Capacitor (C−L−C) Network
- ±15 kV ESD Protection on Each Channel (IEC 61000−4−2 Level 4, Contact Discharge)
- ±30 kV ESD Protection on Each Channel (HBM)
- Greater than −35 dB Attenuation (Typical) at 1 GHz
- WDFN Lead−Free Package with 0.50 mm Lead Pitch:
  - 4−ch. = 8−lead WDFN
  - 6−ch. = 12−lead WDFN
  - 8−ch. = 16−lead WDFN
- Tiny WDFN Package Size:
  - 8−lead: 2.00 mm x 2.00 mm
  - 12−lead: 3.00 mm x 1.35 mm
  - 16−lead: 4.00 mm x 1.60 mm
- Increased Robustness against Vertical Impacts During Manufacturing Process
- These Devices are Pb−Free and are RoHS Compliant

ELECTRICAL SCHEMATIC



1 of 4, 6 or 8 EMI/RFI Filter Channels with Integrated ESD Protection

* See Package/Pinout Diagrams for expanded pin information.

MARKING DIAGRAM



XE = CM1460−04DE
N60E = CM1460−06DE
N608E = CM1460−08DE

ORDERING INFORMATION

Device	Package	Shipping†
CM1460−04DE	WDFN−8 (Pb−Free)	3000/Tape & Reel
CM1460−06DE	WDFN−12 (Pb−Free)	3000/Tape & Reel
CM1460−08DE	WDFN−16 EEP (Pb−Free)	3000/Tape & Reel

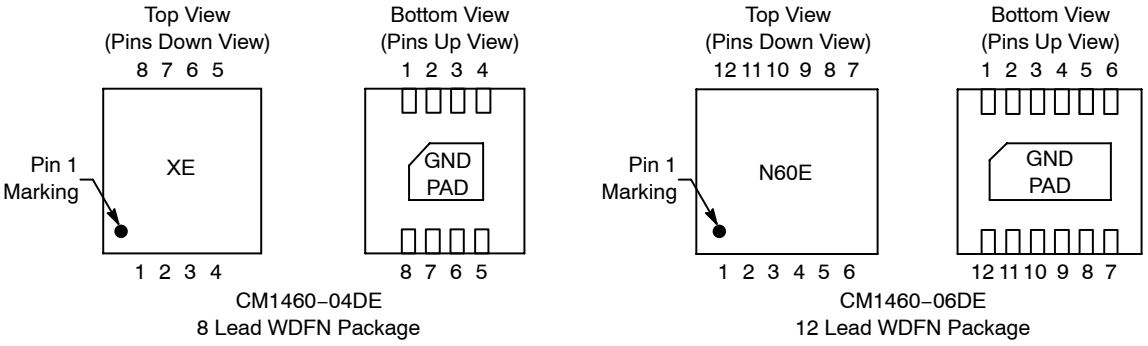
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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Applications

- LCD and Camera Data Lines in Mobile Handsets
- I/O Port Protection for Mobile Handsets, Notebook Computers, PDAs, etc.
- EMI Filtering for Data Ports in Cell Phones, PDAs or Notebook Computers
- Wireless Handsets
- Handheld PCs/PDAs
- LCD and Camera Modules

PACKAGE / PINOUT DIAGRAMS



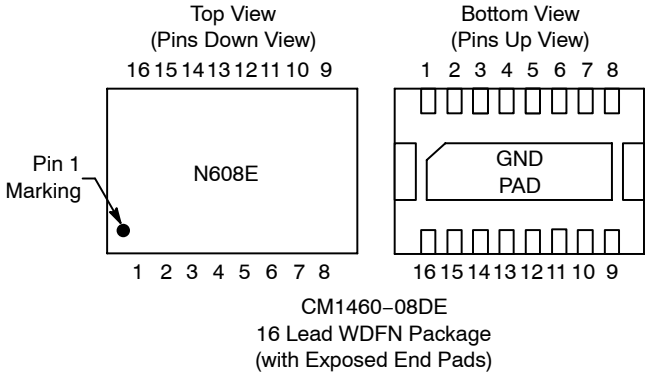


Table 1. PIN DESCRIPTIONS

Device Pin(s)			Name	Description	Device Pin(s)			Name	Description
−04	−06	−08			−04	−06	−08		
1	1	1	FILTER1	Filter + ESD Channel 1	8	12	16	FILTER1	Filter + ESD Channel 1
2	2	2	FILTER2	Filter + ESD Channel 2	7	11	15	FILTER2	Filter + ESD Channel 2
3	3	3	FILTER3	Filter + ESD Channel 3	6	10	14	FILTER3	Filter + ESD Channel 3
4	4	4	FILTER4	Filter + ESD Channel 4	5	9	13	FILTER4	Filter + ESD Channel 4
−	5	5	FILTER5	Filter + ESD Channel 5	−	8	12	FILTER5	Filter + ESD Channel 5
−	6	6	FILTER6	Filter + ESD Channel 6	−	7	11	FILTER6	Filter + ESD Channel 6
−	−	7	FILTER7	Filter + ESD Channel 7	−	−	10	FILTER7	Filter + ESD Channel 7
−	−	8	FILTER8	Filter + ESD Channel 8	−	−	9	FILTER8	Filter + ESD Channel 8
GND PAD			GND	Device Ground	−	−	−	−	

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Storage Temperature Range	−65 to +150	°C
Current per Inductor	30	mA
DC Package Power Rating	500	mW

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. STANDARD OPERATING CONDITIONS

Parameter	Rating	Units
Operating Temperature Range	−40 to +85	°C

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
L	Channel Inductance			17		nH
C_{TOTAL}	Total Channel Capacitance	At 2.5 V DC Reverse Bias, 1 MHz, 30 mV AC	24	30	36	pF
C	Capacitance C1	At 2.5 V DC Reverse Bias, 1 MHz, 30 mV AC		15		pF
V_{DIODE}	Stand−off Voltage	I_{DIODE} = 10 μA		6.0		V
I_{LEAK}	Diode Leakage Current (Reverse Bias)	V_{DIODE} = 3.3 V		0.1	1.0	μA
V_{SIG}	Signal Clamp Voltage Positive Clamp Negative Clamp	 I_{LOAD} = 10 mA I_{LOAD} = −10 mA	 5.6 −1.5	 6.8 −0.8	 9.0 −0.4	V
V_{ESD}	In−system ESD Withstand Voltage a) Human Body Model, MIL−STD−883, Method 3015 b) Contact Discharge per IEC 61000−4−2 Level 4	(Notes 2 and 3)	 ±30 ±15			kV
R_{DYN}	Dynamic Resistance Positive Negative			 2.3 0.9		Ω
f_R	Roll−off Frequency at −6 dB Attenuation Z_{SOURCE} = 50 Ω, Z_{LOAD} = 50 Ω			 350		MHz

1. T_A = 25°C unless otherwise specified.
2. ESD applied to input and output pins with respect to GND, one at a time.
3. Clamping voltage is measured at the opposite side of the EMI filter to the ESD pin (i.e. if ESD is applied to pin A1 then clamping voltage is measured at pin C1). Unused pins are left open.

PERFORMANCE INFORMATION

Typical Filter Performance (T_A = 25°C, DC Bias = 0 V, 50 Ω Environment)

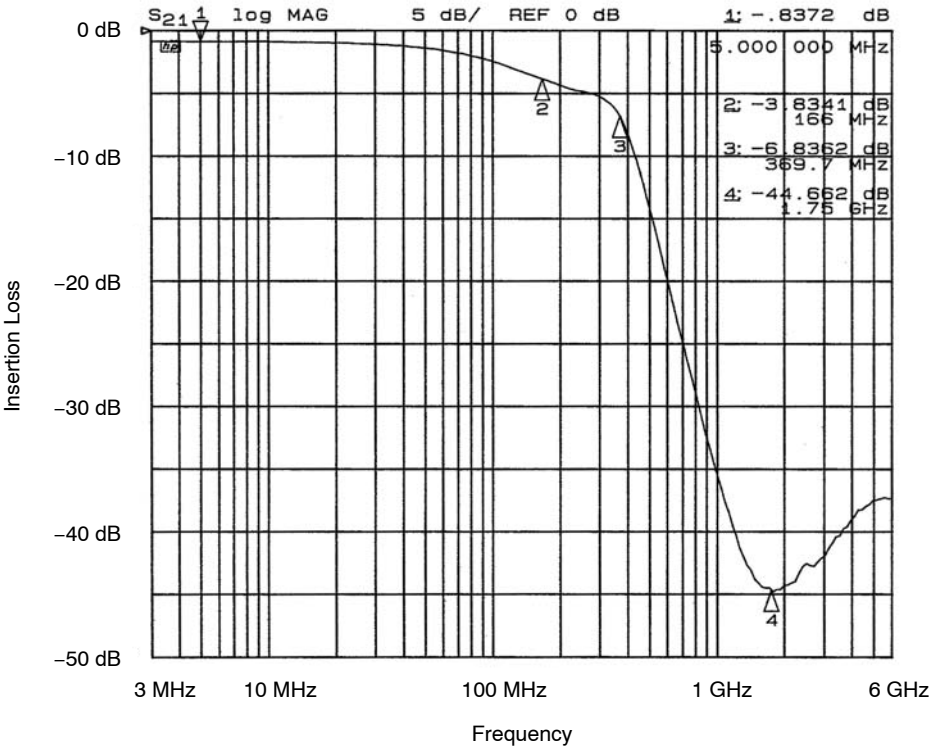


Figure 1. Filter 1 Insertion Loss (CM1460−04DE)

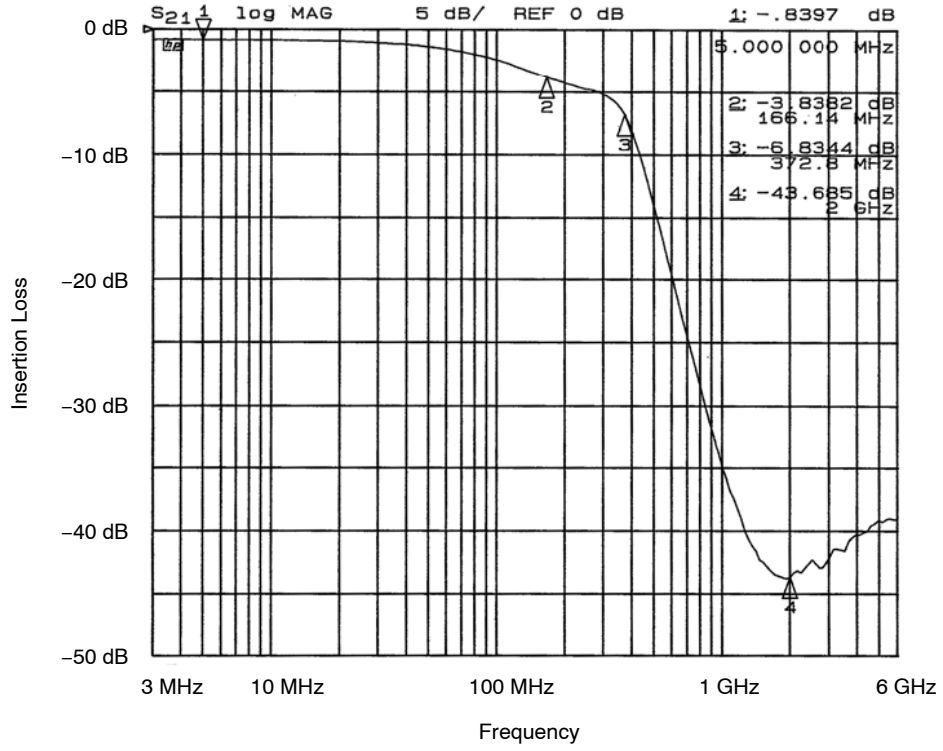


Figure 2. Filter 2 Insertion Loss (CM1460−04DE)

PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance (T_A = 25°C, DC Bias = 0 V, 50 Ω Environment)

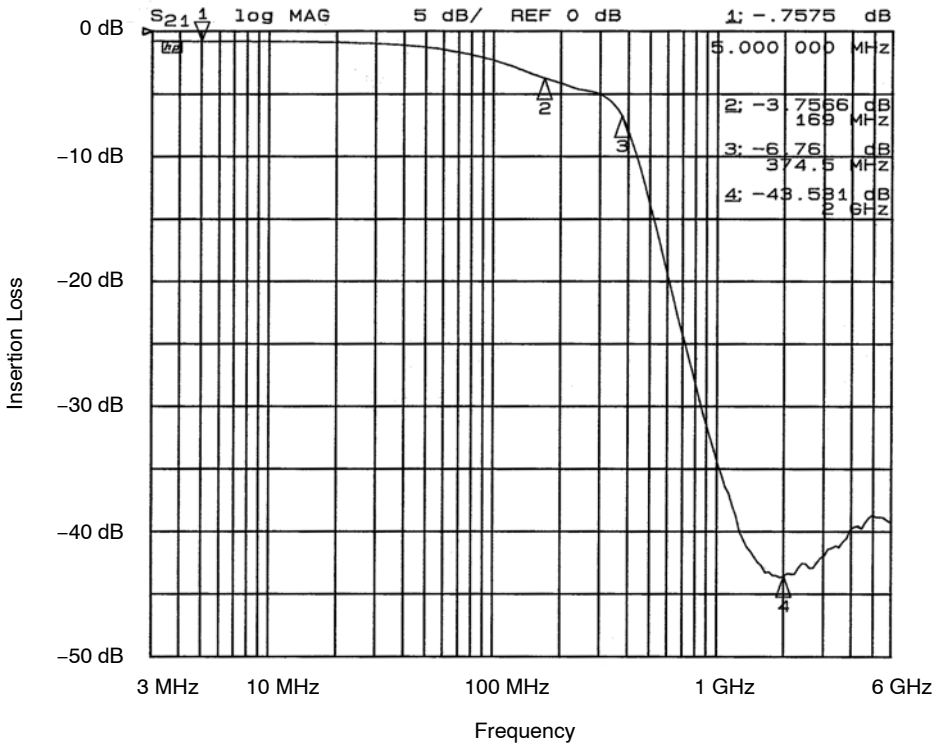


Figure 3. Filter 3 Insertion Loss (CM1460−04DE)

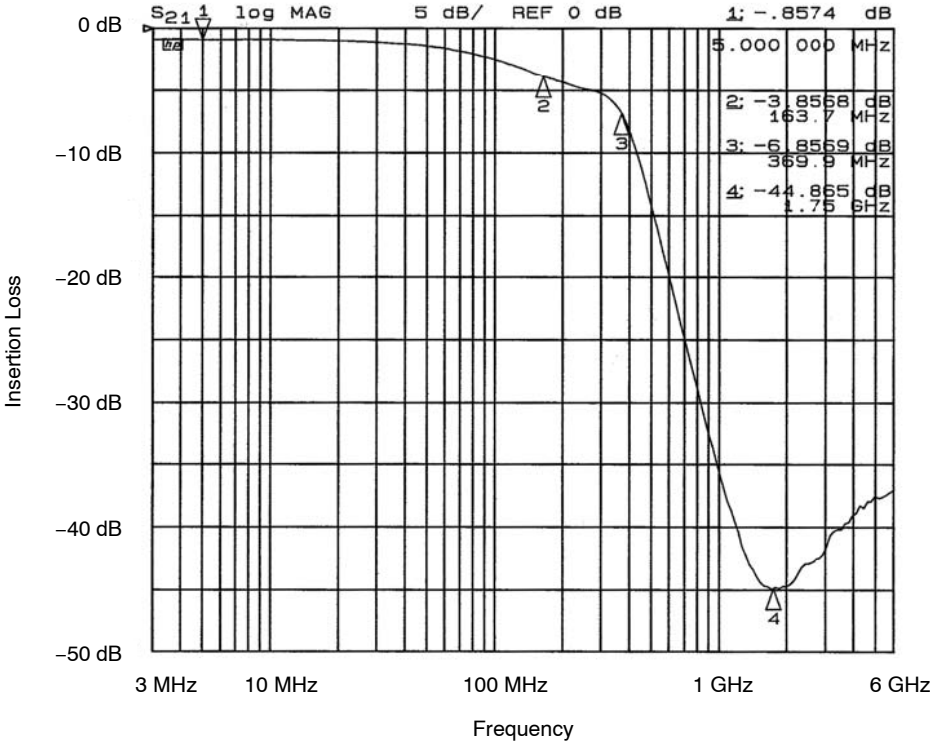


Figure 4. Filter 4 Insertion Loss (CM1460−04DE)

PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance (T_A = 25°C, DC Bias = 0 V, 50 Ω Environment)

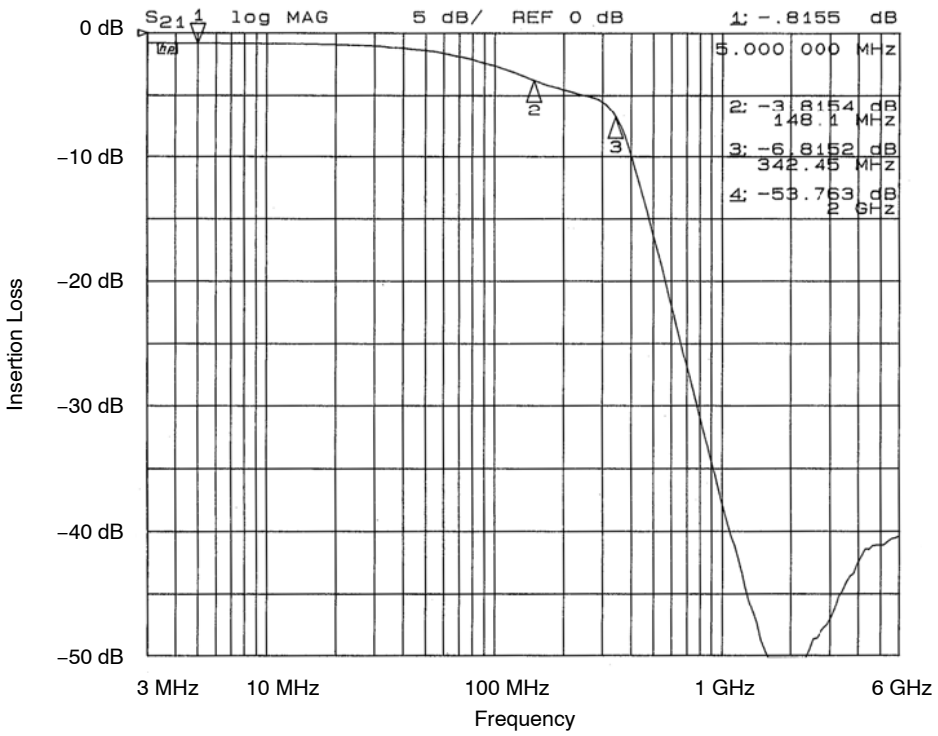


Figure 5. Filter 1 Insertion Loss (CM1460−06DE)

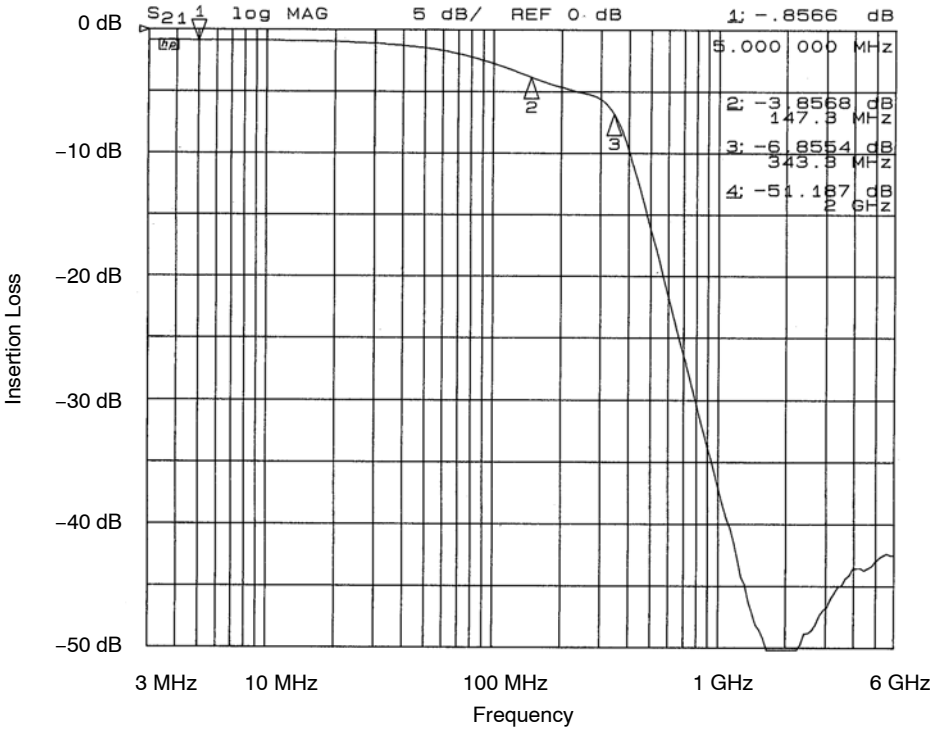


Figure 6. Filter 2 Insertion Loss (CM1460−06DE)

PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance (T_A = 25°C, DC Bias = 0 V, 50 Ω Environment)

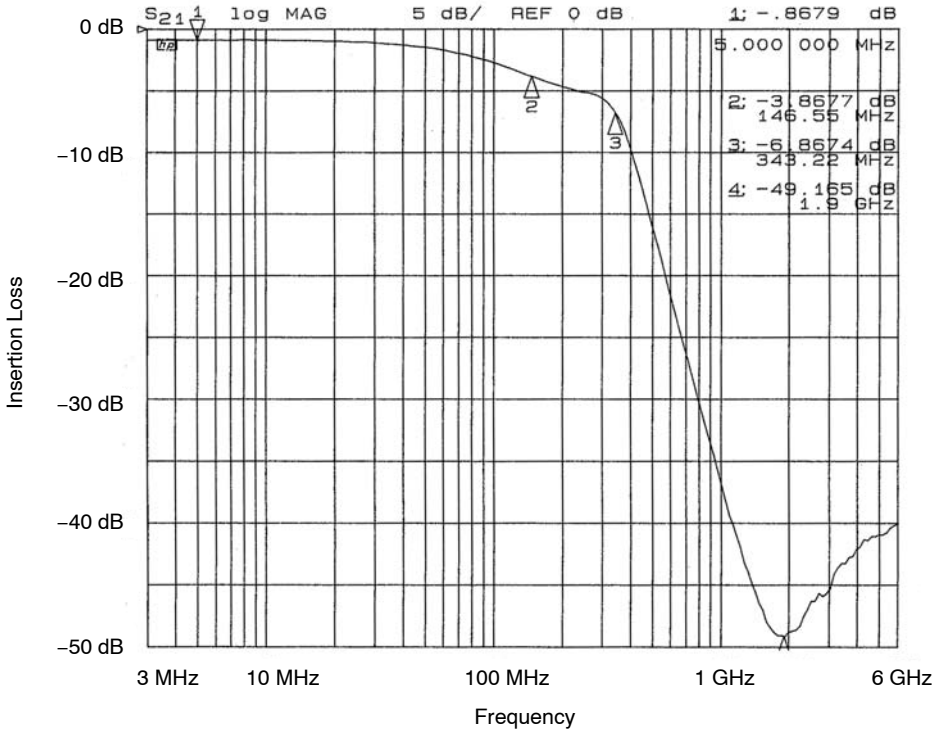


Figure 7. Filter 3 Insertion Loss (CM1460−06DE)

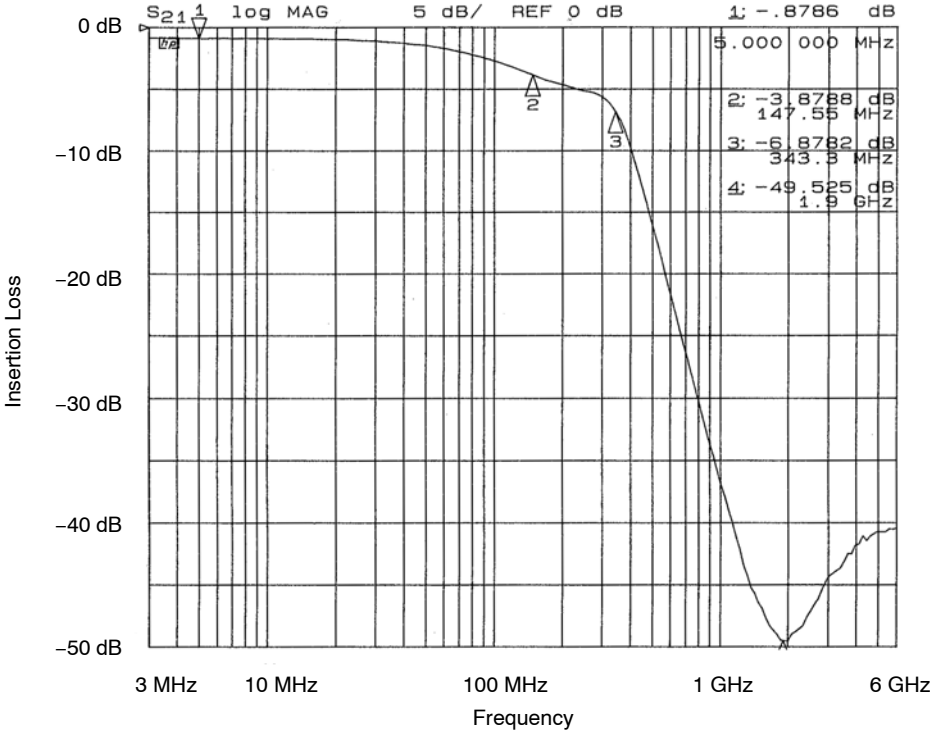


Figure 8. Filter 4 Insertion Loss (CM1460−06DE)

PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance (T_A = 25°C, DC Bias = 0 V, 50 Ω Environment)

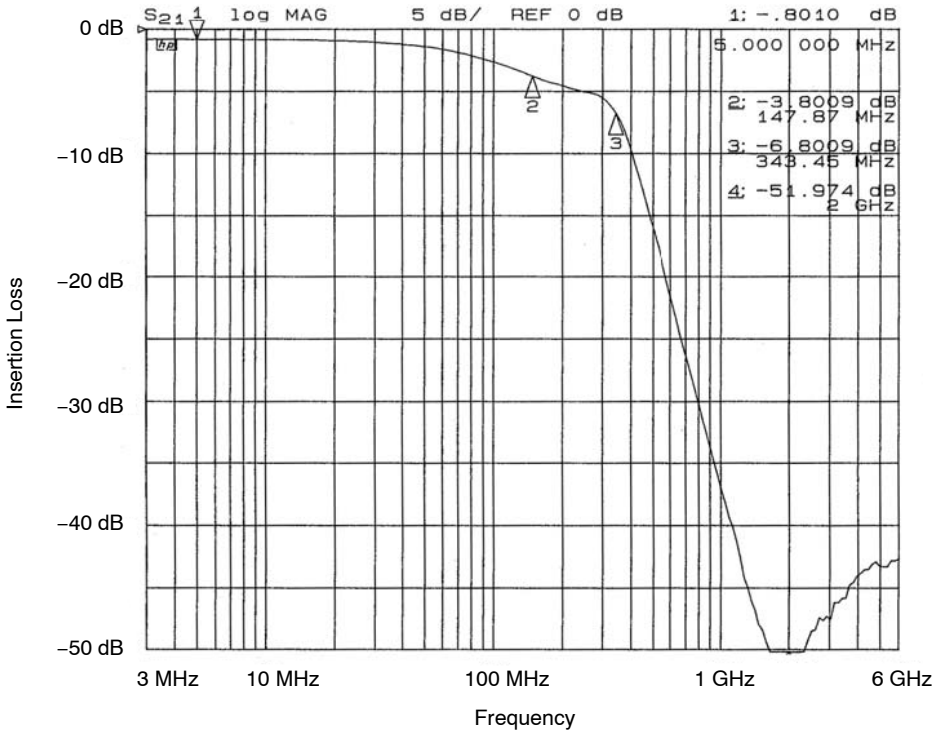


Figure 9. Filter 5 Insertion Loss (CM1460−06DE)

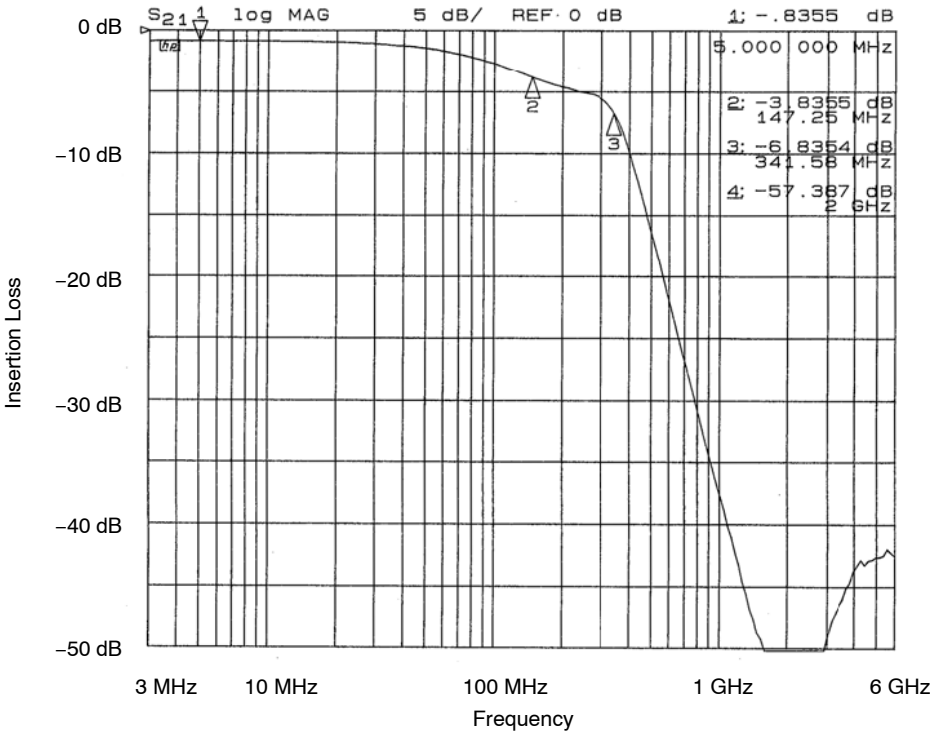


Figure 10. Filter 6 Insertion Loss (CM1460−06DE)

PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance (T_A = 25°C, DC Bias = 0 V, 50 Ω Environment)

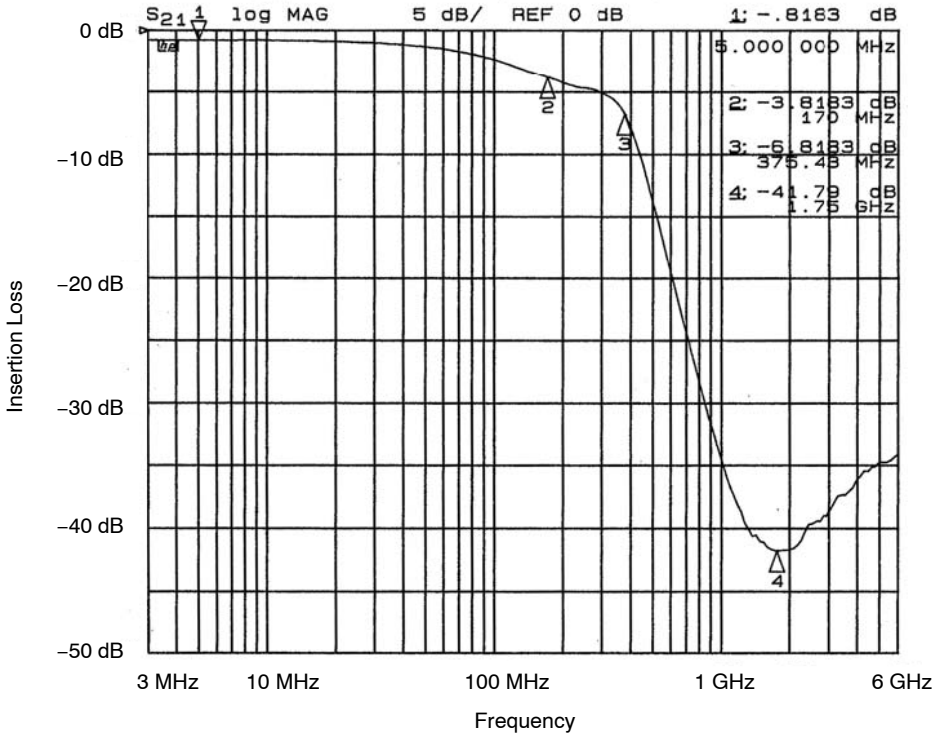


Figure 11. Filter 1 Insertion Loss (CM1460−08DE)

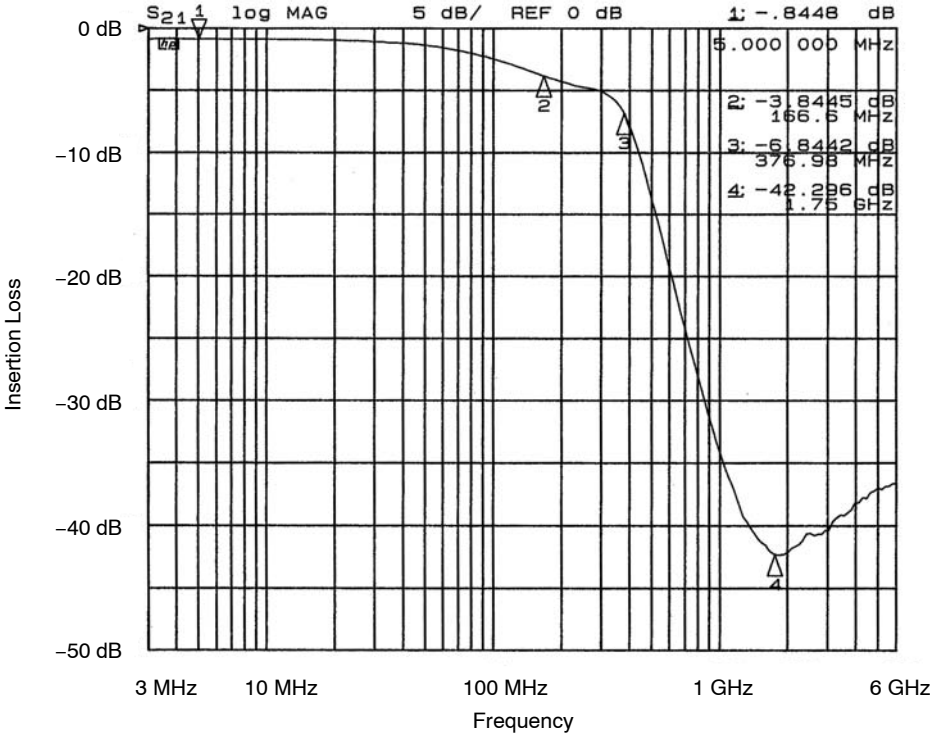


Figure 12. Filter 2 Insertion Loss (CM1460−08DE)

PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance (T_A = 25°C, DC Bias = 0 V, 50 Ω Environment)

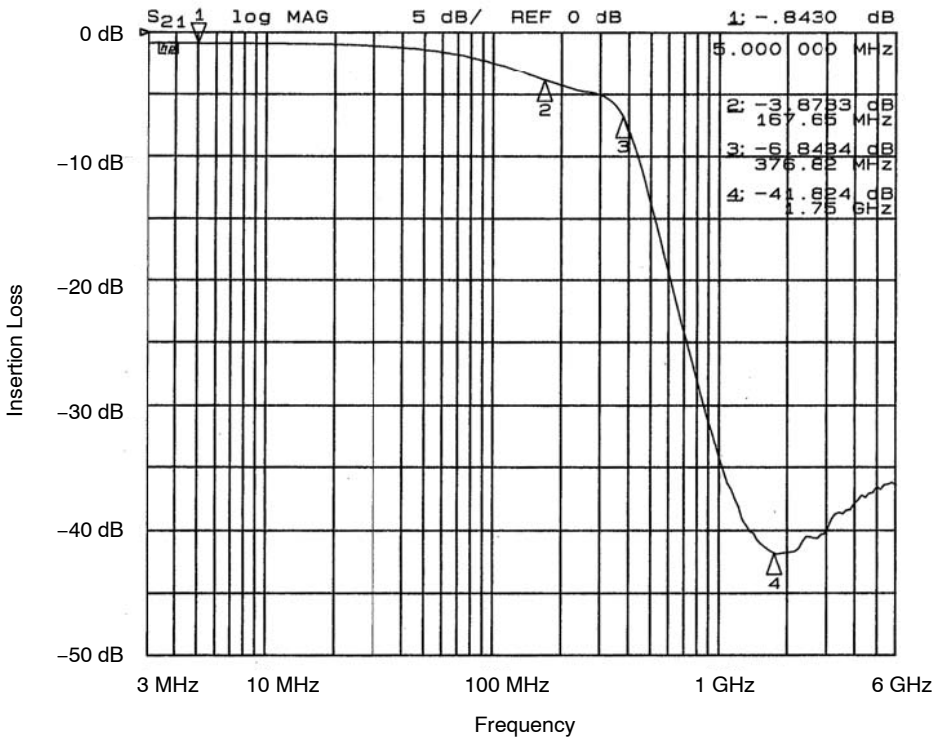


Figure 13. Filter 3 Insertion Loss (CM1460−08DE)

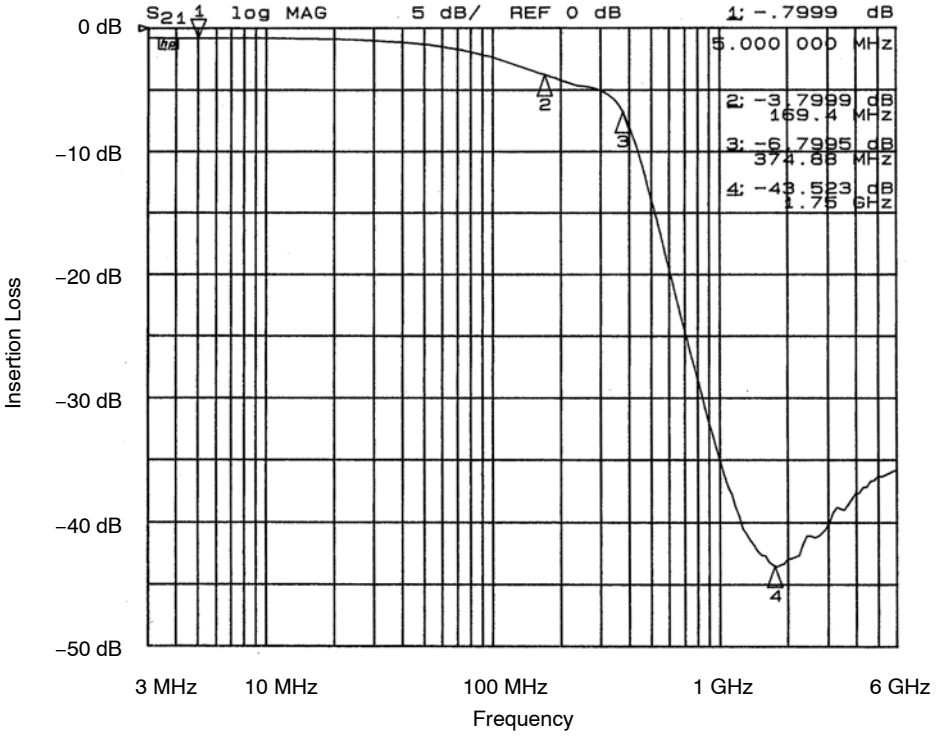


Figure 14. Filter 4 Insertion Loss (CM1460−08DE)

PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance (T_A = 25°C, DC Bias = 0 V, 50 Ω Environment)

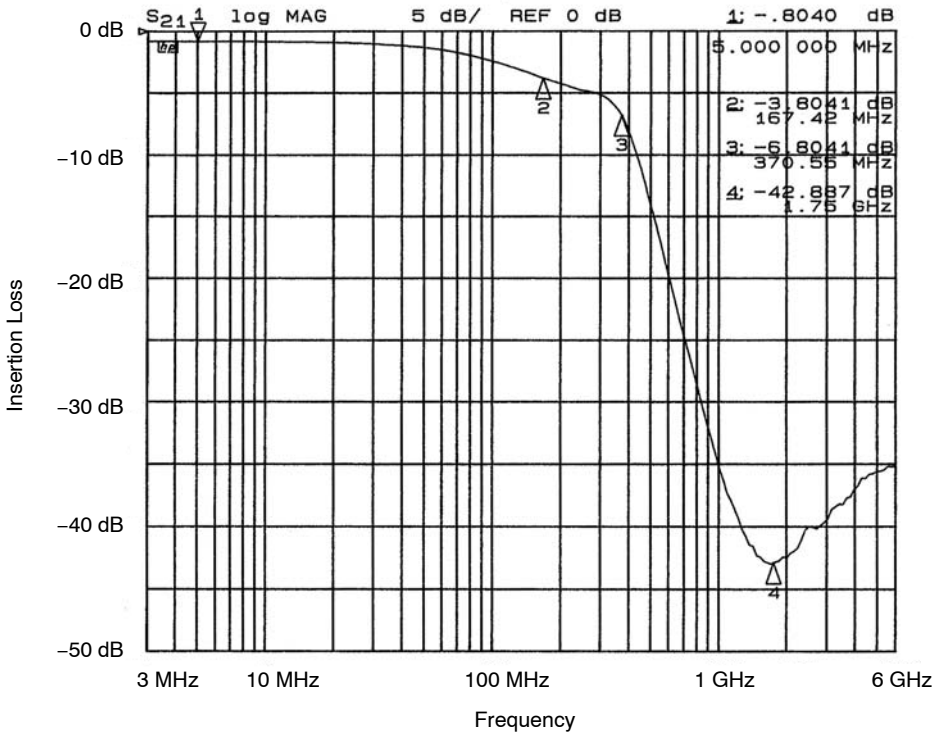


Figure 15. Filter 5 Insertion Loss (CM1460−08DE)

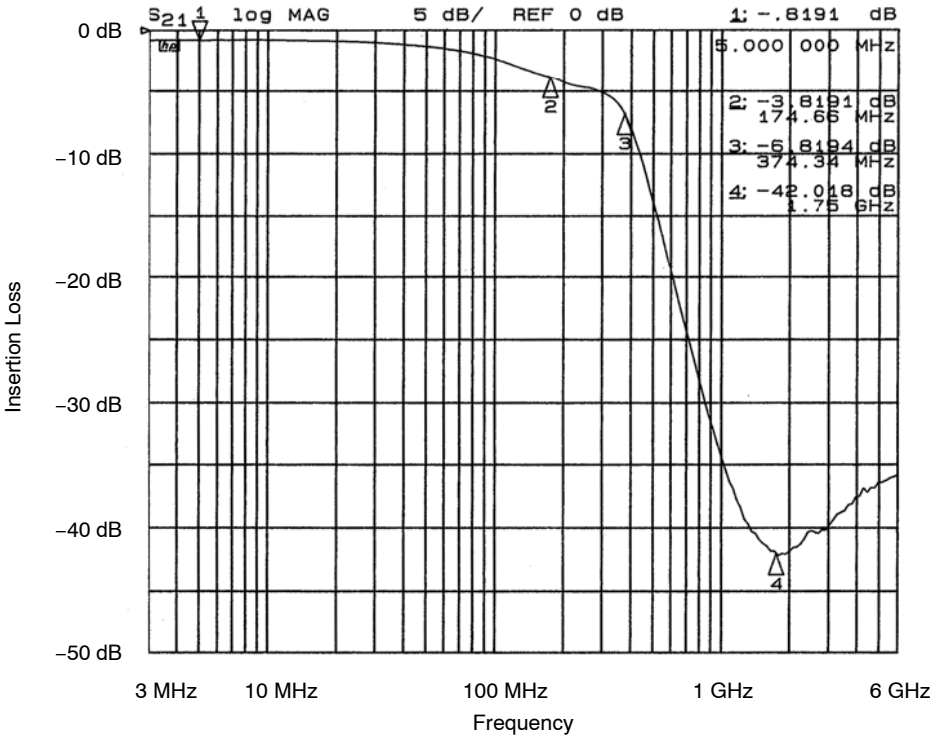


Figure 16. Filter 6 Insertion Loss (CM1460−08DE)

PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance (T_A = 25°C, DC Bias = 0 V, 50 Ω Environment)

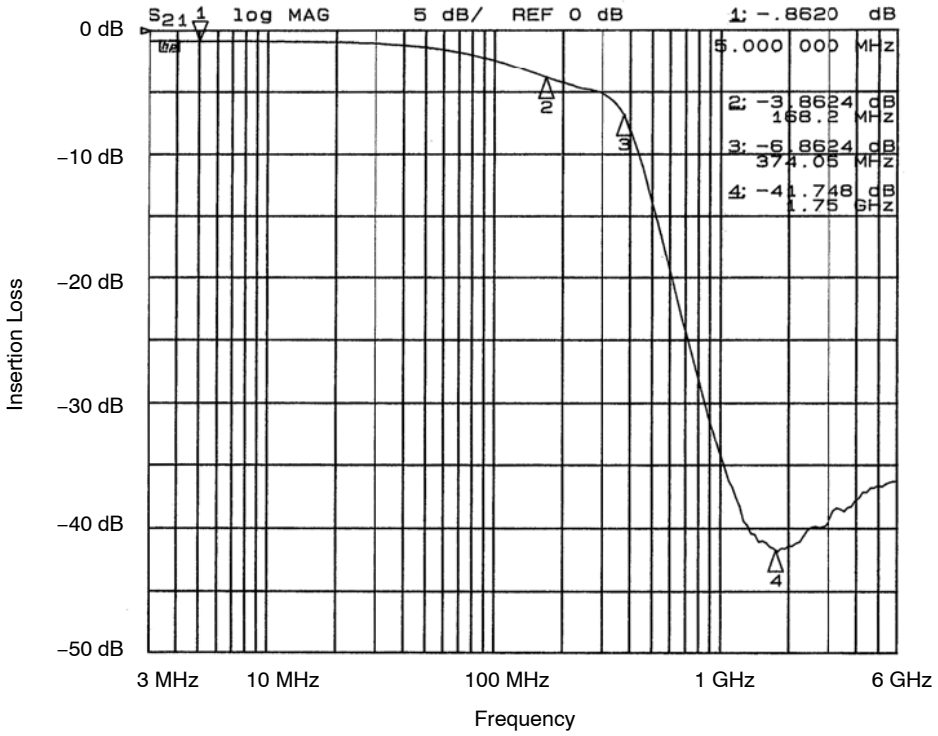


Figure 17. Filter 7 Insertion Loss (CM1460−08DE)

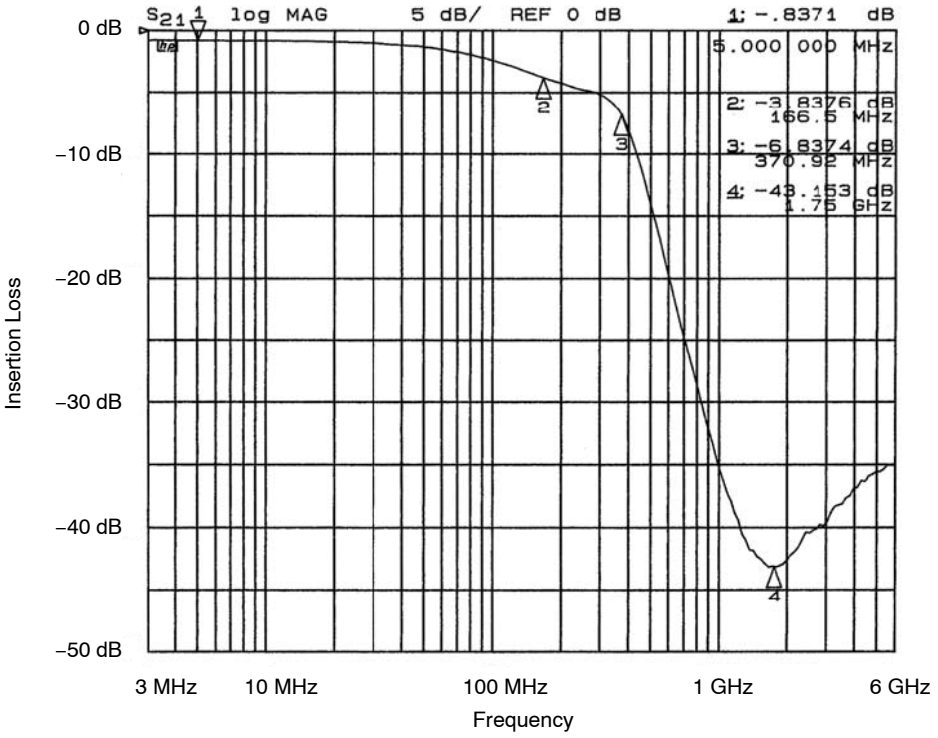


Figure 18. Filter 8 Insertion Loss (CM1460−08DE)

PERFORMANCE INFORMATION (Cont'd)

Typical Diode Capacitance vs. Input Voltage

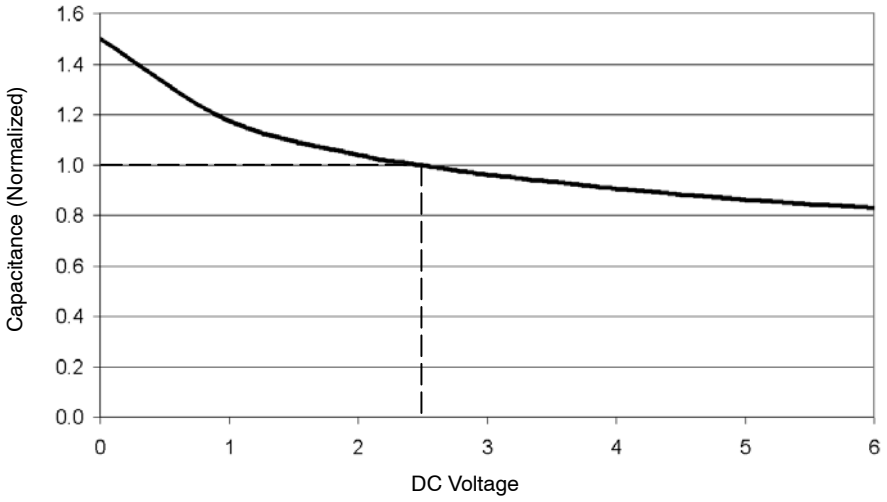
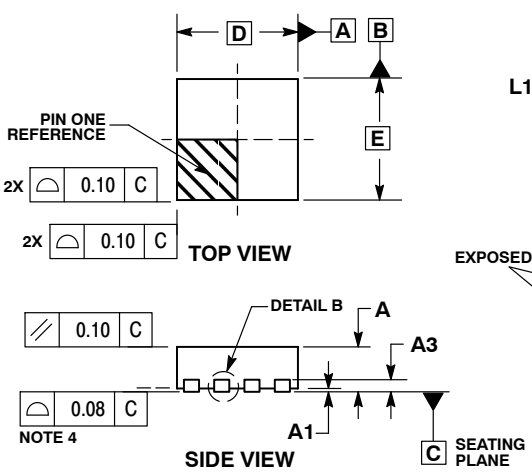
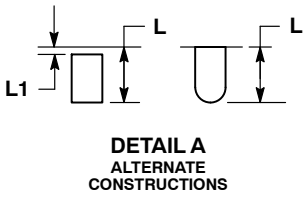


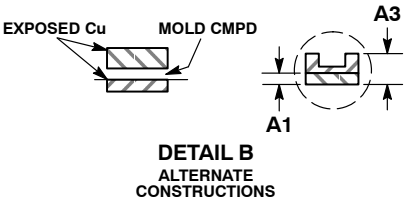
Figure 19. Filter Capacitance vs. Input Voltage (normalized to capacitance at 2.5 V DC and 25°C)

PACKAGE DIMENSIONS

WDFN8 2x2, 0.5P
CASE 511BE−01
ISSUE O

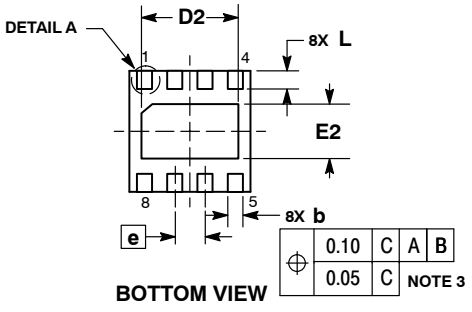




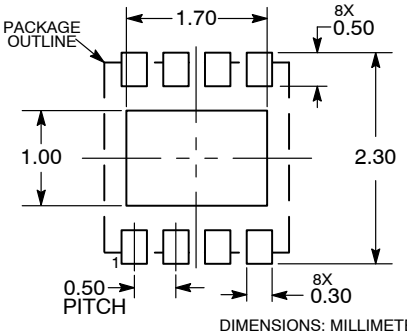


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.80	1.00
e	0.50 BSC	
K	0.25 REF	
L	0.20	0.40
L1	---	0.15



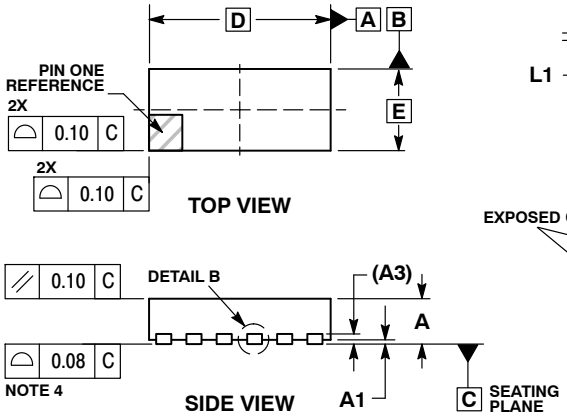
RECOMMENDED SOLDERING FOOTPRINT*

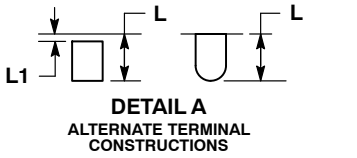


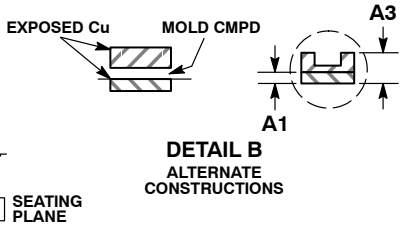
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

WDFN12, 3x1.35, 0.5P
CASE 511AZ−01
ISSUE O

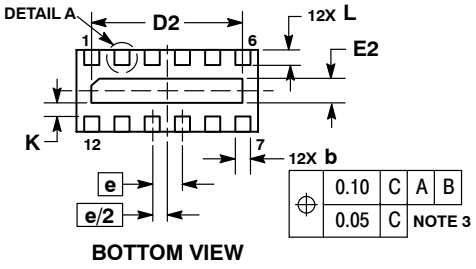




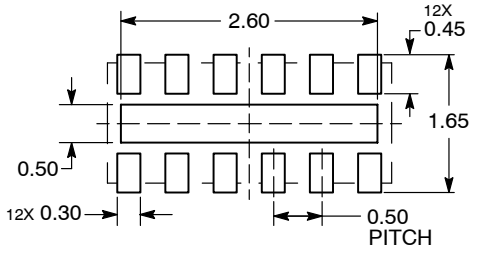


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

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DIM	MIN	MAX
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A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	3.00 BSC	
D2	2.40	2.60
E	1.35 BSC	
E2	0.30	0.50
e	0.50 BSC	
K	0.22 REF	
L	0.20	0.30
L1	−−−	0.15



RECOMMENDED SOLDERING FOOTPRINT*

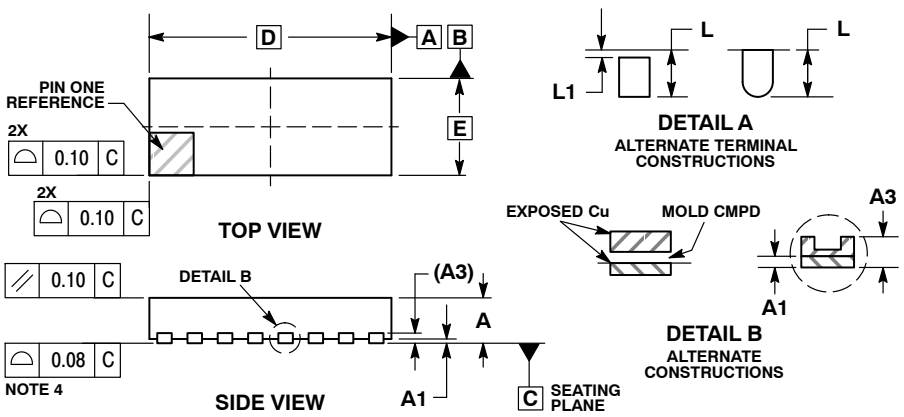


DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

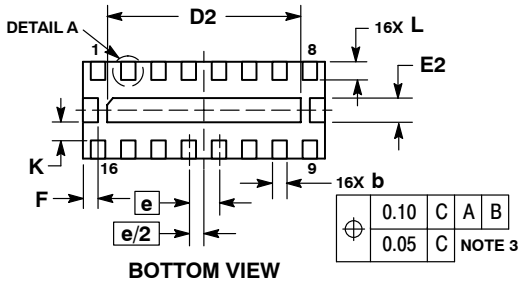
PACKAGE DIMENSIONS

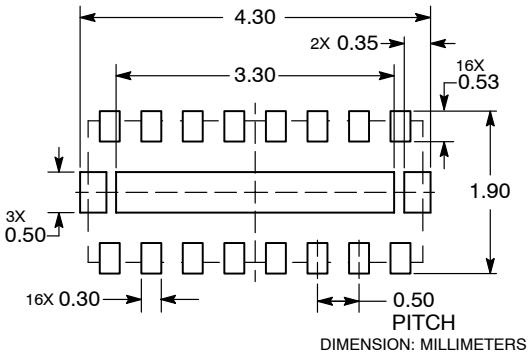
WDFN16, 4x1.6, 0.5P
CASE 511AU−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	3.10	3.30
E	1.60 BSC	
E2	0.30	0.50
e	0.50 BSC	
F	0.25 REF	
K	0.30 REF	
L	0.20	0.40
L1	−−−	0.15





*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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