National Semiconductor

CLC522
Wideband Variable-Gain Amplifier

General Description

The CLC522 variable gain amplifier (VGA) is a dc-coupled, two-quadrant multiplier with differential voltage inputs and a single-ended voltage output. Two input buffers and an output operational amplifer are integrated with the multiplier core to make the CLC522 a complete VGA system that does not require external buffering.

The CLC522 provides the flexibility of externally setting the maximum gain with only two external resistors. Greater than 40dB gain control is easily achieved through a single high impedance voltage input. The CLC522 provides a linear (in Volts per Volt) relationship between the amplifier's gain and the gain-control input voltage.

The CLC522's maximum gain may be set anywhere over a nominal range of 2V/V to 100V/V. The gain control input then provides attenuation from the maximum setting. For example, set for a maximum gain of 100V/V, the CLC522 will provide a 100V/V to 1V/V gain control range by sweeping the gain control input voltage from +1 to -0.98V.

Set at a maximum gain of 10V/V, the CLC522 provides a 165MHz signal channel bandwidth and a 165MHz gain control bandwidth. Gain nonlinearity over a 40dB gain range is 0.5% and gain accuracy at A_{Vmax} = 10V/V is typically ±0.3%.

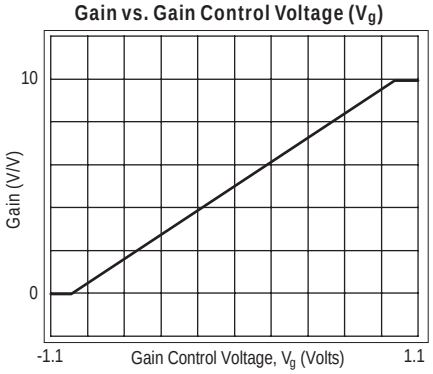
Features

- 330MHz signal bandwidth: A_{vmax} = 2
- 165MHz gain-control bandwidth
- 0.3° to 60MHz linear phase deviation
- 0.04% (-68dB) signal-channel non-linearity
- >40dB gain-adjustment range
- Differential or single-end voltage inputs
- Single-ended voltage output

Applications

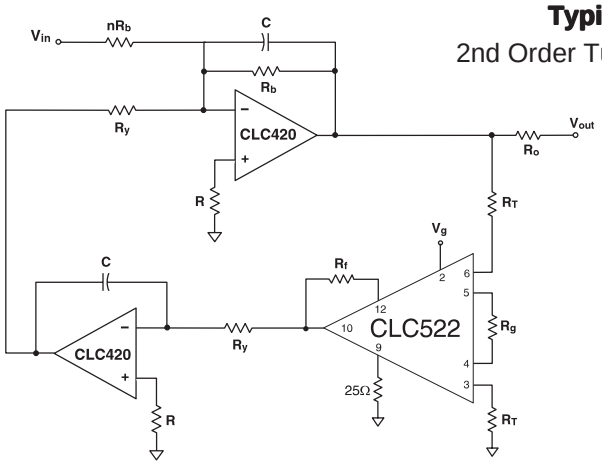
- Variable attenuators
- Pulse amplitude equalizers
- HF modulators
- Automatic gain control & leveling loops
- Video production switching
- Differential line receivers
- Voltage controlled filters

Gain vs. Gain Control Voltage (V_g)



Typical Application

2nd Order Tuneable Bandpass Filter

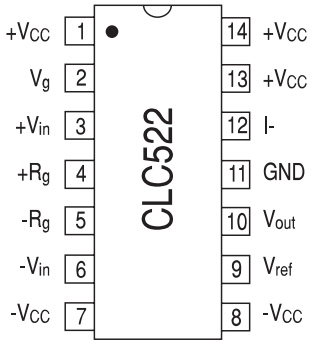


$$\frac{V_o}{V_{in}} = \left(-\frac{1}{n}\right)\frac{s\frac{1}{CR_b}}{s^2 + s\frac{1}{CR_b} + \frac{k}{C^2R_y{}^2}}$$

$$k = 185\frac{R_f}{R_g},\ Q = \frac{\sqrt{k}R_b}{R_y},\ \omega_o = \frac{\sqrt{k}}{CR_y}$$

Pinout

DIP & SOIC



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CLC522 Electrical Characteristics (V_{CC} = ±5V; A_{Vmax} = +10; R_f =1kΩ; R_g =182W; R_L = 100Ω; V_g=+1.1V)

PARAMETERS	CONDITIONS	TYP	MIN/MAX RATINGS			UNITS	NOTES
Ambient Temperature	AJ	+25	+25	0 to +70	-40 to +85	°C	1
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth	V_{out} < 0.5V_{pp}	165	120	115	110	MHz	
	V_{out} < 5.0V_{pp}	150	100	95	90	MHz	
gain control bandwidth	V_{out} < 0.5V_{pp}	165	120	115	110	MHz	3
gain flatness	V_{out} < 0.5V_{pp}						
peaking	DC to 30MHz	0	0.1	0.1	0.1	dB	
rolloff	DC to 30MHz	0.05	0.25	0.25	0.4	dB	
linear phase deviation	DC to 60MHz	0.3	1.0	1.1	1.2	°	
feedthrough	30MHz	- 62	- 57	- 57	-57	dB	4
TIME DOMAIN RESPONSE							
rise and fall time	0.5V step	2.2	2.9	3.0	3.2	ns	
	5.0V step	3.0	5.0	5.0	5.0	ns	
settling time	2.0V step to 0.1%	12	18	18	18	ns	
overshoot	0.5V step	2	15	15	15	%	
slew rate	4.0V step	2000	1400	1400	1400	V/µs	
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp}, 20MHz	- 50	- 44	- 44	-44	dBc	
3rd harmonic distortion	2V_{pp}, 20MHz	- 65	- 58	- 56	-54	dBc	
equivalent input noise	1 to 200MHz	5.8	6.2	6.5	6.8	nV/√Hz	
noise floor	1 to 200MHz	- 152	- 150	- 149	- 149	dBm_{1Hz}	
GAIN ACCURACY							
signal channel nonlinearity (SGNL)	V_{out} = ±2V_{pp}	0.04	0.1	0.1	0.1	%	2
gain control nonlinearity (GCNL)	full range	0.5	2.0	2.2	3.0	%	2
gain error (GACCU)	A_{Vmax}=+10	± 0.0	± 0.5	± 0.5	± 1.0	dB	2
V_g high		+ 990	+ 990±60	+ 990±60	+ 990±60	mV	
low		- 975	- 975±80	- 975±80	- 975±80	mV	
STATIC DC PERFORMANCE							
V_{in} voltage range	common mode	± 2.2	± 1.2	± 1.2	± 1.4	V	
bias current		9	21	26	45	µA	2
average drift		65	---	175	275	nA/°C	
offset current		0.2	2.0	3.0	4.0	µA	
average drift		5	---	30	40	nA/°C	
resistance		1500	650	450	175	kΩ	
capacitance		1.0	2.0	2.0	2.0	pF	
V_g bias current		15	38	47	82	µA	
average drift		125	---	300	600	nA/°C	
resistance		100	38	30	15	kΩ	
capacitance		1.0	2.0	2.0	2.0	pF	
output voltage range	R_L= ∞	± 4.0	± 3.7	± 3.6	± 3.5	V	
current		± 70	± 47	± 40	± 25	mA	
offset voltage	A_{Vmax}=+10	25	85	95	120	mV	2
average drift		100	---	350	400	µV/°C	
resistance		0.1	0.2	0.3	0.6	Ω	
I_{Rgmax}		1.8	1.37	1.26	1.15	mA	
power supply sensitivity	output referred	10	40	40	40	mV/V	
common-mode rejection ratio	input referred	70	59	59	59	dB	
supply current	R_L= ∞	46	61	62	63	mA	2

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

supply voltage	±7V
short circuit current	80mA
common-mode input voltage	±V_{cc}
maximum junction temperature	+150°C
storage temperature	-65°C to+150°C
lead temperature (soldering 10 sec)	+300°C
transistor count	74

Notes

1) AJE (SOIC) is tested/guaranteed with R_f=866Ω and R_g= 165Ω.
2) J-level, spec is 100% tested at +25°C.
3) Specified with V_{in} = 0.2V and V_g < 0.5V_{pp}.
4) Feedtrough is specified at max. attenuation (i.e V_g =-1.1V)

Ordering Information

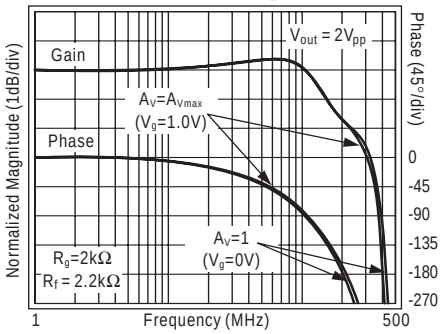
Model	Temperature Range	Description
CLC522AJP	-40°C to +85°C	14-pin PDIP
CLC522AJE	-40°C to +85°C	14-pin SOIC
CLC522ALC	-40°C to +85°C	dice
CLC522AMC	-55°C to +125°C	dice, MIL-STD-883

Package Thermal Resistance

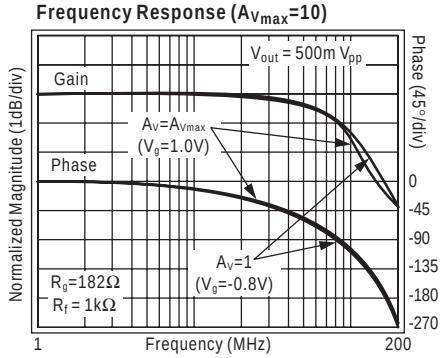
Package	θ_{JC}	θ_{JA}
Plastic (AJP)	55°C/W	100°C/W
Surface Mount (AJE)	35°C/W	105°C/W
CerDIP	40°C/W	95°C/W

CLC522 Typical Performance (T_A=+25°C, V_{CC}=±5V, A_V=+10, V_g=1.1V, R_L=100Ω; unless noted)

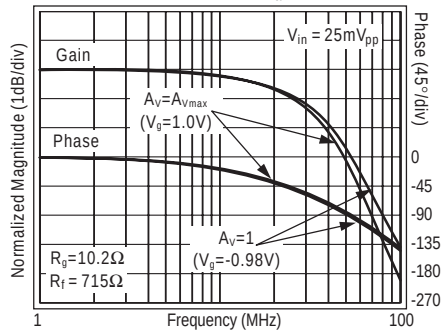
Frequency Response ($A_{V_{max}}$=2)



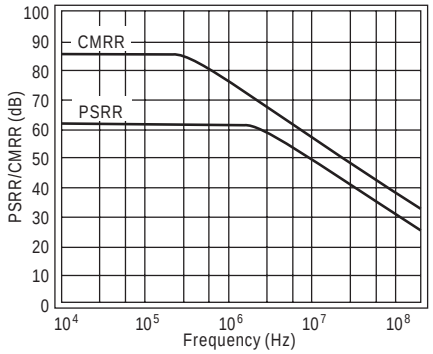
Frequency Response ($A_{V_{max}}$=10)



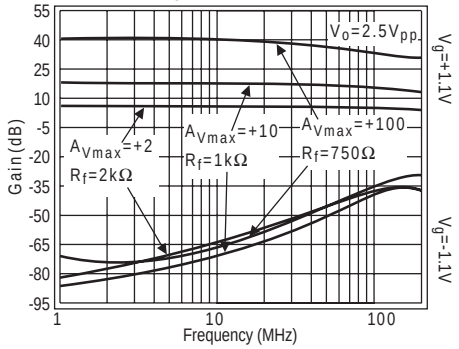
Frequency Response ($A_{V_{max}}$=100)



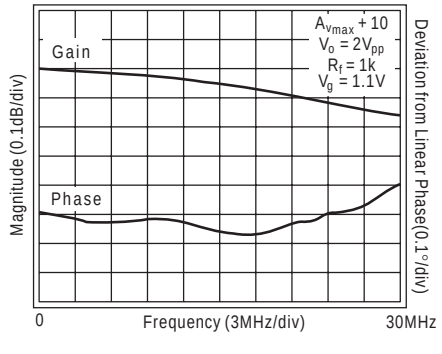
PSRR and CMRR (Input Referred)



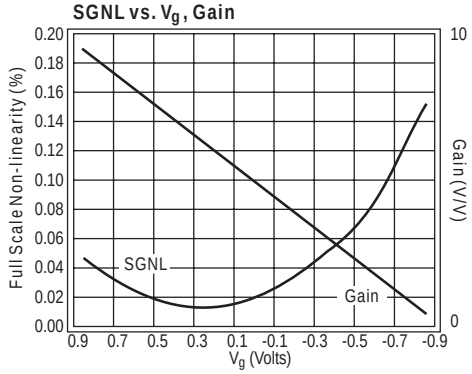
Feed-through Isolation



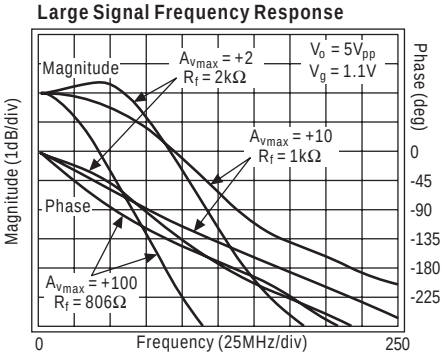
Gain Flatness & Linear Phase Deviation



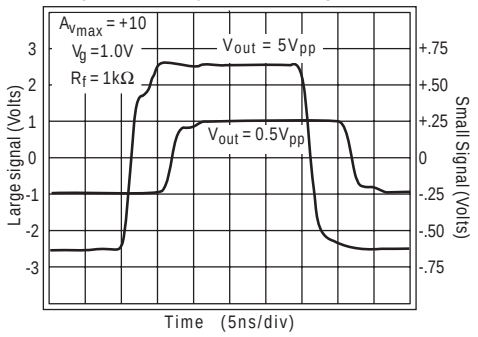
SGNL vs. V_g, Gain



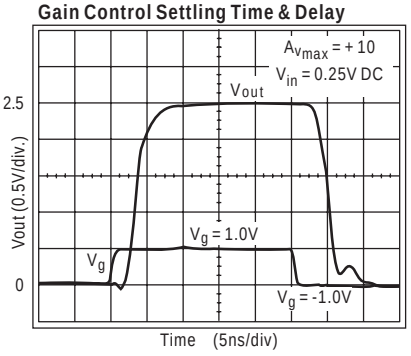
Large Signal Frequency Response



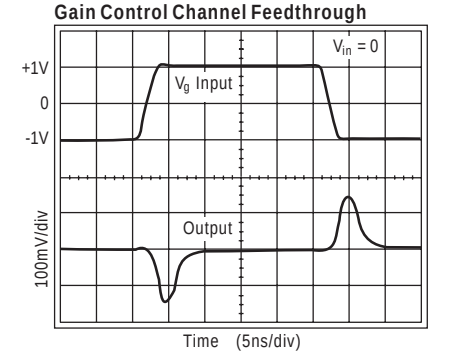
Large & Small Signal Pulse Response



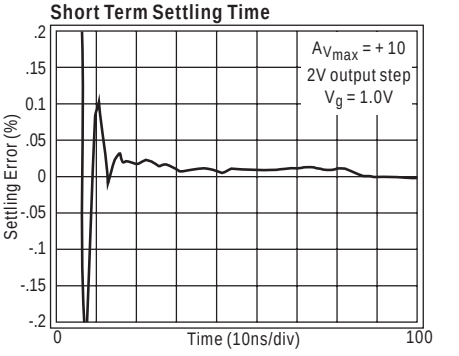
Gain Control Settling Time & Delay



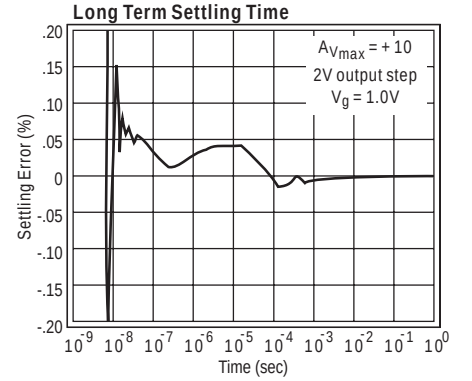
Gain Control Channel Feedthrough



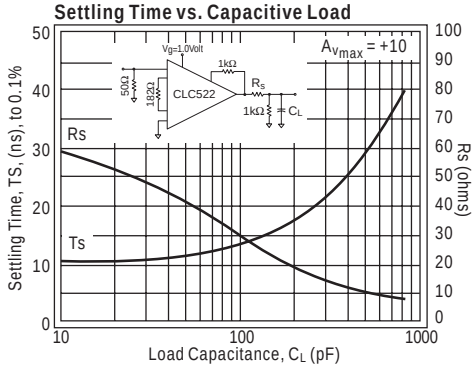
Short Term Settling Time



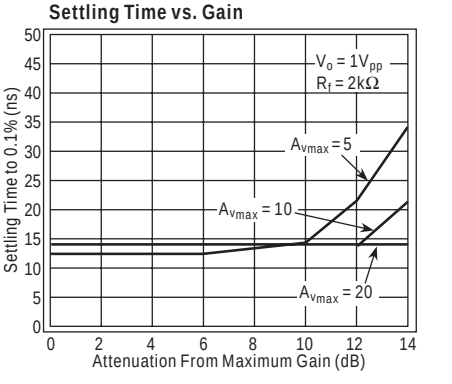
Long Term Settling Time



Settling Time vs. Capacitive Load

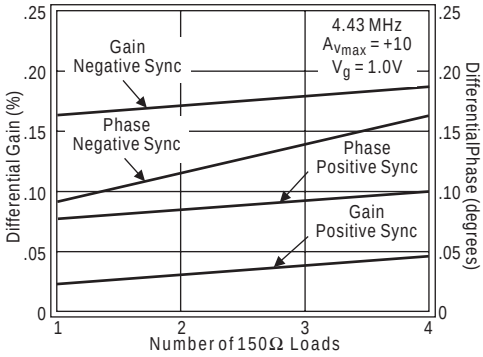


Settling Time vs. Gain

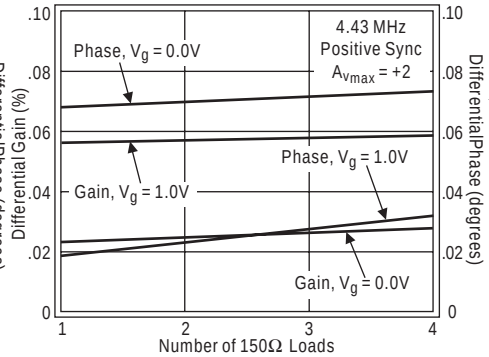


CLC522 Typical Performance (T_A=+25°C, V_{CC}=±5V, A_V=+10, V_g=1.1V, R_L=100Ω; unless noted)

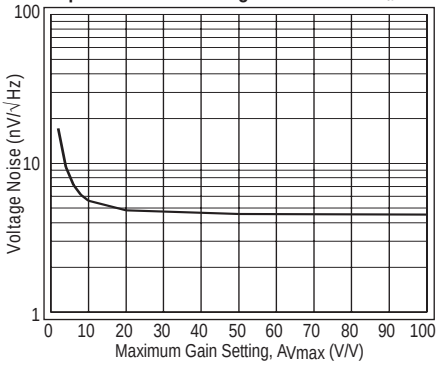
Differential Gain and Phase



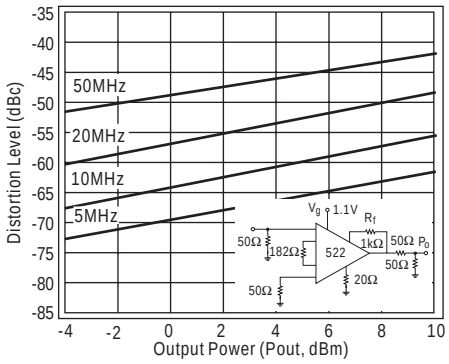
Differential Gain and Phase



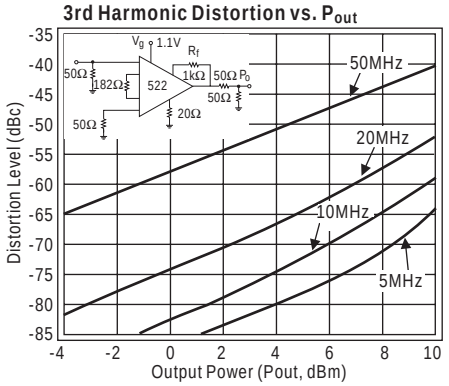
Input Referred Voltage Noise vs A_{Vmax}



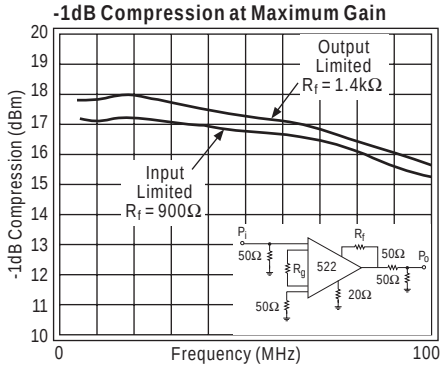
2nd Harmonic Distortion vs. P_{out}



3rd Harmonic Distortion vs. P_{out}



-1dB Compression at Maximum Gain



Application Discussion

Theory of Operation

The CLC522 is a linear wideband variable-gain amplifier as illustrated in Fig 1. A voltage input signal may be applied differentially between the two inputs (+V_{in}, -V_{in}), or single-endedly by grounding one of the unused inputs.

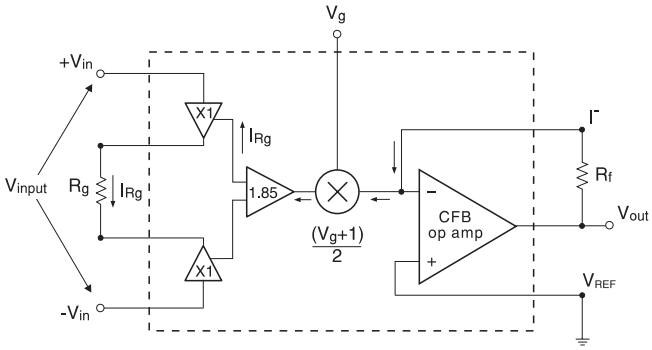


Fig. 1

The CLC522 input buffers convert the input voltage to a current (I_{Rg}) that is a function of the differential input voltage (V_{input} =+V_{in} - -V_{in}) and the value of the gain-setting resistor (R_g). This current (I_{Rg}) is then mirrored to a gain stage with a current gain of 1.85. The voltage-controlled two-quadrant multiplier attenuates this current which is then converted to a voltage via the output amplifier. This output amplifier is a current-feedback op amp configured as a transimpedance amplifier. It's transimpedance gain is the feedback resistor (R_f). The input signal, output, and gain control are all voltages. The output voltage can easily be calculated as seen in Eq. 1.

$$V_{out} = I_{R_g} * 185 * \left(\frac{V_g + 1}{2}\right) * R_f \qquad \text{Eq. 1}$$

$$\text{since } I_{R_g} = \frac{V_{input}}{R_g}$$

$$A_v = 185 * \frac{R_f}{R_g} * \left(\frac{V_g + 1}{2}\right) \qquad \text{Eq. 2}$$

The gain of the CLC522 is therefore a function of three external variables; R_g, R_f and V_g as expressed in Eq. 2. The gain-control voltage (V_g) has a ideal input range of -1V≤V_g≤+1V. At V_g=+1V, the gain of the CLC522 is at its maximum as expressed in Eq. 3.

$$A_{V_{max}} = 185\frac{R_f}{R_g} \qquad \text{Eq. 3}$$

Notice also that Eq. 3 holds for both differential and single-ended operation.

Choosing R_f and R_g

R_g is calculated from Eq.4. $V_{input_{max}}$ is the maximum peak

$$R_g = \frac{V_{input_{max}}}{I_{R_{g_{max}}}} \qquad \text{Eq. 4}$$

input voltage (V_{pk}) determined by the application. $I_{Rg_{max}}$ is the maximum allowable current through R_g and is typically 1.8mA. Once A_{Vmax} is determined from the minimum input and desired output voltages, R_f is then determined using Eq. 5. These values of R_f and R_g are

$$R_f = \frac{1}{185} * R_g * A_{V_{max}} \qquad \text{Eq. 5}$$

the minimum possible values that meet the input voltage and maximum gain constraints. Scaling the resistor values will decrease bandwidth and improve stability.

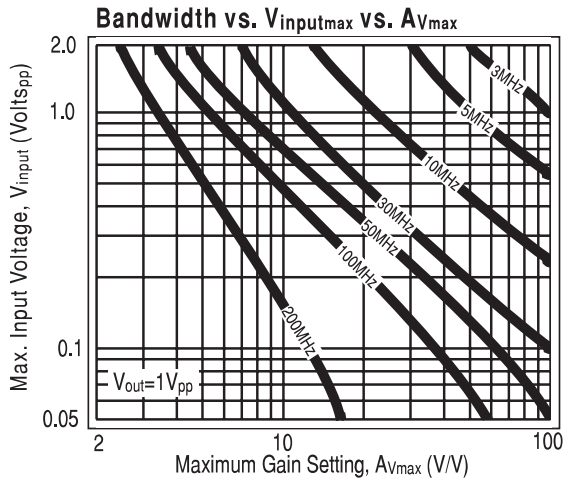


Fig. 2

Fig. 2 illustrates the resulting CLC522 bandwidths as a function of the maximum and minimum input voltages when V_{out} is held constant at $1V_{pp}$.

Adjusting Offsets

Treating the offsets introduced by the input and output stages of the CLC522 is easily accomplished with a two step process. The offset voltage of the output stage is treated by first applying -1.1Volts on V_g, which effectively

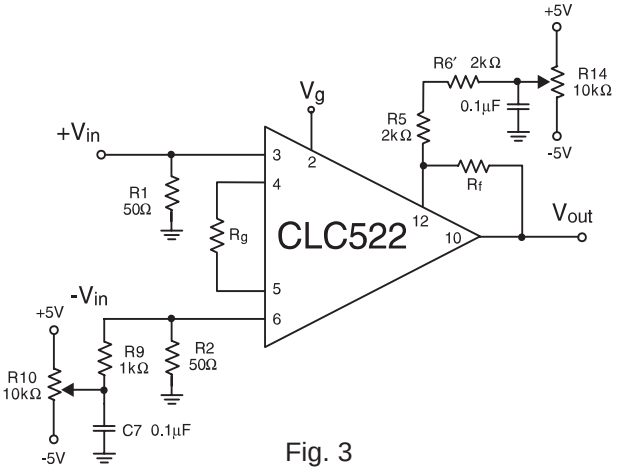


Fig. 3

isolates the input stage and multiplier core from the output stage. As illustrated in Fig. 3, the trim pot located at R14 on the CLC522 Evaluation Board should then be adjusted in order to null the offset voltage seen at the CLC522's output (pin 10). Once this is accomplished, the offset errors introduced by the input stage and multiplier core can then be treated. The second step requires the absence of an input signal and matched source impedances on the two input pins in order to cancel the bias current errors. This done then +1.1Volts should be applied to V_g and the trim pot located at R10 adjusted in order to null the offset voltage seen at the CLC522's output. If a more limited gain range is anticipated, the above adjustments should be made at these operating points.

Gain Errors

The CLC522's gain equation as theoretically expressed in Eq. 2 must include the device's error terms in order to yield the actual gain equation. Each of the gain error terms are specified in the Electrical Characteristics table and are defined below and illustrated in Fig. 4.

GACCU : error of $A_{V_{max}}$, expressed as ±dB.
GCNL : deviation from theoretical expressed as ±%.
$V_{g_{high}}$: voltage on V_g producing $A_{V_{max}}$.
$V_{g_{low}}$: voltage on V_g producing $A_{V_{min}}$ = 0V/V.
$\Delta V_{g_{high}}, \Delta V_{g_{low}}$: error of $V_{g_{high}}, V_{g_{low}}$ expresed as ±mV.

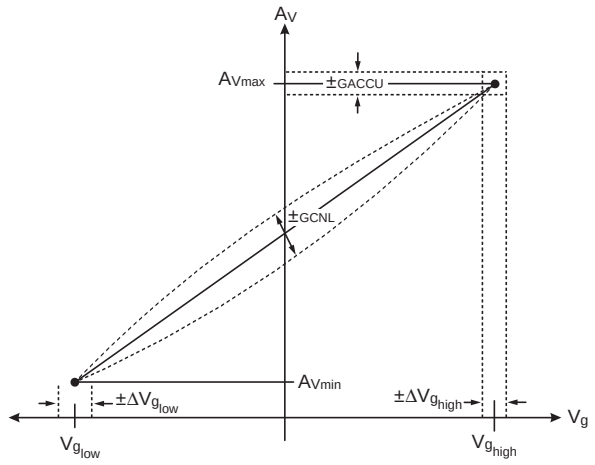


Fig. 4

Combining these error terms with Eq. 2 gives the "gain envelope" equation and is expressed in Eq. 7. From the Electrical Characteristics table, the nominal endpoint values of V_g are: $V_{g_{high}}$ =+990mV and $V_{g_{low}}$ = -975mV.

$$A_V = A_{V_{max}}\left(\frac{10^{\frac{\pm GACCU}{20}}\left(V_g - V_{g_{low}} \pm \Delta V_{g_{low}}\right)}{\left(V_{g_{high}} \pm \Delta V_{g_{high}} - V_{g_{low}} \pm \Delta V_{g_{low}}\right)} \pm \left(1 - V_g^2\right) GCNL\right) \quad \text{Eq . 7}$$

Signal-Channel Nonlinearity

Signal-channel nonlinearity, SGNL, also known as integral endpoint linearity, measures the non-linearity of an amplifier's voltage transfer function. The CLC522's SGNL, as it is specified in the Electrical Characteristics table, is measured while the gain is set at its maximum (i.e. V_g=+1.1V). The Typical Performance Characteristics plot labled "SGNL & Gain vs V_g" illustrates the CLC522's SGNL as V_g is swept through its full range. As can be seen in this plot, when the gain as reduced from $A_{V_{max}}$, SGNL improves to < 0.02%(-74dB) at V_g=0 and then degrades somewhat at the lowest gains.

Noise

Fig. 5 describes the CLC522's input-refered spot noise density as a function of $A_{V_{max}}$. The plot includes all the noise contributing terms. At $A_{V_{max}}$ = 10V/V, the CLC522 has a typical input-referred spot noise density (e_{ni}) of 5.8nV/√Hz. The input RMS voltage noise can be determined from the following single-pole model:

$$V_{RMS} = e_{in} * \sqrt{157 * (-3dB\ bandwidth)} \quad \text{Eq. 8}$$

Further discussion and plots of noise and the noise model is provided in Application Note OA-23. Comlinear also provides SPICE models that model internal noise and other parameters for a typical part.

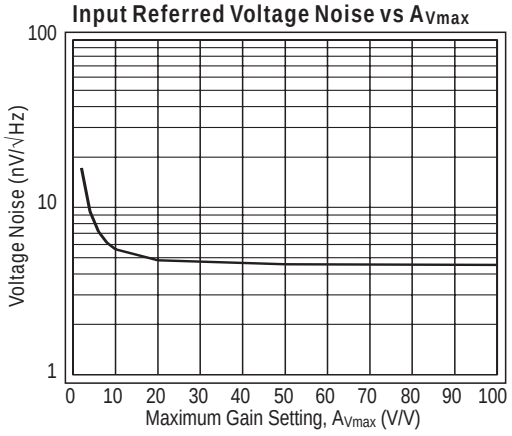


Fig. 5

Circuit Layout Considerations

Please refer to the CLC522 Evaluation Board Literature for precise layout guidelines. Good high-frequency operation requires all of the de-coupling capcitors shown in Fig. 6 to be placed as close as possible to the power

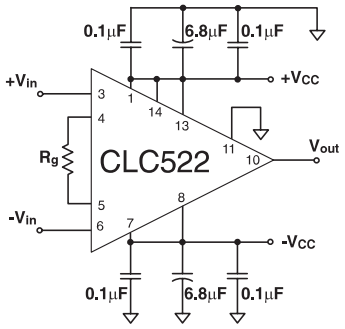


Fig. 6

supply pins in order to insure a proper high-frequency low-impedance bypass. Adequate ground plane and low-inductive power returns are also required of the layout. Minimizing the parasitic capacitances at pins 3, 4, 5, 6, 9,

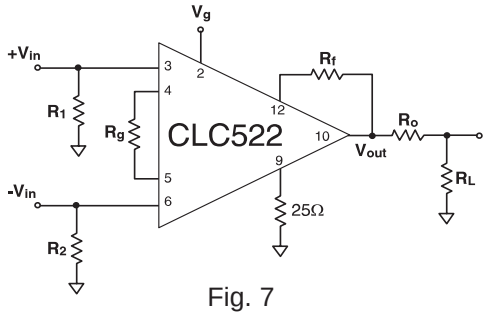


Fig. 7

10 and 12 as shown in Fig. 7 will assure best high frequency performance. Vref (pin 9) to ground should include a small resistor value of 25 ohms or greater to buffer the internal voltage follower. The parasitic inductance of component leads or traces to pins 4, 5 and 9 should also be kept to a minimum. Parasitic or load capacitance, C_L, on the output (pin 10) degrades phase margin and can lead to frequency response peaking or circuit oscillation. This should be treated with a small series resistor between output (pin 10) and C_L (see the plot “Settling Time vs. Capacitive Load" for a recommended series resistance).

Component parasitics also influence high frequency results, therefore it is recommended to use metal film resistors such as RN55D or leadless components such as surface mount devices. High profile sockets are not recommended. If socketing is necessary, it is recommended to use low impedance flush mount connector jacks such as Cambion (P/N 450-2598).

Application Circuits

Four-Quadrant Multiplier

Applications requiring multiplication, squaring or other non-linear functions can be implemented with four-quadrant multipliers. The CLC522 implements a four-quadrant multiplier as illustrated in figure 8.

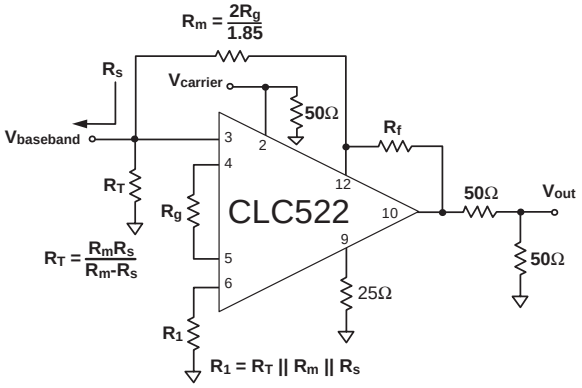


Fig. 8

Frequency Shaping

Frequency shaping and bandwidth extension of the CLC522 can be accomplished using parallel networks connected across the R_g ports. The network shown in the Fig. 9 schematic will effectively extend the CLC522's bandwidth.

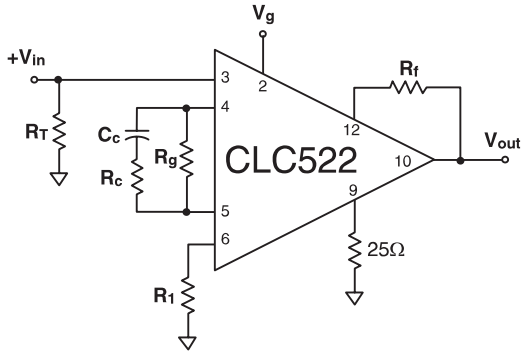


Fig. 9

2nd Order Tuneable Bandpass Filter

The CLC522 Variable-Gain Amplifier placed into feedback loops provide signal processing functions such as 2nd order tuneable bandpass filters. The center frequency of the 2nd order bandpass illustrated on the front page is adjusted through the use of the CLC522's gain-control voltage, V_g. The integrators implemented with two CLC420s, provide the coefficients for the transfer function.

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