National Semiconductor

CLC430
General Purpose 100MHz Op Amp with Disable

General Description

The CLC430 is a low-cost, wideband monolithic amplifier for general purpose applications. The CLC430 utilizes National's patented current feedback circuit topology to provide an op amp with a slew rate of 2000V/µs, 100MHz unity-gain bandwidth and fast output disable function. Like all current feedback op amps, the CLC430 allows the frequency response to be optimized (or adjusted) by the selection of the feedback resistor. For demanding video applications, the 0.1dB bandwidth to 20MHz and differential gain/phase of 0.03%/0.05° make the CLC430 the preferred component for broadcast quality NTSC and PAL video systems.

The large voltage swing ($28V_{pp}$), continuous output current (85mA) and slew rate (2000V/µs) provide high-fidelity signal conditioning for applications such as CCDs, transmission lines and low impedance circuits. Even driving loads of 100Ω, the CLC430 provides very low 2nd and 3rd harmonic distortion at 1MHz (-76/-82dBc).

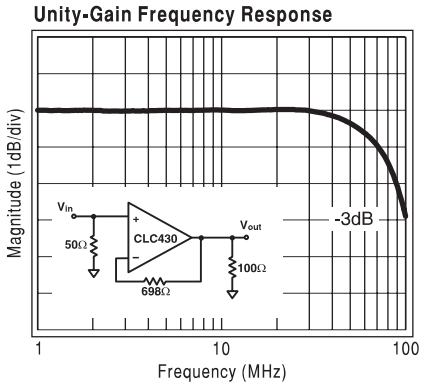
Video distribution, multimedia and general purpose applications will benefit from the CLC430's wide bandwidth and disable feature. Power is reduced and the output becomes a high impedance when disabled. The wide gain range of the CLC430 makes this general purpose op amp an improved solution for circuits such as active filters, differential-to-single-ended drivers, DAC transimpedance amplifiers and MOSFET drivers.

Features

- 0.1dB gain flatness to 20MHz (A_V=+2)
- 100MHz bandwidth (A_V=+1)
- 2000V/µs slew rate
- 0.03%/0.05° differential gain/phase
- ±5V, ±15V or single supplies
- 100ns disable to high-impedance output
- Wide gain range
- Low cost

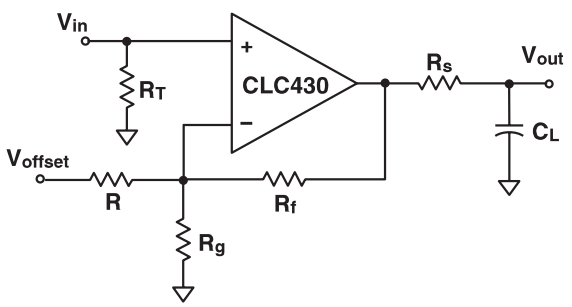
Applications

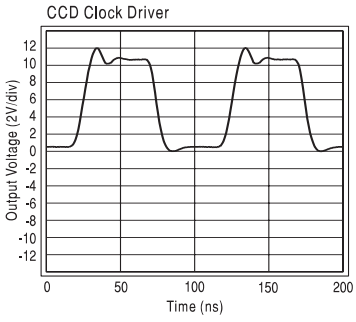
- Video distribution
- CCD clock driver
- Multimedia systems
- DAC output buffers
- Imaging systems



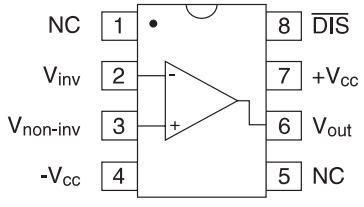
Typical Application

CCD Clock Driver





Pinout
DIP & SOIC



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CLC430 Electrical Characteristics (V_{CC} = ±15V; A_V = +2V/V; R_f =604Ω; R_L = 100Ω; unless noted)

PARAMETERS	CONDITIONS	V_{CC}	TYP	MIN/MAX RATINGS			UNITS	NOTES
Ambient Temperature	CLC430		25°C	25°C	0 to 70°C	-40 to 85°C		
FREQUENCY DOMAIN RESPONSE								
unity-gain bandwidth	V_{out} < 1.0V_{pp}	±15	100				MHz	
small-signal bandwidth	V_{out} < 1.0V_{pp}	±15	75	50	45	42	MHz	
	V_{out} < 1.0V_{pp}	±5	55	35			MHz	
0.1dB bandwidth	V_{out} < 1.0V_{pp}	±15	20	7			MHz	
	V_{out} < 1.0V_{pp}	±5	16				MHz	
large-signal bandwidth	V_{out} = 10V_{pp}		30	22	20	19	MHz	
gain flatness	V_{out} < 1.0V_{pp}							
peaking	DC to 10MHz		0.0	0.1	0.2	0.2	dB	
rolloff	DC to 20MHz		0.1	0.7	1.0	1.2	dB	
linear phase deviation	DC to 20MHz		0.5	1.8	2.0	2.1	°	
differential gain	4.43MHz, R_L=150Ω	±15	0.03	0.05	0.06	0.06	%	
	4.43MHz, R_L=150Ω	±5	0.03	0.05			%	
differential phase	4.43MHz, R_L=150Ω	±15	0.05	0.09	0.12	0.13	°	
	4.43MHz, R_L=150Ω	±5	0.09	0.19			°	
TIME DOMAIN RESPONSE								
rise and fall time	2V step		5	7	7	7	ns	
	10V step		10	14	14	14	ns	
settling time to 0.05%	2V step		35	50	55	55	ns	
overshoot	2V step		5	15	15	15	%	
slew rate	20V step		2000	1500	1450	1450	V/µs	
DISTORTION AND NOISE RESPONSE								
2nd harmonic distortion	1V_{pp},1MHz, R_L=500		-89				dBc	
3rd harmonic distortion	1V_{pp},1MHz, R_L=500		-92				dBc	
input voltage noise	>1MHz		3.0	3.5	3.7	3.8	nV/√Hz	
non-inverting input current noise	>1MHz		3.2	6.0	6.3	6.8	pA/√Hz	
inverting input current noise	>1MHz		15	18	20	21	pA/√Hz	
DC PERFORMANCE								
input offset voltage		±15	1.0	7.5	9.0	10.0	mV	A
average drift			25	---	50	50	µV/ C	
input bias current	non-inverting	±15,±5	3	14	16	20	µA	A
	average drift		10	---	100	100	nA/°C	
input bias current	inverting	±15,±5	3	14	15	17	µA	A
average drift			10	---	60	90	nA/°C	
power-supply rejection ratio	DC		62	56	54	53	dB	
common-mode rejection ratio	DC		62	54	53	52	dB	
supply current	R_L= ∞	±15,±5	11, 8.5	12	13	14.5	mA	A
disabled	R_L= ∞	±15,±5	1.5	2.0	2.2	2.4	mA	A
SWITCHING PERFORMANCE								
turn on time			200	300	320	340	ns	
turn off time	(Note 2)		100	200	200	200	ns	
off isolation	10MHz		59	56	56	56	dB	
high input voltage	V_{IH}	±15	11.8	12.5	12.7		V	
		±5	1.8	2.5	2.7		V	
low input voltage	V_{IL}	±15	10.8	10.5	10.0		V	
		±5	0.8	0.6	0.1		V	
MISCELLANEOUS PERFORMANCE								
Non-inverting input resistance			8.0	3.0	2.5	1.7	MΩ	
Non-inverting input capacitance			0.5	1.0	1.0	1.0	pF	
input voltage range	common mode	±15	±12.5	±12.3	±12.1	±11.8	V	
	common mode	±5	±2.5	±2.3	±2.2	±1.9	V	
output voltage range	R_L= ∞	±15	±14	±13.7	±13.7	±13.6	V	
	R_L= ∞	±5	±4.0	±3.9	±3.8	±3.7	V	
output current			±85	±60	±50	±45	mA	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

supply voltage	±16.5V
short circuit current	(note 1)
common-mode input voltage	±V_{cc}
maximum junction temperature	+150°C
storage temperature	-65°C to+150°C
lead temperature (soldering 10 sec)	+300°C
ESD rating (human body model)	4000V

Notes

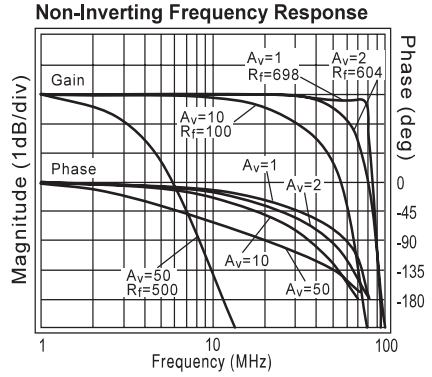
A) J-level: spec is 100% tested at +25°C.

1) Output is short circuit protected to ground, however maximum reliability is obtained if output current does not exceed 125mA.

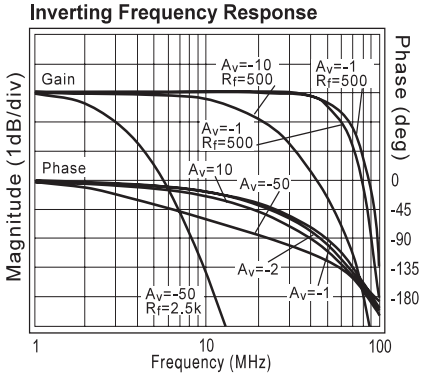
2) To>50dB attenuation @ 10MHz.

CLC430 Typical Performance (V_{CC} = ±15V; A_V = +2V/V; R_f =604Ω ; R_L = 100Ω ; unless noted)

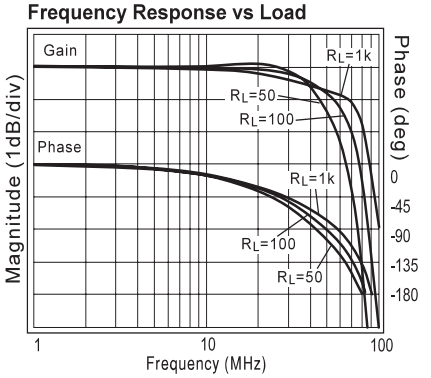
Non-Inverting Frequency Response



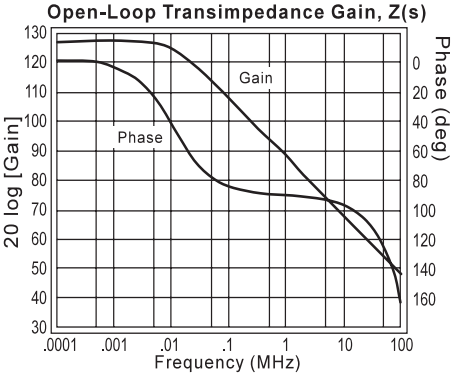
Inverting Frequency Response



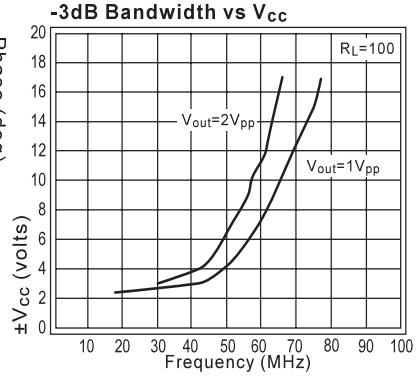
Frequency Response vs Load



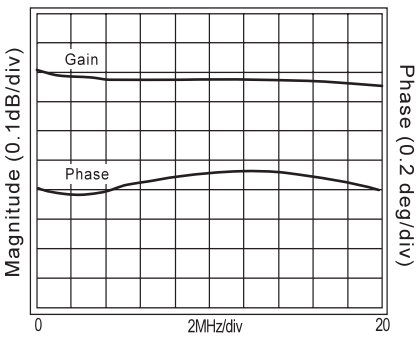
Open-Loop Transimpedance Gain, Z(s)



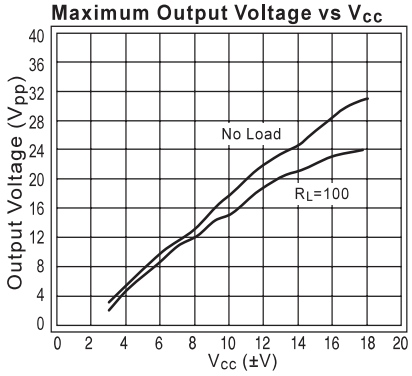
-3dB Bandwidth vs V_{CC}



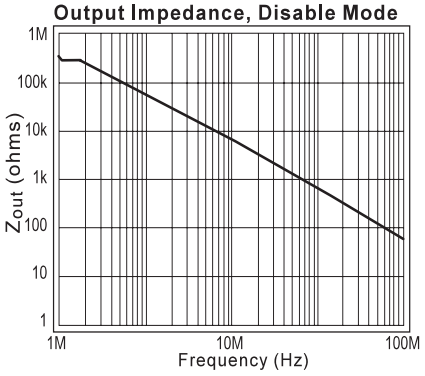
Gain Flatness and Linear Phase



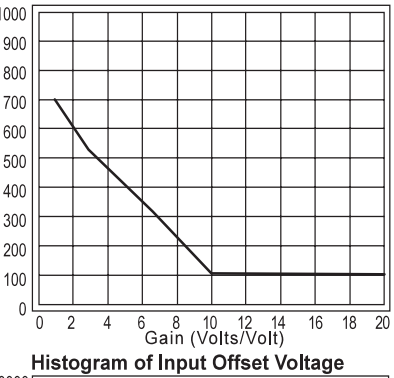
Maximum Output Voltage vs V_{CC}



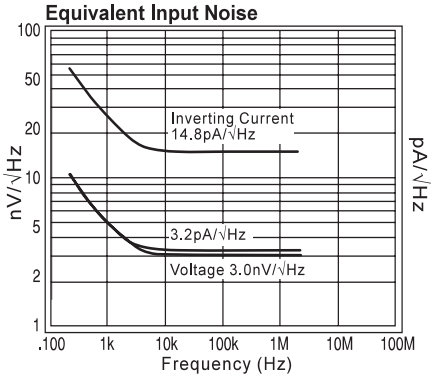
Output Impedance, Disable Mode



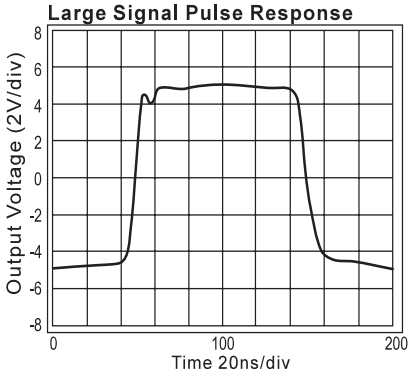
Recommended Rf vs. Gain



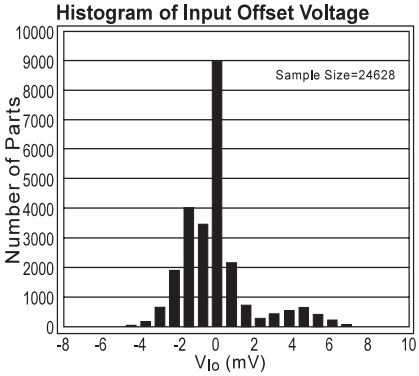
Equivalent Input Noise



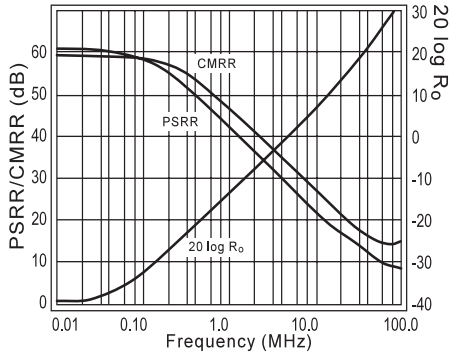
Large Signal Pulse Response



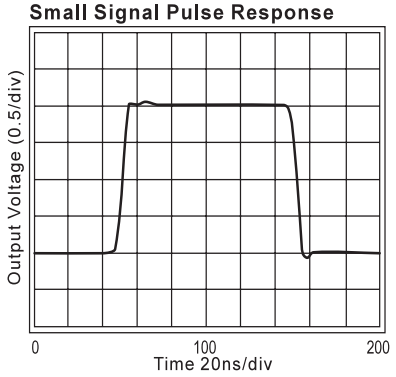
Histogram of Input Offset Voltage



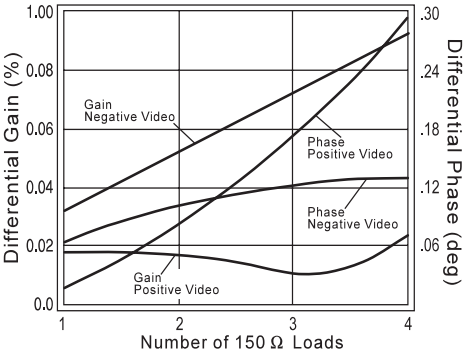
PSRR, CMRR and Closed Loop R_O



Small Signal Pulse Response

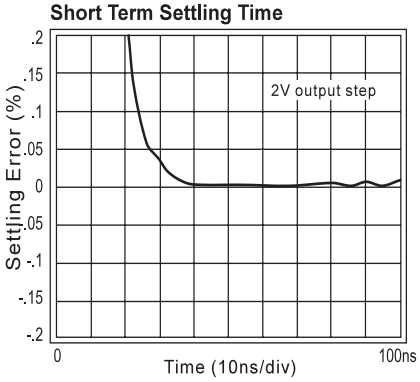


Differential Gain and Phase (3.58MHz)

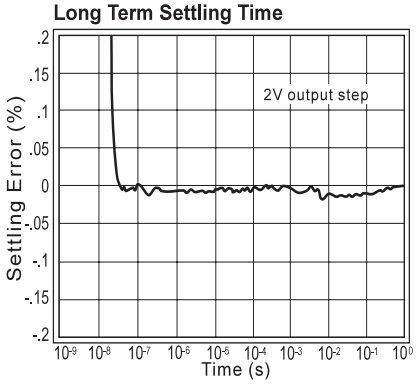


CLC430 Typical Performance (V_{CC} = ±15V; A_V = +2V/V; R_f =604Ω ; R_L = 100Ω ; unless noted)

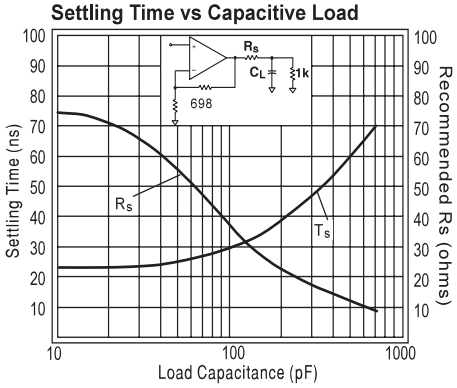
Short Term Settling Time



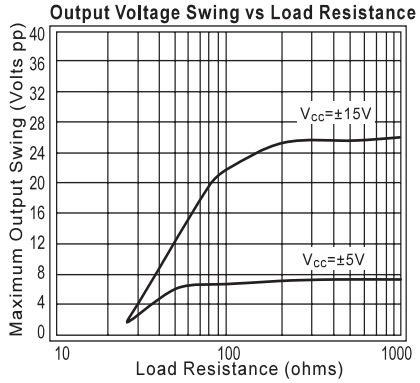
Long Term Settling Time



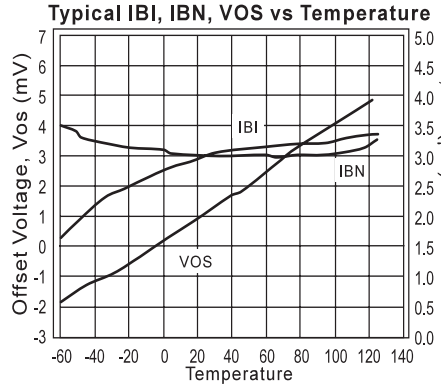
Settling Time vs Capacitive Load



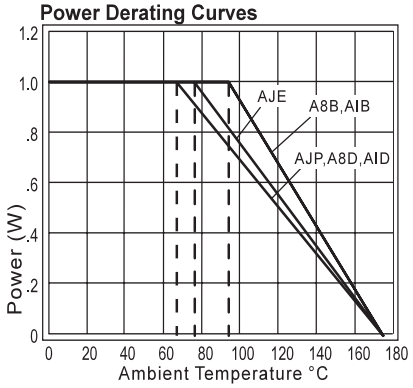
Output Voltage Swing vs Load Resistance



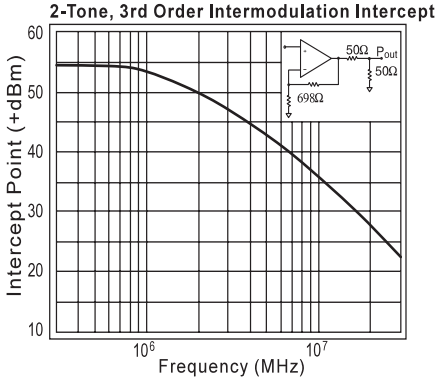
Typical IBI, IBN, VOS vs Temperature



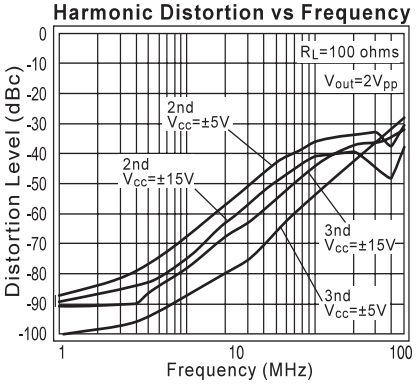
Power Derating Curves



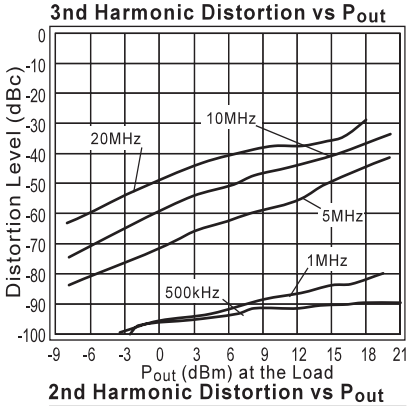
2-Tone, 3rd Order Intermodulation Intercept



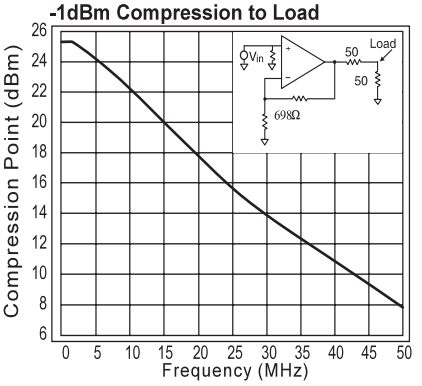
Harmonic Distortion vs Frequency



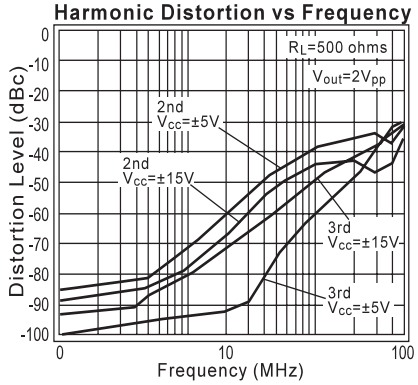
3nd Harmonic Distortion vs P_{out}



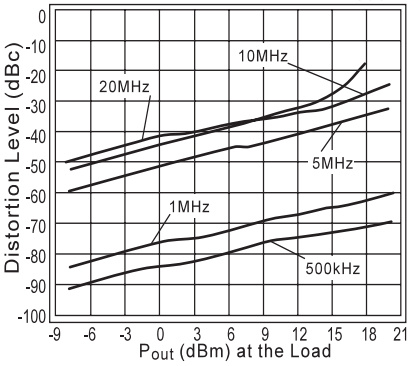
-1dBm Compression to Load



Harmonic Distortion vs Frequency



2nd Harmonic Distortion vs P_{out}



Ordering Information

Model	Temperature Range	Description
CLC430AJP	-40°C to +85°C	8-pin PDIP
CLC430AJE	-40°C to +85°C	8-pin SOIC
CLC430A8B	-55°C to +125°C	8-pin CERDIP, MIL-STD-883

DESC SMD number: 5962-92030.

Package Thermal Resistance

Package	θ_{JC}	θ_{JA}
AJP	60°C/W	115°C/W
AJE	55°C/W	135°C/W
A8B	30°C/W	120°C/W

Reliability Information

Transistor count	38

General Design Considerations

The CLC430 is a general purpose current-feedback amplifier for use in a variety of small- and large-signal applications. Use the feedback resistor to fine tune the gain flatness and -3dB bandwidth for any gain setting. Comlinear provides information for the performance at a gain of +2 for small and large signal bandwidths. The plots show feedback resistor values for selected gains.

Gain

Use the following equations to set the CLC430's non-inverting or inverting gain:

$$\text{Non-Inverting Gain} = 1 + \frac{R_f}{R_g}$$

$$\text{Inverting Gain} = -\frac{R_f}{R_g}$$

Choose the resistor values for non-inverting or inverting gain by the following steps.

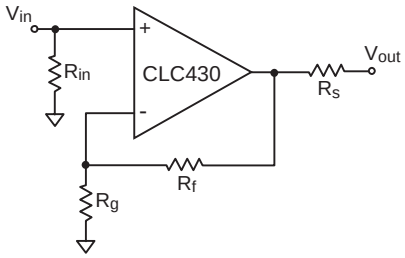


Fig. 0 Component Identification

1) Select the recommended feedback resistor R_f (refer to plot in the plot section entitled *R_f vs Gain*).
2) Choose the value of R_g to set gain.
3) Select R_s to set the circuit output impedance.
4) Select R_{in} for input impedance and input bias.

High Gains

Current feedback closed-loop bandwidth is independent of gain-bandwidth-product for small gain changes. For larger gain changes the optimum feedback register R_f is derived by the following:

$$R_f = 724\Omega - 60\Omega \cdot (A_v)$$

As gain is increased, the feedback resistor allows bandwidth to be held constant over a wide gain range. For a more complete explanation refer to application note OA-25 Stability Analysis of Current-Feedback Amplifiers.

Resistors have varying parasitics that affect circuit performance in high-speed design. For best results, use leaded metal-film resistors or surface mount resistors. A SPICE model for the CLC430 is available to simulate overall circuit performance.

Enable / Disable Function

The CLC430 amplifier features an enable/disable function that changes the output and inverting input from low to high impedance. The pin 8 enable/disable logic levels are as follows:

V_{cc}	±15V	±5V
Enable	>12.7V	>2.7V
Disable	<10.0V	<0.8V

The amplifier is enabled with pin 8 left open due to the 2kΩ pull-up resistor, shown in Fig. 1.

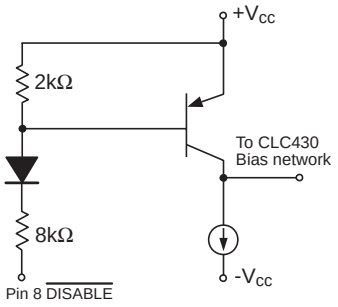


Fig. 1 Pin 8 Equivalent Disable Circuit

Open-collector or CMOS interfaces are recommended to drive pin 8. The turn-on and off time depends on the speed of the digital interface.

The equivalent output impedance when disabled is shown in Fig. 2. With R_g connected to ground, the sum of R_f and R_g dominates and reduces the disabled output impedance. To raise the output impedance in the disabled state, connect the CLC430 as a unity-gain voltage follower by removing R_g. Current-feedback op-amps need the recommended R_f in a unity-gain follower circuit. For high density circuit layouts consider using the dual CLC431 (with disable) or the dual CLC432 (without disable).

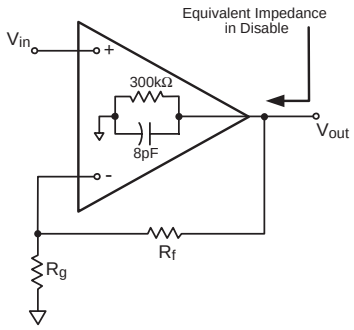


Fig. 2 Equivalent Disabled Output Impedance

2nd and 3rd Harmonic Distortion

To meet low distortion requirements, recognize the effect of the feedback resistor. Increasing the feedback resistor will decrease the loop gain and increase distortion. Decreasing the load impedance increases 3rd harmonic distortion more than 2nd.

Differential Gain and Differential Phase

The CLC430 has low DG and DP errors for video applications. Add an external pulldown resistor to the CLC430's output to improve DG and DP as seen in Fig.3. A 604Ω R_P will improve DG and DP to 0.01% and 0.02°.

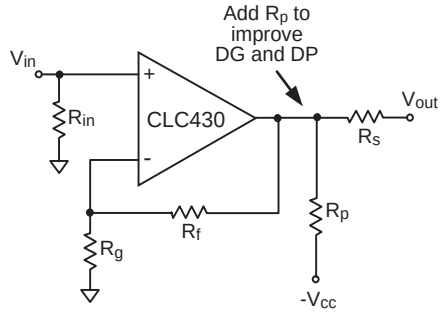


Fig. 3 Improved DG and DP Video Amplifier

Printed Circuit Layout

To get the best amplifier performance careful placement of the amplifier, components and printed circuit traces must be observed. Place the 0.1µF ceramic decoupling capacitors less than 0.1" (3mm) from the power supply pins. Place the 6.8µF tantalum capacitors less than 0.75" (20mm) from the power supply pins. Shorten traces between the inverting pin and components to less than 0.25" (6mm). Clear ground plane 0.1" (3mm) away from pads and traces that connect to the inverting, non-inverting and output pins. Do not place ground or power plane beneath the op-amp package. Comlinear provides literature and evaluation boards 730013 DIP or 730027 SOIC illustrating the recommended op-amp layout.

Applications Circuits

Level Shifting

The circuit shown in Fig. 4 implements level shifting by AC coupling the input signal and summing a DC voltage. The resistor R_{in} and the capacitor C set the high-pass break frequency. The amplifier closed-loop bandwidth is fixed by the selection of R_f. The DC and AC gains for circuit of Fig. 4 are different. The AC gain is set by the ratio of R_f and R_g. And the DC gain is set by the parallel combination of R_g and R_2.

$$V_{out} = V_{in_{ac}}\left(1+\left(\frac{R_f}{R_g||R_2}\right)\right) - V_{in_{DC}}\left(\frac{R_f}{R_2}\right)$$

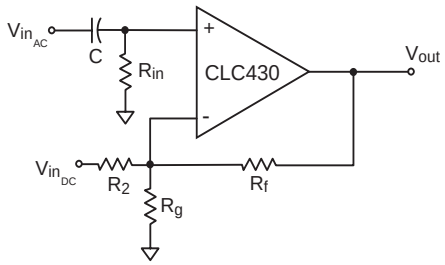


Fig. 4 Level Shifting Circuit

Multiplexing

Multiple signal switching is easily handled with the disable function of the CLC430. Board trace capacitance at the output pin will affect the frequency response and switching transients. To lessen the effects of output capacitance place a resistor (R_o) within the feedback loop to isolate the outputs as shown in Fig. 5. To match the mux output impedance to a transmission line, add a resistor (R_s) in series with the output.

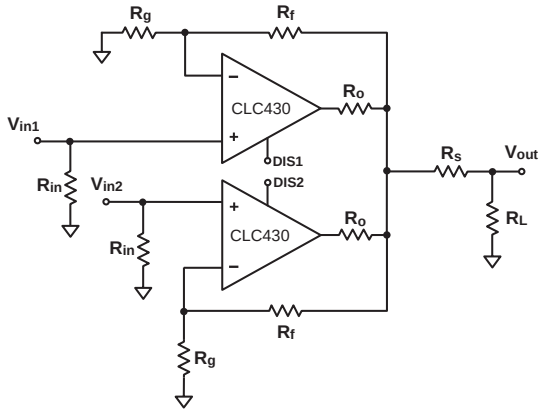
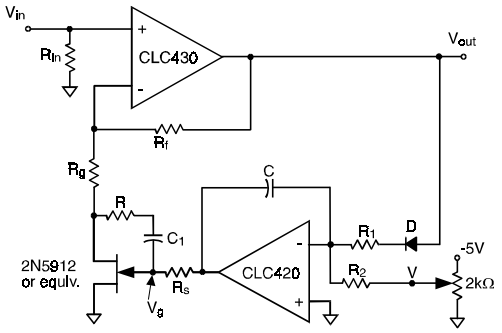


Fig. 5 Output Connection

Automatic Gain Control

Current-feedback amplifiers can implement very fast automatic-gain control circuits. The circuit shown in Fig. 6 shows an AGC circuit using the CLC430, a half-wave rectifier, an integrator and a FET. The CLC430 current-feedback amplifier maintains constant bandwidth and linear phase over AGC's gain range. This circuit effectively controls the output level for continuous signals.

Fig. 6 AGC Circuit



The bandwidth of the CLC430 AGC is limited by R_f, the feedback resistor. The FET gate voltage is limited to a range of:

$$-2.5 < V_g < -1$$

R of 750Ω and C1 of 1.0µF gives a useful R_{ds} range of approximately 150 to 2K ohms. Scaling the integrator gain or adding attenuation before the diode D accommodates large signal swings. Determine the overall gain by:

$$1+\frac{R_f}{R_g+R_{ds}}$$

The integrator sets the loop time constant.

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